Novel AC Coupled Gate Driver for Ultra Fast Switching of Normally-Off SiC JFETs

Benjamin Wrzecionko, Stefan Käch, Dominik Bortis, Jürgen Biela and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich
Zurich, Switzerland
Email: wrzecionko@lem.ee.ethz.ch

***Abstract*—Over the last years, more and more SiC power semiconductor switches became available in low production volumes in order to prove their superior behavior with respect to fast switching speed, low on-resistance per chip area, high voltage range and high temperature operation. A very promising device among those introduced in numerous publications over the last years is the 1200 V 30 A JFET introduced by SemiSouth. It features a very low on-resistance (2.8 mΩcm^2), switching operation within 20 ns, a normally-off characteristic and has already been commercialized in contrast to many other SiC switches.**

To fully exploit the potential of the SiC normally-off JFET, conventional gate drivers for unipolar devices must be adapted to this device due to its special requirements: During on-state the gate voltage must not exceed 3 V, while a current of around 300 mA must be fed into the gate, during switching operation the transient gate voltage should be around ± 15 V and the low threshold voltage of 0.7 V requires a high noise immunity which is a severe challenge as the device has a comparably low gate-source but high gate-drain capacitance.

To meet these requirements, several concepts have been published recently. They deal with the challenges mentioned, but they also note certain limitations (e. g. frequency and duty cycle limitations or need for additional cooling). In this paper, a novel gate driver consisting only of one standard gate driver IC, resistors, capacitors and diodes is designed and experimentally validated. It supplies enough gate current for minimum on-resistance, allows fast switching operation, features a high noise immunity and can be used for any duty cycle and usual switching frequencies without significant self-heating.

***Index Terms*—SiC; JFET; Gate Driver; Enhancement Mode; Normally-off**

I. Introduction

Against the background of continuing quest for higher power density and efficiency of power electronic converters, an upcoming interest in new semiconductor materials, especially wide band-gap (WBG) semiconductors, can be observed. The group III-V compound semiconductor Silicon Carbide (SiC) is particularly promising for power electronic applications.

Compared to Silicon (Si) as the conventional material for power semiconductors, SiC has a three times higher band-gap (energy difference between the valence and conduction band of the material) leading to an order of magnitude higher breakdown electrical field (328 MV/m for 4H-SiC, the most common SiC crystal structure for SiC power semiconductors, compared to 29 MV/m for Si) while having a comparable electron mobility [1]–[4].

This leads to lower conduction losses per chip area for unipolar SiC devices compared to Si devices of the same blocking voltage class. SiC Field-Effect-Transistors (FETs) are feasible for high voltage ratings up to 10 kV [5] and are — in terms of losses — very competitive to Si IGBTs, e. g. in the 1200 V blocking voltage class. Here, unipolar SiC devices offer in particular fast switching operation and thus lower switching losses compared to bipolar Si devices currently used in this voltage range [6].

Additionally, SiC devices can be operated at significantly higher junction temperatures than 175 °C due to the several orders of magnitude lower intrinsic charge carrier concentration of SiC compared to Si favoring them for applications with high ambient temperatures [7], [8].

Currently, the main research and development focus concerning unipolar SiC devices is on Schottky Barrier Diodes (SBDs), Metal-Oxide-Semiconductor-FETs (MOSFETs) as well as normally-on and normally-off Junction-FETs (JFETs). While SiC Schottky diodes have already been commercially available for a few years and are now increasingly deployed in applications where the absence of any reverse recovery charge can significantly improve the converter performance, SiC MOSFETs are not yet commercially available. The main issues are a low electron mobility at the channel surface and gate oxide reliability uncertainties [7], [9].

Considering the available SiC JFETs, in particular enhancement mode (EM) SiC JFETs are of interest. In contrast to normally-on JFETs, no safety concerns for voltage source converters occur because the EM SiC JFET is a truly normally-off device and blocks its nominal drain-source voltage at zero gate-source voltage. Nevertheless, it still features a pure SiC solution with all of its benefits (especially regarding high temperature operation capability) compared to cascode approaches using a Si MOSFET connected in series to the SiC JFET, which additionally brings up the question of matching the right MOSFET to the JFET [9]. Furthermore, the available normally-off device shows superior performance in terms of drain-source on-resistance per chip area (2.8 mΩcm^2 for a 1200 V device). The 1200 V 30 A normally-off JFET has been commercialized by SemiSouth Laboratories, Inc. in 2009 [10].

This device makes special demands on the gate driver circuit compared to other unipolar SiC or Si devices. To fully exploit the potential of SiC normally-off JFETs, conventional gate

978-1-4244-5226-2/10/$26.00 ©2010 IEEE

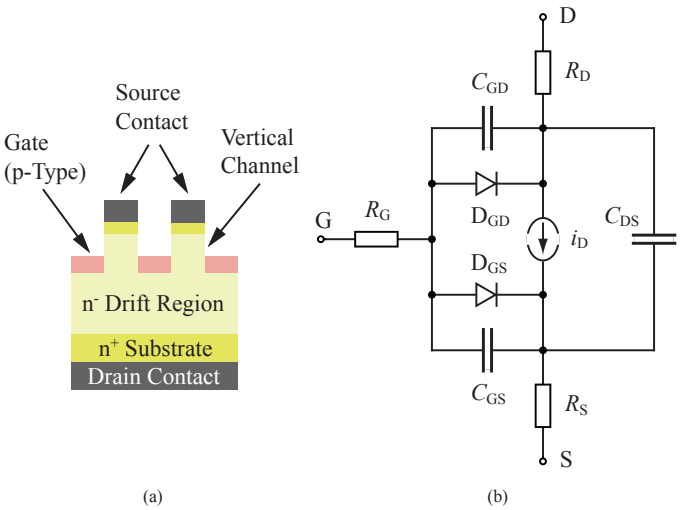

Fig. 1. SiC normally-off 1200 V JFET: cross-section (a), equivalent circuit diagram (b). Notable is with respect to gate driver design in particular the pn-junction diode at the gate as well as the purely vertical structure of the device leading to an inherently high gate-drain capacitance (*cf.* Section II-A1 and Section II-A2).

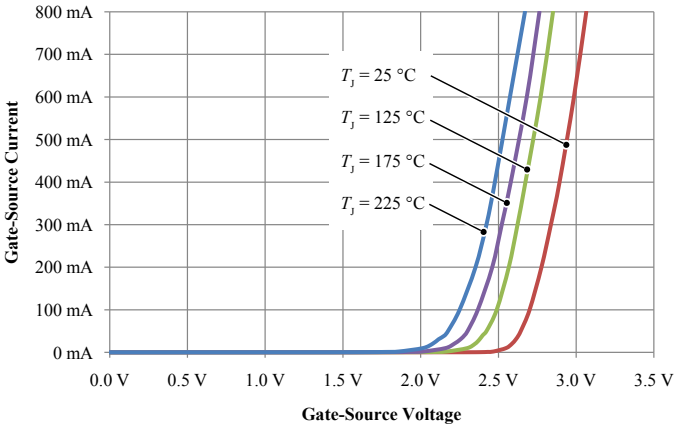

Fig. 2. Measured forward characteristic of the gate-source diode D_{GS} of the 1200 V 30 A SiC normally-off JFET against its junction temperature. During the on-state of the SiC normally-off JFET, the gate-source voltage should not exceed 3 V in order to avoid large currents flowing into the gate.

driver circuits for unipolar switches need to be adapted for use with these switches. In the literature, several concepts for adapted gate drivers have been presented so far. Some still have certain limitations, e. g. with respect to switching frequencies and possible duty cycles, and some of them are very complex solutions with the need for several integrated circuits, own DC-DC converters or additional cooling [10]–[15].

In this paper, a novel gate driver topology is presented that overcomes the current limitations while still having a low circuit complexity using one gate driver IC and passive components only. The design of this gate driver circuit is shown in Section II, focussing first on the special gate driver requirements of the normally-off JFET (Section II-A), summarizing shortly the present concepts (Section II-B) and then explaining the proposed novel concept in detail (Section II-C). In Section III, the theoretical considerations are validated with an half-bridge test setup showing experimental waveforms of the switching action.

II. Gate Driver Design

A. Gate Driver Requirements of the Normally-Off JFET

Fig. 1 shows a cross-section (a) and the equivalent circuit diagram (b) of the SiC 1200 V normally-off JFET. The structure of the investigated device influences the design of the gate driver that is used to control the behavior of the switch largely.

1) On-state: From the cross-section Fig. 1 (a) the major difference between a *junction* and a *metal-oxide-semiconductor* FET becomes obvious: The gate is not insulated from the channel by an oxide, but forms a pn-junction with the source (diode D_{GS} in the JFET model in Fig. 1 (b)) and the drain (D_{GD}), respectively. The resulting depletion layer in the channel makes sure, that the device can block its nominal voltage without any reverse biasing of the pn-junction (and thus further extending the depletion region), i. e. with $V_{GS} = 0$.

Forward biasing the pn-junction reduces the width of the space charge region. The threshold voltage $V_{GS,th}$ of the device is typically around 1 V, decreasing with temperature at the rate of approx. $1.5\,\mathrm{mV/°C}$ to less than 0.7 V at 250 °C. If V_{GS} exceeds the built-in potential of the pn-junction $V_{bi} \approx 3\,\mathrm{V}$ at room temperature, a significant amount of holes is injected into the channel. Fig. 2 shows the temperature dependent forward characteristic of the gate-source diode. The consequence for the gate driver is the limitation, that no more than 3 V should be applied to the JFET's gate with respect to the source during the on-state to avoid large currents flowing into the gate.

The correlation between the drain-source on-resistance $R_{DS,on}$ and the applied gate bias to D_{GS} (in this case in terms of the current, which can be transformed to the respective voltage using the diode characteristic in Fig. 2) is shown in Fig. 3 for different drain currents I_D and junction temperatures T_J. It can be seen, that $R_{DS,on}$ depends on T_J *and* on I_D. The latter dependency increases with temperature and the drain current saturation limit can be observed for junction temperatures of 175 °C and higher: While $R_{DS,on}$ increases at 175 °C for $I_D = 16\,\mathrm{A}$ by 14% compared to $I_D = 7\,\mathrm{A}$, a drain current level of 24 A at a junction temperature of 175 °C leads to a more than 50% increase in $R_{DS,on}$, even for gate currents of 600 mA and more. (For lower gate currents, the on-resistance is even higher.)

The resulting requirement for the gate driver can be extracted from Fig. 4. It shows the for a minimum $R_{DS,on}$ required gate-source current for drain currents from 4 A to 30 A and junction temperatures from 25 °C to 225 °C. This gate current varies from 100 mA for $I_D = 4\,\mathrm{A}$ at 25 °C to 400 mA for $I_D = 16\,\mathrm{A}$ at 175 °C.

The required gate-source currents (one for each temperature level), that have to be determined for the gate driver design in Section II-C, cannot be identified application independent. That is, for each application, the current density depending on the converter specifications and available chip area limited by cost as well as the on-resistance limited by efficiency

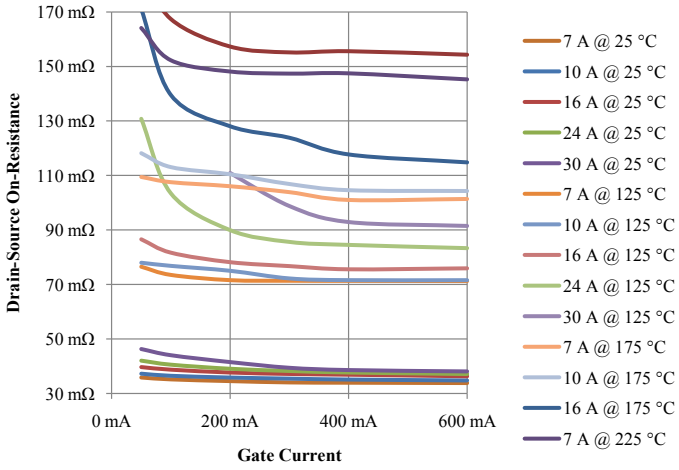

Fig. 3. Measured drain-source on-resistance of the 1200 V 30 A SiC normally-off JFET for different drain currents against the gate-source current with its junction temperature as a parameter. It can be clearly seen, that a significant amount of gate current is necessary to operate the device with its minimum on-resistance. With increasing temperature, the difference in $R_{\mathrm{DS,on}}$ for different gate currents increases. At high temperatures, the maximum drain current should be decreased to avoid high values of $R_{\mathrm{DS,on}}$.

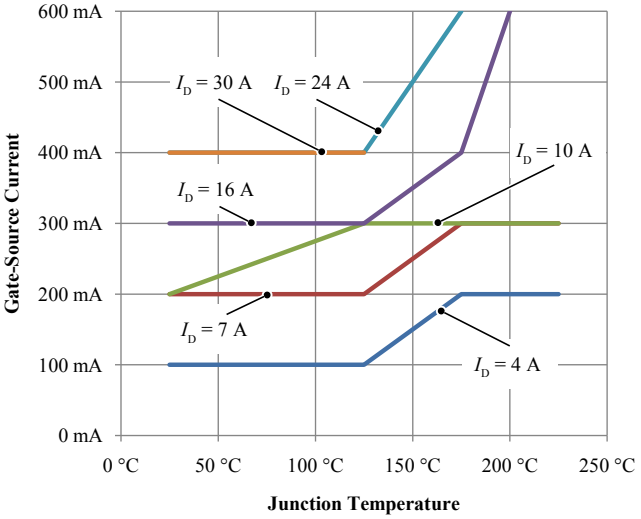

Fig. 4. Minimum gate-source current that is required for different drain current and junction temperature levels to operate the 1200 V 30 A SiC normally-off JFET with lowest possible drain-source on-resistance. For this example design a drain current limit of 10 A at 175 °C is assumed leading to a gate current of 300 mA.

requirements have to be determined. This will be an iterative optimization, as these different aspects interact.

Furthermore, it has to be noted, that at the discussed gate current levels, the required power at the gate-source terminal can be more than 1 W. Taking the efficiency of the gate driver supply converters or restrictions with respect to self-heating of the the drive components (e. g. due to high ambient temperature levels) into account, the gate-source current, that has to be delivered by the gate driver, and its influence on the on-resistance is also subject to the overall converter optimization.

To stay within the scope of this paper and to summarize the requirements for the gate driver during the on-state of the JFET, the drain current limit is chosen to $I_{\mathrm{D}} = 10\,\mathrm{A}$ at $T_{\mathrm{J}} = 175\,^{\circ}\mathrm{C}$ (*cf.* Fig. 3) and the upper limit of the gate-source current is chosen for minimum on-resistance at this operating point to 300 mA (*cf.* Fig. 4) corresponding to a gate-source voltage of 2.52 V (*cf.* Fig. 2) for this paper. This choice allows the design of a gate driver in Section II-C that has challenging requirements meeting the needs of the SiC normally-off JFET while being significantly different to those for MOSFET drivers. Additionally, choosing these values, a design is introduced that can be easily adapted for other applications towards lower or higher gate currents for other on-resistances or the parallelization of several chips.

2) Switching Transients: During the switching transients, the gate driver must deliver the charge required by the parasitic input capacitance C_{iss}, which is the sum of the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} of the JFET model in Fig. 1 (b). As can be seen from the cross-section in Fig. 1 (a), the investigated normally-off JFET has a vertical channel in contrast to typical SiC normally-on JFETs [16] as well as (Si and SiC) MOSFETs [17]. This purely vertical structure leads on the one hand to a comparably low gate-source capacitance C_{GS}, but at the same time to an inherently high gate-drain (Miller) capacitance C_{GD}.

This fact is illustrated by Fig. 5, which compares C_{iss} and C_{rss} of the 1200 V 30 A SiC normally-off JFET with the C_{iss} and C_{rss} of a typical SiC MOSFET with similar voltage and current rating. C_{rss} is C_{GD} in the JFET model, and is significantly higher for the JFET (by a factor of 3 to 10 depending on the drain-source voltage V_{DS}). C_{iss} as the sum of C_{GS} and C_{GD} is lower for the JFET (by a factor of approx. 1.5), i. e. the JFET's C_{GS} is much smaller, as expected from the device cross-section.

To turn the device on, C_{GS} must be charged by the gate driver to approx. 3 V and C_{GD} (charged to approx. V_{DS} when the device is in the off-state) must be discharged by feeding current from the gate terminal to the drain. To turn the device off, the opposite action is necessary: The gate driver must sink current in order to discharge C_{GS} and charge C_{GD} to approx. V_{DS}.

As depicted in the JFET model in Fig. 1 (b), the gate-source path shows also resistive behavior with $R \approx 3\,\Omega$ in a frequency range of 100 kHz to 1 MHz, limiting the achievable switching speed. In order to be able to reach the desired voltage levels during turn-on ($V_{\mathrm{GS}} \approx 3\,\mathrm{V}$ desired for the on-state, *cf.* Section II-A) and -off ($V_{\mathrm{GS}} \leq 0\,\mathrm{V}$ desired for the off-state) fast, the gate driver should apply voltages higher than these steady state values for a short period of time at each switch state transition. SemiSouth allows $V_{\mathrm{GS,AC}} = \pm 15\,\mathrm{V}$ for a duration of less than 200 ns [18].

For applications with limitations regarding the switching speed due to requirements set by EMI, common mode or insulation issues, the gate driver should be able to switch with a pre-set (less than the maximum achievable) speed.

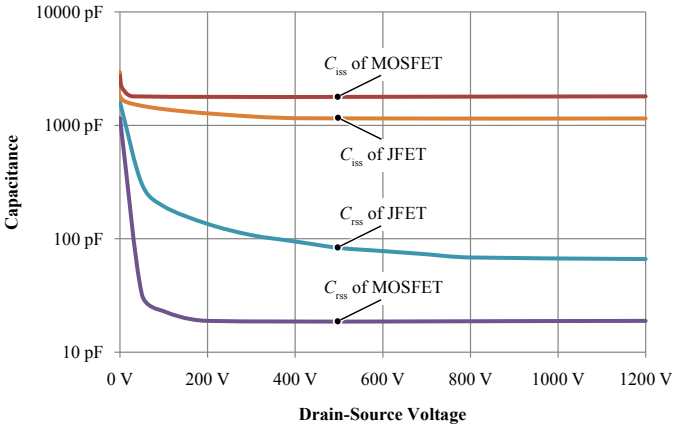

Fig. 5. Comparison of the measured input and reverse transfer capacitance (C_{iss} and C_{rss}, respectively) of a SiC normally-off 1200 V 30 A JFET and a typical SiC MOSFET with similar voltage and current rating showing the high gate-drain and low gate-source capacitance of the JFET.

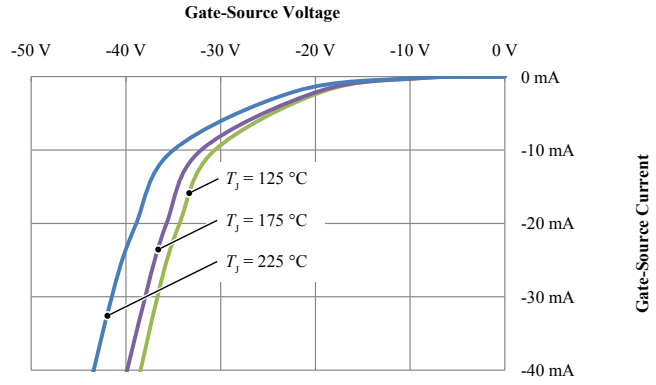

Fig. 6. Measured reverse characteristic of the gate-source diode D_{GS} of the 1200 V 30 A SiC normally-off JFET against its junction temperature. A bias exceeding -15 V should not be applied to the gate in order to limit the losses during the off-state.

3) Off-state: As the threshold voltage can decrease down to 0.7 V for SiC normally-off JFET, the gate driver has to apply a negative bias to the gate with respect to the source during the off-state of the switch in order to add noise immunity and guarantee a safe turn-off during normal converter operation. (I. e. this is not necessary during start-up of the converter and hence makes an important difference to the use of normally-on devices.) Fig. 6 shows the measured characteristic of the gate-source diode in reverse direction. Bearing in mind, that the leakage currents occur in the off-state of the device and that the device may remain in the off-state for a longer time than only a few microseconds if for example the overall converter is on standby, the losses in the diode should be limited to a low level. Hence, the negative bias should not be larger than 15 V.

4) Temperature Behavior: Some of the requirements for the gate driver set by the switch characteristics investigated so far are temperature dependent, especially with respect to the gate current. Ideally, the gate driver behaves over the operating temperature range such that it caters to these changing requirements and does not add any more temperature variations itself. In this case, it is especially important with respect to the power loss of the gate driver, that the gate current is always just as high as needed. I. e. if due to lower junction temperatures not such a high gate current as the above determined 300 mA is needed, the gate driver should supply less current.

5) Standard Requirements: All of the above mentioned requirements for the investigated gate driver are given by the properties of the SiC normally-off JFET. A novel, ubiquitous gate driver has to fulfill also standard requirements that apply to any gate driver used in power electronic converters:

- Low power consumption
- Performance invariance against spread for factory standard models (of the gate driver IC itself as well as the switch)
- Qualification for switching frequencies of standard power electronic converters in the investigated voltage range up to around 100 kHz
- Enabling arbitrary duty cycles from 0% to 100%
- Robustness against steep voltage changes
- Low (circuit) complexity and cost

B. Existing Gate Drivers for the Normally-Off JFET

Against the background of the summarized requirements of gate drivers for the SiC normally-off JFET, the existing solutions are very shortly reviewed.

1) Two-stage Gate Drivers: To meet the different requirements for transient turn-on and -off on the one hand and the steady on-state on the other hand, gate drivers with one stage supplying a short pulse with a high voltage (around 15 V) and a second stage delivering the DC current from the same supply voltage rail via a resistor during the on-state have been introduced [10], [13]–[15]. The second stage is either realized by a second output of a dual gate driver IC or by low-voltage transistors connected to the supply voltage of the gate driver. The control of the second stage is realized by an additional logic IC.

To limit the power loss in the resistor during on-state, a DC-DC converter can be deployed. Still, the power loss can become significant for this concepts at duty cycles close to 100% and switching frequencies higher than 25 kHz [15]. This frequency limitation can be somewhat undesirable as one of the unique selling propositions of SiC devices is their low switching losses allowing significantly higher switching frequencies than for Si devices.

2) AC-coupled Gate Drivers: To reduce the high complexity of the two-stage gate drivers, AC-coupled gate drivers have been published [11], [12], [19] where the supply voltage is fed through a capacitor to the gate during the turn-on and -off and through a resistor during the on-state. The limitations of this concept include frequency and duty cycle limitations as the coupling capacitor needs to discharge during turn-off via a high impedance path [13], a high power loss in the DC current resistor and the need for an external gate-source

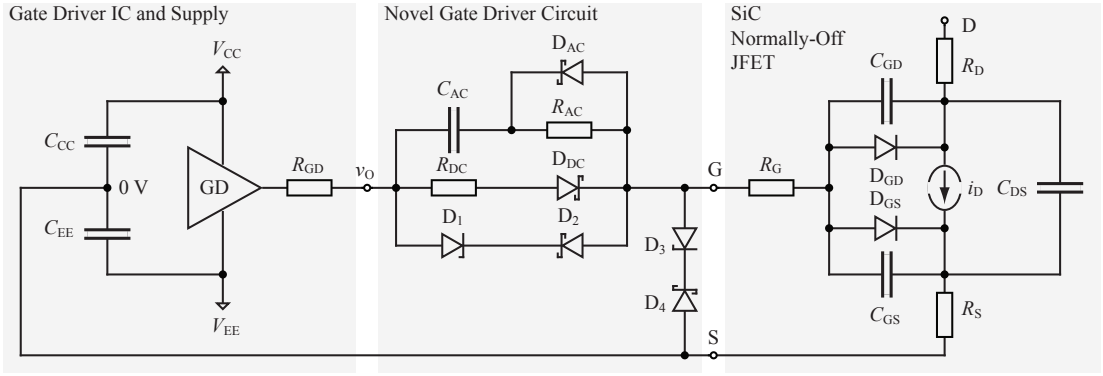

Fig. 7. Proposed novel AC coupled gate driver for ultra fast switching of normally-off SiC JFETs. During the on-state of the JFET, a DC current flows through R_{DC} and D_{DC} causing very low losses in these devices due to the low voltage drop. During turn-off and the off-state $V_{Z,D3}$ is applied to the gate for a high noise immunity making this gate driver together with D_1 and D_2 resistant against the Miller effect. During turn-on the sum of V_{CC} and V_{CAC} is applied to the gate for fast turn-on. This gate driver does not have any duty cycle or frequency limitations of significant self-heating.

capacitor that can sink the current arising from the high gate-drain capacitance of the JFET [13], [19].

C. Proposed Novel AC Coupled Gate Driver

The proposed gate driver for the SiC normally-off JFET is shown in Fig. 7. First, the basic operation principle will be described and then the circuit elements and voltage levels will be dimensioned in detail.

A standard gate driver IC is supplied with a differential voltage $V_{CC} - V_{EE}$ with the midpoint (0 V) connected to the source of the JFET, V_{CC} being close to the desired gate voltage of around 3 V and V_{EE} in the range of -25 V.

During the on-state of the switch, V_{CC} is applied to the gate through the output resistance R_{GD} of the gate driver IC, a resistor R_{DC} and a Schottky diode D_{DC} to provide the required DC current to the JFET during the on-state. As the voltage drop across the resistor is low, the power dissipation will be significantly lower as for the existing gate drivers shown in Section II-B.

During the off-state of the device, the output v_O of the gate driver IC is at V_{EE}. The Zener voltage $V_{Z,D3}$ of the Zener diode D_3 determines the sharing of the voltage V_{EE} between the gate-source terminals of the JFET and the capacitor C_{AC}. $V_{Z,D3}$ fulfills the requirement of negative bias at the gate during the off-state (*cf.* Section II-A) and D_{DC} makes sure, that no current flows through R_{DC} during the off-state.

During turn-on of the JFET, the voltage $V_{CAC} = V_{EE} - V_{Z,D3}$ across C_{AC} is added to V_{CC}, making sure that a positive voltage around 15 V is applied to the gate terminal for fast charging of the JFET's input capacitance while discharging C_{AC}. To dampen oscillations or to slow down the switching speed, a resistor R_{AC} can be connected in series to C_{AC}.

During turn-off, the required negative bias can be applied by V_{EE} (limited to the allowed value of -15 V by D_3), and the diode D_{AC} provides with C_{AC} a low impedance path for fast turn-off of the channel.

The state of charge of C_{AC} does not impose any duty cycle or frequency limitations: If the on-time is low, it is still fully discharged as it is connected to D_{GS} through a low impedance path. D_4, D_3 and D_{AC} form a low impedance path that allows charging of C_{AC} also for very low off-times of the JFET (*cf.* Section III).

After turn-off of the channel, i. e. after discharging C_{GS} from approx. 3 V to $V_{Z,D3}$, it can happen in half-bridge configurations, such as depicted in Fig. 9, that C_{GD} is charged to V_{DS} significantly later than the actual turn-off of the switch: Consider i_L in Fig. 9 freewheeling in $JFET_{HS}$, before the channel of $JFET_{HS}$ is turned off. i_L will continue freewheeling in D_{HS}, until $JFET_{LS}$ is turned on. Once it is turned on, the source (and thus the gate) of $JFET_{HS}$ will be clamped to approximately 0 V, while the drain of $JFET_{HS}$ remains at V_{DC} resulting in quick charging of C_{GD} to V_{DS}.

The current charging C_{GD} (which is very large for this JFET, *cf.* Section II-A) should not flow through C_{GS} as it would then charge it (charging also C_{AC} further at the same time) and thus turn $JFET_{HS}$ on (called the "Miller Effect") which would short the DC link voltage. To clamp the gate voltage to $V_{Z,D3}$ the proposed gate driver has an anti-series connection of Zener diode D_1 and Schottky diode D_2 that makes sure, that the current charging C_{GD} can flow to the source of the JFET without flowing through C_{GS} and thus switching the JFET on. It is important, that the inductance in the path from the gate to the source through the D_1-D_2 path is low, otherwise the gate potential can increase significantly for nanoseconds without being clamped. As zero inductance is not possible, the gate-source voltage must be dimensioned negative enough, that an increase in gate potential to build up current through the diode path, is still well below the threshold voltage of the JFET.

Having explained the basic functionality of the proposed gate driver and its elements, the design of appropriate components and physical values can be conducted in the following subsections:

1) Gate Driver IC: When choosing the right gate driver IC for the proposed gate driver circuit the output current that must be delivered or sunk by the IC is important. The gate charge of the 1200 V 30 A JFET is 60 nC. Due to the series connection with C_{AC}, the charge, that the gate driver IC must deliver is doubled. If this has to be delivered for fast switching

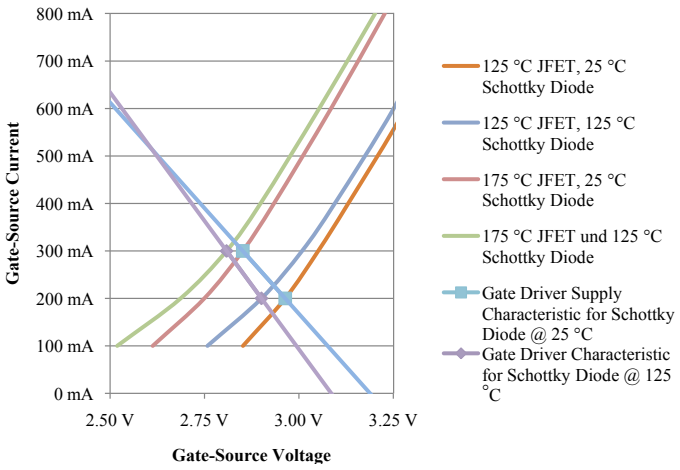

Fig. 8. Characteristic of series connection of gate-source diode D_{GS} and Schottky diode D_{DC} at junction temperatures of 125 °C and 175 °C for the JFET as well as 25 °C and 125 °C for D_{DC}. From these characteristics, the required gate driver supply characteristic in terms of V_{CC} and R_{DC} can be derived.

within a minimum time of e. g. 10 ns, the peak output current of the IC has to be 12 A.

To limit the self-heating of the IC during the large current peaks during the switching transients as well as during the DC current in the on-state of the JFET and especially to limit the RC time constant, the output resistance R_{GD} should be as small as possible.

Here the IXYS IXDE514SIA in a SO-8 package is chosen, the peak output current is 14 A, the maximum output resistance for the high and low state 1.25 Ω and the maximum supply voltage 35 V.

2) V_{CC}, R_{DC}, D_{DC}: The elements R_{DC} and D_{DC} as well as V_{CC} determine together with D_{GS} the gate current supplied to the JFET during the on-state of the device and thus the on-resistance of the JFET. According to Section II-A1, the gate driver must deliver 300 mA at $T_J = 175\,°C$ for this design example.

If the gate driver was an ideal voltage source, i. e. a vertical line in the current-over-voltage characteristic, it would supply significantly less current to its load D_{GS} at lower junction temperatures and much higher currents at higher temperatures. If it was an ideal current source, it would supply the same current for all temperature levels, i. e. the gate driver would not fulfill the requirement of Section II-A4 to supply a gate current that is only as high as needed for the respective temperature level. (If a converter design is such, that the nominal rms-value of the drain current is 10 A and the nominal junction temperature is 175 °C, the junction temperature is likely to be well below the nominal value at part load, corresponding to a lower drain current and thus a lower gate current needed. The precise value of the junction temperature at a given part load drain current level depend on the thermal impedance of the respective converter.)

Hence, for this example design, it is assumed, that the drain current of 10 A at 175 °C corresponds to a drain current of

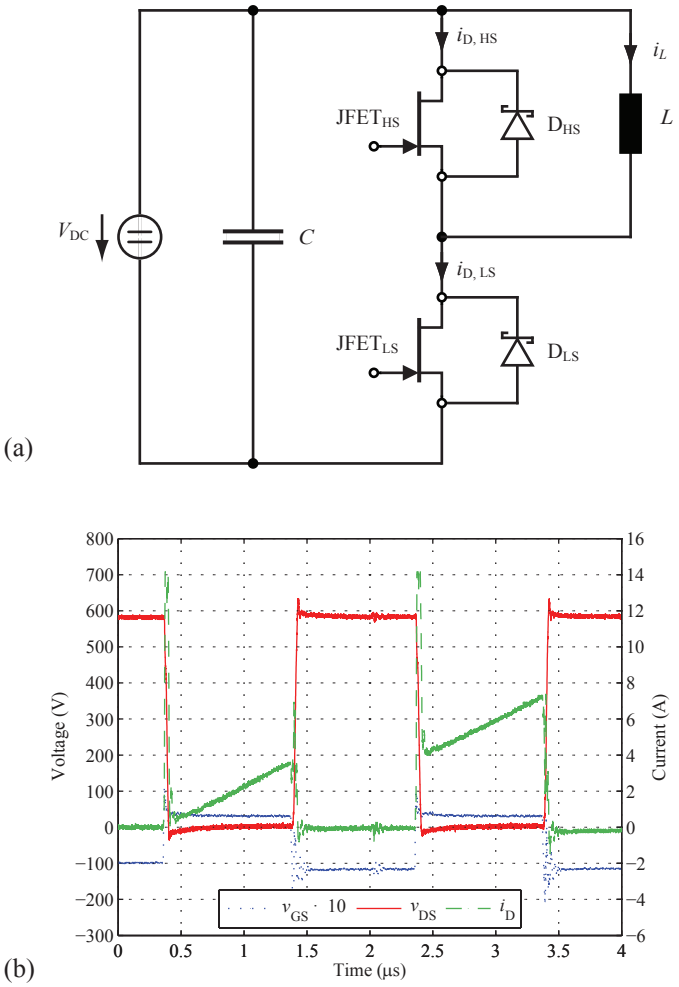

Fig. 9. (a) Test setup used for the validation of gate driver circuit. Half-bridge connection of 2 1200 V 30 A SiC normally-off JFETs with antiparallel freewheeling diodes (Schottky Barrier Diodes Infineon IDH15S120) and an inductive load. (b) Waveform patterns showing the drain current, drain-source and gate-source voltage of the low-side switch.

7 A at 125 °C which leads to a gate current of 200 mA for minimum on-resistance (*cf.* Fig. 4).

Using the D_{GS} characteristic (*cf.* Fig. 2, the values of R_G and R_S for DC current are already included as R_G, R_S and D_{GS} can hardly be measured separately under DC conditions) and considering D_{DC} as part of the load the gate driver has to supply, V_{CC} as an ideal voltage source and R_{DC} as the internal resistance of this voltage source (together with R_{GD}), the required values for V_{CC} and R_{DC} can be dimensioned. This is shown in Fig. 8 for different temperature levels of the Schottky diode D_{DC}: for 25 °C in case the diode is at room temperature level, and for 125 °C assuming the diode is placed close to hot devices or at high ambient temperatures. The results are $V_{CC} = 3.2\,V$ and $R_{DC} = 1.1\,\Omega$, if the gate driver circuit is operated at 25 °C as well as $V_{CC} = 3.1\,V$ and $R_{DC} = 0.9\,V$ at 125 °C gate driver temperature level.

For the choice of D_{DC} a low forward voltage drop for currents of a few hundred Milliamps is important to minimize the losses during the on-state of the JFET, which is why a

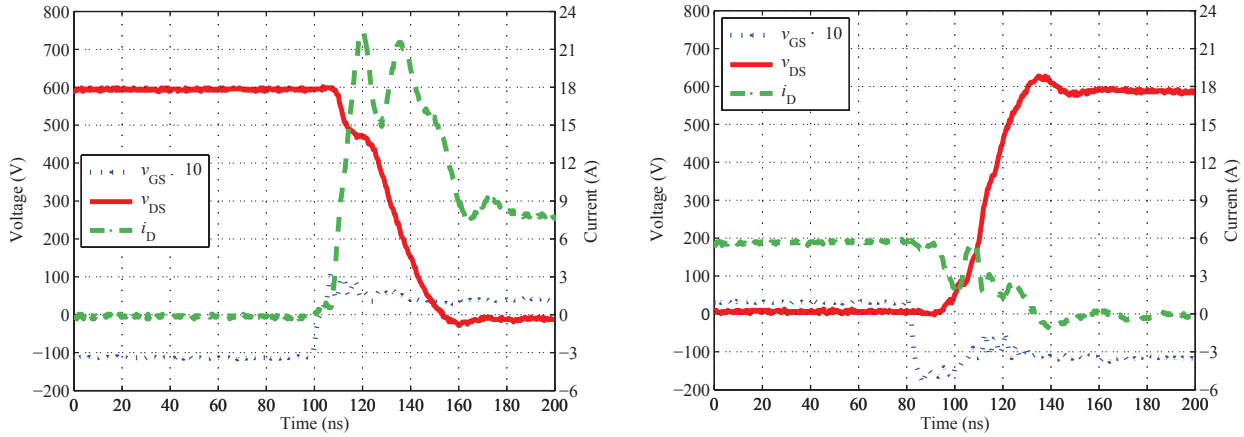

Fig. 10. Switching transient with the optimized gate driver circuit switching the JFET in an inductive load test circuit as shown in Fig. 9. Turn-on (a) and turn-off (b) are finished after 30 ns and 20 ns, respectively.

Schottky diode has been selected. Furthermore, the leakage current, that is for Schottky diodes higher than for pn-diodes, should be smaller than 3 mA for voltages around $V_{Z,D1}$ in order to minimize the gate driver losses in the off-state of the JFET. To achieve these requirements, an oversized 60 V 1 A Schottky diode in SMB package (IR 10BQ060) is chosen.

3) D_{AC}, D_2, D_4*:* The other Schottky diodes D_{AC}, D_2 and D_4 should also have a low forward voltage drop to limit the losses. IR 10MQ040NPbF diodes in SMA packages are selected.

4) D_3*:* The Zener diode D_3 determines the negative bias at the gate during the turn-off of the JFET. It is limited to -15 V due to leakage currents of D_{GS}. The Zener voltage should be chosen to this voltage level, so that the immunity against the Miller Effect is as high as possible and a high voltage can be applied to the unavoidable inductances in the D_1-D_2 path in order to feed the Miller charge through this path (and not through C_{GS}).

5) V_{EE}, D_1, R_{AC}*:* V_{EE} sets together with $V_{Z,D3}$ the voltage that C_{AC} is charged to during the off-state and that is applied to the gate during turn-on in addition to V_{CC}. As the AC voltage applied to the gate is limited to 15 V, C_{AC} should not be charged to more than 12 V, leading to $V_{EE} = 27\,\text{V}$. At the same time, it should not be charged to a significantly smaller value as a higher voltage aids in feeding current fast into the gate and to charge the gate quickly to the desired value. Hence, $V_{Z,D1}$ is chosen to 12 V. The differential resistance of the diode in reverse direction should be as small as possible to make sure the voltage drop across D_1 remains close to $V_{Z,D1}$ if the gate-drain capacitance is charged. If the switching speed has to be limited, R_{AC} can be increased starting from $0\,\Omega$.

6) C_{AC}*:* To guarantee a fast turn-on of the JFET, the charge stored in C_{AC} during the off-state must equal the gate-source charge, if C_{GD} is not charged (e. g. if the freewheeling diode is already conducting). If the gate-drain potential difference increases rapidly when the channel is turned on, the charge in C_{AC} must equal the sum of the gate-source and -drain charge.

The upper limit of the charge stored in C_{AC} is given by efficiency considerations, as the energy stored in C_{AC} is dissipated when the capacitance is charged. A capacitance value corresponding to charges larger than the lower limit mentioned in the last paragraph helps slightly to achieve fast turn-on as the voltage of capacitor decreases less fast in this case. Here, 6 nF are chosen for C_{AC}.

Furthermore, the difference in the leakage currents of D_1 and D_3 is stored in C_{AC} for typical off-times during converter operation. For off-times longer than several tens of microseconds the leakage currents of both diodes will match leading to a voltage distribution that is determined by their voltage-over-current characteristic and no longer simply by their Zener voltage.

III. Gate Driver Measurement Results

The gate driver circuit and resulting switching action has been tested in a half-bridge inductive test circuit with a SiC freewheeling diode as shown in Fig. 9 (a) with switching patterns as exemplarily shown in Fig. 9 (b) to validate the theoretical considerations.

The optimized gate driver has been tested for varying JFET drain currents. No noticeable change in behavior was discovered. Switching speed is practically independent of drain current at turn-on, and turn-off is faster for increased currents, as they charge the intrinsic drain-source capacitance faster. Moreover, the JFET was subjected to elevated temperatures up to 250 °C in part showing reduced switching speed, e. g. slower turn-on transients of approximately 50 ns at 175 °C and 16 A, which is expected due to the on-resistance increasing with temperature and therefore slower discharge of the drain-source capacitance at turn-on.

The EM SiC JFET is suitable for parallelization in order to increase current rating because of the positive temperature coefficient of its on-resistance. The 30 A device is in fact a parallelization of 2 identical chips. Symmetrical setup is of great importance for balanced currents in the parallel connections. If more chips are to be driven in parallel, the value of C_{AC} has to be increased accordingly and the design of

V_{CC} and R_{DC} has to be conducted according to Section II-C2.

IV. Conclusion

Against the background of increasing importance of SiC as a semiconductor material for power electronic devices, appropriate gate drivers for the already commercialized normally-off 1200 V 30 A SiC JFET with very promising performance in terms of the device losses have been of large interest and subject to many recent publications. These publications mention certain limitations of the proposed and partly very complex gate drivers with respect to noise immunity, possible duty cycles and switching frequencies as well as significant self-heating.

To fully exploit the potential of the SiC normally-off JFET and to make sure that it can also be used in power electronic converters with high switching frequencies, a novel gate driver topology is presented and dimensioned in this paper, after the exact demands for the gate driver are identified and analyzed in detail. The proposed gate driver meets the requirements of the SiC normally-off JFET while using only one standard gate driver IC, one capacitor, two resistors and six diodes: It delivers the required charge very fast during turn-on of the switch by means of a pre-charged capacitor. During turn-off, a low impedance path quickly removes the charge from the gate and negative biasing during the off-state allows the gate-drain capacitance to be charged via a low impedance path without the risk of turning the JFET unintentionally on. During the on-state, the gate driver delivers up to 300 mA at a gate-source voltage of only 2.5 V without significant self-heating to make sure that the JFET is operated with the lowest possible on-resistance.

Finally, measurement results are provided showing that this gate driver offers fast turn-on and -off of the switch while still having a high noise immunity and allowing operation at all duty cycles and at high switching frequencies. The latter is especially important to enable promising SiC power semiconductors like the SiC normally-off JFET to prove the superior performance in power electronic converters.

References

[1] G. Pensl, F. Ciobanu, T. Frank, M. Krieger, S. Reshanov, F. Schmid, and M. Weidner, *SiC Materials and Devices*, ser. Selected Topics in Electronics and Systems, Vol. 40. World Scientific Publishing Co. Pte. Ltd., 2006, vol. 1, ch. SiC Material Properties, pp. 1–41.

[2] G. L. Harris, *Properties of Silicon Carbide*, ser. EMIS Datareviews Series, no. 13, INSPEC, Ed. Institution of Engineering and Technology, 1995.

[3] T. Ayalew, "SiC semiconductor devices technology, modeling, and simulation," Ph.D. dissertation, Technical University Vienna (Austria), January 2004. [Online]. Available: http://www.iue.tuwien.ac.at/phd/ayalew/

[4] A. Melkonyan, "High efficiency power supply using new sic devices," Ph.D. dissertation, University of Kassel (Germany), February 2007.

[5] R. Callanan, A. Agarwal, A. Burk, M. Das, B. Hull, F. Husna, A. Powell, J. Richmond, S.-H. Ryu, and Q. Zhang, "Recent progress in SiC DMOSFETs and JBS diodes at Cree," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, nov. 2008, pp. 2885 –2890.

[6] J. Biela, M. Schweizer, S. Waffler, B. Wrzecionko, and J. W. Kolar, "SiC vs. Si - evaluation of potentials for performance improvement of power electronics converter systems by SiC power semiconductors," *Materials Science Forum*, vol. 645 - 648, pp. 1101–1106, Silicon Carbide and Related Materials 2009.

[7] P. Friedrichs, "Silicon Carbide power devices - status and upcoming challenges," in *Proc. European Conference on Power Electronics and Applications*, 2007, pp. 1–11.

[8] B. Wrzecionko, J. Biela, and J. Kolar, "SiC power semiconductors in HEVs: Influence of junction temperature on power density, chip utilization and efficiency," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, nov. 2009, pp. 3834 –3841.

[9] M. Treu, R. Rupp, P. Blaschitz, K. Ruschenschmidt, T. Sekinger, P. Friedrichs, R. Elpelt, and D. Peters, "Strategic considerations for unipolar SiC switch options: JFET vs. MOSFET," in *42nd IAS Annual Meeting Industry Applications Conference Conference Record of the 2007 IEEE*, 2007, pp. 324–330.

[10] R. Kelley, A. Ritenour, D. Sheridan, and J. Casady, "Improved two-stage DC-coupled gate driver for Enhancement-Mode SiC JFET," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, feb. 2010, pp. 1838 –1841.

[11] R. L. Kelley, M. Mazzola, S. Morrison, W. Draper, I. Sankin, D. Sheridan, and J. Casady, "Power factor correction using an enhancement-mode SiC JFET," in *Proc. IEEE Power Electronics Specialists Conference PESC 2008*, 2008, pp. 4766–4769.

[12] M. S. Mazzola and R. Kelley, "Application of a normally off Silicon Carbide power JFET in a photovoltaic inverter," in *Proc. Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition APEC 2009*, 2009, pp. 649–652.

[13] SemiSouth, "Application note AN-SS1: Silicon Carbide Enhancement-Mode Junction Field Effect Transistor and recommendation for use," SemiSouth Laboratories, Inc., Application Note, 2009.

[14] R. Kelley, R. Fenton, and D. Schwob, "Optimized gate driver for Enhancement-Mode SiC JFET," in *Proceedings of the International PCIM Europe 2009 Conference*, Nuremberg, Germany, May 2009.

[15] S. Laboratories, *Two-Stage Opto Coupled Gate Driver Demo Board*, rev 1.2 ed., SemiSouth Laboratories, Inc., 201 Research Boulevard, Starkville, MS 39759 USA, February 2010.

[16] D. Stephani and P. Friedrichs, *SiC Materials and Devices*, ser. Selected Topics in Electronics and Systems, Vol. 43. World Scientific Publishing Co. Pte. Ltd., 2006, vol. 2, ch. Silicon Carbide Junction Field Effect Transistors, pp. 75–104.

[17] S.-H. Ryu, S. Krishnaswami, M. O'Loughlin, J. Richmond, A. Agarwal, J. Palmour, and A. Hefner, "10-kV, 123-mΩcm^2 4H-SiC power DMOSFETs," *Electron Device Letters, IEEE*, vol. 25, no. 8, pp. 556 – 558, aug. 2004.

[18] I. SemiSouth Laboratories, *Normally-OFF Trench Silicon Carbide Power JFET (Datasheet)*, 1st ed., SemiSouth Laboratories, Inc., 201 Research Boulevard Starkville, MS 39759 USA, May 2009.

[19] C. Wilhelm, D. Kranzer, and B. Burger, "Development of a highly compact and efficient solar inverter with Silicon Carbide transistors," in *Proceedings of the 6th International Conference on Integrated Power Electronics Systems*, 2010.