SiC vs. Si – Evaluation of Potentials for Performance Improvement of Power Electronics Converter Systems by SiC Power Semiconductors

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Abstract. Switching devices based on wide band gap materials as SiC offer a significant performance improvement on the switch level compared to Si devices. A well known example are SiC diodes employed e.g. in PFC converters. In this paper, the impact on the system level performance, i.e. efficiency/power density, of a PFC and of a DC-DC converter resulting with the new SiC devices is evaluated based on analytical optimisation procedures and prototype systems. There, normally-on JFETs by SiCED and normally-off JFETs by SemiSouth are considered.

Introduction

In power electronic systems there has been a continuous trend towards a higher system power density in the last decades and due to environmental concerns and rising energy costs, also the efficiency of the systems became an important system performance criteria, over the past years besides costs. For meeting these demands, the development of power semiconductors is a crucial enabling factor besides passive components, control, cooling and EMC.

With the recent technological progress in manufacturing power devices based on wide band gap materials as e.g. silicon carbide (SiC) or gallium nitride (GaN), the operating voltage range, the switching speed and/or specific on-resistance have been and will be improved significantly compared to silicon power devices. In case these new devices are applied in power electronic systems, the improvements on the device level will impact also the system performance, which is usually measured by power density, efficiency, weight, reliability, and costs.

In this paper, the system level performance of a single phase PFC converter and of an isolated DC-DC converter, which is achievable with the new SiC devices, is evaluated by means of analytical optimisation algorithms, which provide a design that enables an optimal usage of the features of the new devices. The models used in optimisation algorithms have been verified by measurements on prototype system.

In hard switched applications, SiC Schottky diodes already proved a significant loss reduction and an increase of efficiency/power density. Also switching losses can be reduced enabling either a higher efficiency or an higher switching frequency, i.e. higher power density.

Additionally, SiC devices offer the advantage of high temperature operation. However, the application of this feature is limited by the available packaging technology, the reliability, which significantly decreases with increasing temperature, and the temperature limit of commercial electronic components as gate drive, control IC or capacitors, which is usually below 125°C and which make the design of a high temperature SiC system considerably more complicated and costly. Therefore, a limitation of T_j below 175°C is assumed here.

Before the system performance of the PFC and the DC-DC converter is evaluated in Section III and Section IV, first the specifications of the applied SiC devices is shortly presented in Section II.

Data of SiC Switches

In the following the performance of current SiC devices considered in the system performance evaluation is discussed. There, the focus is on devices, which are relatively mature and which could become commercially available soon.

In Table 1 the data of the SiC devices is listed for the normally-on JFETs by SiCED and the normally-off JFET (SJEP120R125) by SemiSouth. Besides the breakdown voltage and the $R_{DS(on)}$ at T_j=25°C, also the specific output capacitance and the figure of merit FOM = $\frac{1}{R_{DS(on)}E_{400V}}$, which are important for hard switched applications, are listed. Furthermore, the data of the reference Si devices is given. For soft switching applications, the switching losses and also the output capacitance plays only a minor role and the main focus is on the specific $R_{DS(on)}$, which determines how much chip area is required for achieving a specific performance/efficiency.

In the table, the significant improvement of the specific $R_{DS(on)}$ with SiC devices could be clearly seen, so that lower conduction losses at a given chip area can be expected with SiC devices. However, looking at the specific output capacitance, the SiC devices do not offer an improvement yet. A tremendous reduction as with the $R_{DS(on)}$ could not be expected, as with the shrinking die area, also the length of the drift region must become smaller, in order to limit the resistance of the drift region.

The 1.2kV JFET from SemiSouth has a relatively low capacitance value, which also results in a relatively high FOM. There, it is important to note, however, that due to the vertical channel, which is required for the normally-off behaviour of the JFET, the $R_{DS(on)}$ basically depends significantly on I_D at higher current densities and – especially at higher temperatures – the increase of $R_{DS(on)}$ will result in a significant deterioration of the FOM.

Also with the other SiC devices, the $R_{DS(on)}$ increases with rising T_j, what finally also results in a reduction of the FOM. This reduction, however, is not as large as with the JFETs by SemiSouth at higher current densities. In applications striving for high efficiency, the current density in the switches is limited to relatively small values in order to reduce the conduction losses, so that this disadvantage of the SemiSouth JFETs does not have a significant effect.

Due to the $R_{DS(on)}$ of the JFETs, which increases more than linearly with T_j, there is an optimal operation T_j with respect to a maximal current density [4]. At higher junction temperatures than the optimal one, the current density must be decreased in order to avoid a thermal runaway.

Table 1: Current status of SiC switches. Further information could be e.g. found on [1, 2]. E_{400V} is the energy stored in the output capacitance, when charged form 0V...400V, and the figure of merit FOM=$1/\left(R_{DS(on)}E_{400V}\right)$ is a performance index for hard switching [3]. As max. I_D depends significantly on the cooling, the values should just give a hint on the capabilities of the switch for operation at $T_j \geq 125$°C. The (specific) $R_{DS(on)}$ is given for 25°C and for the total chip area and for $R_{DS(on)}$ typical values are depicted.

	$V_{(BR)DSS}$	I_D	$R_{DS(on)}$	$R_{DS(on)}A_{Chip}$	C_{Out}/A_{Chip}@25V	FOM	A_{Chip}	E_{400V}
JFET (SiCED)	500V	∼5A	0.2Ω	11.5mΩcm^2	59.3pF/mm^2	0.37	5.76mm^2	13.4μJ
JFET (SiCED)	1.2kV	∼5A	0.33Ω	19mΩcm^2	35.7pF/mm^2	0.33	5.76mm^2	9.1μJ
JFET (SiCED)	1.2kV	∼17A	0.12Ω	21mΩcm^2	35.6pF/mm^2	0.3	17.3mm^2	28.2μJ
JFET (SemiSouth)	1.2kV	>15A	0.125Ω	5mΩcm^2	24.5pF/mm^2	∼1.65	4mm^2	4.9μJ
MOSFET (Cree)	1.2kV	>20A	0.075Ω	12.5mΩcm^2	39pF/mm^2	0.76	16.6mm^2	17.5μJ
Si Reference Devices								
IPP60R099CP	650V	31A	0.09Ω	25.2mΩcm^2	130pF/mm^2	0.97	28mm^2	11.5μJ
APT50M75B2	500V	57A	0.075Ω	90mΩcm^2	9.8pF/mm^2	0.53	120.1mm^2	25.1μJ
STW77N65M5	650V	41A	0.03Ω	≈21.3mΩcm^2	≈6pF/mm^2	1.94	≈71mm^2	17.2μJ

The transient behaviour of the 1200V JFETs by SiCED and by SemiSouth shows similar $\mathrm{d}i/\mathrm{d}t$ & $\mathrm{d}v/\mathrm{d}t$ values at turn on and different values at turn off because of the different drain source capacitance values. Both devices turn on faster than 50ns and the turn off transient is mainly governed by the parasitic output capacitance of the devices.

Single Phase Rectifier

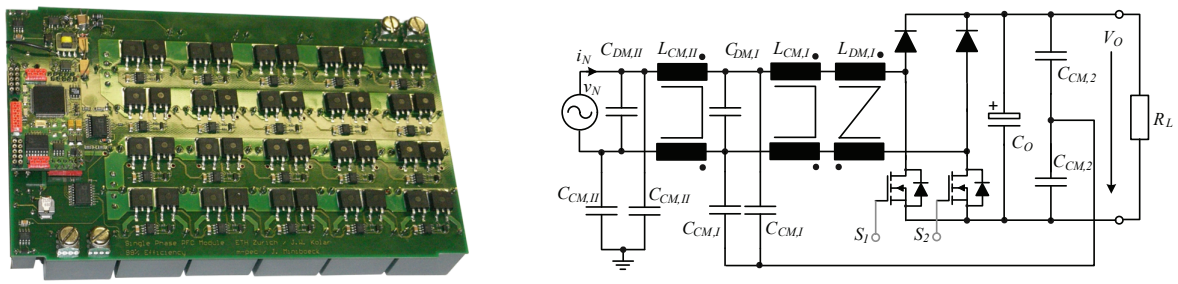
A typical low voltage application in the kW range with hard switching are PFC converters, where the switching losses only can be avoided with relatively complex soft switching topologies, which have not gained a significant market share so far. Such hard switched PFC converters are e.g. applied in telecom power supplies. There, a major driving force has been the power density besides costs. Due to rising energy prices and the continuous operation of such systems, the efficiency became more and more important, so that now a multi-criteria optimisation of such systems as shown in [3] is necessary for determining the optimal set of design parameters. In [3] a ultra efficient PFC system with 99.1% efficiency (cf. Fig. 1a) and a highly compact system with a power density of almost $6\mathrm{kW/dm^3}$ are presented.

This ultra high efficiency PFC converter is based on Si CoolMOS devices and in the following, the achievable performance with SiC devices is evaluated. Further details about the design can be found in [3].

For the prototype system a bridgeless PFC system has been chosen, as the conduction losses are in principle lower than with a standard boost PFC [3]. Furthermore, a capacitive coupling between the mains and the output is inserted to limit the CM noise [3]. During normal operation one switch is always closed and the other one is shaping the input current and controlling the power flow by PWM.

For identifying the set of design parameters, which result in the maximal efficiency, analytical models of the converter including the magnetic components, EMI filter and the thermal design as well as an automatic optimisation procedure have been developed [3]. With this procedure the optimal geometric design of the inductors, the turn number as well as the optimal chip area for the MOSFETs and the diodes is determined. There, the on-resistance as well as the parasitic capacitances are considered for evaluating the semiconductor losses.

Based on this procedure the optimal parameters for the Si and the SiC devices for different cases as shown in Fig. 2 have been determined. Due to the relatively high specific output capacitance of the 500V JFET and the resulting low FOM, the efficiency and the power density are lower with the SiC devices than with the Si reference MOSFETs + SiC diodes.



(a) (b)

Fig. 1: a) Prototype of the efficient 3.2kW dual-boost PFC rectifier composed of two interleaved 1.6kW units with an input voltage of 230V and an output voltage of 365V; dimensions: 275x130x85mm; power density: 1.1 kW/l. b) Circuit diagram of the dual boost rectifier with capacitive coupling.

The optimal area for the 500V JFET is 37mm^2, which is approximately 28% of the Si MOSFET area. With the low specific capacitance of the 1.2kV JFET by SemiSouth, a slightly better efficiency could be achieved at a chip area of 30mm^2, i.e. 23% of the area of the Si MOSFET. A SemiSouth JFET with a lower blocking voltage could probably achieve a higher efficiency, but is not available at the moment.

The power density is roughly the same for all three designs and just varies slightly due to the different semiconductor packages and the number of parallel connected devices. There, the major share of the volume is occupied by the passives and all components are naturally cooled.

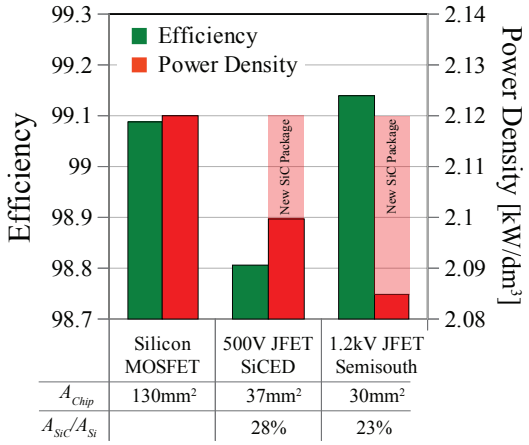


Fig. 2: Efficiency and power density for an optimised PFC system with Si MOSFETs (IPP60R099CP), 500V and 1200V JFETs.

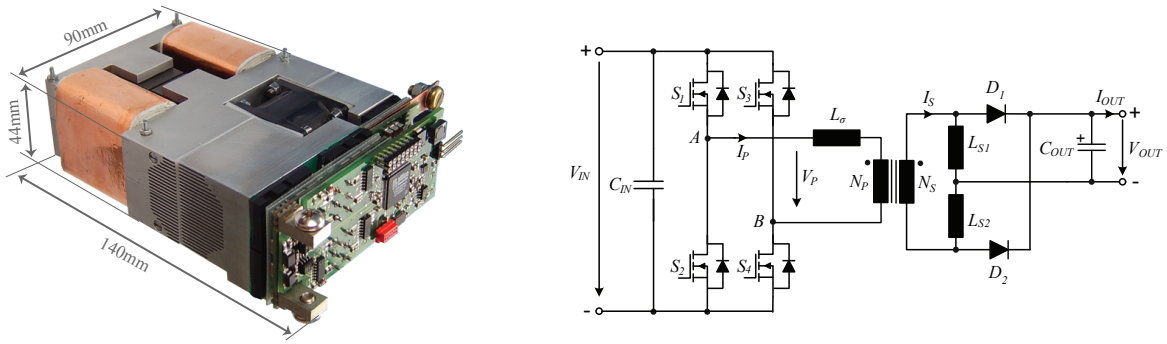
The major benefit of SiC for hard switched applications are the Schottky diodes, which show no reverse recovery losses and which have a forward voltage drop comparable to Si diodes.

DC-DC Converter

As a 2nd example an isolated DC-DC converter for telecom power supplies is considered. There, the most important performance criteria are costs and power density, besides efficiency.

Here, a phase-shift converter with current doubler rectifier as shown in Fig. 3 is considered. The design of the converter is based on an optimisation algorithm, which includes also the thermal/electromagnetic design besides the electrical model. Further details on the design/optimisation procedure can be found in [5].

Due to the leakage inductance L_σ of the transformer and the phase shift modulation, all four switches operate under ZVS condition resulting in negligible switching losses at a very low effort on circuit and control side. Thus, only the conduction losses and therewith the $R_{DS(on)}$ is interesting. For achieving ZVS conditions, a minimum output capacitance is required, which depends on the switching speed. With a smaller capacitance, witching losses increase, but can help to increase part load efficiency.

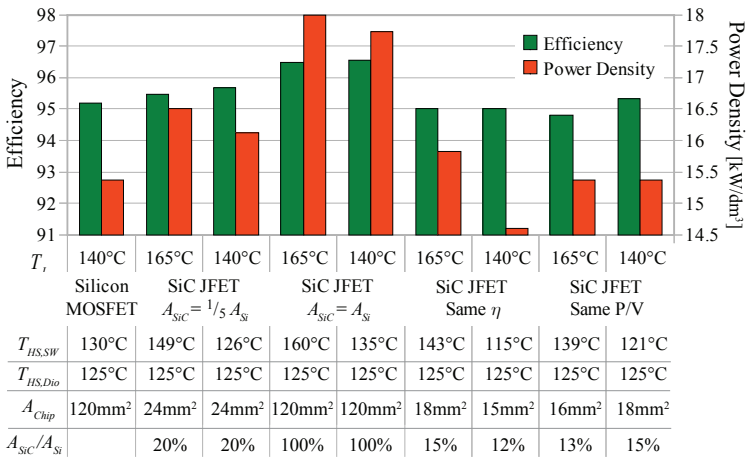


(a) (b)

Fig. 3: a) 5kW prototype of the 400V/48V...54V phase-shift full bridge converter with current doubler rectifier: Height: 1U, volume: 0.56dm^3, power density: 9kW/dm^3. b) Schematic of the converter.

In spite of the negligible switching losses, the optimal switching frequency of the converter, which results in maximal power density, is just 200kHz. Increasing the frequency results in a smaller power density and efficiency [6].

Based on the optimisation procedure, the full-bridge converter has been optimised with the data of the APT50M72B2 from Microsemi and for the 500V normally-on JFET from SiCED. For the details about the optimisation please refer to [5].



T_j	140°C	165°C	140°C	165°C	140°C	165°C	140°C	165°C	140°C
	Silicon MOSFET	SiC JFET $A_{SiC}=1/5\,A_{Si}$		SiC JFET $A_{SiC}=A_{Si}$		SiC JFET Same η		SiC JFET Same P/V	
$T_{HS,SW}$	130°C	149°C	126°C	160°C	135°C	143°C	115°C	139°C	121°C
$T_{HS,Dio}$	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C
A_{Chip}	120mm²	24mm²	24mm²	120mm²	120mm²	18mm²	15mm²	16mm²	18mm²
A_{SiC}/A_{Si}		20%	20%	100%	100%	15%	12%	13%	15%

Fig. 4: Efficiency/power density for the DC-DC converter with Si MOSFETs (APT50M75B2) and/or the 500V JFETs for the cases where the chip area of the SiC devices is 1/5 ($A_{SiC}=1/5 A_{Si}$) and the same ($A_{SiC}=A_{Si}$) of the one of the Si MOSFET and for the cases where the SiC chip area is scaled so that the converters have the same η or P/V. For the SiC devices a 140°C and a 165°C limit for the junction temperature and separate heat sinks for the Si rectifier diodes and the switches of the full-bridge have been assumed. Below the graph, the heat sink temperature $T_{HS,SW}$ of switch and $T_{HS,Dio}$ of the rectifier diodes is given. In the power density only the net component volume is included, i.e. the power density decreases by roughly 1/3, due to mounting/insulation requirements and due to geometrically not matching component housings.

In Fig. 4 the results for the case, where the chip area of the SiC devices is fixed to 1/5 and/or to 1/1 of the Si MOSFET and where the chip area is adapted, so that the efficiency η and/or the power density P/V is the same for the Si and the SiC based converter are shown. In all cases, results for a junction temperature limit of the SiC JFET of 140°C and of 165°C are shown and it is assumed that the switches of the full-bridge are mounted on a different heat sink than the output rectifier diodes. With $T_j \leq 165$°C the heat sink temperature reaches a peak temperature of 160°C for the case $A_{SiC}=A_{Si}$, what requires a thermal isolation between the heat sink and the other components. Limiting the heat sink temperature to lower temperatures with a junction temperature of 165°C is not reasonable since this case only could be achieved by artificially deteriorating the thermal resistance between junction and heat sink.

The calculated peak power density of 18kW/dm^3 also has to be considered against the background of the high heat sink temperature, because a thermal isolation is not included in the power density calculation, so that in the real system the power density might be lower.

For achieving the same efficiency with SiC devices app. 12% to 15% of the chip area is required for the SiC JFET. Due to the higher thermal resistance of the smaller SiC devices the high power density only could be achieved by increasing the junction and the heat sink temperature. With $T_j = 140$°C the power density decreases from 15.4kW/dm^3 to 14.6kW/dm^3.

The same power density could be achieved if the the SiC devices have 13% to 15% of the Si MOSFET chip area. There, with a lower junction temperature a bit a higher efficiency could be achieved with the SiC devices as the $R_{DS(on)}$ increases with T_j.

Conclusion

Currently, SiC switching devices show very fast turn on/off transients (comparable to Si MOSFETs) and low specific $R_{DC,on}$, which are significantly lower than the ones of unipolar Si devices. However, due to the relatively high output capacitance, the figure of merit $1/R_{DS(on)}/E_{Out}$,

which is important for hard switching, is not better than the one of Si devices. This is confirmed by the efficiency optimisation results for a 1-Φ PFC converter, where some of the JFETs by SiCED are worse than the Si switches and only the JFETs by SemiSouth show an slight improvement from 99.09% to 99.14% efficiency. However, it is important to note, that the SiC freewheeling diodes offer an substantial improvement, as has been shown in various publications. It is also important to bare in mind, that the SiC devices are relatively young and will improve significantly in future. Furthermore, at higher operating voltage levels, there are no superjunction FETs and if a fast switching speed is required, SiC components show a significantly better performance than Si ones.

In the area of low voltage DC-DC converter, where very often soft switching conditions can be achieved with low effort, SiC devices mainly offer the possibility to reduce the chip area for a desired efficiency. This could help to increase the power density. Due the limited space in this publication, the results proofing this statement using the example of a non-isolated bidirectional buck boost converter must have been omitted but will be provided in an IEEE journal publication. There, also results for inverter drives are given.

For isolated DC-DC converter, for which a phase shift converter with current doubler rectifier has been evaluated in the paper, the main benefit is an improvement of power density and efficiency. There, however, the costs for the SiC devices play an important role, since these benefits often can be realised by significantly increasing the costs for the semiconductors. This might change in future if the prize of SiC devices drops.

Besides the semiconductors, in all the high performance systems, passive components, isolation issues and converter design also play an important role and are often the limiting devices. A good example are motor drives, where the dv/dt often must be reduced even with IGBTs, in order not to harm the isolation of the windings or to limit capacitive charging currents.

Besides SiC also other WBG materials as e.g. gallium nitride (GaN) show interesting properties and theoretically enable a tremendous reduction of the specific $R_{DS(on)}$, which has an even lower theoretical limit than SiC. Furthermore, the processing of the material is simpler and might allow a faster decrease of production costs than is possible with SiC.

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