Performance Trends and Limitations of Power Electronic Systems

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***Abstract*—In 2003 the Roadmapping Initiative of the European Center of Power Electronics (ECPE) has been started based on a future vision of society in 2020 in order to define the future role of power electronics, and to identify technological barriers and prepare new technologies well in time.**

In the framework of this initiative a new mathematically supported approach for the roadmapping in power electronics has been developed. As described in this paper the procedure relies on a comprehensive mathematical modeling and subsequent multi-objective optimization of a converter system. The relationship between the technological base and the performance of the system then exists as a mathematical representation, whose optimization assures the best possible exploitation of the available degrees of freedom and technologies. Thus an objective Technology Node of a system is obtained, whereby physical limits are implicitly taken into account. Furthermore, the sensitivity of the system performance with regard to the technological base can be calculated directly and the internal interdependence of Performance Indices directly studied. Accordingly, the improvement in performance achievable by improvements in the technology base can be tested and assessed in advance. Moreover, different system concepts, i.e. circuit topologies, control procedures, etc. can be evaluated and directly compared with regard to achievable efficiency, power density and costs in the form of the associated Pareto Front which defines the boundary of the Feasible Performance Space. If the target performance lies outside the Pareto Envelope of known system concepts and state-of-the-art technologies, a new technology must be employed. The necessity of a technological leap, i.e. the introduction of a Disruptive Technology can thus be recognized at an early stage. This offers an excellent basis for effective roadmapping for various main application areas in power electronics.

I. Introduction

Technology roadmaps show the temporal organization and quantification of the further development of a technology and are used by industry for effective medium and long term planning of research and development activities. Technology gaps and/or the necessity of a technology change are in this way recognized at an early stage and suitable research can be started in time. Furthermore, roadmaps provide public institutions orientation for the funding of research of new generations of technology and give users security with regard to the longer term availability of a technology. Finally, the vision implied in a roadmap creates a basis for the cooperation of research institutes with industry, which potentially leads to innovative solutions. Correspondingly, the large power electronics research centres

- ECPE (European Center for Power Electronics, EU [1]),
- CPES (Center for Power Electronics Systems, USA [2]) and
- AIST-PERC (Japan National Institute of Advanced Science and Technology - Power Electronics Research Center [3])

have organized since 2005 meetings, i.e. the

- AIST Power Electronics New Wave Workshops in 2005, 2006, and 2008, the
- CPES Technology Roadmap Workshops in 2005, 2006, and 2008, and the
- ECPE Workshops on Power Electronics Research and Technology Roadmaps in 2007, and 2009,

in order to collectively draw up global roadmaps, based on previous work at the individual centres for the main application areas of power electronics and to discuss important topics of future research. Moreover, through collective declarations, the importance of power electronics as an enabling technology should be underlined.

On the part of universities, J.D. van Wyk, with wide vision, started already in 1991 a series of Workshops on the Future of Electronic Power Processing and Conversion (FEPPCON, [4]) in which international participants from universities and industry considered the long term further development of the field and identified new technologies of fundamental importance. Thus already within the framework of the first workshop in 1991, the importance of integration, packaging and reliability was pointed out [5], the future relevance of environmental compatibility and the recycling of power electronics converters emphasized and the increasing manufacture of converters as integrated building blocks forecast. Furthermore, in 1994 at the 2$^{\mathrm{nd}}$ FEPPCON the potential limitation of the further development of power electronics by the materials available for

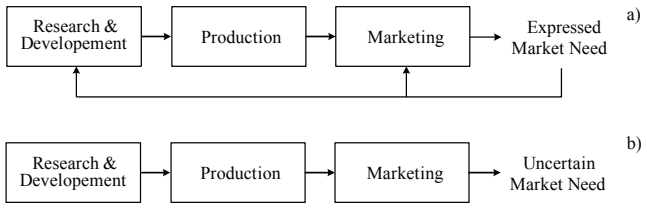


Fig. 1. Demand-pull a) and technology-push b). A technology-push implies that a new invention is pushed onto the market without prior analysis of the user needs. In contrast, an innovation based on demand(market)-pull is in response to an identified market need.

the realization of passive power components was underlined [4], a limitation that today, 15 years later, is becoming clearly felt.

Also in 1991, on the part of the US-based Power Sources Manufacturing Association [6], a Power Technology Workshop was established to determine the state of the technology and to draw up quantitative roadmaps for further developments in IT power supplies over 5 years. The workshop, which takes place every three years and each time defines the requirements of the following 5 years, is widely supported by the inclusion of original equipment manufacturers (OEMs), as well as the manufacturers of power supplies and components. This approach will be generalized to other main application areas by the abovementioned initiative of ECPE, CPES and AISTPERC, which aims at prediction of research and development requirements over 15 years, similarly to the ITRS (International Technology Roadmap for Semiconductors [7]) in the field of integrated circuits.

General considerations on the division of power electronics into Application Technology Spaces with specific roadmaps, as well as on the temporal structuring of roadmaps and on the choice of the performance goals [8], can offer support here. Furthermore, the representation of the development of power semiconductor technology with the aid of Figures of Merit (FOM) [9] forms an important basis.

The preparation of a roadmap can in principle be carried out on the basis of an extrapolation of current product lines and technologies or on retrapolation from future scenarios.

Power electronics converters assume in many applications only a supporting partial function, which enables a main function to be realized, but does not itself represent the main function. Hence power electronics, as also microelectronics, is not primarily driven by new technologies. On the contrary, the development of new technologies takes place as a reaction to market requirements that cannot be fulfilled by existing concepts. Thus the innovation follows a market-pull or demand-pull (Fig.1a). Correspondingly, roadmaps are designed starting from the state of the technology by extrapolation. Examples are to be found in the ITRS [7], the roadmap of the PSMA [6], the roadmap of the Freedom Car Partnership [10] or also in one of the core ideas of the CPES - standardize/modularize/integrate - which had the goal to initiate a transition from complex, application specific converter systems to modular, integrated building blocks that can be manufactured at low cost, and which triggered a series of innovations.

Alternatively, new technological requirements and an associated roadmap can also be defined by backward projection of comprehensive future societal drafts. Examples are the Pictures of the Future [11] and the Strategic Technology Roadmap for the Energy Sector by the Japanese METI (Ministry of Economy, Trade and Industry [12]). Resulting from the Energy Technology Vision 2100, a long term strategy is thereby drawn up for the further development of energy technologies and for the redesign of the entire energy system; power electronics is named explicitly as an important cross boundary technology. In this connection, for example, the Vision of the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center [13] established by the National Science Foundation (USA) 2008 should be noted, which is preparing a revolutionary new energy distribution system, an "Internet of Electrical Energy", that is based upon power electronics, communication of high bandwidth, and distributed control/regulation. This shows clearly that retrapolation of future systems can lead to fundamentally new concepts and indirectly also trigger a technology-push (Fig.1b).

The Roadmapping Initiative of the ECPE which was started in 2003 to realize demonstrators for determining the state of the technology also refers to a future vision of society in 2020 that is based on megatrends (Fig.2, [16]). Starting from this

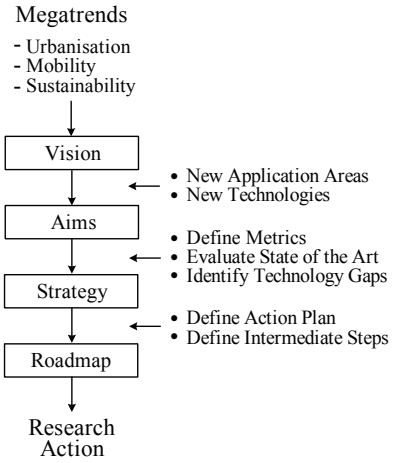


Fig. 2. Active roadmapping approach of the European Center for Power Electronics (ECPE). Roadmaps are established for key application areas of power electronics systems, i.e. for power generation/transmission/distribution, large drives, high performance motor drives, small drives for home appliances, high frequency power conversion - P <1kW, high frequency power conversion – P >1kW, automotive power electronics, aerospace power electronics, and future (renewable) energy sources.

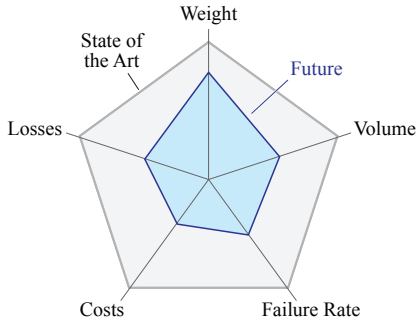


Fig. 3. State of the art and required future performance improvement of power electronics systems. The system performance is characterized by relative quantities, i.e. Performance Indices like output power density ρ (kW/dm^3), efficiency η, output power per unit weight γ (kW/kg), output power related to costs σ (kW/\$), and failure rate (MTBF^{-1}). Further improvement trends like shorter development cycle time or shorter time-to-market for custom designs [6] are not shown.

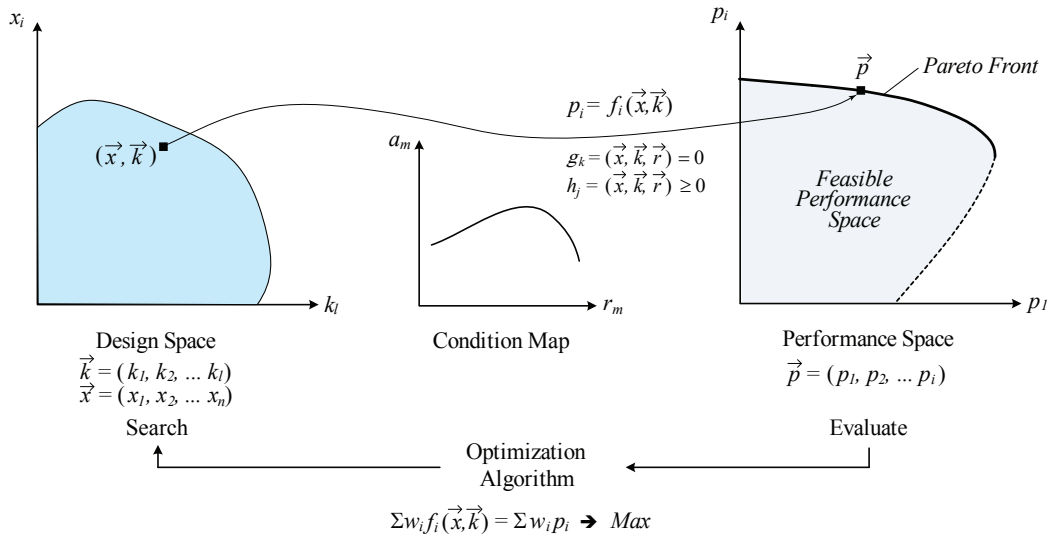


Fig. 4. Abstraction of the design and multi-objective optimization of a power electronics converter as mapping of a multi-dimensional Design Space (or Decision Space) into a multi-dimensional Performance Space (Objective Space). The boundary of the Feasible Performance Space is defined by the Pareto Front which indicates the best possible compromise with respect to different performance indices [14]. In case the whole mission profile of a converter is considered for the optimization, a probability density a_m is assigned to the various operating points, resulting in a multi-dimensional Condition Map [15].

vision, the future role of power electronics is sketched and strategic technological and market economy goals are defined. After an analysis of the state of the technology, a strategy is worked out to overcome technological barriers and achieve the goals, and a set of Performance Indices is defined that enable the strategy to be implemented in a quantitative plan of action with measurable intermediate goals in 2010 and 2015. The fundamental trends given here for the further development of power electronics converters are shown in Fig.3.

The Performance Indices considered in the course of roadmapping are mutually coupled. Thus, for example, high power densities imply high frequencies, which potentially lead to a reduction in efficiency. But this coupling has previously flowed into the definition of goals of roadmaps only via the experience of the engineers and researchers involved. Moreover, it is generally not checked whether a desired target performance is fundamentally achievable [17] on the basis of given materials (which typically, within the framework of a roadmap encompassing only 5 to 10 years, will experience no essential change).

Finally, in the implementation of the roadmap, a clear picture of the performance achievable through individual concepts (circuit concepts, control procedures and operating modes) based on state-of-the-art technologies is missing. Furthermore, the effect of a change in the technology base, e.g. of an improvement of the FOM of the employed power semiconductors on the target performance is not well known, which could hinder the effective introduction of new technologies.

As shown by the present work, these deficits can be removed by mathematical modeling and subsequent multi-objective optimization of converter systems [14]. The relationship between the technological base and the performance of a system then exists as a mathematical representation, whose optimization assures the best possible exploitation of the available degrees of freedom and technologies. Thus an objective Technology Node of a concept is obtained, whereby physical limits are implicitly taken into account. Furthermore, the sensitivity of the system performance with regard to the technological base can be calculated directly and the internal coupling of Performance Indices directly studied.

This new approach was developed within the framework of the Roadmapping Initiative of the ECPE started in 2003, is generally applicable and has already been successfully employed for the realization of ultra-compact and ultra-efficient demonstrators of single-phase PFC rectifier systems and telecom DC/DC converter systems [14], [18]. In the following, in Chapter II, the mathematical abstraction and multi-objective optimization, i.e. determination of the Pareto Front of a generalized converter system is shown and the definition of the Technology Node is explained. Then, in Chapter III, follows the description of the determination of the state of the technology of a class of converters with reference to the envelope of the Pareto Fronts of various circuit concepts. Furthermore, the interdependence of Performance Indices, as well as the technological sensitivity of the Performance Indices is analyzed. Moreover, technological limits to the system performance are discussed and the progress of the development of converter systems is illustrated with the aid of technology S-curves. Finally, in Chapter IV, tasks of future research are briefly described and new fields of application of power electronics are identified.

II. Mapping of Component Technologies into System Performance

In the course of designing industrial power electronics systems, the goal is generally to comply with the specifications

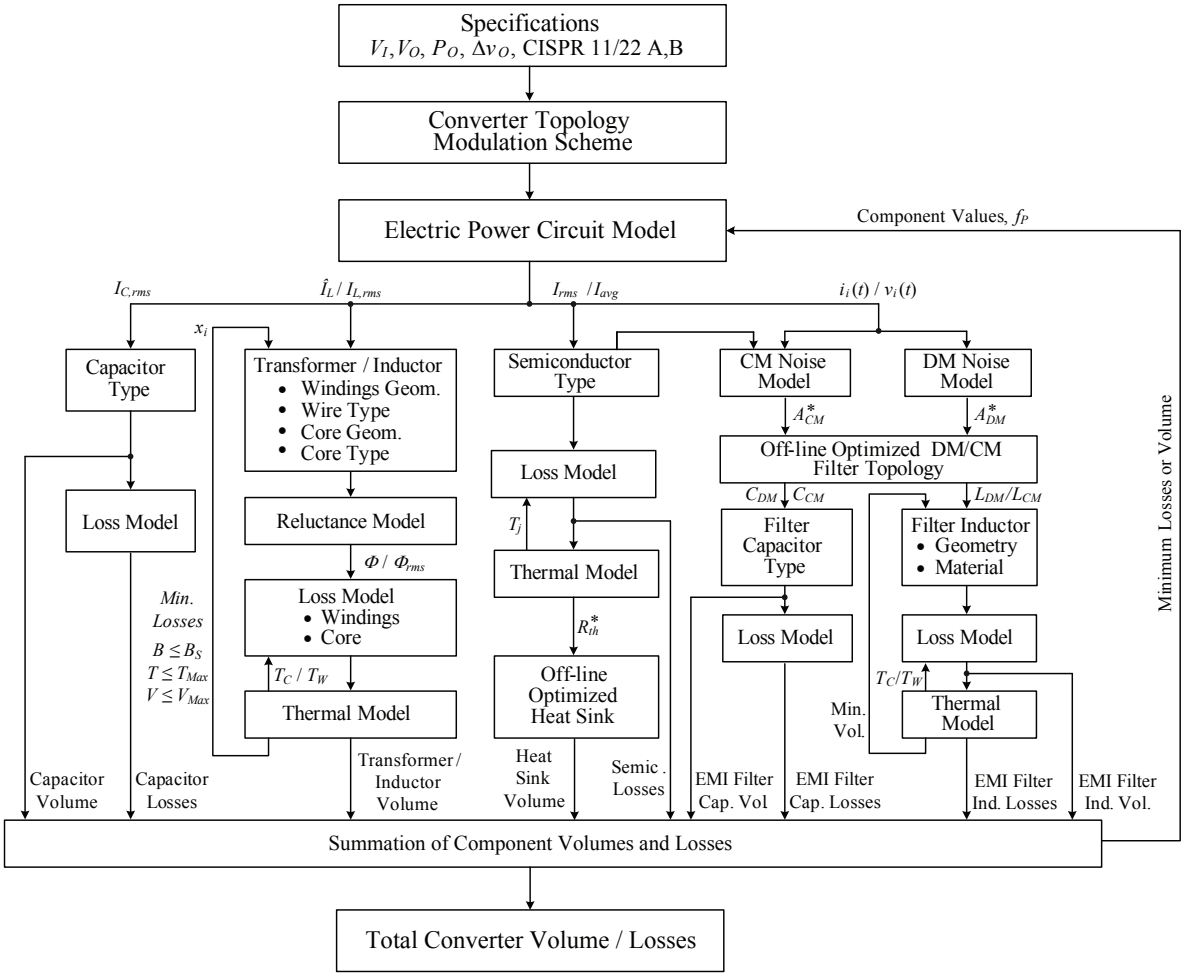


Fig. 5. Flowchart of the design and local (component level) and global (system level) optimization of a power electronics converter considering the selection and design of the main functional elements of the power circuit, i.e. power semiconductors and heat sink, inductors/transformers, capacitors and differential mode (DM) and common-mode (CM) EMI filter. When neglecting parasitic effects (wiring inductances, electromagnetic and thermal coupling of components, etc.) the component designs are largely decoupled and/or individual local optimizations can be performed; only the component values and the switching frequency f_P are then determined by an outer global optimization loop.

in the best possible way, e.g. at minimal costs. Alternatively, for a specified cost framework one can strive for maximum efficiency or power density. The choice of component values and operating parameters is conducted at present mainly based upon the experience of development engineers and earlier product generations. In order to fully exploit the potential of a given technological base, it is hence an obvious strategy to support and eventually replace this evolutionary process by a mathematical procedure, i.e. by means of multi-objective optimization. As will be shown in the following, the first step for this is to mathematically describe the realization and functioning of a converter system, starting from the basic materials and components and also determined by the selected circuit topology and operating mode (Section II-A). After agreement on Performance Indices (Section II-B), the design variables can then be specified via optimization with regard to maximum performance, whereby the weighting of individual performance goals may be selected (Section II-C). The essential result, apart from the values of the design variables, is a Pareto Front that shows the best possible compromise between competing performance goals and limits the Feasible Performance Space (Section II-IV). Furthermore, in analogy to microelectronics, "Technology Nodes" may be defined that characterize the state of the technology. Finally, the mathematical description and optimization also enables one to study the effect of an improvement in the basic technologies on system performance. The resulting sensitivities show directly the effectiveness of a new technology and thus offer an excellent base for drawing up a roadmap (Section III).

A. Abstraction of the Realization of Power Electronics Systems

From a mathematical viewpoint, the design of a power electronics system involves allocation of values to the free design parameters

$$\vec{x} = (x_1, x_2, \ldots x_n) \tag{1}$$

taking into consideration design constant

$$\overrightarrow{k} = (k_1, k_2, \ldots k_l), \tag{2}$$

e.g. the permeability and saturation flux density of magnetic materials, as well as specifications and system operating requirements

$$\overrightarrow{r} = (r_1, r_2, \ldots r_m) \tag{3}$$

(input and output voltage, output power, etc.) [14]. Thus each design is allocated to a point in the multi-dimensional Design Space, which is defined by $\overrightarrow{x}$ and $\overrightarrow{k}$.

The performance of a design may be evaluated by calculating Performance Indices

$$p_i = f_i(\overrightarrow{x}, \overrightarrow{k}) \tag{4}$$

whereby the inner converter function and system specifications,

$$g_k(\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) = 0 \qquad k = 1, 2, \ldots p \tag{5}$$

$$h_j(\overrightarrow{x}, \overrightarrow{k}, \overrightarrow{r}) \geq 0 \qquad j = 1, 2, \ldots q \tag{6}$$

which are partly formulated as minimum requirements, are included as side conditions. Finally, this leads to a mapping of a multi-dimensional Design Space (also referred to as Decision Space) into a multi-dimensional Performance Space (or Objective Space), defined by the Performance Indices p_i (Fig.4).

The functions g_k reflect on the one hand the physical behavior of the main functional elements of the converter system and on the other hand their interaction, as determined by the circuit topology and mechanical construction. The mathematical description of the system behavior is here simplified by the fact that the main functions are realized by separate components such as inductors, capacitors, power semiconductors and heat sinks. Neglecting parasitics, there hence exist only relatively loose couplings between the elements (Fig. 5). Stronger couplings are established, apart from the circuit structure, solely by parameters dependent on the geometry such as thermal resistances and electromagnetic couplings, as well as by the temperature dependence of the power semiconductor properties.

From the variety of possible designs, by means of an optimization

$$p_i \Rightarrow \text{Max} \tag{7}$$

the best design with regard to a Performance Index p_i, e.g. the efficiency can be found directly via single-objective optimization. Alternatively, a multi-objective optimization enables several competing performance goals to be considered. Before treating the various optimization options, however, the definition of the Performance Indices is briefly dealt with.

B. Performance Metrics

By means of Performance Indices integral properties of a converters are evaluated with relative, i.e. per unit quantities, e.g. the volume or the realization costs referred to the output power, or, as for calculation of the efficiency, the ratio of power values. This normalization allows the characterization of a system independent of nominal values.

However, what is important here is to compare only systems similar with regard to the type of energy conversion (e.g. AC/DC or DC/DC) and cooling concept, etc. with similar specifications with regard to input or output voltage ranges and ambient temperature, etc. Only then Performance Indices are reflecting the state of the technology objectively and can be used as a base for roadmapping. For example, higher current values result at lower input voltages, which cause correspondingly larger space requirements of the magnetic components and higher losses. Furthermore, it is decisive, for example, whether single- or a three-phase AC/DC conversion is required. The rectification of a single-phase system requires fundamentally energy storage dimensioned for twice the mains frequency, whereas a three-phase system, in the case of symmetrical sinusoidal current consumption, delivers a constant instantaneous power, i.e. in the ideal case requires only storage at switching frequency. Highly compact three-phase rectifiers thus exhibit typical power densities of $8\ldots10\,\mathrm{kW/dm^3}$ [19], single-phase systems on the other hand typically show values in the range of only $4\ldots6\,\mathrm{kW/dm^3}$ [14].

In the following the definitions of the most common Performance Indices are summarized.

1) Power Density: The (Continuous) Output Power Density ($P_{O,N}$ designates the rated output power)

$$\rho = \frac{P_{O,N}}{V_g} \quad \left(\frac{\mathrm{kW}}{\mathrm{dm}^3}, \frac{\mathrm{kVA}}{\mathrm{dm}^3}\right) \tag{8}$$

($1\,\mathrm{kW/dm^3}$=$1\,\mathrm{W/cm^3}$≈$16\,\mathrm{W/in^3}$ and/or $100\,\mathrm{W/in^3}$≈$6\,\mathrm{W/cm^3}$ = $6\,\mathrm{kW/dm^3}$) serves to characterize the degree of compactness of a converter or the volume required for realization at a given rated power. Here, apart from the volumes of the main components, i.e. the inductive components and the cooling system, are also the volume requirements of the EMC filter, the power semiconductors with driver circuitry and auxiliary power supply, as well as the control electronics and the housing have to be included in the construction volume V_g. Unfortunately this is often not the case for parameters stated in the literature where without further details, e.g. the heatsink is not taken into account, i.e. mounting on a cold-plate is assumed, or the EMI input filter is omitted.

Systems working in pulsed operation, e.g. converters for the power supply of actuators, may be characterized by a Peak Output Power Density

$$\rho_{max} = \frac{P_{O,max}}{V_g} \quad \left(\frac{\mathrm{kW}}{\mathrm{dm}^3}, \frac{\mathrm{kVA}}{\mathrm{dm}^3}\right) \tag{9}$$

whereby higher values are naturally obtained compared to ρ. In order to enable an objective comparison between various systems, it is mandatory to specify here the duration T_{max} of

the maximum power delivery or overload $P_{O,max}$ as well as the repetition rate of the power pulse or its duty cycle.

If e.g. with water cooling the volume V_x of the heat exchanger is not taken into account, a local power density

$$\rho_l = \frac{P_{O,N}}{V_g - V_x} \tag{10}$$

may be defined. Here the temperature of the cooling medium has a significant effect on the dimensioning or construction volume of the system and must be stated in all cases.

If the calculation of the converter volume is done via summation of the individual volumes V_i of the components, additional volume requirements resulting from differing geometric shapes of the packages must be considered. Utilization of the total volume V_g by active parts can be characterized here by a coefficient

$$C_P = \frac{\sum V_i}{V_g}. \tag{11}$$

Typical values are C_P=0.5...0.7. Higher values can be achieved only by adaptation of component shapes, by omission of packaging materials, or by multi-functional use of some components, e.g. of a magnetic core for magnetic flux guidance and dissipation of heat losses [20].

The power density can also be defined via the chip area requirement, i.e. relative to area in kW/cm^2 or kVA/cm^2. This is appropriate for converter systems such as PWM inverters of variable speed drives, where the basic structure contains only the input, i.e. DC link capacitor as a passive power component. The relative area requirement then enables a simple estimation of the dimensions required for the DCB substrate, baseplate and housing of a power module.

It should be noted that also a cooling system can be characterized by a power density in the sense of a thermal conductivity per unit volume, i.e. by a Cooling System Performance Index

$$CSPI_V = \frac{G_{th}}{V_c}. \tag{12}$$

For example, highly optimized air coolers attain values in the range of 20...30 W/(m^{3}K) [17], extruded standard heatsink profiles, in contrast, values of only 5...10 W/(m^{3}K).

For mobile applications a corresponding weight-related index

$$CSPI_W = \frac{G_{th}}{W_C} \tag{13}$$

should be defined, where W_C denominates the weight of the cooling system.

2) Efficiency: In connection with rising energy prices and the demand for conservation of resources, the efficiency of power electronics systems

$$\eta = \frac{P_O}{P_I} \tag{14}$$

gains increasingly in importance. Thus, e.g., for photovoltaic inverters or for the AC/DC and DC/DC converter stages of telecom power supply modules, an efficiency $\eta > 99\%$ is required.

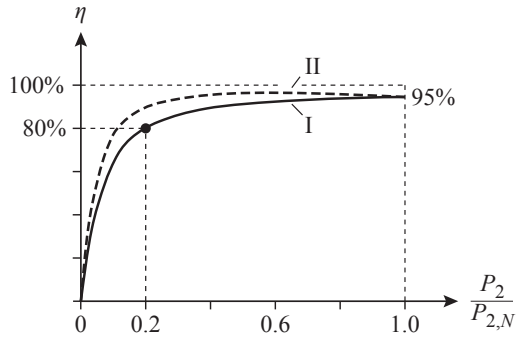


Fig. 6. Efficiency characteristic I of a power converter showing constant losses independent of the output power P_2. An efficiency of 95% (5% power loss) is assumed at rated power $P_{2,N}$; this corresponds to an efficiency of 80% at 20% $P_{2,N}$. Furthermore shown: Efficiency characteristic II with high part load efficiency as typically required by efficiency standards.

Calculation of the efficiency starts in general from the rated power. With redundant operation, furthermore, the partial load efficiency, e.g. at 50% and 20% rated power, $\eta_{50\%}$ and $\eta_{20\%}$, is of importance and is specified in corresponding regulations [21]. Moreover, for photovoltaic energy conversion a mean efficiency is calculated over the output power range [22]. A more precise statement of the Mean Mission Efficiency [23] of a system,

$$\eta_M = \frac{1}{1 + \frac{\int_0^{T_m} P_L(t)\mathrm{dt}}{\int_0^{T_m} P_O(t)\mathrm{dt}}}, \tag{15}$$

however, can only be made with knowledge of the mission and/or load profile (P_L denominates the system losses).

It is important to state that a defined value of the efficiency at partial load leads to lower absolute losses than at full load, which must be considered in the demand for high partial load efficiency. An efficiency curve with constant losses over the entire power range is shown in Fig.6. For example, an efficiency $\eta_{20\%}$ of 80% with regard to the occurring power loss corresponds to a rated point efficiency of 95%. But for parallel operation of converters, the demand for high part load efficiency is justified in all cases, since the total power would otherwise only be made available with a low efficiency of the individual systems.

Apart from the efficiency, the relative losses

$$\frac{P_L}{P_O} = \frac{1-\eta}{\eta} \tag{16}$$

are often also considered for characterization of a system, since in this way the heat emission or the cooling effort can be directly calculated. In this, with variation of the output power P_O, the associated value of the efficiency must always be taken into account.

It must again be pointed out that for ascertaining the state of the technology, systems with the same operating conditions

and approximately the same realization effort (e.g. the same total power semiconductor area) must be selected. For systems with broad input and/or output voltage ranges and/or with low input or output voltages, a high efficiency is naturally difficult to attain. Comparison with a system that was optimized for a specified voltage transformation ratio is not sensible here and yields no useful result.

Apart from the efficiency, energy-related Performance Indices may also be defined, such as the standby energy consumption or the costs of the losses over the lifetime referred to the procurement costs. For example, with electrical drive systems, energy costs occur over the useful lifetime in the order of 100 times the procurement costs, so that for an efficiency increase by 1%, double the procurement costs could be accepted. With more widespread use of power electronics systems, finally, questions of the energy input during manufacturing (grey energy) and of the overall energy consumption over the lifetime in the sense of a cradle-to-grave consideration or the recyclability will gain in importance.

3) Output Power per Unit Weight: Low converter weight and/or high output power per unit weight

$$\gamma = \frac{P_O}{W_g} \quad \left(\frac{\mathrm{kW}}{\mathrm{kg}}, \frac{\mathrm{kVA}}{\mathrm{kg}}\right) \tag{17}$$

is especially interesting for mobile applications, where high weight W_G results in increased fuel consumption. The importance of weight optimization, which up to now was hardly treated in literature, will hence increase significantly in the future. The reference value for the power, as with the power density, again requires a distinction between continuous and peak power.

4) Relative Costs: The power that can be installed for a given cost C_g

$$\sigma = \frac{P_O}{C_g} \quad \left(\frac{\mathrm{kW}}{\$}\right) \tag{18}$$

represents an extremely important industrial Performance Index. The costs for realization of a system, however, depend heavily on the number of units manufactured (economy of scale). Moreover, there exist for magnetic components, depending on the complexity of the winding construction and manufacturing site, significant differences in the production costs. A reliable calculation of the relative costs is hence only possible if cost models are available (which are often not public), which makes research considerably more difficult. The publication of standard cost models by industrial consortia, e.g. ECPE, would be of great assistance here.

Only with extremely high numbers of pieces, where the material costs are dominant over the manufacturing costs, a rough estimate of the basic costs is possible via the world market prices of the base materials. Finally, here in the sense of cost minimization, a minimization of the materials employed should be striven for.

Apart from primary performance indices related to the rated power, i.e. of efficiency, power density and costs, secondary indices such as manufacturability, time-to-market etc. can be defined, which cannot be considered further here in the interest of brevity. The simultaneous maximization of several of the above mentioned primary indices is the aim of the multi-objective optimization described in the following.

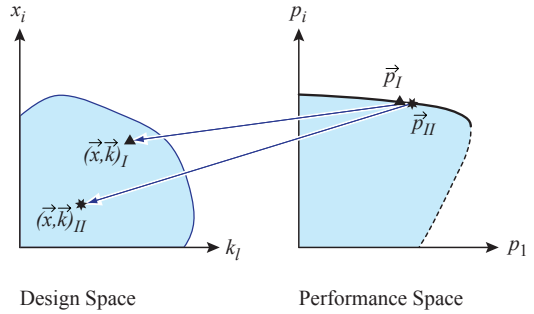


Fig. 7. Illustration of the Decision Space Diversity in multi-objective optimization. For analyzing the Decision Space Diversity the set of design variables and design constants $(\vec{x}, \vec{k})_I$ and $(\vec{x}, \vec{k})_{II}$ corresponding to two adjacent points $\vec{p}_I$ and $\vec{p}_{II}$ of the Pareto Front are determined.

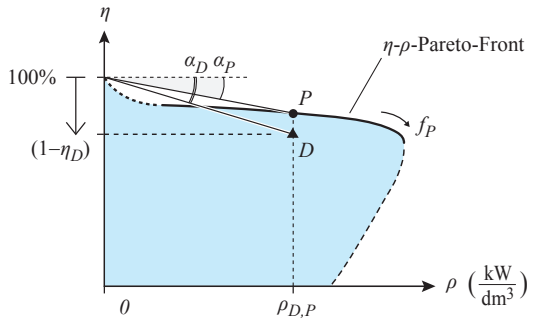


Fig. 8. η-ρ-Pareto Front resulting for optimization of a power converter concerning efficiency η and power density ρ, i.e. $(w_\eta\ \eta + w_\rho\ \rho) \Rightarrow$ Max. In case of a lower weighting w_η of the efficiency, higher switching losses are tolerated and/or higher frequencies f_P are selected by the optimization algorithm resulting in higher power densities. In order to consider the inherent trade-off between efficiency and power density the performance of a converter system and/or design D should be evaluated based on the ratio $\tan\alpha_D = (1-\eta_D)/\rho_D$, where $\tan\alpha_P$ represents the maximum obtainable performance.

C. Multi-Objective Optimization

In the course of the design of a power electronics converter, the present practice is to simulate the system behavior only for specified operating parameters (e.g. for a selected switching frequency) and for specified component values and forms of realization. However, beyond that the values of the design variables may be specified with computer assistance in such a way that an optimal system performance is achieved. The base of such an optimization is the mathematical model described in Section II-A. Alternatively, for the components of a circuit simulation, on-line parameter entry can be provided, so that an optimization algorithm can vary the values of the design variables until the optimal parameter combination is found (cf. Fig.5). Thereby, on the base of the separation of the partial functions described in Section II-A, local optimization loops can be provided for specifying the geometry of magnetic components or heatsinks. The significant advantage of this optimization is that evolutionary or market-driven stepwise

improvement in systems need not be waited for, and the potential of a set of existing technologies is exploited in a single step in the best possible way.

For the design of a technical system, a compromise must be found between several competing requirements, e.g. with regard to efficiency and realization costs, i.e. a multi-objective optimization

$$\sum w_i p_i = \sum w_i f_i(\overrightarrow{x}, \overrightarrow{k}) \;\Rightarrow\; \text{Min} \qquad (19)$$

is to be executed [14]. For each weighting w_i of the Performance Indices p_i there then results an optimal point in the Design Space to which a point in Performance Space is allocated. Different weightings w_i of the individual Performance Indices thus lead to different design points or to a multitude of solutions in the Performance Space known as a Pareto-Front. The solutions of single-criterion optimizations, which in each case consider only a single Performance Index, are contained herein as a subset.

After completion of the optimization, it is interesting to analyze the separation of the points in Design Space allocated to the Pareto Front, i.e. the Decision Space Diversity (cf. Fig.7, [24]). In this way characteristic couplings of design variables can be recognized; furthermore, one can estimate whether a sufficiently good suboptimal solution can be obtained with constant values of selected design variables (e.g. of the parameters determining the magnetic core geometry of inductors and transformers).

In the typical case, the optimization is carried out for one circuit topology, one specified control procedure and one fixed operating point, i.e. for a defined input and output voltage and output power. But e.g. for optimization with regard to efficiency, several operating points or a Mission Profile of the system can also be taken into account. The operating points must then be described in a Condition Space [15], which shows, on a further coordinate axis, the probability density resulting from the Mission Profile (Condition Map, [15]). In order to keep the computing effort low, however, only selected points of the Condition Space, i.e. operating points in ranges with high probability, can be taken into account for die optimization. In this way, e.g. the semiconductor geometry leading to minimal losses of a converter can be determined, i.e. the component behavior can be related to the integral system behavior over a Mission Profile [25].

Apart from the optimization of a single converter, a combination of systems can also be considered, e.g.

- the interleaved parallel operation of several converters, or
- the series connection of converter stages.

In the first case, e.g. the rated power and the operation of the individual systems must be chosen via multi-objective optimization in such a way that a minimum construction volume and maximum efficiency result for a given Mission Profile [23]. In the second case, the intermediate voltage levels of the converters can be determined in the sense of maximum compactness and overall efficiency. There, each system must be optimized for itself and also with regard to its effect in the overall system. Such a task arises e.g. with the voltage supply of future microprocessor systems where an overview can hardly be gained without optimization.

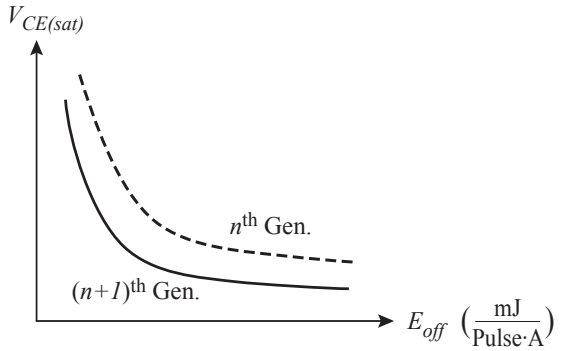


Fig. 9. Pareto performance limit of Insulated Gate Bipolar Transistors (IGBTs). The trade-off between saturation on-state voltage drop $V_{CE(sat)}$ and relative turn-off switching losses E_{off} is determined by properly adjusting the minority carrier lifetime. For a respective next device generation an improvement of the overall performance, i.e. of $V_{CE(sat)}$ and E_{off} is achieved.

It must be noted, however, that power electronics converters in most cases represent only a part of an overall system, i.e. for example one component in the drive train of an electric vehicle. In order to find an overall optimum, one must therefore in all cases at least roughly consider the overall picture, even for the optimization of a partial system. For example, through a comparably small increase in weight of a power electronics converter, a significant increase in efficiency might be attained, which overall would allow to decrease the electrical storage in size which could overcompensate the weight increase.

D. Pareto Front and Technology Nodes

As explained above, the Pareto Front describes a set of best possible solutions of a multi-objective optimization and thus defines the resulting (concave shaped) performance limit for a given system and for the technology base used for realization, i.e. the Feasible Performance Space. If two competing Performance Indices, e.g. efficiency η and power density ρ are considered, the Pareto Front is formed by a boundary line in the η-ρ-plane [14] (Fig. 8). On the level of components, a similar (convex shaped) boundary curve is known for IGBTs, where in the course of the design, a compromise must be found between saturation voltage and turn-off energy loss (Fig.9, [26]).

If the relative costs are also included in the considerations, i.e. the optimization is extended to a three-dimensional (3-D) Performance Space, an η-ρ-σ-boundary surface results as the Pareto Front (Fig.10). Correspondingly, at higher dimension of the Performance Space, the Pareto Front is described by a hypersurface. Apart from the costs, a further Performance Index that offers itself is the reliability, which essential depends on the variations of the component temperatures occurring in operation or in general on the degree of integration, i.e. on the number of individual components in a system. But existing reliability models still exhibit very high scattering of the results [27]. New approaches [27] could bring here a

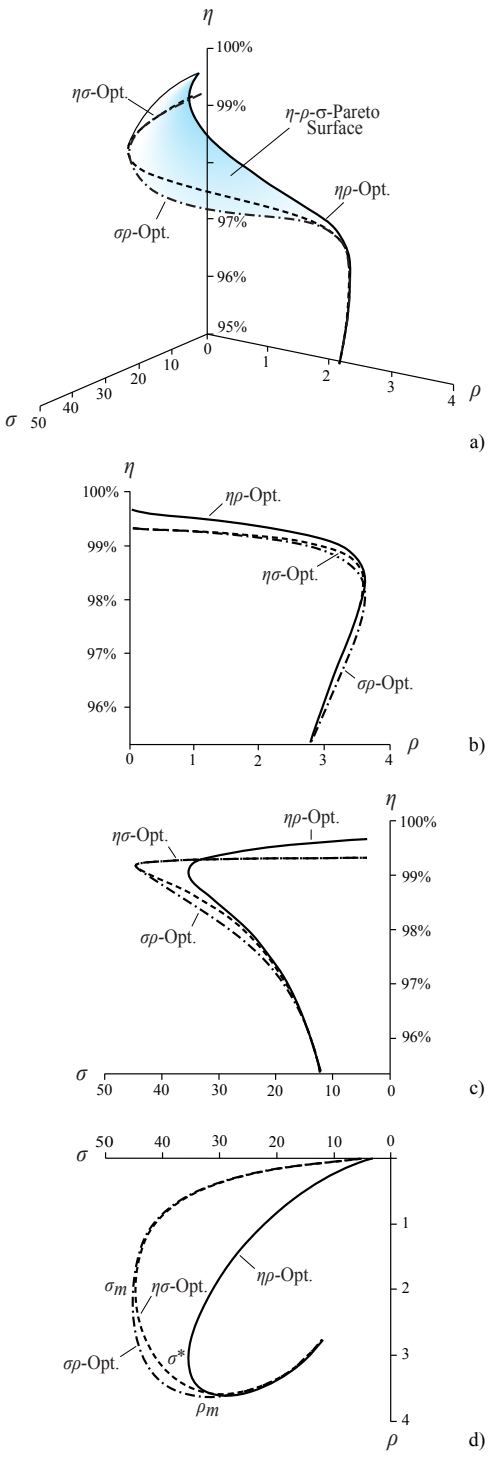


Fig. 10. η-ρ-σ-Pareto Surface of a single-phase bridgeless PFC rectifier where costs of inductors and capacitors are considered proportional to the component volumes and the semiconductor costs are related to the total installed semiconductor area. Projections of the Pareto Surface onto the η-ρ-plane, the η-σ-, and the σ-ρ-plane are shown in b), c) and d); c) clearly indicates maximum power per costs ratio σ_m located in between maximum efficiency (100%) and maximum power density ρ_m (e.g. η-ρ-Opt. indicates an optimization concerning ρ and η) .

significant improvement and in future allow the reliability to be included in the optimization of a system.

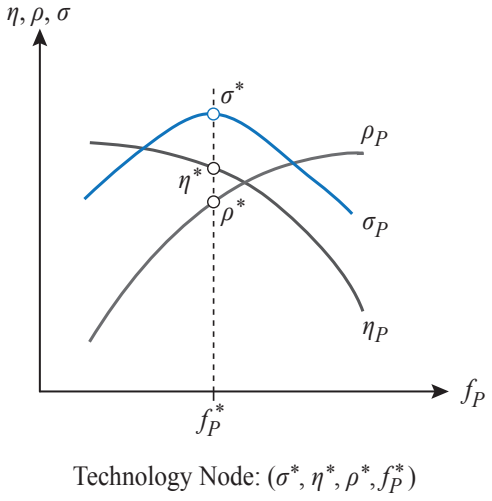


Fig. 11. Variation of the efficiency η, power density ρ and cost related output power σ along the Pareto Front (index P), i.e. in dependency of the switching frequency f_P. As the realization of highly efficient or highly compact converters is connected to a high realization effort, σ reaches a maximum at medium values of f_P. This maximum σ^* and the related values η^*, ρ^*, and f_P^* can serve as a basis for defining a Technology Node of a converter concept and the underlying components technology.

In [14] the η-ρ-Pareto Front for single-phase PFC rectifier systems shown schematically in Fig.8 was calculated. Rising values of the power density and falling efficiency are associated here with rising values of switching frequency. Referring to Fig. 10, a representation of the realization costs along the η-ρ-Pareto Front offers itself for simple characterization of a converter system and the technology base chosen for realization (Fig.11). By means of this diagram, the question can be directly answered as for which switching frequency f_P^* or which power density ρ^* and efficiency η^* minimum relative realization costs σ^{*-1} are attained. The parameters (η^*, ρ^*, σ^*) and the value of the switching frequency f_P^* are then to be seen as a Technology Node of the converter system and technology base. Here it should be noted that in microelectronics, the dependency of manufacturing costs on the packing density - in analogy to power density - is considered. The Moore's Law always refers to that production process or that packing density which exhibits minimum costs per circuit component [7].

III. Roadmapping based on Multi-Objective Optimization

For the preparation of a roadmap, the first step is to determine the maximum achievable performance using existing technologies, i.e. the envelope of the Pareto Fronts (Pareto Envelope) of known converter concepts (Section III-A). The term technology here includes the circuit concepts and control procedures, etc. Next the effect of a change in the base technologies on the system performance must be investigated, i.e. the attainable shift of the Pareto Envelope must be determined. As discussed in the following (Section III-B, the technological sensitivities calculated in this way enable a direct statement concerning the most effective approach for improvement of the base technologies. Or it may turn out that

a performance goal planned in the course of a roadmap can fundamentally not be achieved through further development of state-of-the-art technologies (Section III-C). This then gives a clear indication of the necessity of a technological leap, i.e. the use of a fundamentally new (disruptive) technology (Section III-D).

A. Optimization-Based Comparative System Evaluation

The Pareto Front directly shows the capability of a system to fulfill several competing performance criteria simultaneously. In this way, for a given specification, possible circuit concepts may be compared with reference to the associated Pareto Front and thus the best solution can be found in a simple way. Furthermore, via the Pareto Envelope of all circuit concepts, the overall performance limit existing for a type of converter (e.g. of single-phase PFC rectifier systems), which is to be used as a starting point for roadmapping, is completely defined.

In the following, two examples for such a concept comparison will be shown. On the one hand, different topologies

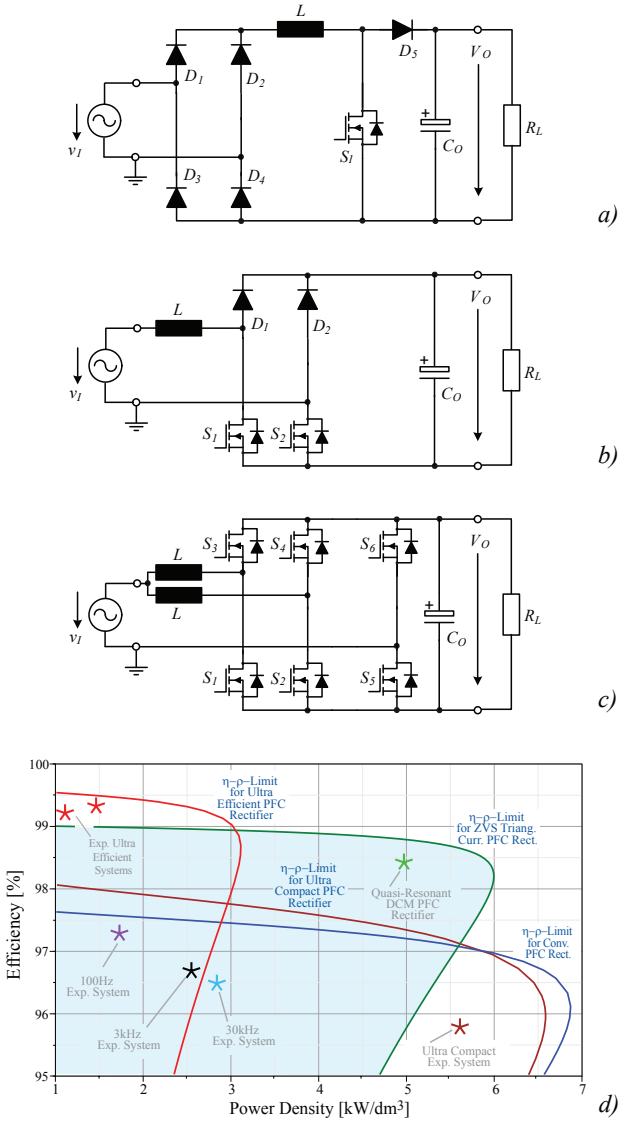
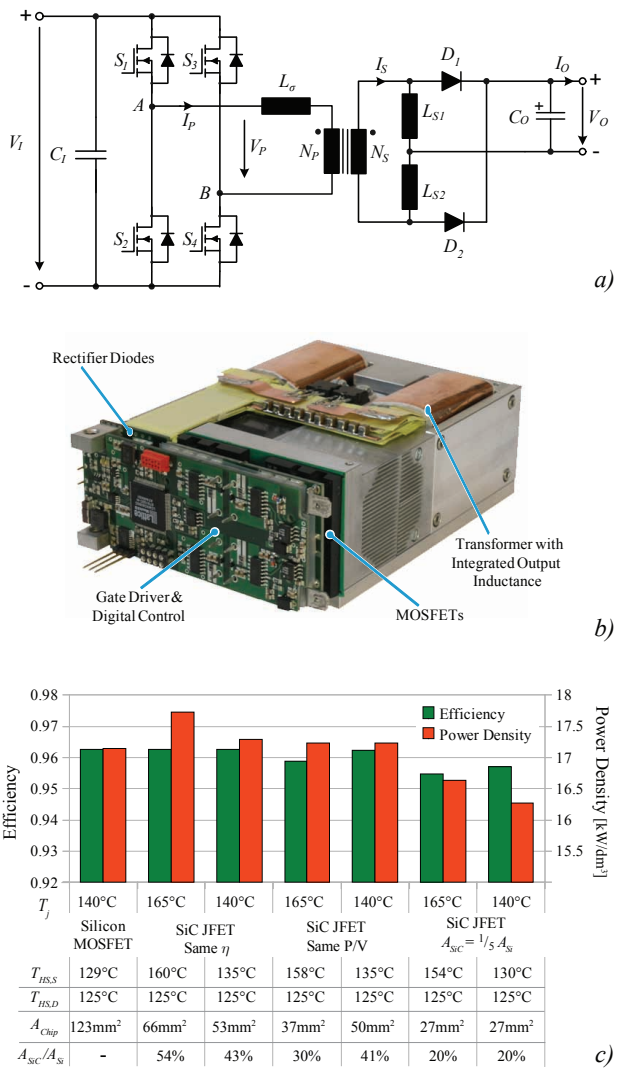


Fig. 12. Basic structure of the power circuit of a conventional single-phase power factor corrected (PFC) rectifier a), a bridgeless PFC rectifier b) and a resonant transition zero voltage switching (ZVS) PFC rectifier c). Furthermore shown: η-ρ-Pareto Fronts of the circuits identifying c) as preferable concerning the trade-off between efficiency η and power density ρ; a power density of 5kW/dm^3 and an efficiency of 98.5% can be achieved.



T_j	140°C	165°C	140°C	165°C	140°C	165°C	140°C
	Silicon MOSFET	SiC JFET Same η		SiC JFET Same P/V		SiC JFET $A_{SiC}=1/5\,A_{Si}$	
$T_{HS,S}$	129°C	160°C	135°C	158°C	135°C	154°C	130°C
$T_{HS,D}$	125°C	125°C	125°C	125°C	125°C	125°C	125°C
A_{Chip}	123mm²	66mm²	53mm²	37mm²	50mm²	27mm²	27mm²
A_{SiC}/A_{Si}	-	54%	43%	30%	41%	20%	20%

Fig. 13. Basic structure of the power circuit a) of an isolated phase-shift full-bridge DC/DC converter with current doubler rectifier; b) converter prototype optimized with respect to power density (specifications: V_I=400V, V_O=48V. . .54V, P_O=5kW, power density ρ=9kW/dm^3 /147W/in^3; for further details see [28]); c) efficiency and power density in case Si superjunction MOSFETs (STY112N65M5) or 500V SiC JFETs (SiCED) are employed for realizing the power transistors S_1 - S_4. Two different junction temperature limits, i.e. $T_{j,max}$=140°C and 165°C are considered for the SiC devices and the chip area is scaled such that an equal efficiency or equal power density is achieved. Furthermore, the properties for an overall die area of the SiC JFETs of A_{SiC}=1/5A_{Si} is shown ($T_{HS,S}$ denotes the heatsink temperature of the active switches, $T_{HS,D}$ is the temperature of the separate heatsink of the output diodes). The power density values are calculated based on a converter volume determined by summation of the individual component volumes. Accordingly, lower values would result for a practical realization due to not matching geometrical shapes of the components and remaining spaces in between the components.

and realizations of single-phase PFC rectifiers are compared; on the other hand, for a telecom DC/DC converter of given topology, the gain in performance by replacing Si by SiC semiconductor technology is analyzed.

1) Single-Phase PFC Rectifier: In Fig. 12 the η-ρ-Pareto Fronts of

1) a hard-switching bridgeless PFC rectifier, cooled by natural convection,
2) a forced air cooled hard-switching bridgeless PFC rectifier, and
3) a forced air cooled conventional PFC rectifier, and
4) a system with zero voltage switching (ZVS) and synchronous rectification, working with triangular shaped input current (similar to discontinuous conduction mode), without forced air cooling

are shown. The optimization of all systems was based on a rated output power of 3.2kW, a rated input voltage of $230V_{rms}$ and an output voltage of $365V_{DC}$. Details are given in [29]. As shown by closer analysis, the performance of the hard-switching systems with regard to efficiency is limited by the Figure of Merit $FOM_{\eta\rho} = \sqrt{G^*/C^*}$ of the power MOSFETs [14]. With an increase in the number of parallel connected power MOSFETs, the conduction losses decrease and the capacitive switching losses increase. Higher efficiency is hence only possible with relatively low switching frequency or low power density. A similar picture arises for the forced air cooled systems, whereby the efficiency here is overall lower because of the power consumption of the fans and the higher power requirement of the control electronics. However, based on the improved cooling, a higher switching frequency and hence a higher power density are attainable. As a whole, the effect of the technology employed (FOM of the power MOSFETs and cooling concepts) on the system performance is easily seen.

A relatively high efficiency and high power density can only be achieved by extension of the converter structure and a change in the operating mode, i.e. by change to synchronous rectification and resonant transition switching and/or ZVS. Since with suitable control, then the output capacitance of the power MOSFETs can be discharged prior to turn-on, the FOM loses its limiting effect and a high clock frequency can be selected in spite of the higher number of switches, or a high power density at high efficiency (typically 5kW/dm^3 @ 98.5%) can be achieved [29].

If the Pareto Fronts of all known PFC rectifier concepts would be shown in Fig.12 and for this e.g. the use of SiC power transistors and of various magnetic core materials for realization of the boost inductors would be considered, a complete picture of the capability of the presently available technology would be obtained. New approaches, considered in the course of roadmapping, could then be directly evaluated and assessed for their effectiveness with regard to performance improvement.

2) Telecom DC/DC Converter: Multi-objective optimization also offers e.g. the possibility of virtually testing a new semiconductor technology prior to its market introduction, e.g. of clarifying how much improvement with regard to efficiency and power density results from a higher switching speed or higher maximum permissible junction temperature. In Fig. 13 such an investigation is shown for a 5kW 400V/48V telecom DC/DC converter [28]. Instead of the Pareto Front, characteristic values of power density and efficiency are given. It becomes clear that because of the soft switching of the converter and the low on-state resistance of Si-superjunction MOSFETs, only a slight improvement in the Performance Indices results. For more complex systems, it would be more difficult to gain an overview of this situation and the performance improvement could hardly be quantified with regard to efficiency and power density without optimization. This shows clearly the value of the calculation procedure presented here.

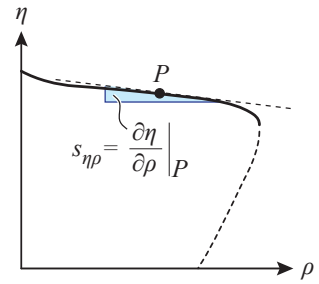


Fig. 14. Characterization of the trade-off between efficiency and power density by the partial derivative $s_{\eta\rho} = \partial\eta/\partial\rho$ in a design point P; $s_{\eta\rho}$ can also be interpreted as sensitivity of the efficiency concerning a required increase or tolerable decrease of the power density in the design process; e.g. highly efficient PFC rectifier systems show typical values of $s_{\eta\rho} \approx 0.5\%/(\text{kW/dm}^3)$, whereas highly compact PFC rectifier systems are characterized by $s_{\eta\rho} \approx 1\%/(\text{kW/dm}^3)$ [14].

It should be noted that for a given converter system, the overall $V_{CE(sat)}$-E_{off}-trade-off characteristic (Pareto Front) of an IGBT [30] could be illustrated in a multitude of Pareto Fronts of the system performance. The improvement in performance by means of a next semiconductor generation would thus be directly clear.

B. Sensitivities of System Performance

1) Sensitivities along the Pareto Front: With mathematical modeling and subsequent optimization, the Pareto-Front gives an immediate impression of the compromise to be taken for a given system between competing Performance Indices. Hence

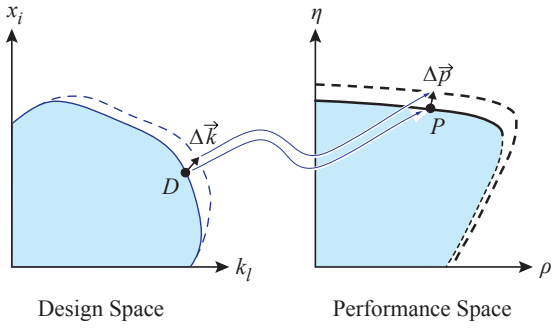


Fig. 15. Improvement of the system performance, i.e. resulting displacement $\Delta\vec{p}$ of the Pareto Front for an improvement $\Delta\vec{k}$ of the technology base, i.e. of the (limit) values of the design constants.

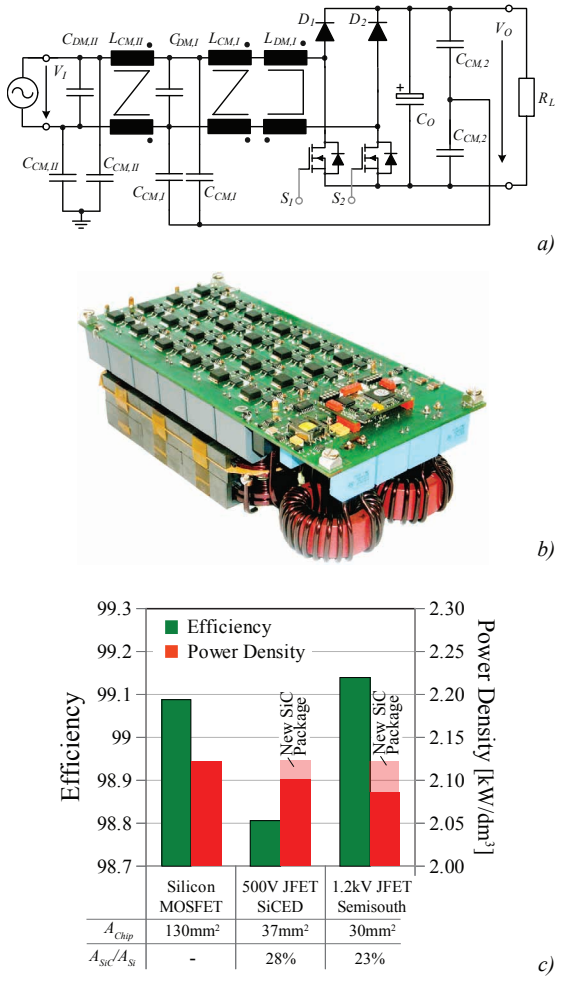


Fig. 16. Basic structure of the power circuit a) of a single-phase bridgeless PFC rectifier with capacitive coupling of the output voltage to ground (capacitors $C_{CM,1}$ and $C_{CM,2}$, [14]); b) converter prototype optimized with respect to efficiency (specifications: V_I=230Vrms±10%, V_O=365V, P_O=3.2kW, rated power efficiency η=99.2%; for further details see [14] and [28]); c) efficiency and power density for realizing the power transistors S_1 and S_2 with Si-superjunction MOSFETs (IPP60R099CP) of a normally on 500V SiC JFETs (SiCED) or 1.2kV normally off SiC JFETs (SemiSouth). The power density values are calculated based on a converter volume determined by summation of the individual component volumes. Accordingly, lower values would result for a practical realization of the converter systems due to not matching geometrical shapes of the components and remaining spaces between the components. Furthermore given: chip areas resulting from the efficiency optimization.

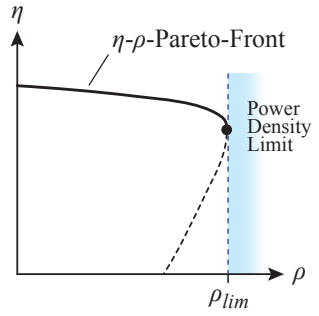


Fig. 17. Pareto-Front and Power Density Limit.

if an improvement of a Performance Index is required, a reduction in at least one other Performance Index must be accepted. If e.g. the efficiency is to be improved, a reduction in the power density and perhaps also an increase in costs is inevitable. Precise information is given by the gradients of the tangents to the Pareto Front in the design point P (Fig.14),

$$s_{\eta\rho} = \left.\frac{\partial\eta}{\partial\rho}\right|_P, \qquad s_{\sigma\eta} = \left.\frac{\partial\sigma}{\partial\eta}\right|_P, \qquad s_{\sigma\rho} = \left.\frac{\partial\sigma}{\partial\rho}\right|_P, \tag{20}$$

which could be designated as sensitivities along the Pareto Front. In this way, for a given design, the consequences of a change in a target performance can be estimated.

2) Sensitivities to Base Technologies: The mathematical model further allows to study the extent of the shift $\Delta\overrightarrow{p}$ in the Pareto Front resulting for an improvement $\Delta\overrightarrow{k}$ in the technology base (Fig. 15), i.e. to calculate the sensitivity matrix

$$\mathbf{s}_{\overrightarrow{p}\,\overrightarrow{k}} = \begin{bmatrix} \frac{\partial p_1}{\partial k_1} & \cdots & \frac{\partial p_1}{\partial k_l} \\ \vdots & & \vdots \\ \frac{\partial p_i}{\partial k_1} & \cdots & \frac{\partial p_i}{\partial k_l} \end{bmatrix} \tag{21}$$

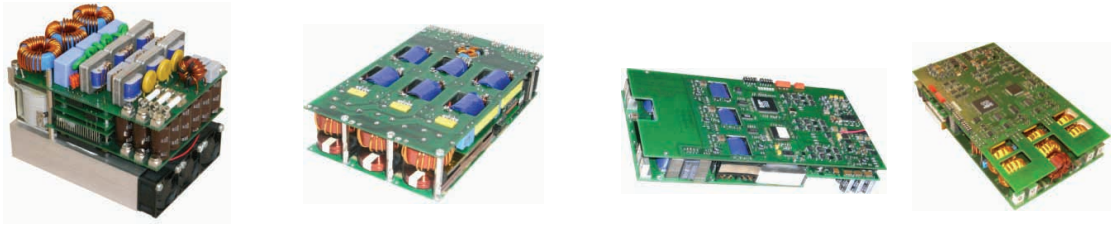
and subsequently

$$\Delta\overrightarrow{p} = \mathbf{s}_{\overrightarrow{p}\,\overrightarrow{k}}\ \Delta\overrightarrow{k}. \tag{22}$$

The components k_l of the technology vector here comprise design constants, such as the maximum junction temperature, the saturation limit of a magnetic material or the on-state resistance per unit area of unipolar power semiconductors, or in general the Figures of Merit of the power semiconductors.

Fig. 16 shows an example of the efficiency and power density of a 3.2W bridgeless PFC rectifier optimized for efficiency for realization of the turn-off power semiconductors with Si-superjunction power MOSFETs and alternatively by normally-on and normally-off SiC JFETs. The boost diodes are realized with SiC Schottky diodes. Details of the individual components can be found in [28]. Unexpectedly, it becomes clear that a change in the semiconductor technology has only a relatively small effect on the performance. The efficiency cannot be improved by the use of SiC JFETs. (Small differences in the power density could be compensated by more compact packaging of the SiC semiconductors.) On the other hand, according to [31], an increase in the rated power efficiency to η=99.3% and in the power density by 30% would be possible by magnetic integration of the boost inductance $L_{DM,1}$ and the common-mode inductance $L_{CM,1}$ and by using electrolytic instead of foil capacitors besides employing latest superjunction semiconductor technology. It thus turns out that the analysis of technological changes should by no means be limited to the power semiconductors.

If the target performance is now specified for a roadmap, with the sensitivities known, the most effective way of gaining the required performance improvement can be chosen, i.e. that technology identified which has the strongest effect on the performance. Furthermore, it will become directly clear whether a desired improvement is at all feasible, or which



f_P =	72kHz	250 kHz	500kHz	1MHz
ρ =	4.5 kW/dm^3	10 kW/dm^3	13 kW/dm^3	14 kW/dm^3

Fig. 18. Dependency of the power density of a unidirectional three-phase/level PFC rectifier system (Vienna Rectifier) on the switching frequency. Only for the system with f_P=72kHz the heatsink volume is considered in the given power density figure (4.5kW/dm^3 and/or 74W/in^3); accordingly the systems with f_P=250 / 500 / 1000kHz actually show a lower power density, i.e. a power density limit of $\rho \approx$ 10kW/dm^3 could be assumed for f_P= 1MHz.

combination of improvements is necessary to attain the goal. In order to obtain an approach that is economically justifiable, the resulting costs C_g for a change in performance must always be considered, i.e. the sensitivity

$$\frac{\partial C_g}{\partial p_i} = \left[\frac{\partial C_g}{\partial k_1} \cdots \frac{\partial C_g}{\partial k_l}\right] \begin{bmatrix} \left(\frac{\partial p_i}{k_1}\right)^{-1} \\ \vdots \\ \left(\frac{\partial p_i}{k_l}\right)^{-1} \end{bmatrix} \tag{23}$$

must be taken into account.

Moreover, if the sensitivities in the vicinity of a design point are calculated, the robustness of a concept can be assessed, e.g. against fabrication-related variations in the characteristics of the magnetic core material (hysteresis and eddy current losses, permeability etc.) used for the realization of inductors. Thus the advantage of greater robustness is weighed against the disadvantage of perhaps limited technological influence on the system performance. Since power electronics converters are strongly heterogeneous systems (power semiconductors, electrical and magnetic energy storages, etc.) and hence depend on numerous base technologies, the change in only one technology, in general will have only a relatively small effect. Thus there exists typically a relatively low sensitivity to individual technologies and a significant gain in performance can only be achieved by simultaneous improvement in several technologies [14].

If the sensitivities with regard to a technology are analyzed along the entire Pareto Front, a statement results on how the technological parameters must be selected on average such that a broad usability is given, i.e. both a design with high efficiency as well as one with high power density are well supported. Finally, as shown in the following with a sensitivity analysis also the requirement of a technological leap can be recognized. If a desired improvement in performance cannot be achieved, even with a combined change in the base technologies, the use of a Disruptive Technology is inevitable.

C. Technological Limits

Apart from the interdependency and the technological sensitivity of the Performance Indices, a statement on the fundamental physical or conceptional limits can also be gained from the Pareto-Front. Such a limit appears wherever a Performance Index can no longer be increased, even accepting a massive deterioration in other Performance Indices. For example, for the η-ρ-optimization the power density limit is given where even a complete disregard of efficiency brings no further improvement (Fig.17),

$$\partial\rho/\partial\eta \;\Rightarrow\; 0. \tag{24}$$

This point would also be reached with single-objective optimization directed to maximum power density.

In general, a limit exists for the power density achievable by an electronics system. This is because the switching operation mode always requires a switching frequency filter and a cooling system of finite volume has to be provided to dissipate the conduction and switching losses [14]. An example is given in Fig.18, where various realizations of a unidirectional three-phase PFC rectifier system with 10kW rated power are shown (input voltage 400V_{rms} line-to-line, output voltage 800V_{DC}). The systems are dimensioned for various switching frequencies f_P, are extremely compactly built and include an EMI filter to fulfil the conducted emissions standard CISPR 11/22, Class A. Dependent of the switching frequency, power density values of ρ=4kW/dm^3 (f_P=72kHz) up to ρ=14kW/dm^3 (f_P=1Mz) are attained [19]. The saturation of the power density gain with increasing switching frequency clearly shows the existence of a physical/technological limit (Fig.19), which must definitely be taken into account in the course of roadmapping.

Fundamental limits are also visible where an increase in the complexity or the costs of a system leads to no further improvement in performance. For the realization of a system with specified characteristics, several circuit topologies, control and modulation procedures are usually available. Typically, on optimization, several of these approaches will lead to a similar Pareto Front defining the Pareto Envelope. The Inherent Performance Limit thus resulting can then only be slightly increased even for accepting a significant increase in complexity or significantly higher costs (Fig.20). Only an improvement in the base or component technologies can bring an increase in system performance here, whereby the packaging and especially the thermal management of the components also represent important aspects.

As an example, consider the realization of a bidirectional non-isolated DC/DC converter for applications in hybrid vehicles with an overlapping input and output voltage range of 150V. . .400V [32]. If e.g. the dependence of the efficiency on the output power is calculated for the circuits shown in Fig.21a) and Fig.21b) with the precondition of the same overall silicon area, the characteristics shown in Fig. 21c) result. The approximately same performance of the two systems despite significantly differing complexity and operation modes, indicates directly that a Inherent Performance Limit has been reached. Hence no further significant improvement can be expected by using other circuit concepts or operating modes.

A similar situation exists e.g. for telecom DC/DC converters where a phase-shift, full-bridge topology and an LLC converter exhibit a similar performance limit after optimization. This is easily understandable because in the final analysis, in all cases only 4 switches are present on the primary side and the number of degrees of freedom of the control is limited because in all cases a symmetrical magnetization of the transformer must be assured. In the course of the design, therefore, there remains only a relatively small freedom concerning topology and control technique. The optimization possibilities are hence limited to the choice of the operating mode and optimization of the components, for example the winding arrangement and the geometrical dimensions of the transformer and inductors.

In this manner, therefore, the exhaustion of the possibilities of a technology can be clearly recognized. Only in special cases it is economically sensible and justifiable to exceed this limit. In summary, the converter structures and control procedures used should be as simple as possible and their

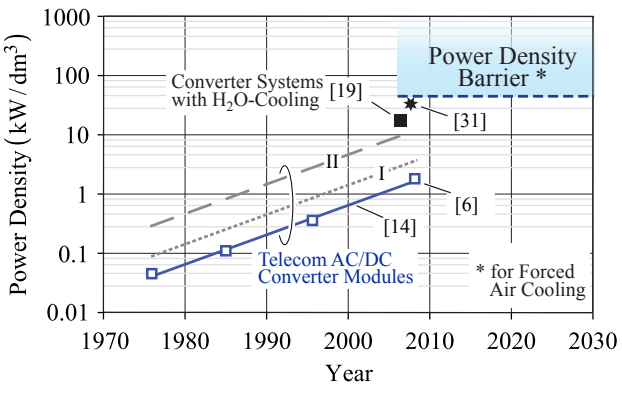


Fig. 19. Improvement of the power density of commercial single-phase telecom AC/DC converter modules (comprising two converter stages, i.e. a PFC rectifier and a DC/DC converter) over the past decades according to [14] and [6]. The increase in power density by a factor of 10 every 20 years has been achieved by changing from natural convection to forced air cooling and by increasing the converter switching frequency. Curve I characterizes the power density trend of the individual converter stages, i.e. of the PFC rectifier or DC/DC converter stage; II indicates the performance development of research demonstrator systems which are translated into commercial products typically within 10 years. Furthermore shown: Power Density Barrier of forced air cooled converter systems as calculated in [17] and local power density of a water cooled non-isolated bi-directional automotive DC/DC converter (Fig.21a)) and of an unidirectional three-phase/level PFC rectifier system (Fig.18).

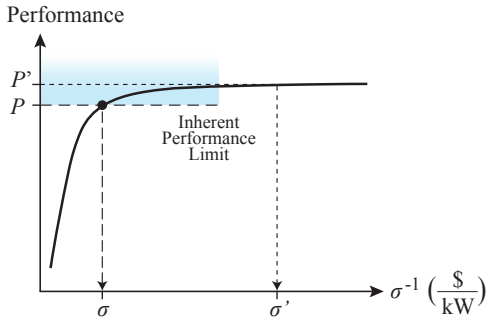


Fig. 20. Illustration of the relation of converter performance, e.g. efficiency or power density and relative costs. Once a Inherent Performance Limit is reached a further increase in system performance is connected with a substantial increase of the system complexity and/or realization costs. The Inherent Performance Limit is dependent on the employed technology base but largely independent of the converter concept (in case of selection of a suitable topology and modulation scheme).

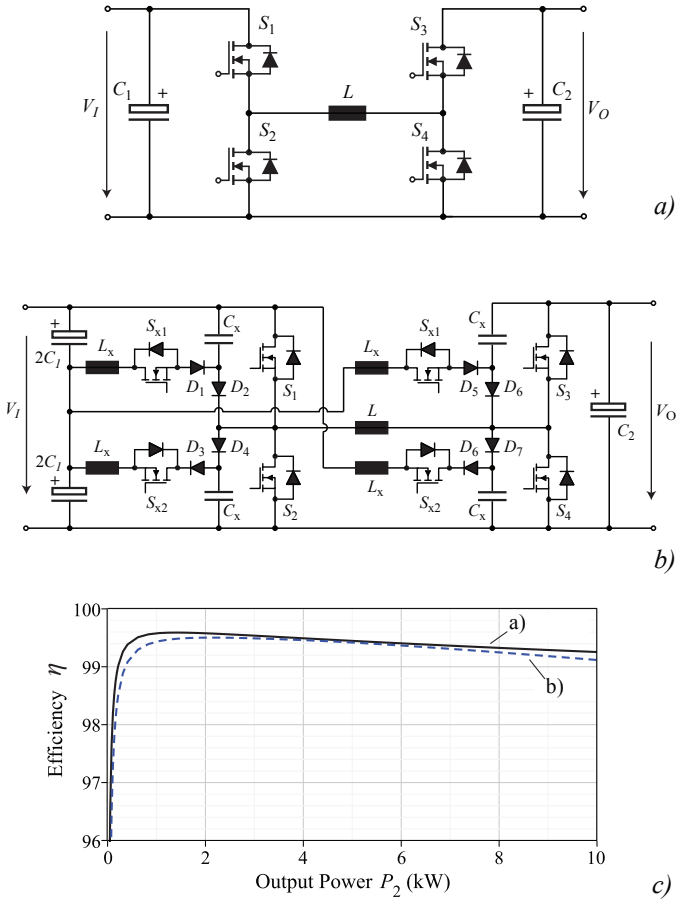


Fig. 21. Comparative evaluation of bi-directional non-isolated buck+boost DC/DC converter concepts. a) constant frequency ZVS DCM converter and b) snubber assisted zero voltage and zero current transition converter; c) calculated efficiency in dependency on the output power for employing equal overall power semiconductor silicon areas for a) and b); both converters are designed for the following specifications: V_I=150V. . .400V, V_O=150V. . .400V, P_O=12kW; for further details see [32]. Despite the significantly higher complexity of b) no substantial performance improvement is achieved. This indicates that a Inherent Performance Limit (cf. Fig. 20) resulting from the employed base technologies has been reached.

potential should be fully exploited via optimization in the best possible way.

D. Power Electronics S-Curves and Disruptive Technologies

The development of technologies is described by so-called S-curves [33], in which the progress of a technology is plotted against research effort or time (Fig.22). If a technology has matured, no significant improvement in performance takes place, even with massive research efforts or over a lengthy period of time. Such a limit is, for example, reached when a technological limit is fully exploited via optimization (Section III-C). For example, in Fig.19 it is seen that on the basis of state-of-the-art technologies, a limit to the power density of converter systems will be reached. Because of the time difference of approximately 10 years [34] lying between the research S-curve and the marketing S-curve, this power density limit is already already today on demonstrator systems in research.

If saturation in the performance growth of an S-curve has been reached, a further increase in the performance can only be attained via a significant increase in the complexity and/or if a significant increase in the power-related costs σ^{-1} is accepted. This can only be avoided by means of a change in technology, i.e. by leaping onto a new technology curve. By means of the new Disruptive Technology, a further improvement in the system performance is then possible at acceptable cost.

As already mentioned, a power electronics converter is a complex system that depends on numerous base technologies. Correspondingly, several Candidate Technologies are available for performance improvement. If one considers the development of power electronics since the introduction of solid-state switches, one observes a significant impulse for performance improvement from progress in semiconductor technology (Fig. 23). Examples of such technological discontinuities are the change from bipolar transistors to IGBTs [30], or the replacement of analog control circuits by programmable digital controls. But as shown above (Section III-A), hardly any improvement is obtained e.g. with SiC active switches for applications requiring relatively low voltage blocking capability. New technologies are thus variously effective in various fields of application. Hence it is advisable to virtually test a new technology in the sense of "look before you leap" [33], i.e. to apply the concept presented in this work. The problem of today's decoupling of the semiconductor manufacturer from applications can thus be solved, a problem that did not exist in this form in the beginnings of modern power electronics (1980). For example, with the introduction of bipolar power transistors and power MOSFETs, customers were offered comprehensive application descriptions in the form of application notes and manuals. The performance of a new component in a specific application was thus known in advance.

Note: In microelectronics, too, limits are more and more reached with regard to feature size and power losses, and the continuation of Moore's Law (doubling of the number of transistors every 24 months) is questionable. Here, too, various branches in the technological path, i.e. alternatives

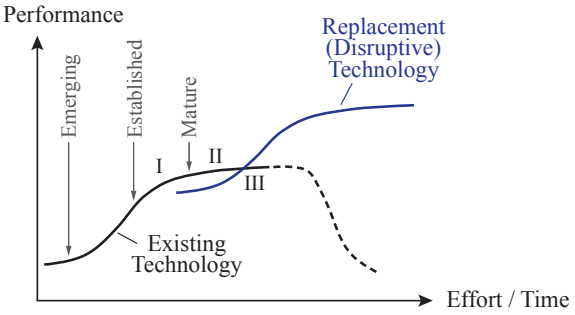


Fig. 22. Progress of a base technology in dependency on the research efforts and/or time (Technology S-Curve). The process of leaping to a new technology can be divided into three phases: step - stretch - leap [8]. Within the step phase I a state-of-the-art technology is employed; within the stretch phase II the existing technology is further improved but due to the saturation of the S-curve no substantial performance gain can be achieved. Within the leap phase III finally the switching to a new technology offering higher performance is performed.

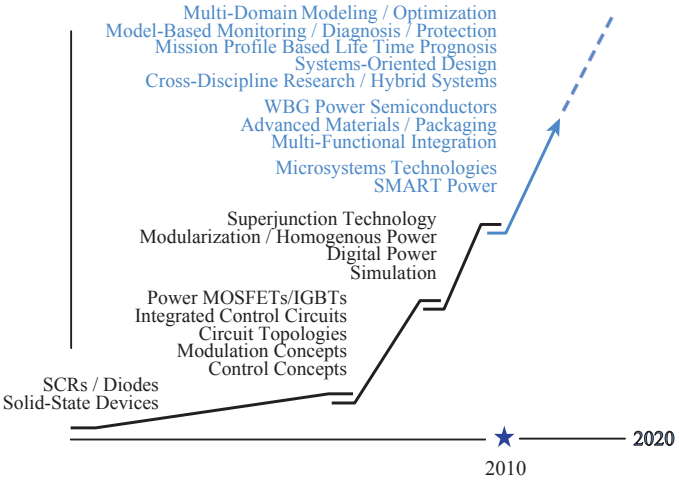


Fig. 23. Main S-curves of the development of solid-state power electronics and relevant enabling technologies. Only technologies which have resulted in a substantial performance gain are shown. For the future progress of power electronics numerous candidate technologies, e.g. multi-domain modeling and multi-objective optimization, system oriented design, wide-bandgap power semiconductors and cross-discipline (hybrid) systems are available.

to lowering the feature size are being discussed, whereby concepts such as different voltage levels in some domains of a processor, as well as virtualization of the tasks and above all the use of parallel processors are being considered. On the whole, therefore, performance gain is not (only) attained on the processor and technology levels, but also on the system level.

There are strong analogies to this in power electronics. Examples are the increasing spread of interleaved parallel connected systems, which enables an increase in the effective switching frequency without raising the switching losses, i.e. with a heatsink of low volume and enables operation of a partial system with discontinuous current (DCM). The reverse recovery behavior of power diodes is thus without importance, i.e. no expensive SiC diodes are required. Furthermore, a continuous input or output current results from the superposition

of partial currents such that only a small-sized EMI filter must be provided. Overall, an efficient, compact and low-cost solution is achieved.

IV. Technology Hype Cycles

New technologies often show so-called Hype Cycles (Fig.24), which can lead to an initial overestimation of the potential of a technology. An example is the matrix converter [36], which for decades was regarded as the ultimate replacement for conventional voltage source inverters. The MOS-controlled thyristor (MCT) or Model Predictive Control could serve as further examples.

Above all with already considerable technological saturation of a field, the few remaining alternatives are often overvalued in their importance. This is supported by a corresponding focussing of publications; articles in the mainstream result in a high citation index, independent of the industrial relevance, i.e. a kind of positive feedback is established. Only after the decay of the hype the actual potential of a technology, and the application area in which an improvement in performance is achievable, become objectively visible.

Publications on the comparison of the performance of new technologies with the state-of-the-art can help to objectify and provide damping here. If, for example, one calculates the Pareto Envelope (Section 2.4) or the total chip area requirement and the construction volume of a matrix converter and competing systems, the advantages and disadvantages for various application areas can be directly seen (Fig.25) [35]. For example, the matrix converter is superior with regard to power density to a back-to-back converter with voltage DC link at relatively low switching frequencies, since for the rectifier stage no boost inductance is necessary, but on the other hand, it has a high chip area requirement. In summary, then, for a new technology the associated Technology Node should be calculated as early as possible and compared with the Technology Node of the state-of-the-art with the same side conditions.

V. Conclusion

The present work describes a procedure based on multi-objective optimization that allows to utilize the available technological base in the best possible way for the realization of a power electronics converter. Through use of the procedure, different system concepts, i.e. circuit topologies, control procedures, etc. can be evaluated with regard to achievable efficiency, power density, costs, etc. and directly compared in the form of the associated Pareto Front. Furthermore, there follows a characteristic triple value (η^*,ρ^*,σ^*), which specifies the efficiency and power density of a concept attainable with minimum costs/kW and which can be seen as the Technology-Node of a system.

The Pareto-Front resulting from the optimization defines the Feasible Performance Space of a system. If the target performance lies outside this area, a new technology must be employed. The necessity of a technological leap, i.e. the introduction of a Disruptive Technology can thus be recognized at an early stage from the location and shape of the Pareto Front. Moreover, by calculation of Technological Sensitivities, the improvement in performance achievable by improvements in the technology base can be tested and assessed in advance. The interaction and importance of the technologies employed for the realization of a converter system are thus directly transparent. This offers an excellent basis for effective roadmapping

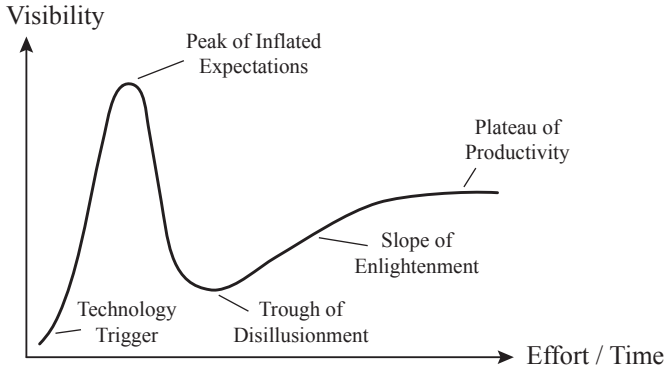


Fig. 24. Hype Cycle of technologies.

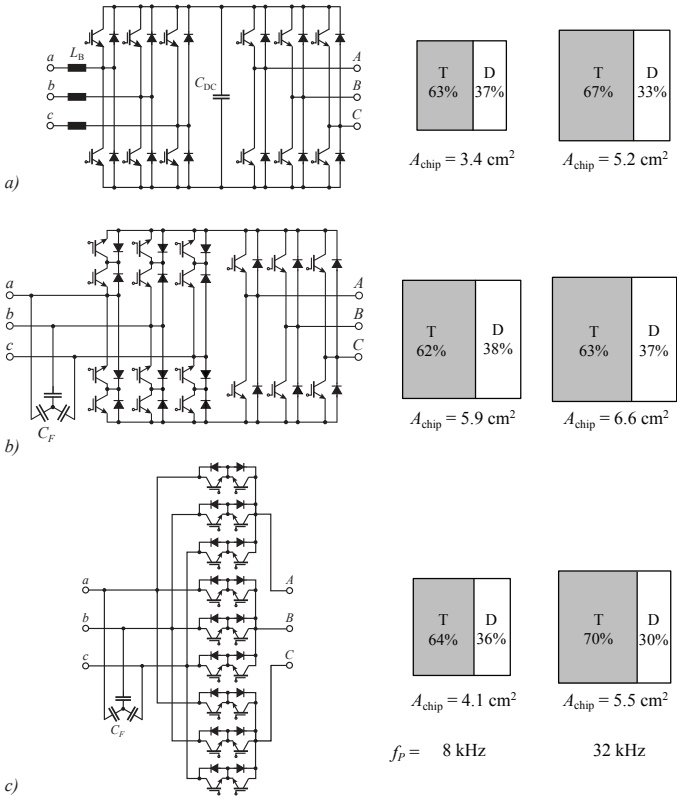


Fig. 25. Comparative evaluation of bi-directional three-phase AC/AC converter systems concerning the overall silicon area required for realization of a variable speed drive systems with given operating area in the torque-speed-plane for f_P=8kHz and f_P=32kHz switching frequency (see [35] for details); a) voltage DC link back-to-back converter, b) indirect matrix converter and c) direct (conventional) matrix converter.; D indicates the overall diode and T the overall transistor chip area requirement. Assumptions: Input phase voltage: 230V$_{rms}$/50Hz, rated output power: 15kW, maximum output frequency: 150Hz, maximal admissible junction temperature: 150°C.

for various main application areas in power electronics.

As shown, for example in [14] and [31], an efficiency of nearby 99% at high power density can be realized by multi-domain optimization on the basis of state-of-the-art technology. Attempts to extend the technology-related limit, e.g. by extension of basic circuits with supplementary or auxiliary circuits leads to a strong increase in system complexity. The associated higher realization costs or the potential reduction in reliability can be justified only in exceptional cases. Such extensions are anyway often overtaken by improvements in semiconductor technology; examples are bipolar transistors and snubber circuits, which completely lost their importance with the introduction of the IGBT.

For effective research, there thus remains a relatively limited freedom in the classical areas of power electronics. Also the further development of products, which after focussing on power density - apart from the ever important cost reduction - now runs predominantly in the direction of improvement in efficiency (Fig.26), will meet technological and cost-related limits. An example is the improvement in efficiency of photovoltaic inverters, which presently exhibit an efficiency of 99% and for which a halving of the losses typically every 5 years can be deduced from observation of previous development [37].

In order to be able to reduce the costs while achieving high performance and to further expand the use of power electronics, a well-known approach used for integrated circuits and power supplies for microprocessors, i.e. Standardize - Modularize - Integrate, is promising; this was also one of the core ideas for the foundation of the Center of Power Electronics Systems (CPES). It should be noted here that of course new power semiconductors and also new materials (e.g. with significantly higher thermal conductivity) will play an important supporting role. But both areas were up to now not the core elements of classical power electronics research, which has been targeted predominantly to converter systems and not to components.

Finally, in the following, the research areas in power electronics, that will be important in future, are briefly discussed.

Technical innovations proceed in a wide variety of application areas according to similar patterns [TIPS (Theory of Inventive Problem Solving) [38]]. Such a solution concept is e.g. the stronger integration of functions or the change from the single element to the system.

1) Integration: Opportunities of higher integration exist e.g.

- in variable speed drives technology in the form of a constructive integration of the power electronics converter and of the drive motor, or
- with power modules in the form of integration of the power semiconductors with the drivers and sensors or monitoring technology, whereby apart from closed loop control of the switching transient, the decentralization of control or synchronization functions becomes possible, or in the form of
- magnetic integration of inductors and transformers and the multi-functional integration [39] of EMC filters in connecting lines [20],
- the integration of cooling systems into magnetic components to improve heat dissipation [40] and
- the integration of converter stages, e.g. of a three-phase PWM rectifier and inverter function in the form of a matrix converter [36] or single-stage, off-line power supplies that combine an active PFC rectifier stage with an isolated DC/DC converter [41].

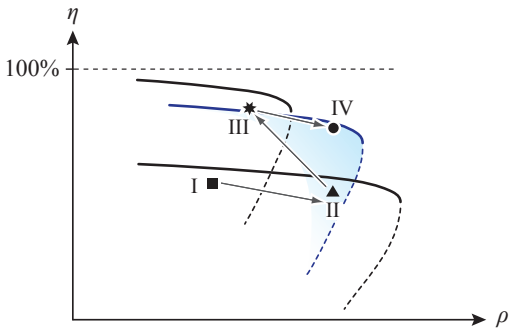


Fig. 26. Typical trajectory of the performance improvement of telecom AC/DC converter modules and related Pareto Limits of the respective converter systems. In the past development efforts were concentrated on increasing the converter power density (I-II); subsequently a significant increase of the conversion efficiency had to be performed (II-III) while still keeping a sufficiently high power density. Finally, a slight decrease in efficiency might be accepted in order to again improve the power density and to achieve lower the realization costs (III-IV).

However, by integration causes e.g. system parts that are dimensioned for different temperature levels (power electronics/motor, driving electronics/power semiconductors) are brought into immediate vicinity or with multi-functional integration, material properties are demanded that require a compromise with regard to performance. The use of separate materials in each case optimized for a main property can hence eventually lead to higher performance. Furthermore, integration of several conversion tasks typically limits the degree of freedom of the control of a system, so that overall a lower performance of the integrated system results. The matrix converter or isolated single-phase/stage AC/DC power supplies could serve as typical examples here. The detailed and unbiased clarification of these facts offers a broad field of research.

2) Modularization: A general trend in power electronics is directed to volume reduction or the replacement of passive power components by the increased use of power semiconductors. Here important basic concepts are interleaving and parallel connection and the series combination of converter stages to multi-level or multi-cell systems. Through multi-level voltage formation a desired voltage value can be better approximated, so that filter elements that have to take up the difference between target and actual voltage values are smaller in size. The same applies for interleaved parallel connection, where despite discontinuous partial currents, a total current with low switching frequency ripple results. Furthermore, in both cases, through voltage or current splitting, a corresponding splitting of the power to be transmitted is assured, whereby

heat dissipation and the covering of a broad power range are simplified. The higher control effort caused by splitting into partial systems can be simply managed with digital control circuits. In any case, the use of this concept in different application areas of power electronics should be examined in the course of research.

3) System Consideration: Power supplies have over the last two decades experienced a significant improvement in performance, but their inner structure and appearance has not fundamentally changed.

After the essential development potential of converter systems is exhausted, and only cost reduction remains as the main development path, research must detach itself from the details of the converters and start considering system aspects. Here, in particular, the closer connection of power electronics

- with the grid [13], e.g. also in the form of smart housing (green or low-energy buildings) or Smart Grids, and
- with the load, e.g. in the field of E-mobility

are main topics. Research of classical power electronics, orientated to converter topologies and control and modulation schemes, accordingly must be extended to energy systems (Fig.27), electromechanical energy conversion, mechanical systems and economic aspects. This will define a new, modern and strongly interdisciplinary picture of electrical energy technology (Fig.28). Also from an economic viewpoint, this path is extremely interesting, since on the system level simpler successes might be achieved than on the technological base with individual converters.

4) Design Tools: Independent of the exact orientation of the research, modern simulation-supported, multi-domain design tools will in future acquire fundamental importance. Apart from the power circuit simulation available today, which includes simulation of the control electronics, the modeling and simulation of the following should primarily be supported:

- high frequency losses in magnetic components,
- the (transient) thermal behavior of power semiconductors and passive power components (inductors, transformer, capacitors),
- parasitic elements in connection technology (e.g. multilayer busbars or the wiring in power modules),
- conducted electromagnetic interference emission and finally
- reliability.

Here the field of reliability should be emphasized in particular, where starting from the Mission Profile of an application and knowledge of the mechanical construction of the component, e.g. of the material combinations of a power module, a statement on the reliability should be possible, based on physical models [42].

Such a simulation platform has been under development since 2005 at the Power Electronics Systems Laboratory of the ETH Zurich. The goal is to integrate all the above mentioned areas and to be able to conduct Virtual Prototyping or comprehensive multi-objective optimization of power electronics converters in 2015 [43]. Apart from this converter-oriented, detailed simulation, in the medium term, system oriented

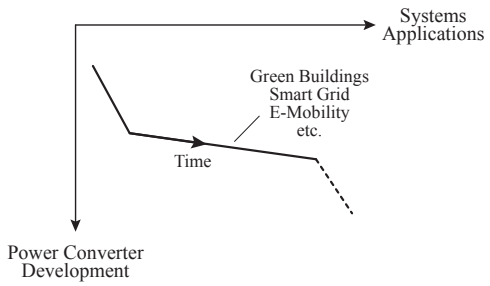


Fig. 27. Extension of the scope of power electronics from converters to (hybrid) energy systems.

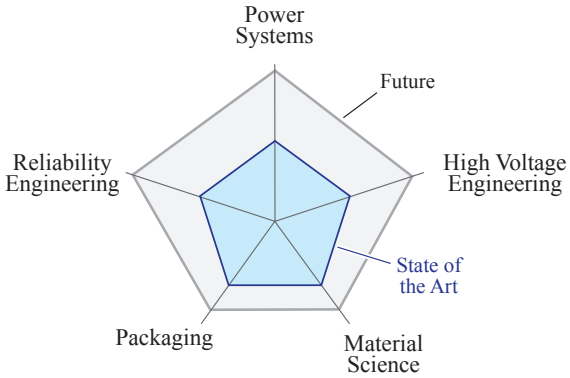


Fig. 28. Required future extension of the competence of power electronics researchers and engineers in order to ensure a further highly dynamic development of the field.

considerations, i.e. the extension to a multitude of converter, sources, loads and energy storages should be enabled, whereby the abstraction and system level modeling of the converter function represents a considerable challenge.

5) Education: The new generalized image of power electronics must also be reflected in teaching, especially in university education. Here lectures in mechanics, thermodynamics/fluid mechanics and materials science must again be included in the core electrical engineering curriculum in order to lay a solid interdisciplinary basis for later activity in the field of power electronics. Furthermore, the gap between classical energy technology with consideration over several mains cycles (several 10ms) and power electronics typically orientated to μs - ms must be closed. Here the field of control engineering is of special importance.

Finally, in all considerations, system orientated analysis must always stand next to the detailed function in order to train the abstraction ability of the students, which will be of fundamental importance in future for the planning of power electronics on all levels of integrated energy transmission and distribution grids.

6) New Application Fields: In order to find new application area and hence new research fields, the traditional value ranges of the main quantities in power electronics, i.e. of power, voltage, temperature, frequency (time) etc. - must be analyzed and those fields identified which are today not yet covered by applications (Fig.29). Through the development of new tech-

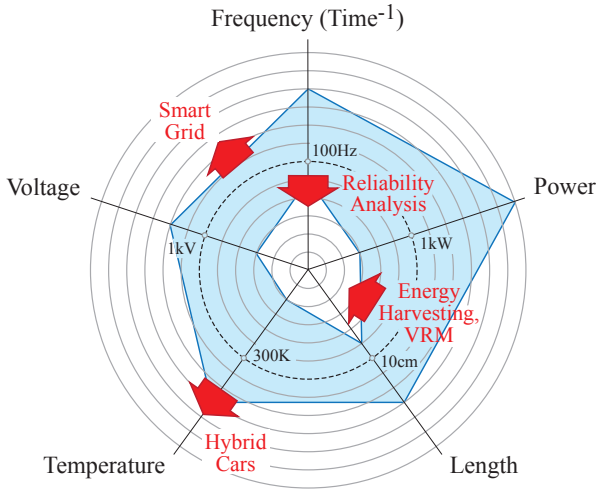


Fig. 29. Typical value ranges of the main physical quantities of power electronics converters shown in a logarithmic polar chart in normalized form. The respective reference values are indicated adjacent to the dashed grid line. Only for the temperature a linear scale is assumed with a temperature difference of 50°C between adjacent grid lines. Possible future extensions of the application of power electronics systems into not yet covered areas are indicated by red arrows.

nologies for these areas, a technology push could potentially be triggered, which finally would lead to the opening of new business areas. Some examples are given in the following.

$T_j > 200°C$

Wide-bandgap power semiconductors such as SiC and GaN enable significantly higher junction temperatures than for Si power semiconductors and can hence in principle be used in high temperature environments [44]. However, there is a lack of suitable packaging materials and capacitor technologies as well as sensor technology and signal processing suitable for high temperature [45].

μs & MW

Solid state power transformers, i.e. medium frequency isolated DC/DC converters or three-phase AC-AC converters with power in the range of 1 - 10 MW represent core elements of future Smart Grids on the distribution level [46]. The realization of corresponding turn-off power semiconductors as well as associated low-inductance, partial-discharge-proof packages for medium voltage represents one of the challenges here. Furthermore, the consideration of the circuit topology, and loss minimization and cooling of the medium frequency transformers offers a broad field of research.

ms $\Rightarrow$ Years

With increasing demands for energy efficiency and conservation of resources, the analysis of power electronics converters must be extended from μs. . .ms (control processes, mains cycles) to the entire lifetime. One example is the calculation of the overall energy input for manufacturing (grey energy), operation and disposal or recycling of a converter. Only in this way higher initial costs can be justified for assurance of a higher performance. Furthermore, the efficiency characteristic can be tailored via optimization in the best possible way to the later application profile and thus the maximum effectiveness of resource use assured.

m (cm) $\Rightarrow$ mm (μm)

The linear scale of present applications in power electronics ranges from typically 100m (HVDC) into the cm-range for Point of Load converters of IT systems. A reduction in the dimensions into the mm- and perhaps μm-range opens up a multitude of new applications. Examples are conventional power supplies with extreme form factor (Power Foil, [47]) or Power Supplies on Chip for the power supply of future microprocessors or in connection with Energy Harvesting [48] and PowerMEMS. Here, predominantly, new passive components must be created that can be realized with microelectronics technologies or in general, a Micro-Power Electronics that is more strongly based on capacitive than on inductive elements has to be established.

In summary, then, research faces fascinating challenges that require, however, a significant extension of classical power electronics and work on subjects outside the previous horizon of experience. The crossing of technological boundaries and interdisciplinary research on the intersections of technology areas always offers a high potential for innovations. The speed of implementation of such a roadmap, however, will essentially depend on the will for change and the leaving of established research subjects.

Acknowledgment

The authors would like to thank Prof. E. Wolfgang, Prof. D. Silber, Dipl.-Phys. T. Harder, ECPE, and Dipl.-Ing J. Koszescha, ECPE, for inspiring discussions on roadmapping in power electronics.

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