# Comprehensive Design and Optimization of a High-Power-Density Single-Phase Boost PFC

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***Abstract*—The design of a single-phase boost power-factor-correction (PFC) circuit is associated with a large variety of considerations, such as the following questions. Which operation mode should be selected (e.g., continuous or discontinuous operation)? How many interleaved boost cells are advantageous? Which switching frequency should be selected? What is the optimum number of EMI input filter stages? Which semiconductor technology should be chosen? All these issues have a significant influence on the converter efficiency and power density. In this paper, the aforementioned questions are addressed for exemplary specifications of the PFC (300-W output power, 400-V output voltage, and 230-V mains voltage), whereby the focus in the design is mainly put on very high power density. As a result, different design points are identified and comparatively evaluated. By considering different aspects such as volume, losses, capacitor lifetime, and also cost issues (e.g., by additional current sensors or expensive silicon carbide devices), a dual-interleaved PFC operated in discontinuous conduction mode at 200 kHz is selected. With an experimental prototype, a superior power density of 5.5 kW/L and a system efficiency of 96.4% are achieved, which is close to the values predicted by the design procedure. Furthermore, measurements verify a near-unity power factor (PF = 99.7%) and the compliance with electromagnetic compatibility conducted noise emission standards. Finally, it is investigated to which extent the power density could be further increased by an integration of the input filter in the PCB.**

***Index Terms*—Electromagnetic compatibility (EMC), interleaved converters, power density, power factor correction (PFC), single-phase boost converter.**

## I. Introduction

POWER SUPPLY units with active power factor correction (PFC) have become very popular since they offer high power density and fulfill harmonic standards for low and high frequencies. A typical topology for boost applications with $n$ number of interleaved boost cells including a needed filter stage to attenuate line-conducted EMI emissions can be seen in Fig. 1.

The design and optimization of such converter types has been discussed extensively in the literature [1]–[6], and a complete guideline for optimization of the main parts such as the boost inductor(s), the output capacitor, and the differential mode (DM) and the common mode (CM) input filter for two different operation modes [continuous conduction mode (CCM) and discontinuous conduction mode (DCM)] has been given in [1]. In CCM, the inductor current(s) never becomes zero during a half mains period, whereas in DCM, the inductor current(s) always becomes zero during each turn-off switching state. In order to reduce the noise emission and thus the input filter size, interleaving several boost stages [7]–[11] can be employed. In this paper, a power supply unit with a rated output power of $P_0 = 300$ W will be designed based on the general guidelines in [1] in order to verify the considerations. The power supply shall be designed for the European market with a rated mains voltage of $U_{\mathrm{in,rms}} = 230\ \mathrm{V}(+10\%\ /-15\%)$ and a nominal output voltage of $U_0 = 400$ V. For the selection of the appropriate design, the main focus shall be put on a maximum power density at acceptable efficiency.

All following examinations are done for CCM and DCM operation mode and for one up to three interleaved boost cells. The design of the boost inductance, including a thermal connection, to an available heat sink or cold plate is shown in Section II. Section III deals with the design and selection of a proper output capacitor in order to ensure highest power density. A selection of possible semiconductors concerning the appearing losses is given in Section IV by taking Si and SiC technology into account. Subsequently, the design of the EMI filter is discussed in Section V, where optimized DM and CM filters are designed. All results are summed up in Section VI, and the total boxed volumes and calculated appearing losses are compared for selected design points. The laboratory prototype of the optimum design is shown along with measurements in Section VII. Finally, it is discussed and experimentally proven in Section VIII to which extent an integrated EMI filter may further increase the power density.

## II. Boost Inductor Design

Designing the boost inductor is one of the main challenges on the way to a high power density boost PFC. On this account, the boost inductor design has been discussed extensively in the literature [4], [6], [11]–[16]. A complete design and optimization

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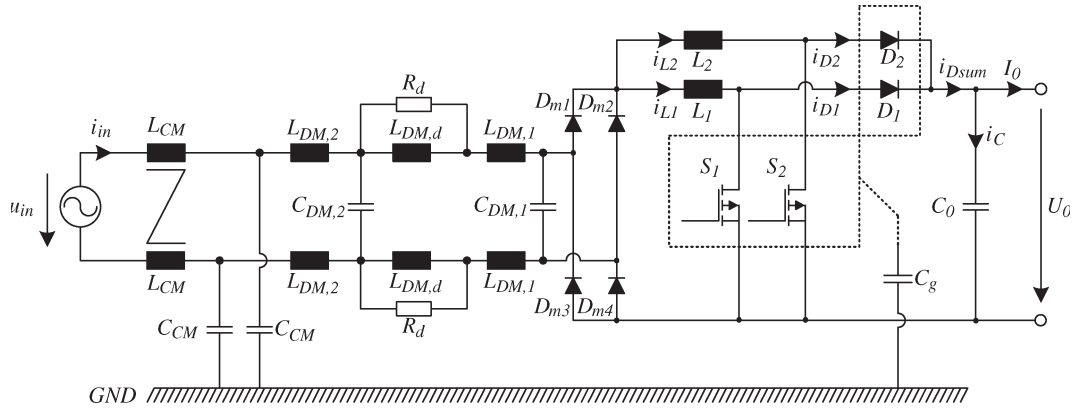


Fig. 1. Topology of a PFC converter with two interleaved boost cells and two-stage EMI DM and one-stage CM filters and the lumped capacitance to ground $C_g$.

process taking the electrical, magnetic, and thermal design aspects into account has already been discussed in [1]. The design process according to [1] is based on the required inductance value, which depends on the rated output power $P_0$ and the operation mode (CCM or DCM) and is given by

$$L_{\mathrm{CCM}} = \frac{U_0}{4 \cdot f_S \cdot \Delta I_{L,\mathrm{CCM,pk-pk,max}}} \tag{1}$$

for CCM with the dc-link voltage $U_0$, the switching frequency $f_S = 1/T_S$, and the maximum allowed peak-to-peak current ripple $\Delta I_{L,\mathrm{CCM,pk-pk,max}}$. The latter depends on the constant ripple factor

$$k_{\mathrm{ripple}} = \frac{\Delta I_{L,\mathrm{CCM,pk-pk,max}}}{\hat{I}_{L,\mathrm{CCM,avg}}} \tag{2}$$

with the amplitude of the local average inductor current

$$\hat{I}_{L,\mathrm{CCM,avg}} = \frac{\hat{I}_{\mathrm{in}}}{n} \tag{3}$$

the number $n$ of interleaved boost cells, and $\hat{I}_{\mathrm{in}}$ representing the mains current amplitude.

For DCM the maximum inductance value is given by

$$L_{\mathrm{DCM}} = \frac{\hat{U}_{\mathrm{in}} \cdot (1-\alpha)}{f_S \cdot \Delta I_{L,\mathrm{DCM}}(\omega t = \pi/2)} \tag{4}$$

with the input–output voltage ratio $\alpha = \hat{U}_{\mathrm{in}}/U_0$ and the maximum allowed peak-to-peak current ripple

$$\Delta I_{L,\mathrm{DCM}}(\omega t = \pi/2) = \frac{2}{n} \cdot \hat{I}_{\mathrm{in}}. \tag{5}$$

The results shown in this paper are based on the optimization routine introduced in [1], which uses a database consisting of the main core material data such as the $A_L$ value (inductance per square turns), core loss data and core dimensions to calculate the needed number of windings, the inductance value at full load by taking saturation effects into account, the total boxed volume, and the total losses for each core. Finally, the optimum core for a specific inductance value and switching frequency can be found. For the design at hand, only *Magnetics MPP* [16] cores have been considered due to their high $A_L$ per volume ratio.

As has been shown in [1], a huge volume reduction is achieved by applying an additional thermal connection between the inductance and an available heat sink or cold plate. The described thermal models of this thermal connection in [1] are based on two principle cooling methods, namely, a cooling pin and a cooling tube as shown in [1, Fig. 4].

The output of the introduced optimization routine in [1] is an optimum core for a specific switching frequency $f_S$ with a minimal volume. The resulting inductor volumes and losses in dependence on the switching frequency are shown in [1, Fig. 7]. For the design at hand, the total appearing losses $P_{L,\max}$ for all boost inductors were limited to 1% of the rated output power $P_0$. Otherwise, the optimization will lead to even smaller and not practically producible inductances and significantly increased losses due to increased current density values.

As mentioned in [1], the resulting inductor volume stays mainly constant for each number of boost stages $n$ in the case of CCM operation mode, since the inductance value is increasing proportionally with $n$ to ensure continuous current operation and maintain a constant inductor current ripple factor. However, due to a limited number of available cores, the resulting inductance volume is not perfectly constant for a different number of boost stages. This can be seen both in Fig. 2(a) for the employment of a cooling pin as heat sink connection and in Fig. 2(b) for the case of a cooling tube (in the case of $n > 1$ already, the total boxed volume of all $n$ inductors is shown).

The tradeoff for the selection of the optimum current ripple factor value $k_{\mathrm{ripple}}$ for the achievement of a minimum total volume is shown in Fig. 3 for a PFC converter driven in CCM with one boost cell, a switching frequency of $f_S = 145$ kHz, and a rated output power of $P_0 = 300$ W. Hereby, the input filter volume is based on the optimization presented in [1], i.e., the optimal number of filter stages and optimal components are chosen for each value of $k_{\mathrm{ripple}}$. It can be seen that the inductance volume is strongly decreasing with increasing current ripple values, whereas the DM EMI input filter volume is only slightly increasing. Thus, the total volume is very large for small current ripple values and stays mainly constant for values larger than $k_{\mathrm{ripple}} \geq 0.4$. Thus, also taking the power losses into

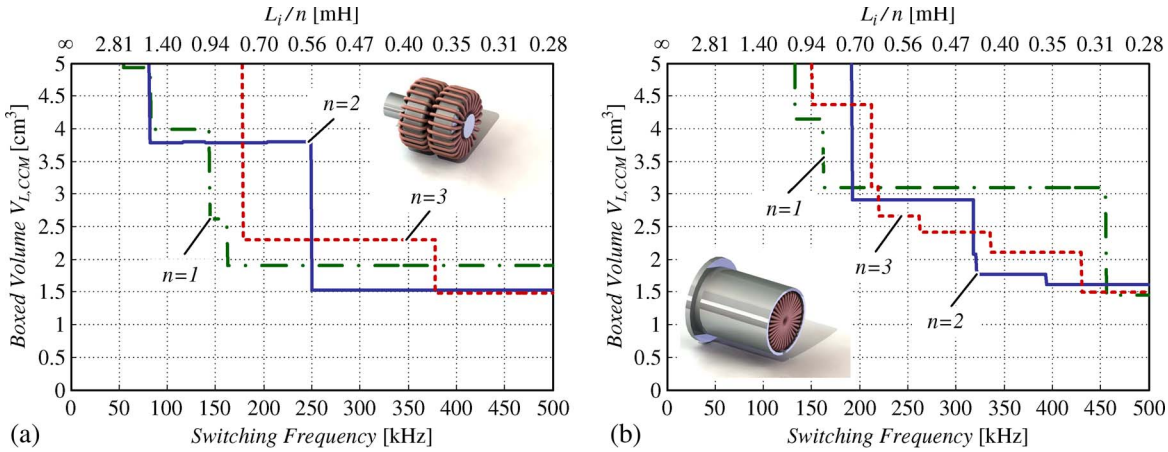


Fig. 2. Resulting total boxed inductor volume [(a) cooling pin and (b) cooling tube] curves for CCM operation in dependence on the number of boost cells $n$ and the switching frequency.

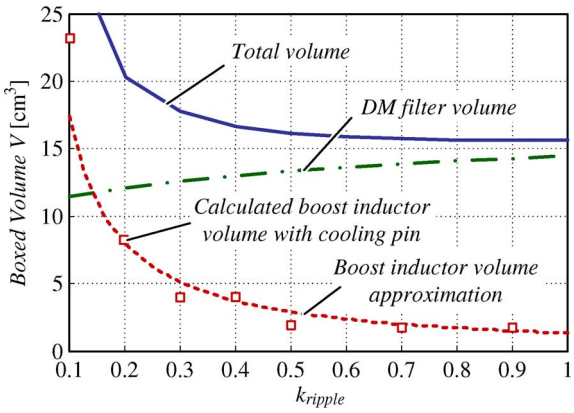


Fig. 3. Dependence of the inductor volume (calculated for a cooling pin based on the results in Fig. 2(a) and approximation curve) and DM EMI filter volume on the inductor current ripple value $k_{\mathrm{ripple}}$ for a boost PFC driven in CCM with one boost cell, a switching frequency of $f_S = 145$ kHz, and a rated output power $P_0 = 300$ W.

account, which are increasing with larger ripple values, for the design at hand $k_{\mathrm{ripple}} = 0.4$ is chosen.

Also in the case of DCM operation, the total inductance volume scales with $V_{L,\mathrm{DCM}} \propto n \cdot L_{\mathrm{DCM}} \cdot i_L^2 \propto$ const [1] and should be constant for a different number of boost stages $n$. Again, due to the limited number of discrete core sizes, there occur differences in the inductor volume for a different number of boost stages (cf. Fig. 4). Thus, for an accurate optimization, the scaling laws are of limited validity and the specific core sizes have to be taken into consideration.

As can be seen in Figs. 2 and 4, the inductance volumes are generally smaller for the DCM operation than for the CCM operation for low switching frequencies in the range of 100–250 kHz due to the fact that, for continuous operation, a higher inductance value is required than for discontinuous operation [1].

Looking at Fig. 2, one can see that for CCM operation, the realization of the heat sink connection by a cooling pin leads to a smaller volume for the design at hand for most switching frequencies. In contrast, in the case of DCM operation (cf. Fig. 4), the cooling tube will be the better choice for terms of a minimum volume design. This is due to the fact that the minimum size of the core in the case of a cooling pin is limited by the required pin diameter for mechanical mounting. For the design at hand, this minimum allowed cooling pin diameter was set to 5 mm to apply an M3 screw head. However, since the difference in volume is not very large, the cooling pin design has been chosen also for the DCM operation due to its easier mechanical construction.

## III. Output Capacitor Design

The choice of the output capacitor has a large effect on the resulting power density of the PFC converter. Following the guideline in [1], the condition $\Delta u_0 < U_0 - \hat{U}_{\mathrm{in,max}}$ leads for a rated output power of $P_0 = 300$ W, an input voltage of $\hat{U}_{\mathrm{in,max}} = \sqrt{2} \cdot 230 + 10\% = 358$ V, and a dc link voltage $U_0 = 400$ V according to

$$\Delta u_0 = \frac{P_0}{2\omega \cdot C_0 \cdot U_0} \tag{6}$$

to a minimum capacitance value of 56 $\mu$F. Concerning the capacitor current ripple, it has been shown in [1] that it only depends on the output power $P_0$ and the voltage ratio $\alpha$. In [1, eqs. 34 and 35], the current ripple values can be calculated analytically for the given specifications and are compared with results derived by numerical simulations in Table I. One can see that the analytical calculation leads to results with adequate accuracy particularly for CCM operation. In the case of DCM operation, the largest deviation of 8% appears for a single boost stage, which is still in an acceptable range. As a result, the analytical derivation is suitable for the capacitor selection.

As expected, the CCM operation leads generally to lower values of the capacitor ripple current as compared to the DCM operation, where a significant current ripple reduction can be achieved by interleaving. In fact, for interleaved operation, the capacitor ripple values for CCM and DCM operations are in a comparable range.

The total boxed capacitor volumes $(V_C)$ of possible dc-link capacitors are shown in Fig. 5, and the specifications of selected components are compiled in Table II. One can see that four capacitors (namely Nr. 2, 3, 4, and 5) lead to a minimum volume design. For the design at hand, capacitor (5) has been chosen

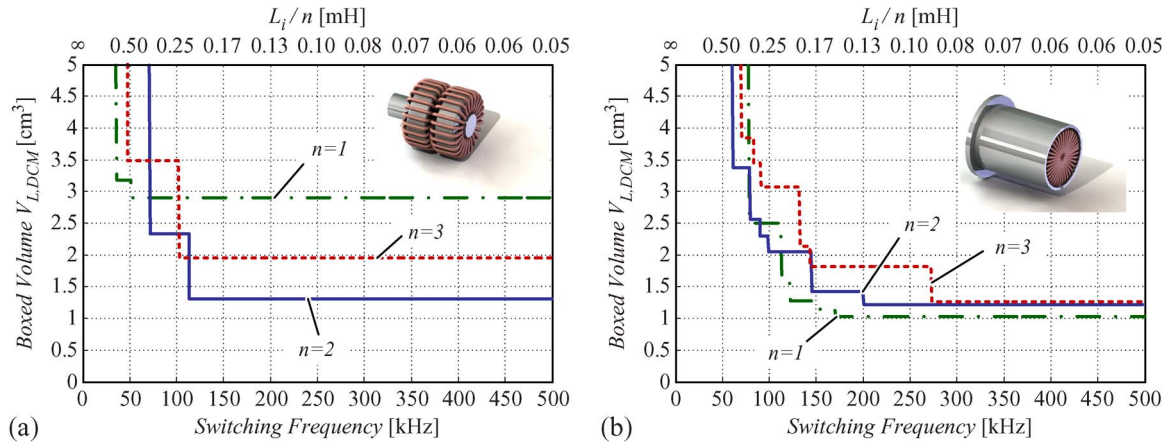


Fig. 4. Resulting total boxed inductor volume [(a) cooling pin and (b) cooling tube] curves for DCM operation in dependence on the number of boost cells $n$ and the switching frequency.

TABLE I
CALCULATED ($I_{C,\mathrm{rms,calc}}$) AND SIMULATED ($I_{C,\mathrm{rms,sim}}$) CAPACITOR rms RIPPLE CURRENTS FOR A PFC WITH A RATED OUTPUT POWER $P_0 = 300$ W, $U_0 = 400$ V, AND $U_{\mathrm{in,rms}} = 230$ V($\alpha = 0.81$) IN DEPENDENCE ON THE OPERATION MODE AND THE NUMBER OF BOOST CELLS $n$

| Operation Mode | $n$ | $I_{C,rms,calc}$ [A] | $I_{C,rms,sim}$ [A] | Deviation [%] |
|---|---|---|---|---|
| CCM | 1 | 0.78 | 0.78 | 0.00 |
| | 2 | 0.61 | 0.62 | 1.00 |
| | 3 | 0.56 | 0.57 | 1.75 |
| DCM | 1 | 1.15 | 1.25 | 8.00 |
| | 2 | 0.83 | 0.78 | 6.41 |
| | 3 | 0.69 | 0.65 | 6.15 |

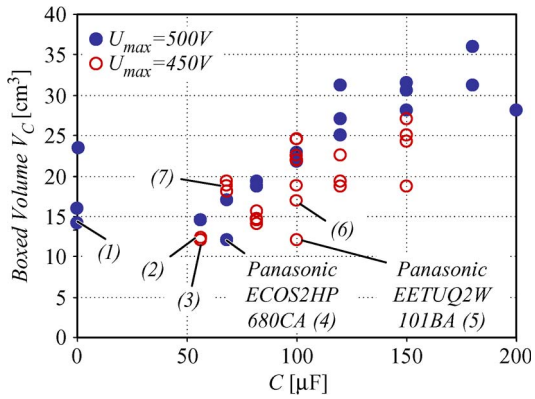


Fig. 5. Total boxed capacitor volumes ($V_C$) of selected capacitors for the boost PFC with a rated output power of $P_0 = 300$ W and a dc-link voltage of 400 V.

due to its highest capacitance/volume ratio and highest allowed current ripple value. For the selected capacitor, the criterion of the maximum allowed capacitor ripple current is fulfilled for all considered operation modes (cf. Table I). Only in the case of DCM operation with one boost stage ($n = 1$) the appearing rms capacitor current ripple is close to the maximum allowed value. Thus, in terms of capacitor lifetime, probably another capacitor could be preferable. However, for the subsequent examinations, capacitor (5) is chosen for all operation modes for reasons of comparability.

## IV. SEMICONDUCTOR SELECTION

Although the realized PFC module will be connected to a cold plate and therefore power losses will be underpart, a loss reduction concerning the semiconductor devices is desirable for reasons of small-size semiconductor packaging and in order to achieve acceptable power efficiency.

The total appearing losses in the semiconductors are generally given by

$$P_{\mathrm{sem}} = n \cdot P_{\mathrm{con}} + n \cdot f_S \cdot \frac{1}{2\pi} \int_0^{2\pi} \left(W_{\mathrm{on}}(\omega t) + W_{\mathrm{off}}(\omega t) + W_{\mathrm{RR}}(\omega t)\right) d\omega t \quad (7)$$

with the conduction losses $P_{\mathrm{con}}$ per boost cell and frequency-dependent switching losses with the loss energy values for the turn-on ($W_{\mathrm{on}}$), turn-off ($W_{\mathrm{off}}$), and the reverse recovery diode ($W_{\mathrm{RR}}$) losses. The calculation of the conduction losses is well defined by datasheet values

$$P_{\mathrm{con}} = I_{T,\mathrm{rms}}^2 \cdot R_{\mathrm{DS,on}} + I_{D,\mathrm{avg}} \cdot U_f + I_{D,\mathrm{rms}}^2 \cdot R_f \quad (8)$$

with the MOSFET on-resistance $R_{\mathrm{DS,on}}$, the diode forward voltage drop $U_f$, and the diode forward resistance $R_f$. The calculation for the transistor rms current $I_{T,\mathrm{rms}}$ and diode avg ($I_{D,\mathrm{avg}}$) and rms ($I_{D,\mathrm{rms}}$) currents can be derived by circuit simulations and/or calculated by integrating the local transistor–diode rms currents over one mains period. The formulas (which lead, in the case of DCM operation, to a considerable calculation effort) are listed in Table III.

Since the loss parameters for turn-on, turn-off, and reverse recovery losses ($W_{\mathrm{on}}$, $W_{\mathrm{off}}$, and $W_{\mathrm{RR}}$) are hard to predict based on datasheet values, several possible transistor–diode combinations have been measured analogously to [17] and [18], and the following simplified dependences could be identified:

$$W_{\mathrm{on}}(\omega t) = a_{\mathrm{on}} + k_{\mathrm{on}} \cdot I_{L,\mathrm{on}}(\omega t) \quad (9)$$

$$W_{\mathrm{off}}(\omega t) = a_{\mathrm{off}} + k_{\mathrm{off}} \cdot I_{L,\mathrm{off}}^2(\omega t) \quad (10)$$

$$W_{\mathrm{RR}}(\omega t) = a_{\mathrm{RR}} + k_{\mathrm{RR}} \cdot I_{L,\mathrm{on}}(\omega t) \quad (11)$$

TABLE II
SPECIFICATIONS OF SELECTED CAPACITORS

| Nr. | Manufacturer | Type | C [$\mu$F] | $U_{max}$ [V] | $I_{C,rms,max}$ @ 10 kHz [A] | $V_{C,tot}$ [cm$^3$] |
|---|---|---|---|---|---|---|
| 1 | muRata | GRM55DR72J224KW01l | 255 × 0.22 | 630 | – | 14.54 |
| 2 | Panasonic | ECOS2WP560BA | 56 | 450 | 0.98 | 12.1 |
| 3 | Panasonic | ECOS2WP560AA | 56 | 450 | 0.98 | 12.0 |
| 4 | Panasonic | ECOS2HP680CA | 68 | 500 | 1.09 | 12.1 |
| 5 | Panasonic | EETUQ2W101BA | 100 | 450 | 1.30 | 12.1 |
| 6 | Epcos | B43501 | 100 | 450 | 1.35 | 16.9 |
| 7 | Evox–Rifa | PEH536YBC2680M2 | 68 | 450 | 1.40 | 18.75 |

TABLE III
CALCULATION OF TRANSISTOR AND DIODE rms CURRENTS FOR CCM AND DCM OPERATIONS

| Operation Mode | Transistor | Diode |
|---|---|---|
| CCM | $I_{T,rms}^2 = \hat{I}_{L,CCM,avg}^2 \cdot \left(\frac{1}{2} - \frac{4}{3\pi} \cdot \alpha\right)$ | $I_{D,rms}^2 = \hat{I}_{L,CCM,avg}^2 \cdot \left(\frac{4}{3\pi} \cdot \alpha\right)$ |
| DCM | $I_{T,rms}^2 = \frac{2}{\pi} \cdot \int_0^{\frac{\pi}{2}} \frac{1}{3} \cdot f_S \cdot t_{on,DCM}(\omega t) \cdot \Delta I_{DCM}(\omega t)^2 \, d\omega t$ [a] | $I_{D,rms}^2 = \frac{2}{\pi} \cdot \int_0^{\frac{\pi}{2}} \frac{1}{3} \cdot f_S \cdot t_{off,DCM}(\omega t) \cdot \Delta I_{DCM}(\omega t)^2 \, d\omega t$ |
| with | $t_{on,DCM} = \frac{d_{DCM}}{f_S}$ [b] | $t_{off,DCM} = \frac{\alpha \cdot \sin(\omega t)}{f_S} \cdot \frac{\sqrt{1-\alpha}}{1-\alpha \cdot \sin(\omega t)}$ |

TABLE IV
MEASURED LOSS PARAMETERS OF COMMERCIALLY AVAILABLE 600-V DIODE–TRANSISTOR COMBINATIONS FOR AN OUTPUT VOLTAGE OF $U_0 = 400$ V

| Diode | Transistor | $a_{on}$ [$\mu$J] | $k_{on}$ $\left[\frac{\mu J}{A}\right]$ | $a_{off}$ [$\mu$J] | $k_{off}$ $\left[\frac{\mu J}{A^2}\right]$ | $R_{DS,on}$ [$\Omega$] | $a_{RR}$ [$\mu$J] | $k_{RR}$ $\left[\frac{\mu J}{A}\right]$ | $U_f$ [V] | $R_f$ [$\Omega$] |
|---|---|---|---|---|---|---|---|---|---|---|
| *Cree CSD 06060* | *FCP7N60* | 7.04 | 2.32 | 4.50 | 0.04 | 0.53 | 4.20 | 0.00 | 0.90 | 0.15 |
| | *FCP11N60F* | 7.24 | 2.21 | 6.00 | 0.03 | 0.32 | 4.20 | 0.00 | 0.90 | 0.15 |
| | *ICTP4N60* | 7.81 | 2.63 | 4.00 | 0.08 | 2.00 | 4.20 | 0.00 | 0.90 | 0.15 |
| | *IXTP7N60* | 7.23 | 2.66 | 5.00 | 0.20 | 1.10 | 4.20 | 0.00 | 0.90 | 0.15 |
| | *IXFP10N60* | 7.55 | 1.85 | 7.00 | 0.07 | 0.74 | 4.20 | 0.00 | 0.90 | 0.15 |
| | *STP7NK60Z* | 7.47 | 2.72 | 4.48 | 0.87 | 1.00 | 4.20 | 0.00 | 0.90 | 0.15 |
| | *STP10NK60Z* | 7.17 | 2.97 | 6.50 | 0.18 | 0.65 | 4.20 | 0.00 | 0.90 | 0.15 |
| *IXYS DSEI 8* | *FCP7N60* | 1.22 | 17.86 | 4.50 | 0.03 | 0.53 | 1.18 | 13.84 | 0.98 | 0.05 |
| | *FCP11N60F* | 1.42 | 16.19 | 6.00 | 0.01 | 0.32 | 1.03 | 12.06 | 0.98 | 0.05 |
| | *IXFP10N60* | 2.56 | 17.97 | 7.00 | 0.18 | 0.74 | 1.03 | 13.52 | 0.98 | 0.05 |
| *STM STTH806TTI* | *FCP7N60* | 4.45 | 1.93 | 4.00 | 0.0024 | 0.53 | 3.08 | 0.40 | 2.45 | 0.15 |

whereby for the CCM operation, $I_{L,\mathrm{on}}(\omega t) \approx I_{L,\mathrm{off}}(\omega t) \approx I_{L,\mathrm{CCM,avg}}(\omega t)$, and for the DCM operation, $I_{L,\mathrm{on}} = 0$ and $I_{L,\mathrm{off}} = \Delta I_{L,\mathrm{DCM}}(\omega t)$ is valid [1]. The parameters for an output voltage of $U_0 = 400$ V are shown in Table IV for several commercially available transistor–diode combinations, including SiC diodes (*Cree CSD 06060*).

One can see that the diode–transistor combinations with SiC *Cree* diodes show no $k_{\mathrm{RR}}$ and significantly reduced $k_{\mathrm{on}}$ values concerning combinations with standard Si diodes (cf. Table IV). This effect is a result of the reduced reverse recovery capacitance of the SiC diodes [19], [20] and leads to the conclusion that diode–transistor combinations with SiC diodes are preferable for PFC applications driven in CCM mode [cf. Fig. 6(a)]. Since the turn-on current in the case of DCM operation is always zero, the advantage of SiC diodes is negligible and transistor–diode combinations with standard Si diodes are preferable in this case for reasons of lower costs. In addition, SiC diodes show a higher value of the forward resistance $R_f$, which will even lead to higher semiconductor losses in the case of DCM operation using SiC diodes compared to transistor–diode combinations with standard Si diodes [cf. Fig. 6(b)].

So-called tandem diodes such as the considered *STTH806TTI* from *STM* consist of two low-voltage Si diodes in series and therefore feature a smaller reverse recovery capacitance and resulting reduced switching loss parameters [20]. However, since two diodes are connected in series to achieve the high voltage ratings, the forward voltage $U_f$ is increased significantly. As a result, tandem diodes can be used to replace cost-intensive SiC diodes for the CCM operation and actually lead to lower semiconductor losses for switching frequencies beyond 350 kHz compared to setups featuring SiC diodes (cf. Fig. 6).

For the design at hand, the diode–transistor combination *IXYS DSEI8* and *FCP7N60* for a PFC converter driven in DCM operation has been chosen, whereby for CCM operation, the combination *Cree CSD 06060* and *FCP7N60* was selected.

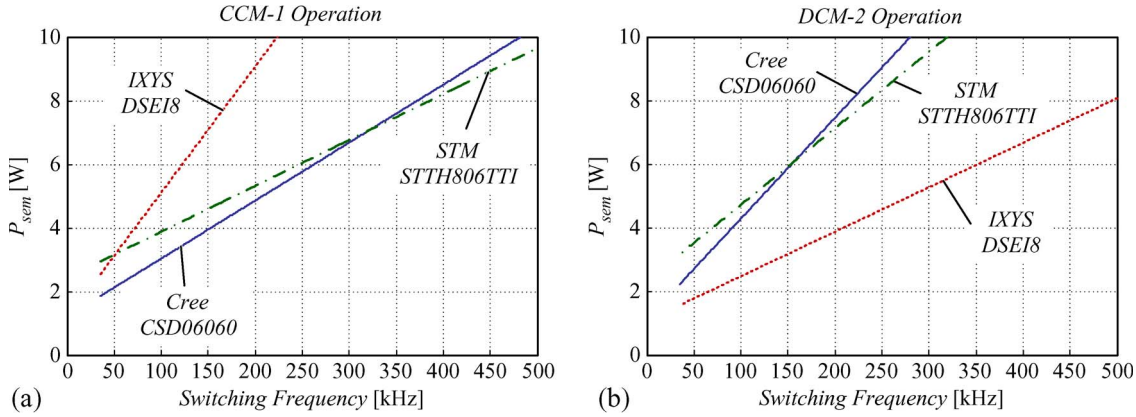


Fig. 6. Total boost semiconductor losses $P_{\rm sem}$ for (a) one PFC cell driven in CCM and (b) two interleaved DCM cells operation in dependence on the used boost diode and the switching frequency exemplarily shown for a rated output power of $P_0 = 300$ W (chosen transistor: *FCP7N60*).

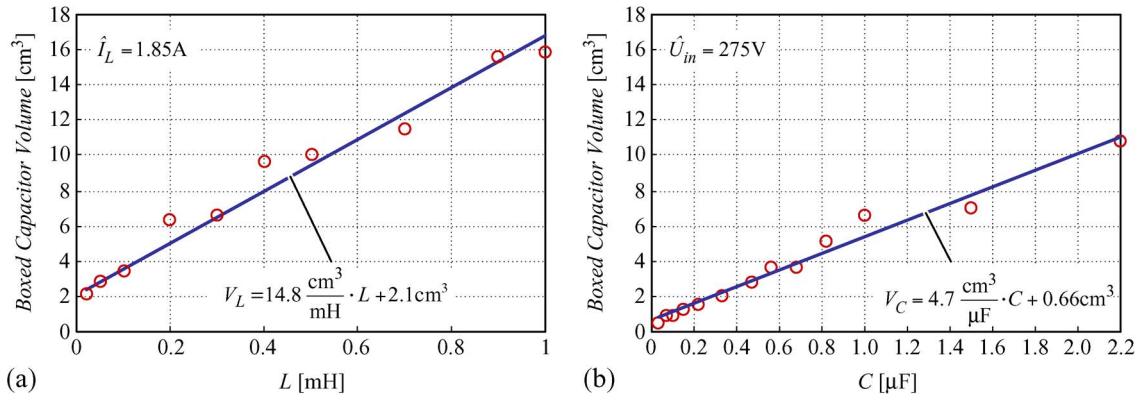


Fig. 7. (a) Linear approximation for the calculation of the filter inductor volume for a specific peak input current of 1.85 A and (b) the approximation for filter capacitance volume based on various X2 foil capacitors and a voltage rating of 275 V.

## V. Input Filter Design

An input filter is desired for switched PWM converters to fulfill the electromagnetic compatibility (EMC) standards [21] regarding conducted emission noise occurring within the frequency range of 150 kHz–30 MHz. A detailed description of the design procedure has already been done in [1]. There, the simulated voltage $U_{\rm meas}$ over $R_{\rm LISN}$ was used to calculate the quasi-peak voltage spectrum by a quasi-peak detection network as defined in [22]. Out of the calculated quasi-peak voltage and the limits given in [21], the required attenuation, which has to be delivered by the EMI filter to fulfill the standards, can be calculated.

The resulting filter volume is a function of the needed attenuation and the boost converter switching frequency. A routine for optimizing this filter volume is described in [1] and [23]. In the following section, results of this optimization routine carried out for a rated output power of $P_0 = 300$ W for CCM and DCM operations for one to three interleaved boost cells will be presented.

### A. DM Input Filter Design

The design of the DM input filter leads to volume optimization since both the filter capacitor and filter inductances are arbitrary as long as [1, eq. 39] is fulfilled. The optimization routine presented in [1, eqs. 40–43] is based on linearized capacitor and inductor volume curves (cf. Fig. 7). For *Magnetics MPP* [24] cores, which are selected here due to their highest inductance/volume ratio, and a selection of various X2 foil capacitors with a rated voltage of 275 V, the volume curves are given by (for $\hat{I}_L = 1.85$ A and $\hat{U}_{\rm in} = 275$ V)

$$V_L = 14.8 \frac{\text{cm}^3}{\text{mH}} \cdot L_{\rm DM} + 2.1 \text{ cm}^3 \tag{12}$$

$$V_C = 4.7 \frac{\text{cm}^3}{\mu\text{F}} \cdot C_{\rm DM} + 0.66 \text{ cm}^3. \tag{13}$$

A more general approximation of the inductor and capacitor volumes with dependences on current and voltage is given in [25]. This leads to a minimum volume for the DM component values of $L_{\rm DM}$ and $C_{\rm DM}$ for a certain number of filter stages $n_f$. Subsequently, the number of filter stages $n_f$ can be varied in order to identify the input filter topology with minimum volume. Exemplarily, the optimum number of DM filter stages for a dual-interleaved 300-W PFC operated in DCM is $n_f = 2$ for a switching frequency of $f_S = 200$ kHz (cf. [1, Fig. 12(b)]), and the following optimal DM filter values (cf. Fig. 1) are derived: $C_{\rm DM,1} = C_{\rm DM,2} = 150$ nF and $L_{\rm DM,1} = L_{{\rm DM},d} = L_{\rm DM,2} = 44.6$ $\mu$H according to [1, eqs. 41 and 42] and $R_d = 33$ $\Omega$ for optimum filter damping [1], [26]. Interestingly, for single CCM operation as well as for single DCM operation, $n_f = 2$ leads to a minimal filter volume for 300-W output power and for

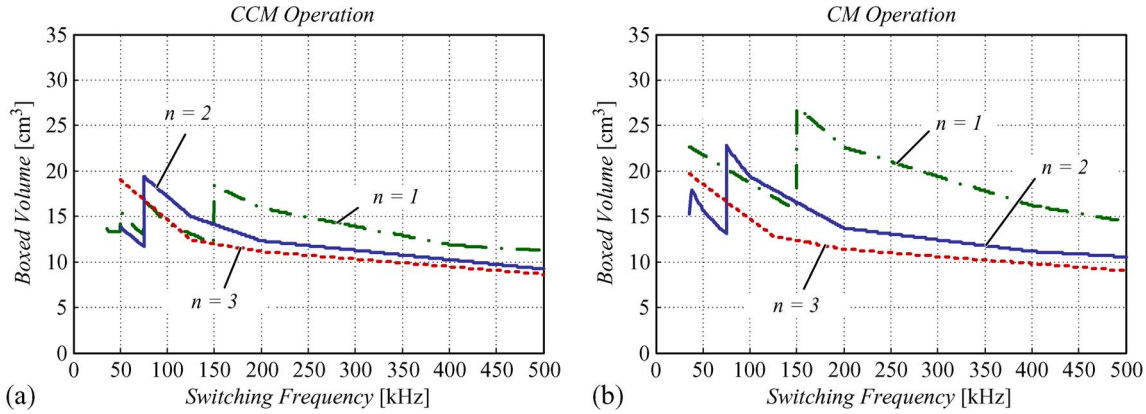


Fig. 8. Boxed volume curves for the DM filter (for optimum number of filter stages $n_f = 2$) in dependence on the switching frequency and the number of boost cells $n$. (a) For CCM operation. (b) For DCM operation.

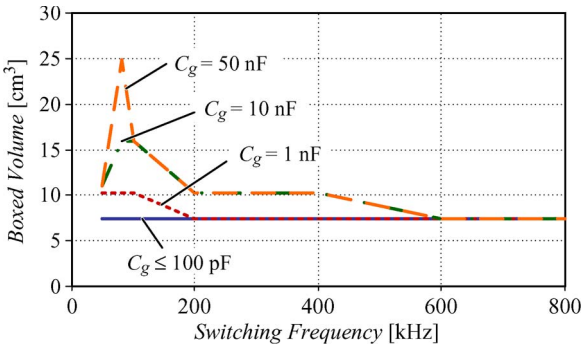


Fig. 9. CM filter volume in dependence on the capacitance to ground $C_g$ for $n_f = 1$.

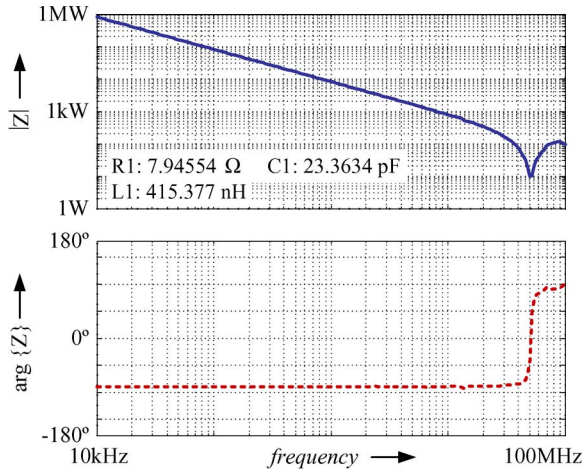


Fig. 10. Measured impedance to ground along with the equivalent circuit parameters for the design at hand.

the considered switching frequency range. This fact is due to similar attenuation requirements of these operation modes in the range of 40–60 dB, where $n_f = 2$ is optimal [25].

The resulting DM filter volumes for the optimum number of filter stages $n_f = 2$ are shown in Fig. 8(a) for CCM operation mode and in Fig. 8(b) for DCM operation mode for a different number of interleaved boost cells $n = 1, 2, 3$. A general tendency is the decreasing filter volume with increasing number of boost cells and increasing switching frequency. Particularly in the case of DCM operation, the volume reduction by interleaving is significant between $n = 1$ and $n = 2$. If interleaving is employed, the difference between CCM and DCM operation modes is becoming smaller with a higher number of boost cells so that for two and more boost cells and switching frequencies beyond 200 kHz, the resulting filter volumes for CCM and DCM are comparable.

Hereby, constant switching frequencies have been considered for both operating modes. As mentioned in [1], the variation of the switching frequency within a defined range would lead to a reduction of the attenuation requirement for the input filter and consequently to a smaller filter size [27]–[29]. For the designs at hand, this would lead to a reduction of the input filter volume by about 2 cm$^3$ for both operation modes.

### B. CM Input Filter Design

In contrast to the DM filter design, the CM capacitance per phase is limited to a total maximum value of $C_{\mathrm{CM,max}} = 44$ nF due to the maximum leakage current to ground $I_{\mathrm{GND,max,rms}} = 3.5$ mA [30]. Due to parasitic and stray capacitances appearing in the circuit and tolerances in the capacitance values [23], a lower value has been chosen for the design at hand, i.e., $C_{\mathrm{CM}} = 2 \times 10$ nF $= 20$ nF. As described in [23], *VITROPERM 500 F* [31] nanocrystalline cores from *Vacuumschmelze GmbH (VAC)* turn out to be the best choice for CM filter inductances $L_{\mathrm{CM}}$ for reasons of high permeability, resulting in a high inductance/volume ratio, and excellent high-frequency behavior. Since the number of available cores is limited, linearization of the inductance volume data of the cores is not reasonable, and the calculated volumes will show discrete volume steps in the following section.

As mentioned in [1], the capacitance to ground $C_g$, which is most responsible for the CM noise emission, is hardly predictable in an accurate manner due to many uncertainties in the noise propagation path. Therefore, the filter calculation has been done in a parametric way for several possible values of $C_g$, namely, 10 pF, 100 pF, 1 nF, 10 nF, and 50 nF. Furthermore, single-layer winding construction has been assumed for the CM choke [1]. With this, a single filter stage $n_f = 1$ is sufficient to attenuate the CM noise and results in a minimal volume [1]. As can be seen in Fig. 9 for parasitic capacitance values below 100 pF, the same boxed volume results for all considered

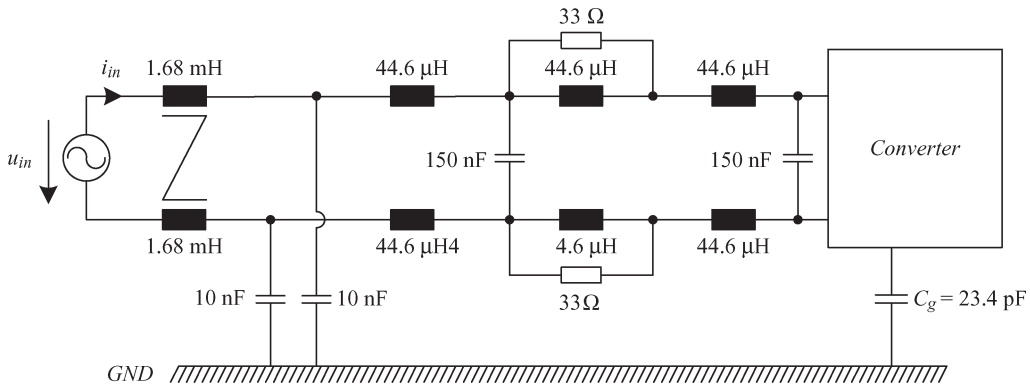


Fig. 11. Final filter topology for the 300-W PFC in 2-DCM operation with $f_S = 200$ kHz and two DM filter stages and one CM filter stage.

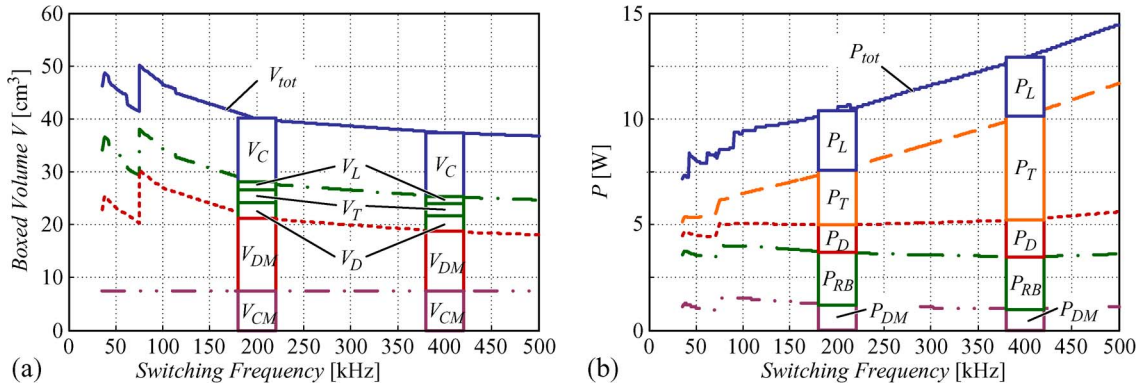


Fig. 12. (a) Calculated boxed volume and (b) loss curves for a two-stage PFC driven in DCM operation with $n = 2$ boost stages ($C_g = 23.4$ pF).

switching frequencies for the dual DCM operation. For all other considered operation modes, similar conclusions can be drawn, since the parasitic capacitances $C_g$ (and, therefore, the noise emission levels) are in a comparable range.[1] For the laboratory setup (dual-interleaved DCM), a capacitance of $C_g = 23.4$ pF (cf. Fig. 10) has been measured.

As a result, for the PFC driven in 2-DCM operation at 200 kHz, a CM filter with the following values has been employed: $C_{\rm CM} = 10$ nF and $L_{\rm CM} = 1.68$ mH (at 400 kHz). The total input filter for this case is shown in Fig. 11 along with the filter parameter values. The DM inductances are symmetrically partitioned to the two input lines [32] in order to suppress the mixed mode noise in combination with the DM capacitance [33].

## VI. Overall Comparison

The optimum operation mode (CCM or DCM) and number of boost stages $n$ can now be found by combining all results of the previous sections. Exemplarily, the resulting volumes for a two-stage PFC driven in DCM operation are shown in Fig. 12(a). Here, $V_{\rm tot}$ means the resulting total volume, including the CM filter ($V_{\rm CM}$), the DM filter volume ($V_{\rm DM}$), the volume of all boost elements, such as boost diode(s) ($V_D$) (including the rectifier bridge), the boost transistor(s) (including heat sink connection) ($V_T$), the boost inductor(s) ($V_L$), and the output capacitor ($V_C$). The resulting power losses for each part are drawn in Fig. 12(b). One can see the losses of the DM input filter ($P_{\rm DM}$), the rectifier bridge ($P_{\rm RB}$), the boost diode(s) ($P_D$), the boost transistor(s) ($P_T$), the boost inductance(s) ($P_L$), and the total overall losses $P_{\rm tot}$. The power losses of the CM input filter have been neglected here, since they are very small and additionally show the same amount for all considered topologies and therefore do not have any influence on the comparison of the several topologies. In addition, the losses of auxiliary devices have not been considered for this comparison.

In such a way, the total volume and loss curves can be calculated both for CCM and DCM operations for a different number of boost stages $n = 1, 2, 3$. The resulting overall volumes and losses are shown in Fig. 13 for CCM and in Fig. 14 for DCM. It has to be mentioned that the total volume in these curves only represents the sum of all boxed volumes of the components. Since, in reality, not all the space in a converter can be utilized for components, this value represents only a theoretical value.

For CCM operation mode, one can see that very similar total volumes result for a different number of boost stages. For switching frequencies below 150 kHz, a single boost stage is sufficient to achieve minimum volume and also minimum losses. For a higher switching frequency, a slight volume reduction can be achieved by interleaving two boost cells. However, this slight advantage is paid by significantly higher losses

[1] Interleaving of more than one boost cell, in general, will lead to higher values of $C_g$. However, the influence of interleaving on the value of $C_g$ is hard to predict in an accurate manner and for small values of $C_g$ as it is the case here that the CM filter volume stays constant.

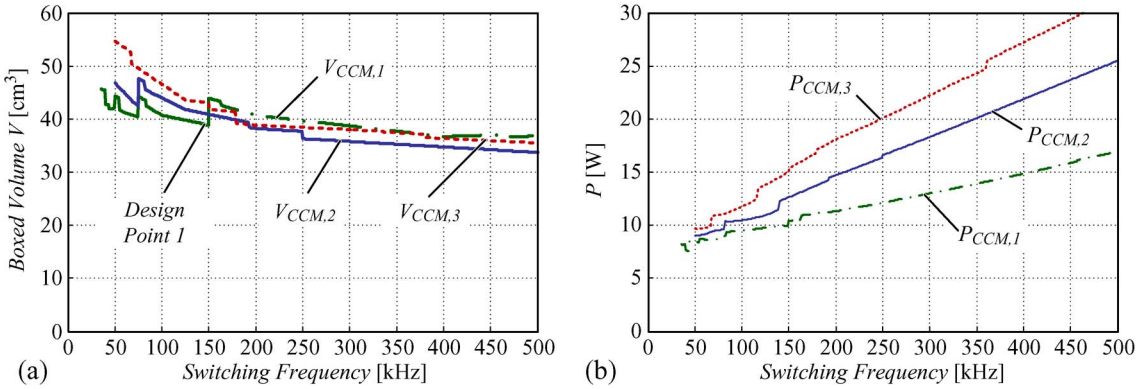


Fig. 13. (a) Calculated total boxed volume and (b) loss curves for interleaved PFC topologies driven in CCM mode with $n = 1$, 2, and 3 boost stages ($C_g = 23.4$ pF).

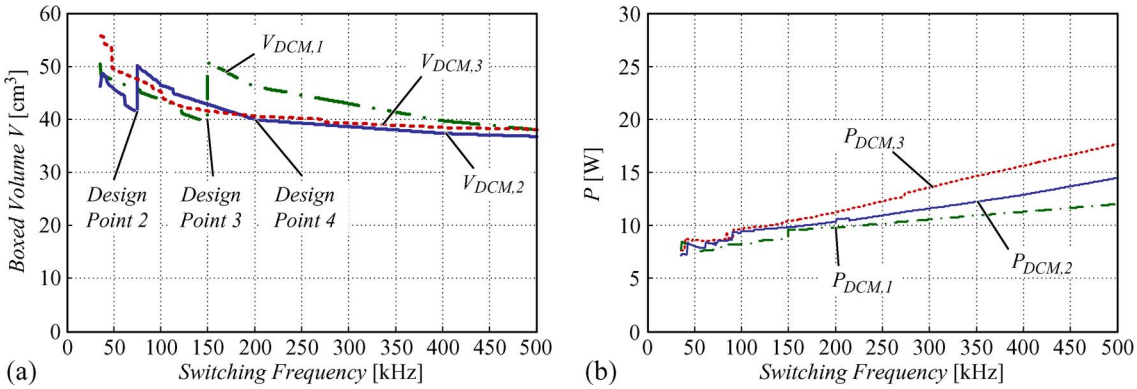


Fig. 14. (a) Calculated total boxed volume and (b) loss curves for interleaved PFC topologies driven in DCM mode with $n = 1$, 2, and 3 boost stages ($C_g = 23.4$ pF).

TABLE V
COMPARISON OF DIFFERENT DESIGN POINTS FOR A PFC CONVERTER WITH A RATED OUTPUT POWER OF $P_0 = 300$ W

| Design Point | Operation Mode | $n$ | $f_S$ [kHz] | Volume [cm$^3$] | Theoretical Power Density [kW/dm$^3$] | $\eta_{th}$ [%] | Lifetime | Current Sensor | Semiconductor Costs |
|---|---|---|---|---|---|---|---|---|---|
| 1 | CCM | 1 | 140 | 39.3 | 7.6 | 96.7 | + | – | – |
| 2 | DCM | 2 | 70 | 41.8 | 7.2 | 97.3 | + | + | + |
| 3 | DCM | 1 | 140 | 40.1 | 7.5 | 97.1 | – | + | + |
| 4 | DCM | 2 | 200 | 39.9 | 7.5 | 96.6 | + | + | + |

[cf. Fig. 13(b)], which makes this design inappropriate (e.g., by comparing CCM-1 at 140 kHz and CCM-2 at 350 kHz, a reduction of 10% of the volume results in 200% power losses). Considering this, the one-stage CCM operation at 140 kHz is identified as a first design point and indicated as "Design Point 1" in Fig. 13(a) and Table V.

For DCM operation, on the other hand, interleaving of two boost stages can make sense for certain frequencies, e.g., for 70 kHz, where the first harmonic (appearing at 140 kHz due to dual interleaving) is still below the measurement range of 150 kHz–30 MHz or above 150 kHz, where the first harmonic falls within the measurement range for single operation. Fig. 14(b) shows that the power losses in the case of interleaved DCM operation do not significantly increase as compared to single operation. Thus, two design points (indicated as "Design Point 2" and "Design Point 4" in Fig. 14(a) and Table V) for 2-DCM operation are identified. Between these two points, single operation leads to a minimum volume design, indicated as "Design Point 3." As can be seen in Fig. 14(a), interleaving of three boost cells will not result in a minimum volume design for the given specifications and is also characterized by the highest losses.

The chosen design points for CCM and DCM operations are summarized in Table V. Interestingly, the resulting theoretical power densities and calculated efficiencies are quite similar. Concerning the achievable efficiency design point 2 with a PFC driven in 2-DCM operation at low switching frequency (70 kHz) might be preferable ($\eta_{\rm th} = 97.3\%$). However, since the resulting power density is more important for the design at hand, this design point was not selected. High power density and high efficiency can be achieved with design point 3 by 1-DCM operation at a switching frequency of 140 kHz. For reasons of lower capacitor lifetime (due to the higher capacitor rms current ripple [1], [34], [35]), this design was not chosen.

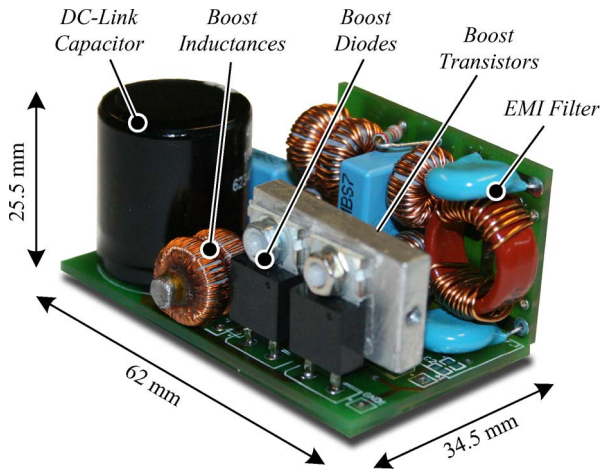


Fig. 15. Experimental setup including EMI filter of the two-stage interleaved boost converter driven in DCM operation with a cooling pin as thermal connection of the boost inductance to the cold plate and a rated output power of $P_0 = 300$ W.

Design point 1 is the classic boost PFC design with a single boost cell driven in CCM operation at a switching frequency of 140 kHz. This design will lead to the highest power density and an acceptable efficiency. However, since cost-intensive SiC diodes and additional current sensors, which are not included in the volume calculation, are necessary, this design was not chosen. For the design at hand, design point 4 was chosen which leads to a theoretical power density of 7.5 kW/dm$^3$ and a calculated efficiency of $\eta_{\text{th}} = 96.6\%$. This design combines an excellent power density with an acceptable efficiency and features good capacitor lifetime and low component costs due to the absence of current sensors and the utilization of standard silicon devices. In the subsequent section, these theoretical values will be compared with measurements on a prototype system.

## VII. Experimental Verification

In order to experimentally verify the previously performed optimizations, a laboratory prototype setup as shown in Fig. 15 has been built up. The laboratory system specifications and assumptions needed for the optimization as described in [1] can be found in Table VI.

In Fig. 16, one can see the current and voltage measurements done with the experimental setup. The inverter input current $i_{\text{in}}$ is in phase with the input voltage $u_{\text{in}}$, and the power factor has been measured to 99.7%. The total harmonic distortion has been measured to 6.4% at full load. In Table VII, one can see the measured losses. The total efficiency is measured to 96.4% and consequently only 0.2% below the calculated efficiency (cf. Section VI).

The measured boxed volumes of all components are shown in Table VIII, and one can see that the calculated component volumes match very well. The resulting total volume (calculated out of the outer dimensions shown in Fig. 14) of the converter is 54.5 cm$^3$, which leads to a power density of 5.5 kW/dm$^3$. The reason for the difference between the theoretical (given by summation of the boxed volumes of the components) and the actual power density lies in the fact that not all the space in the converter can be utilized, mainly due to different heights of the components, electrical clearances, and additional signal electronics circuitry (this difference would be even bigger, if the real volumes instead of the boxed volumes would have been considered).

TABLE VI
Specifications and Assumptions for a Two-Stage DCM @ 200-kHz Laboratory Setup

| Variable | Value | Unit | Description |
|---|---|---|---|
| General Specifications | | | |
| $P_0$ | 300 | W | Max. output power |
| $U_0$ | 400 | V | DC–link voltage |
| $U_{in,rms}$ | 230 | V | Mains voltage and tol. band: $^{+10\%}_{-15\%}$ |
| $\omega$ | $2\pi \cdot 50$ | rad/s | Mains frequency |
| $f_S$ | 200 | kHz | Switching frequency |
| $U_{C,max}$ | 450 | V | Max. capacitor voltage |
| $U_{T,max}$ | 600 | V | Max. transitor voltage |
| $U_{D,max}$ | 600 | V | Max. diode voltage |
| Boost inductor design for a 2–stage interleaved PFC driven in DCM | | | |
| $L_{DCM}$ | 115 | $\mu$H | Boost inductance<br>Core: *Magnetics MPP 55132*, $N = 103$ |
| $r_{pin,min}$ | 5 | mm | Min. needed cooling pin radius |
| $d_{tube}$ | 1 | mm | Cooling tube wall thickness |
| $d_{fill}$ | 0.5 | mm | App. filling material thickness |
| $\lambda_{epoxy}$ | 0.3 | $\frac{\text{W}}{\text{m}^2\text{K}}$ | Thermal conductivity of epoxy |
| $\lambda_{Al}$ | 237 | $\frac{\text{W}}{\text{m}^2\text{K}}$ | Thermal cond. of aluminium |
| $k_f$ | 0.5 | | Filling factor |
| $T_{max}$ | 30 | °C | Max. allowed temp. drop |
| $P_{L,max}$ | 3 | W | Max. allowed inductor losses (1% of $P_0$) |
| EMI filter design for DM ($n_f = 2$) and CM ($n_f = 1$) EMI filter | | | |
| $L_{DM,i}$ | 44.6 | $\mu$H | Differential mode inductance @ $2 \cdot f_S$<br>C: *Magnetics MPP 55291*, $N = 38$ |
| $C_{DM,i}$ | 150 | nF | Differential mode capacitance |
| $L_{CM}$ | 1.68 | mH | Common mode inductance @ $2 \cdot f_S$<br>C: *Vacuumschmelze W620*, $N = 2 \cdot 11$ |
| $C_{CM}$ | 10 | nF | Common mode capacitance |
| $C_g$ | 23.4 | pF | Capacitance to ground |
| $R_d$ | 33 | $\Omega$ | Damping resistor |

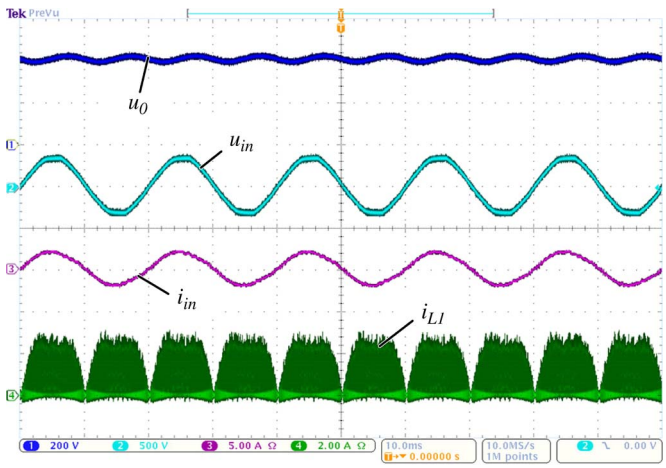


Fig. 16. Voltage and current measurements done with the laboratory setup at full load $P_0 = 315$ W (DCM with $f_S = 200$ kHz) (voltage scale CH1 200 V/div, voltage scale CH2 500 V/div, current scale CH3 5 A/div, current scale CH4 2 A/div, and time scale 10 ms/div).

TABLE VII
MEASURED PARAMETERS FOR A TWO-STAGE DCM PFC @ 200 kHz

| $U_{in}$ [Vrms] | $I_{in}$ [Arms] | PF [%] | THD [%] | $P_{in}$ [W] | $U_0$ [Vrms] | $I_0$ [Arms] | $P_0$ [W] | $P_{tot}$ [W] | Volume [cm$^3$] | Power Density [kW/dm$^3$] | $\eta$ % |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 235 | 1.396 | 99.7 | 6.4 | 327 | 408 | 0.773 | 315 | 11.8 | 54.5 | 5.5 | 96.4 |

TABLE VIII
COMPARISON OF CALCULATED AND MEASURED BOXED COMPONENT VOLUMES IN CUBIC CENTIMETERS

| | $V_{L,b,pin}$ | $V_T + V_D$ | $V_C$ | $\boldsymbol{V_{PFC}}$ | $V_{L,DM}$ | $V_{C,DM}$ | $\boldsymbol{V_{DM}}$ | $V_{L,CM}$ | $V_{C,CM}$ | $\boldsymbol{V_{CM}}$ | $\boldsymbol{V_{tot}}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{calc}$ | 1.3 | 7.8 | 12.1 | **21.2** | 6 × 1.9 | 2 × 2.7 | **13.9** | 2.8 | 2 × 4.7 | **7.5** | **42.6** |
| $V_{meas}$ | 1.4 | 7.7 | 12.6 | **21.7** | 6 × 1.9 | 2 × 2.6 | **13.8** | 3.2 | 2 × 4.0 | **7.3** | **42.8** |

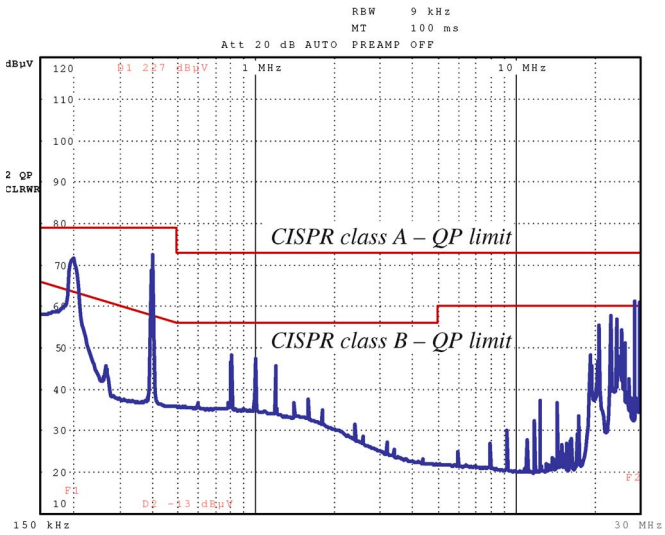


Fig. 17. Measured EMI conducted quasi-peak noise spectrum performed with the laboratory setup at full load $P_0 = 315$ W (2-DCM with $f_S = 200$ kHz).

Furthermore, the EMI filter design has been verified by standardized EMC measurements of the conducted emissions with a quasi-peak test receiver (cf. Fig. 17). The measurements point out that the filter design and optimization routine [1] delivers satisfying results in the frequency range below 10 MHz. The highest measured peak appears at 400 kHz (two times the switching frequency), and the safety margin to the limits given in [21] can be found to be 6 dB. The peaks appearing at frequencies beyond 10 MHz (which are still well below the relevant limits) are presumably caused by parasitics of the filter inductances, which make the filter less effective with increasing frequency [23].

## VIII. FURTHER VOLUME OPTIMIZATION BY INTEGRATED EMI FILTER

In this section, it is evaluated to which extent the power density of the PFC system can be further increased by integrating the EMI filter in the PCB. This step can lead to a volume reduction of the filter and may improve the form factor as the shape becomes more rectangular and the air between the components is removed as can be seen in the photos of the realized discrete (a) and integrated (b) input filters in Fig. 18. In the integrated filter, the DM chokes are realized by PCB tracks, which are covered by magnetically conductive ferrite sheets (*TDK-IRJ08AB*). Since the permeability of the ferrite sheet is relatively low ($\mu_r \approx 100$), for the CM choke, a normal *ELP22* core is utilized in order to achieve the required CM inductance of 1.68 mH. The winding of the CM choke is also realized by PCB tracks.

In Fig. 19, an exploded view of the integrated filter is shown. The two DM chokes—one in the upper and one in the lower rail (cf. Fig. 1)—are realized by two coupled inductors consisting of the package: ferrite sheet–two-layer PCB–$\mu$-metal–two-layer PCB–ferrite sheet. With the $\mu$-metal layer, the coupling of the two inductors is determined. Further details about the design procedure of the integrated filter can be found in [36]. In the considered integrated filter, the damping resistor and the capacitors are implemented by SMD components, which are mounted on top of the ferrite sheet, which is compatible to the PCB manufacturing process, so that on top of the ferrite sheet, a laminate with copper tracks and pads for mounting the components could be realized. In a second step, the capacitors could also be integrated in the PCB by capacitive layers. Since the capacitance per square centimeter values of the available materials are relatively low, this step of integration has not been investigated for the considered EMI filter.

In Fig. 20, the measurement results for the attenuation provided by the integrated and the discrete filter are shown. There, it can be seen that the integrated filter provides approximately the same amount of attenuation as the discrete filter except for the lower frequency range in terms of CM due to the utilized SMD CM capacitors. Furthermore, by increasing the DM capacitance by SMD capacitors mounted on top of the ferrite sheet, where enough space is left, the DM damping of the filter could be improved, so that the damping of the integrated filter perfectly matches with that of the discrete filter.

With the dimensions given in Fig. 18, the volumes of the discrete (18.75 cm$^3$) and the integrated filter (16 cm$^3$) can be calculated. Thus, a reduction of 15% of the input filter volume could be achieved by integration for the design at hand, resulting in a system power density of 6.2 kW/dm$^3$. However, this gain in power density may not be relevant for many practical applications due to the difficult design, high material costs, and difficult handling.

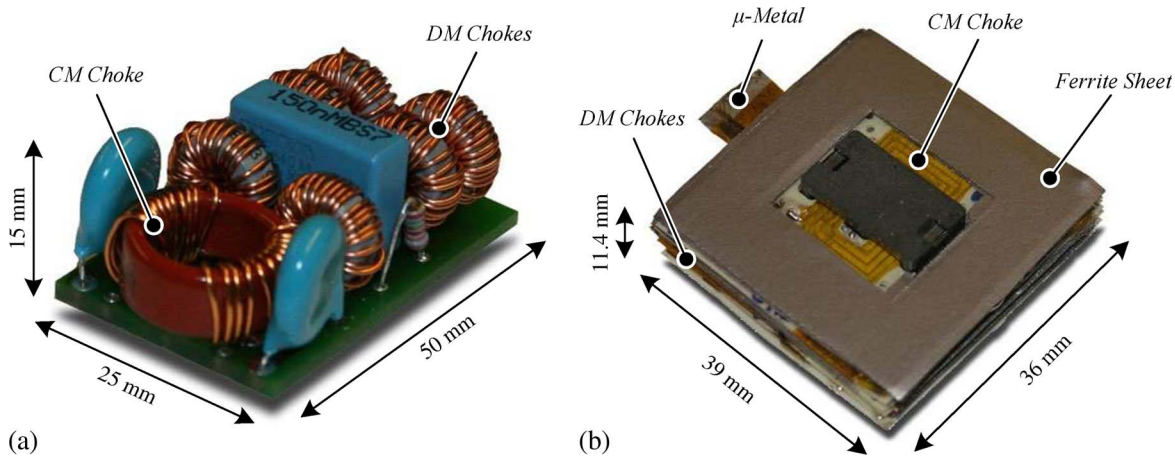


Fig. 18. Photographs of the (a) discrete and (b) the integrated EMI filter.

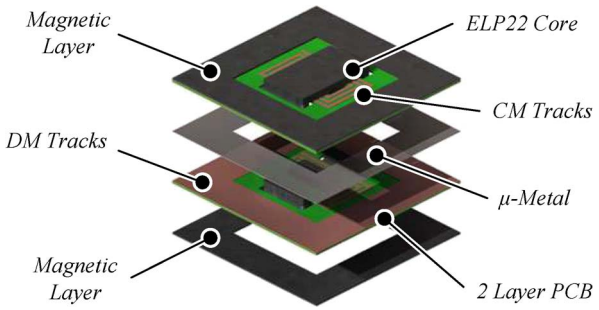


Fig. 19. Exploded/cut view of the integrated EMI filter.

## IX. Conclusion

In this paper, a complete design procedure for a single-phase boost PFC has been undertaken. In order to achieve maximum power density, several aspects have been considered in the design process, such as the number of interleaved boost cells, the switching frequency, the semiconductor material, the number of input filter stages, and also thermal aspects (particularly for the boost inductor design). In this paper, it has been shown that a combined view on all these issues is important to achieve an overall optimized system. The following results have been found:

1) Single CCM operation is comparable to dual DCM operation regarding power density and system efficiency if operated at their optimal switching frequencies and if SiC devices are employed for CCM operation. Due to higher current sensor and semiconductor costs, CCM operation is less preferable for industrial applications.
2) In order to lower the filter requirements, the switching frequency is preferably set below the lower limit of the measurement range of the EMI noise emissions (150 kHz–30 MHz), e.g., 140 kHz for CCM and 70 kHz for DCM operation. However, if power density is the main design criteria, also higher switching frequencies in the range of 200 kHz (particularly for the dual-interleaved DCM operation) can be selected. As a matter of fact, lower system efficiency has to be accepted in this case.
3) Also with single DCM operation (at 140-kHz switching frequency), a comparable power density and efficiency can be achieved. However, a significantly larger capacitor rms current downgrades the converter lifetime, wherefore dual DCM operation appears to be the best choice.
4) A two-stage EMI DM input filter is sufficient and appropriate for the 300-W PFC and leads to minimum filter volume for all operation modes. As for the CM filter, a one-stage filter is sufficient for the setup at hand.
5) A very high power density can be effectively achieved by a thermal connection of the boost inductor(s) to a heat sink by a cooling pin or a cooling tube. In terms of manufacturability, the heat sink connection via cooling pin is preferable.
6) An integration of the EMI input filter in the PCB can further contribute to a further power density decrease; however, for the case at hand, only a filter volume reduction of 15% (which represents a total volume reduction of 7.5%) could be achieved, which may not justify the difficulties in the design and handling and the higher material costs.

The purpose of this paper has been to verify the general guidelines given in [1] for 300-W output power, 230-V mains voltage, and 400-V output voltage. For different power and voltage ratings, the aforementioned conclusions still tend to be correct, and a design could be executed in an analogous manner as done in this paper, whereby the following issues have to be considered.

1) For the boost inductor and the input filter design, the database of available cores and capacitors has to be extended for the considered power range. For the optimization, the parametric volume curves given in [25] can be utilized.
2) For the calculation of the semiconductor losses, appropriate components along with their switching and conduction loss values have to be considered.
3) Since the attenuation requirement for the input filter increases with higher power, a two-stage filter for the DM emissions might not be optimal anymore. However, this can be approximated easily, since twice the input power means about 6-dB higher DM attenuation requirements. With the study in [1], the optimum number of filter stages and component values can then be calculated analogously to the design in this paper.

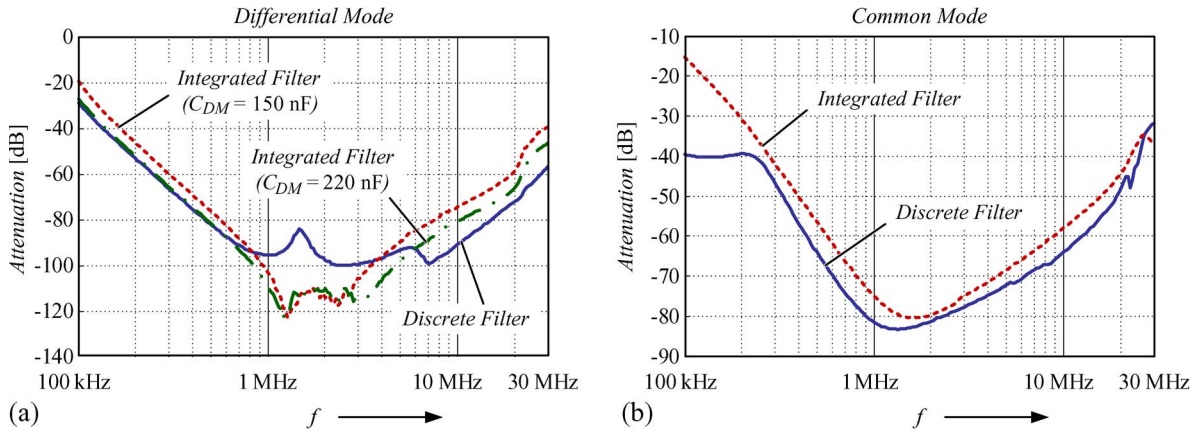


Fig. 20. Measured attenuation of the integrated and the discrete EMI-filter for (a) DM and (b) CM.

For the given specifications, the design has been verified by measurements on an experimental prototype of the PFC operated in dual-interleaved DCM with a switching frequency of 200 kHz. A power density of 5.5 kW/L and a system efficiency of 96.4% have been achieved, which is very close to the predicted values.

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