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A Novel Control Concept for Reliable Operation of a Three-Phase Three-Switch Buck-Type Unity-Power-Factor Rectifier With Integrated Boost Output Stage Under Heavily Unbalanced Mains Condition

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A Novel Control Concept for Reliable Operation of a Three-Phase Three-Switch Buck-Type Unity-Power-Factor Rectifier With Integrated Boost Output Stage Under Heavily Unbalanced Mains Condition

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***Abstract*—In this paper the reliable operation of a three-phase three-switch buck-type pulsewidth-modulation unity-power-factor rectifier with integrated boost output stage under heavily unbalanced mains, i.e., mains voltage unbalance, loss of one phase, short circuit of two phases, or earth fault of one phase is investigated theoretically and experimentally. A brief description of the principle of operation and the most advantageous modulation method are given. The analytical calculation of the relative on-times of the active switching states and of the dc-link current reference value is treated in detail for active and deactivated boost output stage. Based on the theoretical considerations a control scheme which allows for controlling the system for any mains condition without changeover of the control structure is described. Furthermore, digital simulations as well as experimental results are shown which confirm the proposed control concept for different mains failure conditions and for the transition from balanced mains to a failure condition and vice versa. The experimental results are derived from a 5-kW prototype (input voltage range (280. . .480) V_{rms} line-to-line, output voltage 400 V_{DC}) of the rectifier system, where the control is realized by a 32-bit digital signal processor.**

***Index Terms*—Control concept, mains voltage unbalance, power-factor correction, three-phase rectifier, two-phase operation.**

I. Introduction

HIGH-POWER telecommunications power supply modules usually show a two-stage topology, i.e., a front-end three-phase unity-power-factor rectifier and a dc/dc converter output stage. In [1] a three-phase unity-power-factor rectifier formed by integration of a three-switch buck-type input stage and a dc/dc boost converter output stage was presented (cf. Fig. 1), which allows for controlling the output voltage to 400 V_{DC} within a wide input voltage range of (280...480) V_{rms} line-to-line [2]. This results in an advantageous design of the power semiconductors of the rectifier stage and allows the application of a 400-V input dc/dc converter technology being well known from systems with single-phase ac supply.

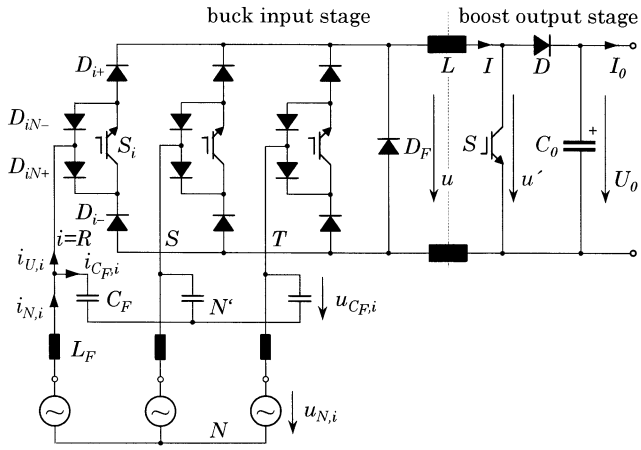

Fig. 1. Power circuit of the three-phase rectifier system with three-switch buck-type input stage and integrated dc/dc boost output stage.

As high reliability is a usual requirement for telecommunications power supplies [3], the pulsewidth-modulation (PWM) rectifier system should also continue in operation in case of a mains failure, i.e., for a transition from a symmetric to a heavily unbalanced mains voltage condition. In [4] the control for a conventional *boost*-type PWM rectifier was treated for unbalanced mains conditions. The operation of a three-phase/three-level PWM *boost*-type (VIENNA) Rectifier in a wide input voltage range and for the loss of a mains phase was investigated in [3]. There a detection of the phase loss is required and a change-over of the control structure has to be performed in case of a phase loss, which could cause problems for some mains failure conditions. In [5] and [6] a control concept for the VIENNA Rectifier is presented and analyzed experimentally which operates for a general unbalance of the mains phase voltage without changeover, i.e., for mains phase voltages showing different amplitudes and/or a deviation from the symmetric 120° phase displacement as well as for a loss of a mains phase, for an earth fault, or for a short circuit between two mains phases.

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In this paper the basic principle of operation and the modulation method which is used to control the rectifier system is described briefly in Section II. Based on this, the theoretical analysis and the practical realization of a control concept which allows for obtaining sinusoidal mains phase currents which are proportional to the mains phase voltages in case of any mains voltage unbalance are discussed in detail for the three-phase *buck*-type PWM rectifier system with integrated boost output stage (cf. Sections III and IV) [7]. The theoretical analysis is verified by digital simulations in Section V; Section VI shows results of an experimental analysis of the proposed control concept for a 5-kW prototype of the PWM rectifier system. There, the transition from balanced mains to a mains failure and vice versa is investigated and the effect of dc-side current limitation is shown. Furthermore, power factor and total harmonic distortion for the investigated mains failure conditions in comparison to an operation under symmetric mains are investigated.

II. Basic Principle of Operation and Modulation Methods

A. Operation Principle

In order to obtain a resistive fundamental mains behavior, mains phase currents $i_{N,i}, i = R,S,T$, and/or fundamentals $i_{U,(1),i}$ of the discontinuous rectifier input phase currents have to be formed, which are proportional to (lying in phase with) the corresponding mains phase voltages $u_{N,i}, i = R,S,T$, i.e., the rectifier system has to emulate a symmetric three-phase star connection of ohmic resistors, where G is the conductivity of one phase

$$i_{N,i} = u_{N,i} \cdot G \approx i_{U,(1),i} = u_{C_F,i} \cdot G \tag{1}$$

(index (1) denotes the fundamental). There, the reactive input filter capacitor current $i_{C_F,i}$ is neglected, i.e., $i_{N,i} \approx i_{U,(1),i}$ is assumed, and the voltage drop across the mains filter inductors L_F is neglected, i.e., $u_{N,i} \approx u_{C_F,i}$[1] (we have $u_{C_F,i} \approx u_{C_F,(1),i}$ for low capacitor voltage ripple, $u_{C_F,i}, i = R,S,T$, is the voltage across the input filter capacitors). For realizing (1) proper on-times of the buck input stage power transistors $S_i, i = R,S,T$, and of the boost output stage power transistor S have to be selected, whereby the buck + boost inductor current i (dc-link current) is distributed sinusoidally to the mains phases. Furthermore, the reference value of the dc-link current has to be set in dependency on the mains voltage condition.

Remark: In this paper, capital letters denote values which are constant over a mains period (e.g., G), the *local* average value (within one pulse period) of a *discontinuous* quantity is denoted by a bar (e.g., $\bar{u}$). Furthermore, for *continuous* quantities instantaneous values are denoted by lower case letters (e.g., u_N) and ripple components with pulse frequency are neglected (e.g., $u_{C_F,i} = u_{C_F,(1),i}$). Reference values which always show a continuous shape are denoted by lowercase letters (e.g., $u^* = \bar{u}^*$).

[1]This is valid only if the mains phase voltages do not contain a zero-sequence system.

For *symmetric* mains, the buck stage modulation index M has been defined in [1] as

$$M = \frac{\hat{I}_N}{I} = \frac{\sqrt{2}}{\sqrt{3}} \cdot \frac{U}{U_{N,\mathrm{ll}}}, \qquad M \in (0;1) \tag{2}$$

where $\hat{I}_N$ is the peak value of the mains phase currents, I is the dc-link current, U is the local average value of the buck stage output voltage, and $U_{N,\mathrm{ll}}$ is the rms value of the mains line-to-line voltages. The dc-link current and, hence, the local average value of the buck stage output voltage, can also show a time-varying behavior within the mains period, e.g., if the buck input stage is continuously operating at its modulation limit (cf. Section III-B). However, a constant dc-link current $(i = \mathrm{const.} = I)$ which corresponds to a constant local average value of the buck stage output voltage $(\bar{u} = \mathrm{const.} = U)$ for symmetric mains is advantageous as it can be set with low control error also by a current control of limited bandwidth (cf. *Remark* in Section III-B).

In a real system, the value of the mains line-to-line voltage is not available, therefore, $U_{N,\mathrm{ll}}$ is calculated from the input filter capacitor voltages $u_{C_F,i}$, which are measured with reference to an artificial neutral point N' (whereby any zero-sequence system is eliminated)

$$U_{N,\mathrm{ll}} = \frac{\sqrt{3}}{\sqrt{2}} \cdot \hat{U}_{N,\mathrm{ph}} \quad \text{with}$$
$$\hat{U}_{N,\mathrm{ph}} = \sqrt{\frac{2}{3}\left(u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2\right)}. \tag{3}$$

In the case of *unsymmetric* mains, the phase voltages $u_{C_F,i}$ are locally interpreted as a symmetric voltage system, whereby definiton (2) for the modulation index can be employed. With this, the maximum local average value $\bar{u}_{\max}$ of the buck stage output voltage can be defined via

$$\bar{u}_{\max} = \frac{\sqrt{3}}{\sqrt{2}} \cdot M_{\max} \cdot \sqrt{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \tag{4}$$

where $M_{\max}$ is the maximum modulation index of the buck input stage. This formal value $\bar{u}_{\max}$ then is used for deciding if the boost ouput stage has to be activated or not: For output voltages $U_0 < \bar{u}_{\max}$ the buck input stage operates at a modulation index $M < M_{\max}$ and the boost output stage is not active, i.e., the duty cycle δ of the boost output stage is $\delta = 0$. For achieving an output voltage $U_0 > \bar{u}_{\max}$ the boost stage has to be activated ($\delta > 0$, cf. Section III-B).

B. Modulation Methods

In the following, the different modulation methods of the buck input stage are summarized and compared in order to find the most advantageous modulation method. Due to the phase symmetry of the converter structure a detailed analysis of the system behavior can be constrained e.g., to the interval of a mains period which is characterized by $u_{C_F,R} > 0 > u_{C_F,S} > u_{C_F,T}$. This interval is denoted as "interval 1" in the following.[2]

[2]If symmetric mains voltages are considered, this interval equals a $\pi/6$-wide interval of the mains period.

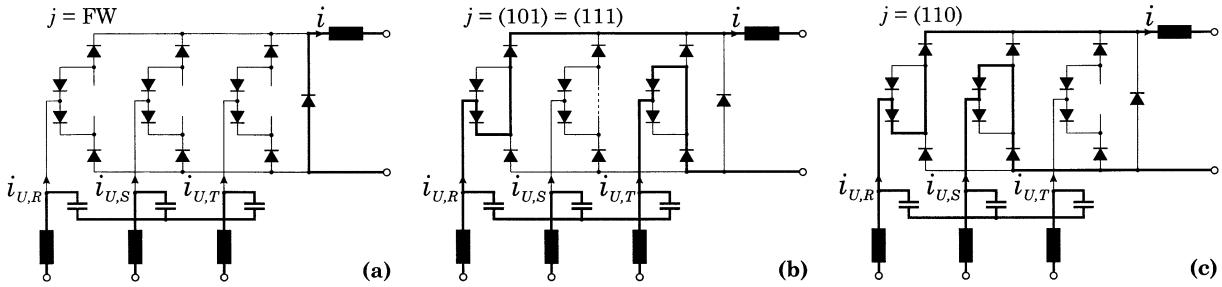

Fig. 2. Conduction states of the buck stage (valid for an input filter capacitor voltage relation $u_{C_F,R} > 0 > u_{C_F,S} > u_{C_F,T}$). The current flow is indicated by a bold line, the power transistors are not explicitly shown for the sake of clarity. (a) Freewheeling state. (b), (c) Active switching states.

TABLE I
DIFFERENT SWITCHING STATE SEQUENCES (MODULATION METHODS) FOR THE BUCK INPUT STAGE WITHIN ONE PULSE PERIOD. t_μ DENOTES THE LOCAL TIME BEING COUNTED WITHIN THE PULSE PERIOD T_P, i.e., $t_\mu \in (0; T_P)$

Modulation method (1):	$\|_{t_\mu=0}\,(101)\,(110)\,(\mathbf{000})\,\|_{t_\mu=T_P/2}\,(\mathbf{000})\,(110)\,(101)\,\|_{t_\mu=T_P}$
Modulation method (2):	$\|_{t_\mu=0}\,(101)\,(\mathbf{000})\,(110)\,\|_{t_\mu=T_P/2}\,(110)\,(\mathbf{000})\,(101)\,\|_{t_\mu=T_P}$
Modulation method (3):	$\|_{t_\mu=0}\,(101)\,(110)\,(\mathbf{000})\,\|_{t_\mu=T_P/2}\,(101)\,(110)\,(\mathbf{000})\,\|_{t_\mu=T_P}$

Within interval 1, there are two active switching states of the buck input stage, where current is drawn from the mains and/or the dc-link current i is distributed to the rectifier input phases. The active switching states $j = (101)$ and $j = (110)$[3] are showing relative on-times $\delta_{(101)}$ and $\delta_{(110)}$ related to one pulse half period. During the freewheeling state (relative on-time $\delta_{\mathrm{FW}} = 1 - \delta_{(101)} - \delta_{(110)}$) the dc-link current freewheels via the diode D_F. In Fig. 2 the conduction states of the buck stage are given for the considered mains interval.

There are several possibilities for arranging the system switching states within one pulse period: The active switching states can either be arranged symmetrically (cf. (1) and (2) in Table I) or asymmetrically (cf. (3) in Table I) with reference to the middle of the pulse period, and the freewheeling state can be placed in the middle, cf. sequence (2), or at the beginning and/or at the end of a pulse half period, respectively, cf. sequence (1). The different modulation methods are given in Table I for interval 1 and, for the sake of clarity, the freewheeling state is shown in bold face.

If the switching power losses are assumed to be proportional to the switched dc-link current i and to the switched voltage, the modulation methods given in Table I show a ratio of the average values of switching power losses within one mains period of $P_{(1)} : P_{(2)} : P_{(3)} = 1 : \sqrt{3} : 2$ for a given pulse frequency f_P. Accordingly, for equal switching losses pulse frequencies showing a ratio

$$f_{P,(1)} : f_{P,(2)} : f_{P,(3)} = 1 : 1/\sqrt{3} : 1/2 \qquad (5)$$

have to be selected [1]. If the modulation methods are compared based on (5) concerning the global rms value of the input filter capacitor voltage ripple [8] as well as the global rms value of the dc current ripple [9] one can see, that modulation method (1) is advantageous over the other two modulation methods. Furthermore, it is possible to clamp one power transistor in the on-state for a $\pi/3$-wide mains interval (considering symmetric mains conditions). There it is advantageous to clamp the switch of the phase showing the minimum absolute voltage (i.e., lying in between the other two phases), resulting in a reduced voltage stress on the power transistor and the bridge leg power diodes as compared to clamping the power transistor of the phase showing the most positive or most negative phase voltage. This furthermore allows to adapt the modulation method easily for balancing the dc-side current of two rectifier systems connected in parallel by simply placing an additional freewheeling state (where another switch is in the on-state) in the middle of the pulse periode [10]. For the most advantageous modulation method there follows for interval 1:

$$\|_{t_\mu=0}(111)(110)(010)\|_{t_\mu=T_P/2}(010)(110)(111)\|_{t_\mu=T_P} \qquad (6)$$

where t_μ denotes the local time being counted within the pulse period T_P.

Concerning the switching actions of the boost output stage it is advantageous to place the on-time interval of the boost power transistor in the middle of a pulse period, i.e., during the freewheeling state of the buck input stage. This results in minimum voltage stress on the dc-link inductor and hence minimum rms value of the dc-link current ripple [9].

III. THEORETICAL ANALYSIS FOR THE CONTROL ALGORITHM

A. Calculation of On-Times and DC-Link Current Reference Value

In the following, the calculation of the relative on-times of the switching states of the buck-type input stage and of the dc-link current reference value is given. For the switching states the following rectifier input current conditions are obtained considering interval 1

$$\begin{aligned} j = \mathrm{FW} &: i_{U,R} = 0 \quad i_{U,S} = 0 \quad i_{U,T} = 0 \\ j = (101) &: i_{U,R} = +i \quad i_{U,S} = 0 \quad i_{U,T} = -i \\ j = (110) &: i_{U,R} = +i \quad i_{U,S} = -i \quad i_{U,T} = 0. \end{aligned} \qquad (7)$$

[3] $j = (s_R s_S s_T)$, where $s_i, i = R, S, T$, are the switching functions of the power transistors. $s_i = 0$ denotes the off-state and $s_i = 1$ denotes the on-state of power transistor S_i.

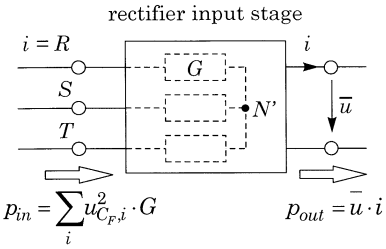

Fig. 3. Equivalent circuit of the input stage of the three-phase rectifier system showing the balance of input and output power.

Therefore, the rectifier input currents $i_{U,i}$ within one pulse half period can be given as follows:

$$\begin{aligned} \bar{i}_{U,R} &= (\delta_{(101)} + \delta_{(110)}) \cdot i \\ \bar{i}_{U,S} &= -\delta_{(110)} \cdot i \\ \bar{i}_{U,T} &= -\delta_{(101)} \cdot i \end{aligned} \tag{8}$$

where $\delta_{(101)}$ and $\delta_{(110)}$ denote the relative on-times of the active switching states $j = (101)$ and $j = (110)$. The local average value of the buck stage output voltage can be calculated from the average value of the volt-seconds being switched to the buck stage output terminals

$$\bar{u} = \delta_{(101)}(u_{C_F,R} - u_{C_F,T}) + \delta_{(110)}(u_{C_F,R} - u_{C_F,S}). \tag{9}$$

With the balance of input power p_{in} and output power p_{out} (i.e., losses of the buck input stage are neglected, cf. Fig. 3)

$$p_{\text{in}} = \sum_i i_{N,i}^2 \cdot \frac{1}{G} = \sum_i u_{C_F,i}^2 \cdot G = \bar{u} \cdot i = p_{\text{out}} \tag{10}$$

one receives with (8) for the ratio of buck stage output voltage and the dc-link current

$$\frac{\bar{u}}{i} = \frac{2}{G} \cdot \left(\delta_{(101)}^2 + \delta_{(101)}\delta_{(110)} + \delta_{(110)}^2 \right). \tag{11}$$

The relations (1), (8), and (11) can be combined in a system of equations

$$\bar{u} = \frac{2}{G} \cdot \left(\delta_{(101)}^2 + \delta_{(101)}\delta_{(110)} + \delta_{(110)}^2 \right) \cdot i \tag{12}$$

$$\bar{i}_{U,R} = u_{C_F,R} \cdot G = \left(\delta_{(101)} + \delta_{(110)} \right) \cdot i \tag{13}$$

$$\bar{i}_{U,T} = u_{C_F,T} \cdot G = -\delta_{(101)} \cdot i \tag{14}$$

where the input filter capacitor voltages $u_{C_F,i}$ are measured with reference to the artificial neutral point N', the buck stage output voltage is set by the dc-link current controller, and the input conductivity is set by the output voltage controller (cf. Section IV), while $\delta_{(101)}$, $\delta_{(110)}$, and i are unknown parameters.

B. Control Reference Values

Based on the system of (12)–(14), the calculation of the reference values which are needed for the control algorithm can be carried out. By solving the system of equations one receives for the relative on-times of the active switching states of the buck input stage and for the dc-link current reference value i^* within interval 1

$$\delta_{(101)} = -\frac{u^*}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,T} \tag{15}$$

$$\delta_{(110)} = -\frac{u^*}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,S} \tag{16}$$

$$i^* = \frac{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}{u_0} \cdot G^*. \tag{17}$$

There, i^* is calculated employing the output voltage u_0. For the calculation of the relative on-times of the active switching states the buck stage output voltage reference value u^* is used, which is due to the proposed control structure (cf. Section IV). The reference value of the input conductivity G^* is calculated based on (10)

$$G^* = \frac{P_{\text{lim}}^*}{\sum_i U_{C_F,i}^2} \tag{18}$$

with the limited reference value P_{lim}^* of the output power and with the sum of the squares of the input filter capacitor voltage amplitudes

$$\sum_i U_{C_F,i}^2 = \frac{1}{2}\left(\hat{U}_{C_F,R}^2 + \hat{U}_{C_F,S}^2 + \hat{U}_{C_F,T}^2 \right). \tag{19}$$

One has to note that the conductivity reference value G^* is essentially constant over one mains period, however, the dc-link current reference value i^* shows a time-dependent behavior within one mains period for unbalanced mains conditions.

One has to differ between two cases, which are treated in the following sections.

- The buck input stage is below its modulation limit, i.e., the voltage reference value u^* can be set by the buck stage ($u^* \leq \bar{u}_{\max}$ and/or $M \leq M_{\max}$). In this case, the boost output stage is not active, i.e., $\delta = 0$.
- The buck input stage is operating at its modulation limit ($M = M_{\max}$), i.e., the buck stage output voltage is limited to $\bar{u}_{\max}$. Therefore, for the calculation of the relative on-times and of the dc-link current reference value u^* has to be limited to $\bar{u}_{\max}$. Accordingly, for achieving an output voltage reference value $U_0^* > \bar{u}_{\max}$ the boost output stage has to be activated, i.e., $\delta > 0$.

1) Deactivated Boost Converter: Since the buck input stage is below its modulation limit ($M \leq M_{\max}$ and/or $u^* \leq \bar{u}_{\max}$), (15)–(17) are incorporated into the calculation of the relative on-times of the active switching states and of the dc-link current reference value.

2) Active Boost Converter: If the buck input stage is operating at its modulation limit ($u^* > u_{\max}$), we have two possibilities for controlling the buck stage.

1) The modulation index is limited to a *constant* value, e.g., $M = 1$, within the mains period. For symmetric mains, this results in a constant buck stage output voltage and a constant dc-link current.
2) The modulation index is kept on its *maximum* possible value, i.e., it varies in between $M = 1$ and $M = 2/\sqrt{3}$ over a mains period, which results in a time-varying local

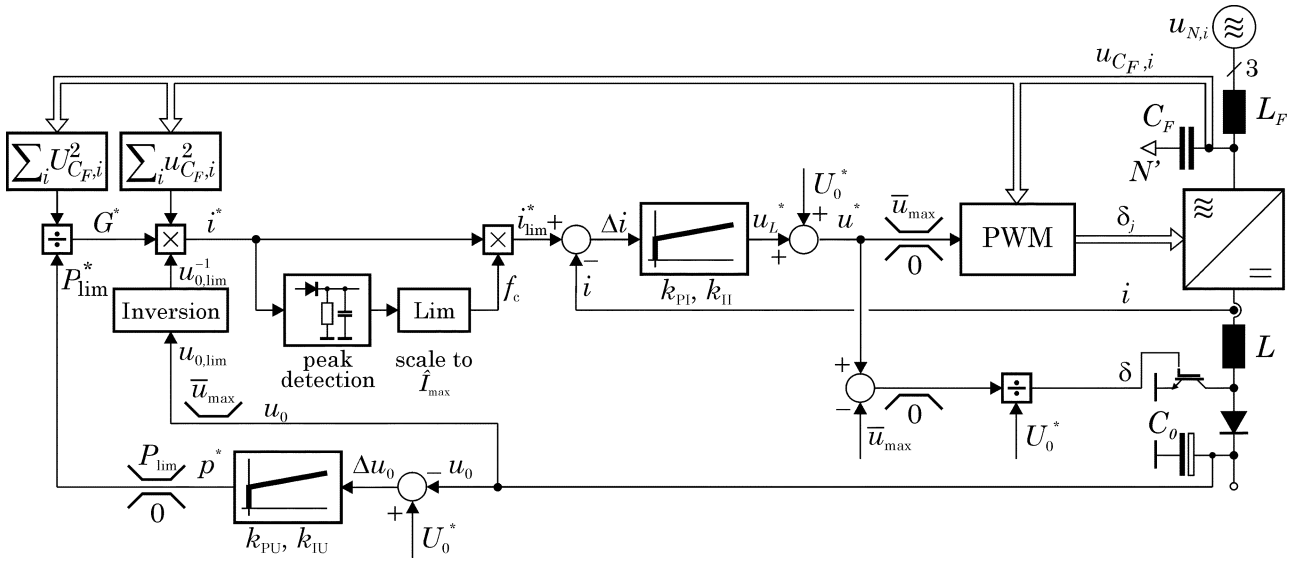

Fig. 4. Control structure guaranteeing unity-power-factor operation under heavily unbalanced mains.

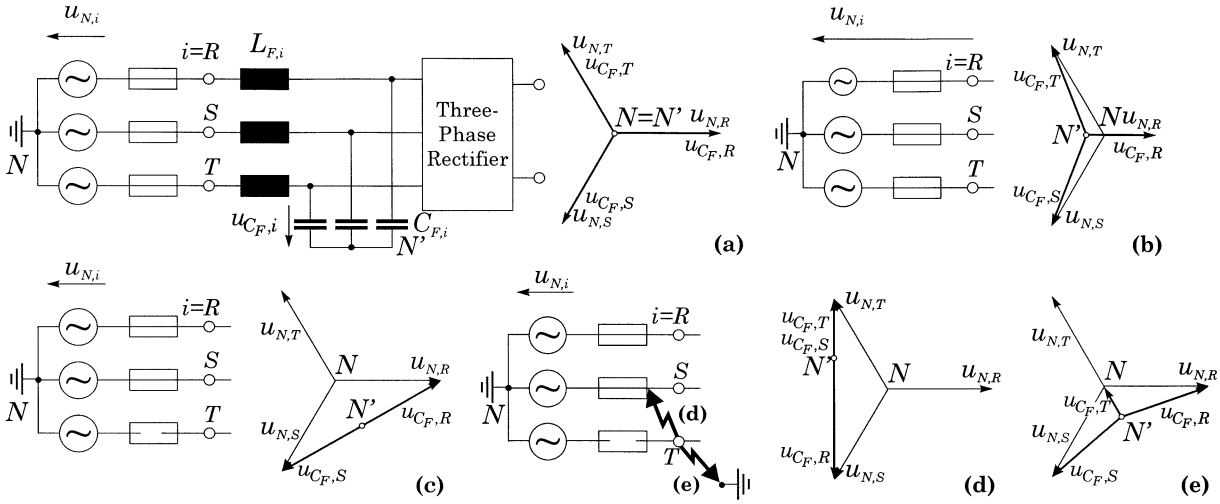

Fig. 5. Mains phase conditions and corresponding phasor diagrams of mains phase voltages $u_{N,i}$ and input filter capacitor voltages $u_{C_F,i}$. (a) Symmetric mains condition. (b) Mains phase voltage unbalance: $u_{N,R}$ is 50% smaller than for symmetric conditions. (c)–(e): Two-phase operation. (c) Loss of phase T. (d) Short circuit between phases S and T. (e) Earth fault in phase T.

average value of the buck stage output voltage and of the dc-link current also for symmetric mains.

In the following, the relative on-times of the switching states of the buck input stage and of the dc-link current reference value are calculated for both cases.

a) Constant Modulation Index Limit: The calculation of the relative on-times $\delta_{(101)}$ and $\delta_{(110)}$ and of the dc-link current reference value i^* is equal to the calculation for deactivated boost converter, cf. (15)–(17), where the buck stage output voltage reference value u^* is limited to $\bar{u}_{\max}$, cf. (4)

$$\delta_{(101)} = -\frac{\bar{u}_{\max}}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,T} \tag{20}$$

$$\delta_{(110)} = -\frac{\bar{u}_{\max}}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,S} \tag{21}$$

$$i^* = \frac{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}{\bar{u}_{\max}} \cdot G^*. \tag{22}$$

The modulation index limit can be set to, e.g., $M_{\max} = 1$, however, in case active damping of the input filter is provided [11], the modulation index limit has to be decreased to, e.g., $M_{\max} = 0.9$ in order to have a margin for control.

b) Maximum Modulation Index Limit: In this case the relative on-time of the freewheeling state is set to zero, i.e., $\delta_{(101)} + \delta_{(110)} = 1$. There, one receives for the relative on-times of the buck input stage and for the dc-link current reference value within interval 1

$$\delta_{(101)} = -\frac{u_{C_F,T}}{u_{C_F,R}} \tag{23}$$

$$\delta_{(110)} = -\frac{u_{C_F,S}}{u_{C_F,R}} \tag{24}$$

$$i^* = \max\{|u_{C_F,i}|\} \cdot G^*. \tag{25}$$

Remark: For symmetric mains and a constant modulation index limit, the current reference value i^* and, hence, the local average value of the buck stage output voltage $\bar{u}$ show constant

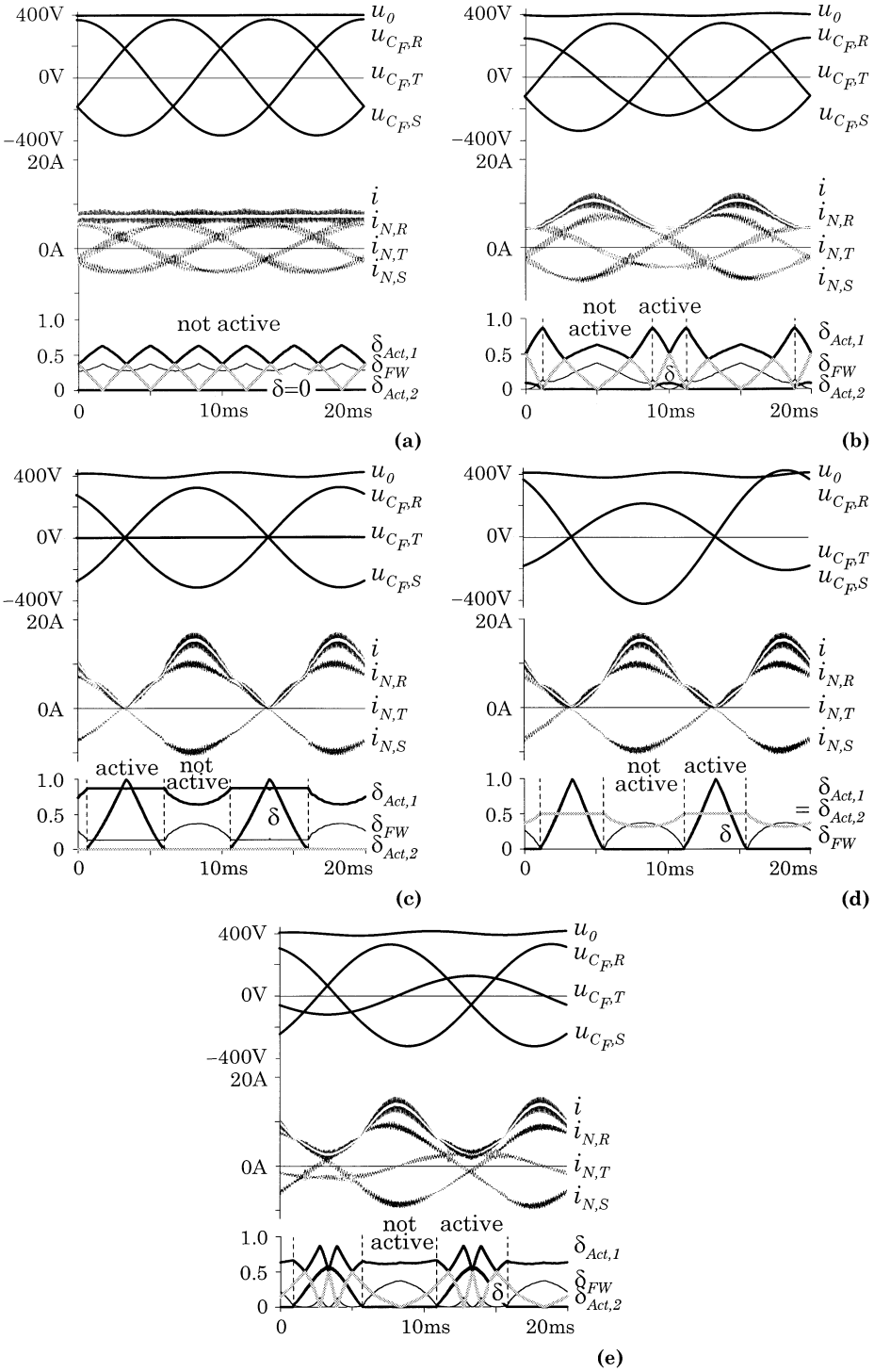

Fig. 6. Digital simulation results for different mains phase conditions (cf. Fig. 5). (a) Balanced mains phase voltages. (b) Unbalanced mains. (c) Loss of phase T. (d) Short circuit between phases T and S. (e) Earth fault of phase T. Time behavior of input filter capacitor voltages $u_{C_F,i}$ and system output voltage u_0 (top), of mains phase currents $i_{N,i}$, dc-link current i and its average value I (depicted in white) (middle) and relative on-times of the two active switching states δ_{Act1} (black), δ_{Act2} (gray), and of the freewheeling state δ_{FW} of the buck input stage and of the relative on-time of the boost transistor δ (bottom). "Active" and "not active" refer to the boost output stage.

values. A constant i^* is advantageous concerning the required bandwidth of the current control and is, therefore, further investigated in this paper. However, operating at the maximum modulation index limit shows advantages concerning the switching losses due to the fact that the freewheeling state is kept to zero. A detailed comparison of both modulation strategies will be the topic of a future paper.

IV. Control Structure

In Fig. 4 the proposed control structure which allows a reliable operation with sinusoidal mains phase currents and unity power factor under any mains unbalance condition is given. The control circuit consists of an outer output voltage control loop and an inner dc-link current control loop. The relative on-times

δ_j and δ of the active switching states of the buck input stage and the boost output stage are derived as given in the following.

- The input filter capacitor voltages are measured against an artificial neutral point N' whereby a zero-sequence system which could occur in case of a mains failure is eliminated.
- The output voltage controller output is interpreted as output power demand p^* according to (10). In order to suppress low-frequency harmonics as occurring in case of a mains failure the controller design is for low unity gain open-loop bandwidth (typically 5 Hz), the output power reference value is limited to the rated power $P_{\lim}$ of the rectifier system.
- The input conductivity reference value G^* is calculated according to (18).
- The dc-link current reference value i^* is calculated employing

$$i^* = \begin{cases} \dfrac{u_{C_F,R}^2+u_{C_F,S}^2+u_{C_F,T}^2}{u_0} \cdot G^*, & \text{for } u_0 \le \bar{u}_{\max} \\ \dfrac{u_{C_F,R}^2+u_{C_F,S}^2+u_{C_F,T}^2}{\bar{u}_{\max}} \cdot G^*, & \text{for } u_0 > \bar{u}_{\max}. \end{cases} \tag{26}$$

- In order to ensure that the current stresses on the power diodes and transistors do not exceed a maximum admissible level and in order to avoid saturation or overheating of the dc-link inductor, the peak value of the dc-link current reference value $\hat{i}^*$ is limited to a maximum value $\hat{I}_{\max}$, which is defined by the dimensioning of the rectifier system (25 A in this case). In case $\hat{i}^*$ exceeds the limit, the reference value i^* is downscaled by a correcting factor f_c

$$f_c = \begin{cases} 1, & \text{for } \hat{i}^* \le \hat{I}_{\max} \\ \hat{I}_{\max}/\hat{i}^*, & \text{for } \hat{i}^* > \hat{I}_{\max}. \end{cases} \tag{27}$$

- The output of the dc-link current controller sets the reference value of the voltage across the dc-link inductor u_L^* which is pre-controlled with the output voltage reference value U_0^* resulting in the buck stage output voltage reference value u^*.
- The relative on-times of the switching states of the buck input stage are then calculated employing (15) and (16) for deactivated boost stage as well as for active boost stage (and a constant modulation index limit), where the buck stage output voltage reference value u^* is limited to $\bar{u}_{\max}$.
- Beyond the modulation limit of the buck input stage, i.e., for $u^* > \bar{u}_{\max}$, the reference value of the voltage across the dc-link inductor can not be generated by the buck stage any longer. Therefore, the boost stage power transistor has to be activated in order to decrease the right hand side potential of the dc-link inductor, i.e., for achieving $\bar{u}' < u_0$, where $\bar{u}'$ is the local average value of the voltage across the boost power transistor. For the boost output stage

$$\bar{u}' = (1-\delta)\, u_0 \tag{28}$$

TABLE II
AVERAGE AND RMS VALUES OF THE POWER SEMICONDUCTOR CURRENTS (FOR $U_{N,\mathrm{ll}} = 208$ V LINE-TO-LINE VOLTAGE AND $P_0 = 6$ kW OUTPUT POWER), MAXIMUM BLOCKING VOLTAGES $V_{\max}$ (FOR $U_{N,\mathrm{ll}} = 480$ V LINE-TO-LINE VOLTAGE AND $U_0 = 400$ V OUTPUT VOLTAGE); TYPE OF SELECTED POWER SEMICONDUCTORS [14], [15], AND CORRESPONDING BLOCKING CAPABILITY V_{RRM} AND CONTINUOUS FORWARD CURRENT RATING I_F

	I_{avg}	I_{rms}	$V_{\max}$	Type	V_{RRM}	I_F
S_i	15.0 A	18.8 A	680 V	IRG4PF50W	900 V	28 A
$D_{i(N)\pm}$	7.5 A	13.3 A	680 V	RURG30100	1000 V	30 A
D_F	1.1 A	5.0 A	680 V	RURG30100	1000 V	30 A
S	8.4 A	14.1 A	400 V	IRG4PC40W	600 V	30 A
D	15.0 A	18.8 A	400 V	RURG3060	600 V	30 A

is valid for continuous conduction mode (CCM). For the voltage across the inductor we have in general

$$u_L^* = \bar{u}_{\max} - \bar{u}'. \tag{29}$$

With this one receives for the relative on-time of the boost power transistor

$$\delta = 1 - \frac{\bar{u}_{\max} - u_L^*}{U_0^*}. \tag{30}$$

For the calculation of $\delta u_0 = U_0^*$ is assumed due to the provided output voltage control. The calculation is realized in the control structure (cf. Fig. 4) by

$$\delta = \frac{u^* - \bar{u}_{\max}}{U_0^*} \tag{31}$$

where $u^* = u_L^* + U_0^*$. By a limitation of the numerator to a lower value of zero, $\delta = 0$ is realized if the operation of the boost stage is not necessary (deactivated boost stage).

Remark: All equations given are valid within the whole mains period, except the equations for calculating the relative on-times, which are only valid for an input filter capacitor voltage condition $u_{C_F,R} > 0 > u_{C_F,S} > u_{C_F,T}$. Equations for other relations of the mains phase voltage instantaneous values could be derived based on [1].

V. SIMULATION RESULTS

In this section results of digital simulation [12] are given which verify the operation behavior of the proposed control structure for different mains conditions (symmetric mains, unbalanced mains, phase loss, short circuit of two phases and earth fault), cf. Fig. 5. There, the rectifier system and the corresponding phasor diagrams of the mains phase voltages $u_{N,i}$ and of the input filter capacitor voltages $u_{C_F,i}$ are shown. The simulations are carried out for a constant modulation index limit $M_{\max} = 1$ for the following system parameters:

$$\begin{array}{lll} U_{N,\mathrm{ll}} = 480\ \mathrm{V} & U_0^* = 400\mathrm{V} & R_0 = 55\ \Omega \\ f_N = 50\ \mathrm{Hz} & f_P = 20\ \mathrm{kHz} & L_F = 200\ \mu\mathrm{H} \\ L = 2 \times 1\ \mathrm{mH} & C_F = 4\ \mu\mathrm{F} & C_0 = 750\ \mu\mathrm{F} \end{array}$$

(f_N denotes the line frequency and f_P the pulse frequency).

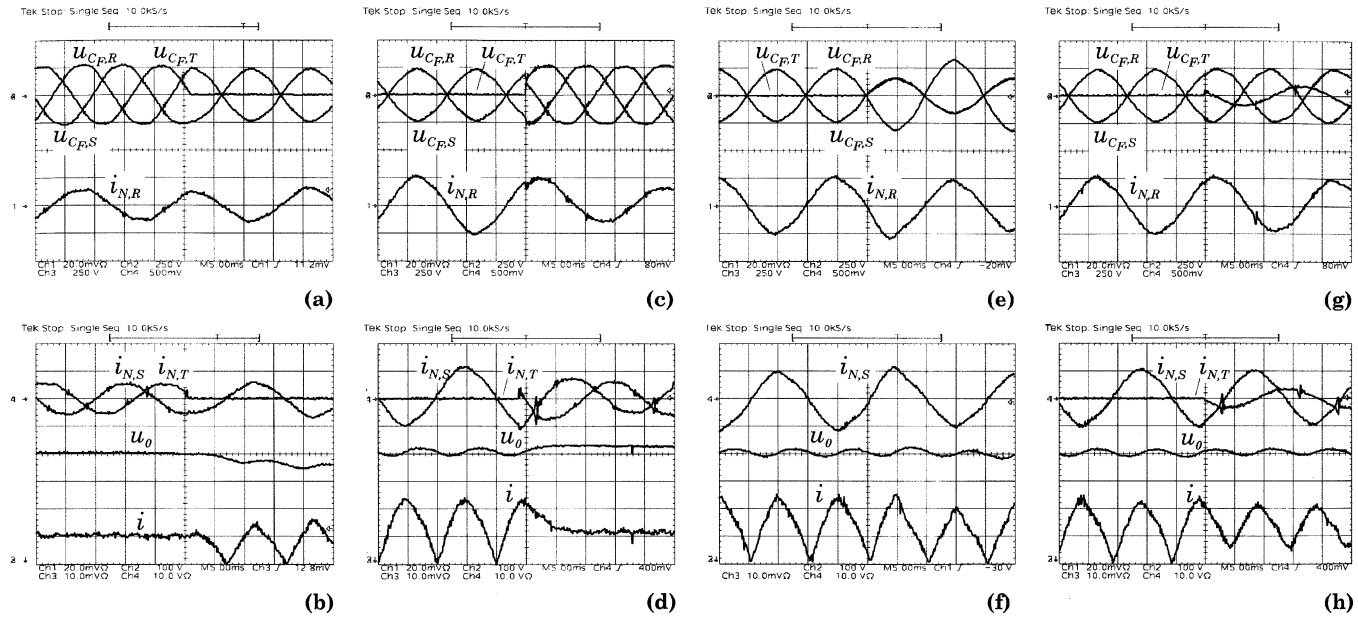

Fig. 7. Experimental results for different mains conditions. (a), (b) Loss of phase T. (c), (d) Reconnection of phase T (return to symmetric mains). (e), (f) Short circuit between phases S and T during loss of phase T. (g), (h) Short circuit to mains neutral during loss of phase T. Operating parameters: 330 $V_{\rm rms}$ line–line input voltage, 400-V output voltages, and 2.2-kW output power. (a), (c), (e), (g) Time behavior of input filter capacitor voltages $u_{C_F,i}$, and mains phase current $i_{N,R}$. (b), (d), (f), (h) Time behavior of mains phase currents $i_{N,S}, i_{N,T}$, output voltage u_0, and dc-link current i. Voltage scales: $u_{C_F,i}$, 250 V/div; u_0, 100 V/div; current scales: $i_{N,i}$: 10 A/div; i: 5 A/div; time scale: 5 ms/div.

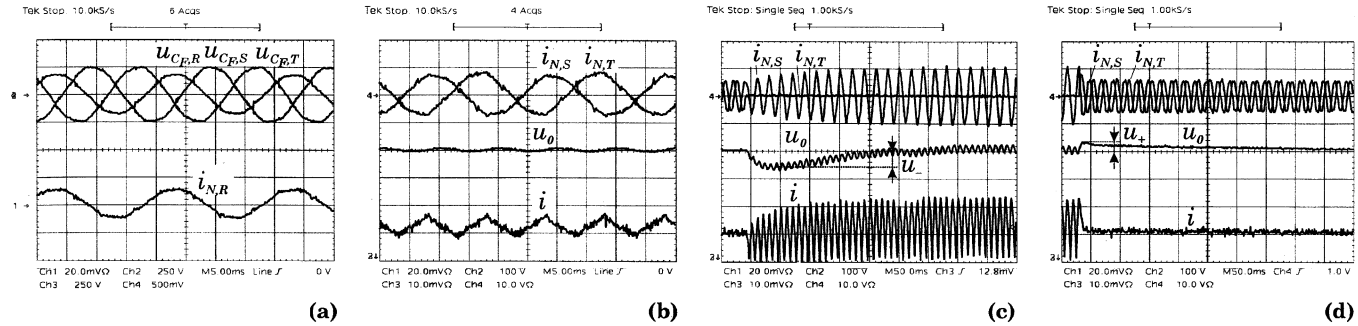

Fig. 8. Experimental results for a mains phase voltage unbalance, where mains phase voltage $u_{N,R}$ is 50% smaller than for symmetric conditions. (a) Time behavior of input filter capacitor voltages $u_{C_F,i}$, and mains phase current $i_{N,R}$. (b) Mains phase currents $i_{N,S}, i_{N,T}$, output voltage u_0, and dc-link current i. (c) Time behavior of the output voltage for the disconnection and (d) for the reconnection of mains phase T. Operating parameters, voltage, and current scales as in Fig. 7: time scale: (a), (b) 5 ms/div; (c), (d): 50 ms/div.

A. Symmetric Mains

For balanced mains [cf. Fig. 5(a)] we have equal amplitudes of the phase voltages (referred to the neutral point N) and of the input filter capacitor voltages (referred to the artificial neutral point N') and a phase displacement of the phase quantities of 120° electrical, cf. Fig. 6(a). The mains phase currents $i_{N,i}$ are sinusoidal and in phase with the mains phase voltages, and the average value of the dc-link current shows a constant value. The boost stage is not active, and the relative on-times of active and freewheeling states show a similar time behavior in each interval of the mains period.

B. Unbalanced Mains

The behavior of the rectifier system in case one phase voltage shows a lower amplitude is depicted in Fig. 6(b). There, the amplitude of voltage $u_{N,R}$ is assumed to be 50% lower than for symmetric conditions. The resulting input filter capacitor voltages are given, the corresponding mains phase currents are sinusoidal and proportional to the input filter capacitor voltages,

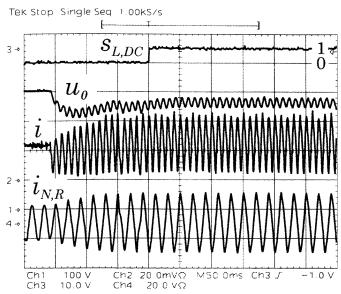

Fig. 9. DC-side current limitation to 22 A peak during loss of phase T, signal indicating limitation $s_{L,\rm DC}$. Operating parameters: load, 73 Ω; line-to-line voltage 208 $V_{\rm rms}$. Voltage scale: u_0: 100 V/div; current scales: i: 10 A/div, $i_{N,R}$: 20 A/div; time scale: 50 ms/div.

i.e., the rectifier system shows a purely ohmic behavior. The dc-link current is proportional to the sum of the squares of the input filter capacitor voltages, cf. (26). Due to the time-varying dc-link current and the relatively low capacitance of the output capacitor, the system output voltage is not constant but varies

by $\pm 1.7\%$ of its global average value, where the actual variation is depending on the amount of unbalance. Furthermore, the different operating intervals are shown where the boost transistor is active ($\delta > 0$), and where the boost stage is deactivated ($\delta = 0$). According to the constant modulation index limit ($M_{\max} = 1$) there is a freewheeling state ($\delta_{\rm FW} \geq 0$) in both operating intervals.

C. Loss of One Phase

If one mains phase is missing, e.g., after tripping of a fuse in phase T, cf. Fig. 5(c), the remaining mains phase currents $i_{N,R}$ and $i_{N,S}$ are proportional to the input filter capacitor voltages $u_{C_F,R}$ and $u_{C_F,S}$. Due to the fact that the dc-link current becomes zero each half mains period, the output voltage does show a higher ripple ($\pm 4.4\%$) as compared to Section V-B [cf. Fig. 6(c)]. During the time interval where the boost stage is active, the relative on-times of the buck stage switching states are constant, the current is modulated by the boost output stage.

D. Short Circuit Between Two Phases

If phase T [cf. Fig. 5(d)] is connected to another phase (phase S) as caused by an input voltage short circuit (after tripping of a fuse in phase T) only one line-to-line voltage is available for delivering the output power. In this case the rectifier input phases S and T are operating in parallel and/or have equal input voltages. Therefore, the relative on-times of the active switching states $\delta_{\rm Act1}$ and $\delta_{\rm Act2}$ are equal. The mains phase currents are proportional to the corresponding mains phase voltages, the output voltage ripple is the same as for the loss of one phase ($\pm 4.4\%$), cf. Fig. 6(d).

E. Earth Fault

If phase T [cf. Fig. 5(e)] is connected to the neutral as could be caused by an earth fault (after tripping the fuse in phase T) there is also only one line-to-line voltage available for delivering the output power. Under this mains phase condition, the mains phase currents are again proportional to the corresponding input voltages $u_{C_F,i}$ [cf. Fig. 6(e)]. The deviation of the output voltage to its average value within one mains period is approximately $\pm 4.0\%$.

VI. Experimental Results

The experimental results are carried out on a prototype of the three-phase rectifier system which has been designed for the following specifications:

$U_{N,\rm ll} = (208 \ldots 480)$ V	$U_0^* = 400$ V	$P_0 = 5$ kW
$f_N = 50$ Hz	$f_P = 23.4$ kHz	$L_F = 130\ \mu$H
$C_F = 4\ \mu$F	$L = 2 \times 0.9$ mH	$C_0 = 750\ \mu$F

the inductance values L_F and L (iron powder cores) are both given for $i_N = 15\ {\rm A_{rms}}$ and/or $i = 15\ {\rm A_{rms}}$, while $L_F = 270\ \mu$H and $L = 3$ mH is valid for $i_N = 0\ {\rm A_{rms}}$ and/or $i = 0\ {\rm A_{rms}}$. The dimensions of the rectifier system are $(16 \times 34 \times 11)$ cm^3 ($(6.30 \times 13.4 \times 4.33)$ in^3), the complete control is implemented in a 32-bit floating-point digital signal processor ADSP-21061 SHARC (Analog Devices). The dimensioning of the power semiconductors is carried out with a safety margin of 20%, i.e., for $P_0 = 6$ kW output power, where the maximum current stress occurs for minimum input voltage, i.e., for $U_{N,\rm ll} = 208$ V. The average and rms values of the buck input stage and the boost output stage power semiconductor currents, the maximum blocking voltages as well as the selected components (all in TO 247 package) are given in Table II.

A. Behavior for Different Mains Phase Conditions

In Fig. 7 experimental results which confirm the proposed control method are given. The operating behavior for the disconnection [cf. Fig. 7(a) and (b)] and for the reconnection [cf. Fig. 7(c) and (d)] of one mains phase (phase T) as well as for the transition from the loss of phase T to a short circuit of mains phases T and S [cf. Fig. 7(e) and (f)] and to a short circuit to the mains neutral [i.e., earth fault, cf. Fig. 7(g) and (h)] are given. The time behavior of input and output quantities for a mains voltage unbalance [cf. Fig. 5(b)] is given in Fig. 8, where mains phase voltage $u_{N,R}$ is assumed to be 50% lower than for balanced mains. In Figs. 7 and 8 the input filter capacitor voltages $u_{C_F,i}$, the mains phase currents $i_{N,i}$, as well as the output voltage u_0 and the dc-link current i are given. The mains phase currents are proportional to the input filter capacitor voltages at any time, i.e., the rectifier system emulates a three-phase ohmic resistor. The deviation of the voltage from a purely sinusoidal shape is not caused by the rectifier system but is also present for no load operation. This distortion is caused by office machines and computers and/or single phase rectifiers with capacitive smoothing which are connected in high numbers to the supplying mains at the University of Technology Vienna, Vienna, Austria.

Regarding Fig. 8(c) and (d) one can see that no overvoltages and/or overcurrents or oscillations do occur at the transition from one mains condition to another. There is only a voltage dip or surge in the output voltage in case of disconnection [cf. Fig. 8(c)] or reconnection [cf. Fig. 8(d)] of one mains phase. In case of a phase loss the output voltage dip u_- is approximately 60 V, for the reconnection a voltage surge u_+ of 20 V does occur for 330-V line-to-line voltage and 2.2-kW output power.

B. DC-Side Current Limitation

In case of a phase loss or short circuit of two phases only one line-to-line voltage is available for delivering the output power, i.e., we have a two-phase operation and a limited output power $P_{\max,2\sim} = P_{\max,3\sim}/\sqrt{3} = 2.9$ kW.[4] The limitation to this maximum admissible value is due to the dc-link current limitation [cf. Fig. 4 and (27)]. The maximum admissible dc-link current value is set to 25 A. Therefore, the limitation concerning the average value is actually 22 A due to the superimposed current ripple. In Fig. 9 the time behavior of mains phase current $i_{N,R}$, dc-link current i, and output voltage u_0 are given in case of a loss of phase T. The binary signal $s_{L,\rm DC}$ indicates dc-link current limitation, $s_{L,\rm DC} = 0 \rightarrow 1$. One can see that the dc-link current limitation results in an output voltage limitation and, hence, in an output power limitation.

[4]Three-phase operation: $P_{\max,3\sim} = \sqrt{3}\, U_{N,\rm ll}\, I_N$. Two-phase operation: $P_{\max,2\sim} = 2\, U_{N,2\sim} I_N = 2\, U_{N,\rm ll}/2\, I_N = U_{N,\rm ll}\, I_N$ [the phase voltage $U_{N,2\sim}$ during two-phase operation equals half the line-to-line voltage $U_{N,\rm ll}$, cf. Fig. 5(c)].

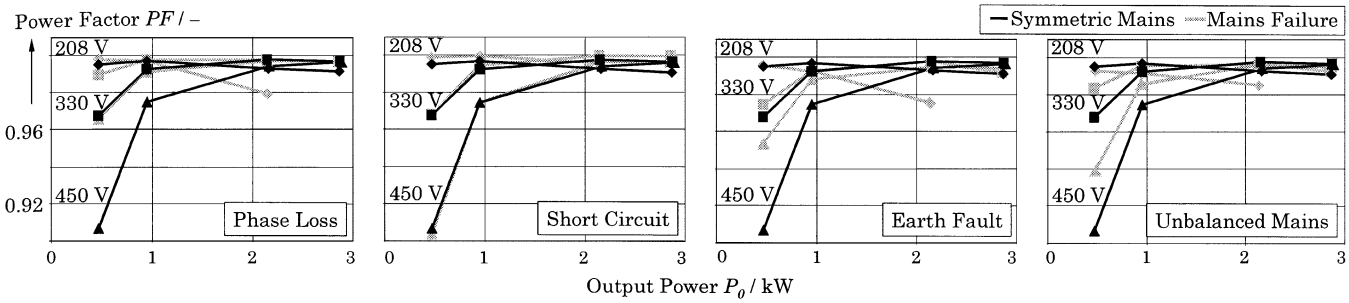

Fig. 10. PF of the rectifier system for symmetric mains and mains failures and different line-to-line rms voltages $U_{N,\mathrm{ll}}$ in dependency on the output power P_0.

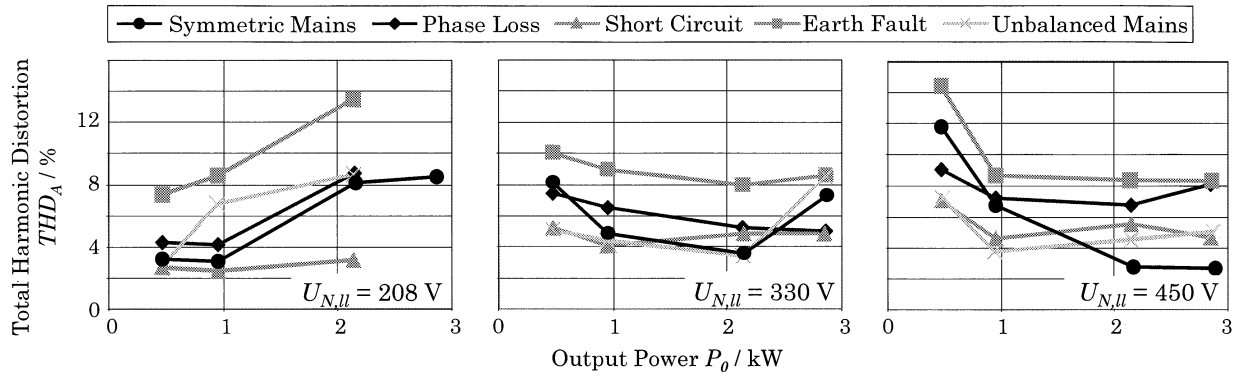

Fig. 11. Total harmonic distortion THD_A of the mains phase currents for symmetric mains and mains failures and different line-to-line rms voltages $U_{N,\mathrm{ll}}$ in dependency on the output power P_0.

C. System Characteristics

In this section quantities which do characterize the system behavior, i.e., power factor PF and total harmonic distortion THD_A of the mains phase currents, are given for symmetric mains and for the investigated mains failure conditions for different output power levels of $P_0 \approx (0.5; 1; 2; 3)$ kW and 400-V output voltage for three mains line-to-line voltages $U_{N,\mathrm{ll}} = (208; 330; 450)\ \mathrm{V_{rms}}$ representing the lower, middle, and upper input voltage range. The operating point for $U_{N,\mathrm{ll}} = 208\ \mathrm{V_{rms}}$ and $P_0 \approx 3$ kW could not be achieved due to the dc-link current limitation (cf. Section VI-B).

Power factor and THD_A where measured in each phase (except in phase T for open circuit failure) employing a three-phase power analyzer Voltech PM 300 [13], the results given in the following are the arithmetic mean values of PF and THD_A phase values. The power factor is defined by

$$\mathrm{PF} = \frac{\frac{1}{T_N}\sum_i \int_0^{T_N} u_{N,i}\, i_{N,i}\, dt}{\sqrt{\frac{1}{T_N}\int_0^{T_N} u_{N,i}^2\, \mathrm{d}t}\sqrt{\frac{1}{T_N}\int_0^{T_N} i_{N,i}^2\, \mathrm{d}t}} \tag{32}$$

and the total harmonic distortion of the mains phase currents is calculated by the power analyzer with reference to

$$\mathrm{THD}_A = \frac{\sqrt{I_{N,i}^2 - I_{N,(1),i}^2}}{I_{N,(1),i}} \cdot 100\% \qquad \forall\ \mathrm{THD}_A > 6\%,$$
$$\mathrm{THD}_A = \frac{\sqrt{\sum_{n\neq 1} I_{N,(n),i^2}}}{I_{N,(1),i}} \cdot 100\% \qquad \forall\ \mathrm{THD}_A < 6\%. \tag{33}$$

The power factor of the PWM rectifier system is given in Fig. 10. At low output power and for high mains voltage, the power factor shows lower values than at higher output power and low input voltage. This is due to the lower mains phase current and the higher percentage of the reactive input filter capacitor current. In case of a mains failure, which results in a two-phase operation and/or a higher load on two mains phases, the power factor is increased especially for low output power levels. The relatively low value of the power factor for a mains failure at $U_{N,\mathrm{ll}} = 208$ V is due to the fact that a resonance of input filter and supplying autotransformer does occur. Generally one can say that the power factor lies between $\mathrm{PF} = 0.992$ and 0.998 for an output power $P_0 \geq 2$ kW.

For low input current values and low output power levels the total harmonic distortion of the mains phase currents shows higher values which is again due to the input filter attracting current harmonics from the mains, for increasing output power the total harmonic distortion is approximately constant, except for low input voltages of $U_{N,\mathrm{ll}} = 208$ V (i.e., high input currents) where a resonance between input filter and autotransformer does occur (cf. Fig. 11). *Remark:* For no-load operation, the total harmonic distortion of the mains phase voltages is $\approx(2.0 \ldots 2.3)\%$.

The efficiency of the rectifier system (excluding the power for fans, voltage and current sensing, signal processing, and gate drives) is in the range of $\approx$92.0% (for high output power and low input voltage) to $\approx$96.5% for high input voltages. In case of a mains failure resulting in two-phase operation these values are reduced to $\approx(90 \ldots 94)\%$.

VII. Conclusion

The basic principle of operation and the preferable modulation method of a three-phase/switch PWM unity-power-factor rectifier with integrated boost output stage and a new control concept for reliable operation of the rectifier system under different mains failure conditions (mains voltage unbalance, loss

of one mains phase, short circuit of two mains phases, and earth fault) have been presented. The control consists of an outer output voltages control loop which sets the dc-link current reference value, and an inner dc-link current control loop which provides the control signals for both the buck input stage and the boost output stage. In order to keep all quantities within allowable values, the dc-link current reference value is limited and scaled to a maximum admissible value. All calculations which are necessary for control (i.e., relative on-times of the switching states of the power stage and dc-link current reference value) are treated in detail in analytically closed form. As shown by simulations and experimental results, the rectifier system behaves like a symmetric ohmic load for balanced and unbalanced mains conditions. The input currents show a sinusoidal shape independent of the mains condition, and at the transition from symmetric mains to a mains failure and vice versa no overvoltages, overcurrents, or oscillations do occur. It is furthermore shown that there are no major deviations for power factor and total harmonic distortion for operation during a mains failure as compared to symmetric mains operation.

The considerations given in this paper are valid only for CCM. However, at low output power discontinuous conduction mode (DCM) does occur. In order to avoid DCM, the dc-link inductor current reference value could be increased by adding an offset. However, this also would result in an increased system output power. Therefore, in order to keep the desired output power value, the duty cycle δ of the boost stage has to be increased and/or the boost stage has to be activated. In connection with lowering the buck-stage modulation index this does result in a component of the dc-link current circulating via the buck stage and the boost switch, whereby the effect of the high dc-link current could be compensated.

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