A Virtual-Flux Decoupling Hysteresis Current Controller for Mains Connected Inverter Systems

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***Abstract*—This paper proposes a new simple method of three-phase, sensorless mains voltage, power control with near constant switching frequency based on a decoupling hysteresis current controller (DHC), and the virtual-flux concept. The virtual flux method is used to extract the mains voltage from the switching state, dc voltage, and line currents. From the desired real and reactive powers the three-phase currents are generated using a DHC. The DHC avoids the switching interaction between the phases, and when a variable hysteresis band is employed a near constant switching frequency is achieved. The method is also extended for high power inverter applications that include an inductance–capacitance–inductance output filter, where some undesirable characteristic, such as filter resonance, have to be compensated. Theoretical analysis is presented and the performance of the proposed method is experimentally verified**

***Index Terms*—Decoupling, grid connected, hysteresis current control.**

I. Introduction

THREE-PHASE voltage source inverters are employed in many mains connected applications, including uninterruptible power supply (UPS) and distributed generating systems. In these applications, appropriate regulation of the power flow is required and this can be achieved by either direct current control or a power regulation method. The direct current control method includes voltage oriented control and current hysteresis control (CHC) and for power regulation, direct power control (DPC) is usually employed.

For mains connected applications, the ideal requirements of the inverter include a fast dynamic response, near constant switching frequency, and a reduced number of sensors. However, all of these characteristics are not found in any of the standard control methods. For instance, the voltage oriented control method guarantees a high static performance via an internal current control loop but suffers from a low dynamic performance [1]. For CHC, the current instantaneously follows any change in the reference and the implementation is relatively simple, however the switching frequency is variable [2]. The DPC method controls the active and reactive power by using two hysteresis controllers to select the switching state from a switching table [3]. The DPC method has a fast and robust response to transients as it behaves like the current hysteresis controllers, however, it also has a similar drawback of a variable switching frequency. A constant switching frequency DPC can be achieved by substituting the modulation strategy from a switching table method to space-vector modulation [4]. Nevertheless, the dynamic response becomes equivalent to voltage orientated control.

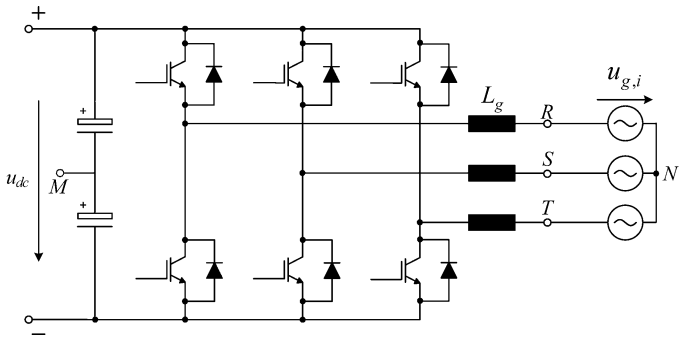

Fig. 1. Three-phase two-level voltage source inverter.

For three-phase, three-wire inverters (Fig. 1) using CHC, coupling between phase currents exists since each phase current does not only depend on the corresponding applied voltage but also on the current in the other two phases [5]–[7]. The decoupling hysteresis control (DHC) [8], [9] has been proposed for three-level rectifiers to minimize the interference between phases while maintaining all the advantages of the CHC. Reducing this phase current interaction results in the switching frequency becoming more uniform and allows for a near constant switching frequency if a variable hysteresis band is implemented.

One of the most important aspects in mains connected inverters, to guarantee the correct operation of the system, is the accurate and fast estimation of the active and reactive power. Normally these are calculated based on the measured mains voltage and current. However, in order to reduce the number of sensors, which gives reliability and economical advantages, a virtual-flux (VF) estimation technique is proposed [10] to replace the ac-line voltage sensors.

For high power applications, a third-order output filter that can achieve reduced levels of harmonics distortion at lower switching frequencies and with less total inductance is usually employed. However, systems incorporating a LCL filter require extra control effort in order to compensate for some undesirable characteristics such as the filter resonance.

This paper proposes a sensorless mains voltage, direct active and reactive power controller operating with a near constant switching frequency. The control scheme uses the DHC, initially proposed for a three-level rectifier [8], to achieve a

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proper current control in a two-level inverter system. Combining the DHC with the VF and power estimation methods allows the advantages of both concepts (DHC and VF–DPC), such as fast dynamic response and relatively simple implementation, to be realized. Moreover, in order to avoid the dependence on [8], the DHC strategy is explained in detail in this paper using a set of equivalent circuits and equations. In Section II, the basic concept of VF estimation is discussed and the calculation of phase currents references based on power quantities is given. In order to reduce the interference between phases, the CHC is replaced by a DHC in Section III and a near constant switching frequency is achieved by adding a variable hysteresis band. Section IV experimentally illustrates the performance of the proposed system. Section V extends the VF–DHC for high power applications, where a third-order LCL filter is necessary. Finally, Section VI verifies experimentally the extended method under different supply voltage conditions (unbalanced and harmonic distortion).

II. VF Hysteresis Control

Recently, the VF strategy [10] was added to the conventional DPC in order to replace the ac-line voltage sensor. The VF strategy assumes that the line voltage and the ac-side inductors are quantities related to a virtual ac motor. Making an analogy with ac motors, R_g and L_g (Fig. 2) represent, respectively, the stator resistance and the stator leakage inductance and the line voltage u_g, represents the machine's electro-motive force.

The mains flux calculation is based on flux definition (1) and the voltage loop equation (2)

$$\bar{\psi}_g = \int \bar{u}_g \cdot dt \tag{1}$$

$$\bar{u}_g = \bar{u}_{\text{inv}} - R_g \cdot \bar{i}_g - L_g \cdot \frac{d\bar{i}_g}{dt}. \tag{2}$$

Neglecting the series resistance of the line inductor, the line virtual flux can be calculated based on the measured line current $\bar{i}_g$ and the inverter voltage $\bar{u}_{\text{inv}}$

$$\bar{\psi}_g = \int \bar{u}_{\text{inv}} \cdot dt - L_g \cdot \bar{i}_g. \tag{3}$$

The inverter output voltage in the stationary coordinates system can be calculated based on the dc link voltage and the converter switching states, s_i, as

$$u_{\text{inv},\alpha} = \frac{2}{3} u_{\text{dc}} \left(s_R - \frac{1}{2}(s_S + s_T) \right) \tag{4}$$

$$u_{\text{inv},\beta} = \frac{1}{\sqrt{3}} u_{\text{dc}} (s_S - s_T) \tag{5}$$

where $s_i = 1$ denotes the top switch on and $s_i = 0$ denotes the bottom switch on.

Using (4) and (5) into (3), the grid VF $\psi_{g,\alpha\beta}$ can be calculated and then used to estimate the active and reactive power

$$p = \frac{3}{2} \omega \cdot (\psi_{g,\alpha} \cdot i_{g,\beta} - \psi_{g,\beta} \cdot i_{g,\alpha}) \tag{6}$$

$$q = \frac{3}{2} \omega \cdot (\psi_{g,\alpha} \cdot i_{g,\alpha} + \psi_{g,\beta} \cdot i_{g,\beta}) \tag{7}$$

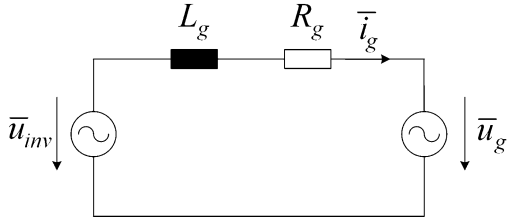

Fig. 2. Equivalent circuit of a mains connected three-phase VSI with L filter.

assuming the stationary $(\alpha\beta)$ transformation as follows:

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} u_R \\ u_S \\ u_T \end{bmatrix}. \tag{8}$$

For DPC, the calculated active and reactive powers are used to generate the switching states and consequently achieve the proper current regulation. However, direct current controller methods, such as CHC, compare a reference current to the actual current in order to control the switching. Therefore, in the proposed controller the reference currents must be first calculated from the power references and the mains VF using

$$i_{\alpha,\text{ref}} = \frac{2}{3} \frac{\psi_{g,\alpha} \cdot q_{\text{ref}} - \psi_{g,\beta} \cdot p_{\text{ref}}}{\omega \cdot \left(\psi_{g,\alpha}^2 + \psi_{g,\beta}^2 \right)} \tag{9}$$

$$i_{\beta,\text{ref}} = \frac{2}{3} \frac{\psi_{g,\alpha} \cdot p_{\text{ref}} + \psi_{g,\beta} \cdot q_{\text{ref}}}{\omega \cdot \left(\psi_{g,\alpha}^2 + \psi_{g,\beta}^2 \right)}. \tag{10}$$

The phase quantities are then obtained by a stationary coordinates transformation and controlled by a current hysteresis controller. The combined VF current hysteresis control (VF-CHC) system is shown in Fig. 3.

The strategy maintains the main characteristics of the CHC and VF–DPC, such as the fast dynamic and relatively simple implementation. On the other hand, it is also affected by the drawbacks of the interaction between phases [Fig. 4(a)] and a variable switching frequency as can be seen in the frequency spectrum and switching frequency behavior in Fig. 4(b) and (c).

These disadvantages can be avoided by replacing the CHC by the DHC, which decouples the phases and avoids the interaction of the switching allowing for a near constant switching frequency.

III. Decoupling Hysteresis Controller

The DHC [8], as shown by shaded DHC area in Fig. 5, has the same basic outer structure as the standard CHC where the phase current is subtracted from a current reference and the hysteresis controller generates a switching signal from the current error.

The DHC has an additional control loop that generates the current control signal, i_0. By summing the measured line current, $i_{g,i}$ with i_0, a virtual current $i'_{g,i}$ is formed. With the correct formation of i_0 the switching of the hysteresis controller can occur without any interaction between each of the phase controllers. The phase interaction is caused because the dc bus midpoint to neutral voltage is not constant, as it is dependent on each of the inverter output voltages.

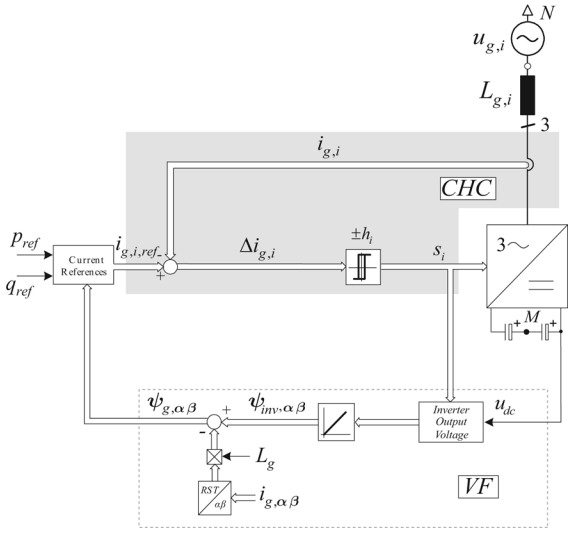

Fig. 3. VF current hysteresis control (VF-CHC) structure.

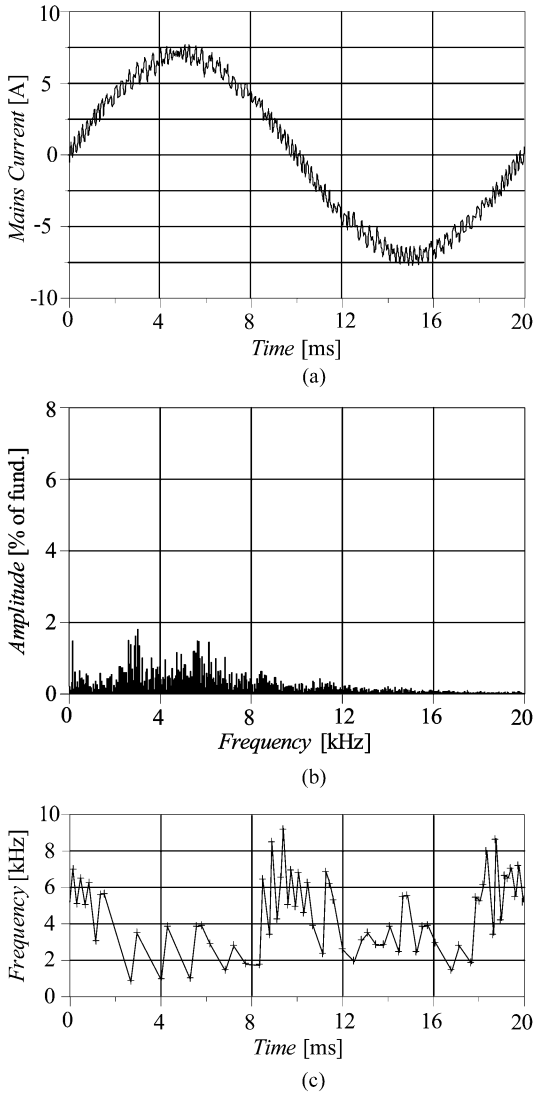

Fig. 4. Simulated performance of VF–CHC with average switching frequency of 4 kHz. The (a) resulting mains current, (b) frequency spectrum, and (c) switching frequency behavior during one fundamental cycle.

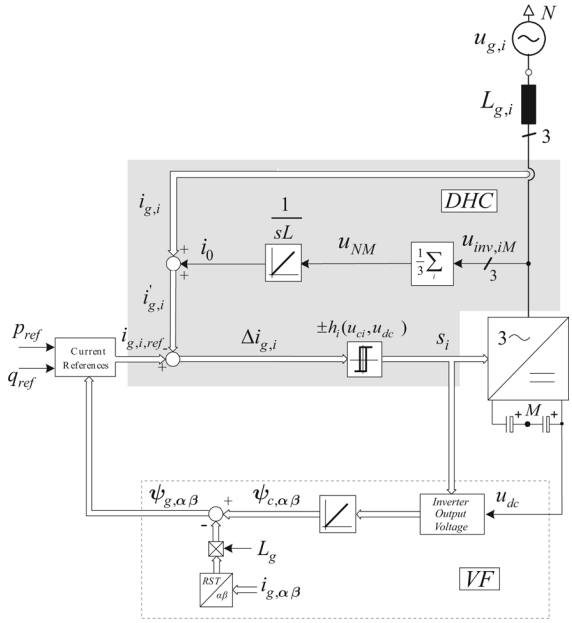

Fig. 5. VF–DHC structure.

The phase current is defined by the voltage across the output filter inductor, which is represented in Fig. 6 by the difference between the converter output voltage and the grid voltage referred to the neutral point

$$\begin{aligned} L_g \frac{di_{g,R}}{dt} &= u_{L_g,R} = u_{\text{inv},R} - u_{g,R} \\ L_g \frac{di_{g,S}}{dt} &= u_{L_g,S} = u_{\text{inv},S} - u_{g,S} \\ L_g \frac{di_{g,T}}{dt} &= u_{L_g,T} = u_{\text{inv},T} - u_{g,T}. \end{aligned} \tag{11}$$

If the mains star point, N, and the dc midpoint, M are not connected [Fig. 6(a)], then the inverter output voltage is given by

$$\begin{aligned} u_{\text{inv},R} &= u_{\text{inv,RM}} + u_{\text{MN}} \\ u_{\text{inv},S} &= u_{\text{inv,SM}} + u_{\text{MN}} \\ u_{\text{inv},T} &= u_{\text{inv,TM}} + u_{\text{MN}} \end{aligned} \tag{12}$$

where $u_{\text{inv,iM}}$ are the inverter ac voltages referred to M, and u_{MN} is the zero sequence voltage occurring between the mains star point and dc midpoint.

The inverter output voltage $(u_{\text{inv,iM}})$ shown in Fig. 6(a) can be split into two parts, as presented in Fig. 6(b). The first part consists of a low frequency $(u_{\text{inv,iM}+,l})$ and a ripple $(u_{\text{inv,iM}+,r})$ voltage of the current shaping component, and the second represents the low frequency $(u_{M}+_{M,l})$ and ripple $(u_{M}+_{M,r})$ component of the zero sequence voltage.

Given that the zero sequence voltages are connected at the same potential (M^+), the equivalent circuit can be simplified to that shown in Fig. 6(c). From that, the equation which describes the inverter output voltage referred to the midpoint can be derived as

$$\begin{aligned} u_{\text{inv},RM} &= u_{\text{inv,RM}^+} + u_{M^+M} \\ u_{\text{inv,SM}} &= u_{\text{inv,SM}^+} + u_{M^+M} \\ u_{\text{inv,TM}} &= u_{\text{inv,TM}^+} + u_{M^+M} \end{aligned} \tag{13}$$

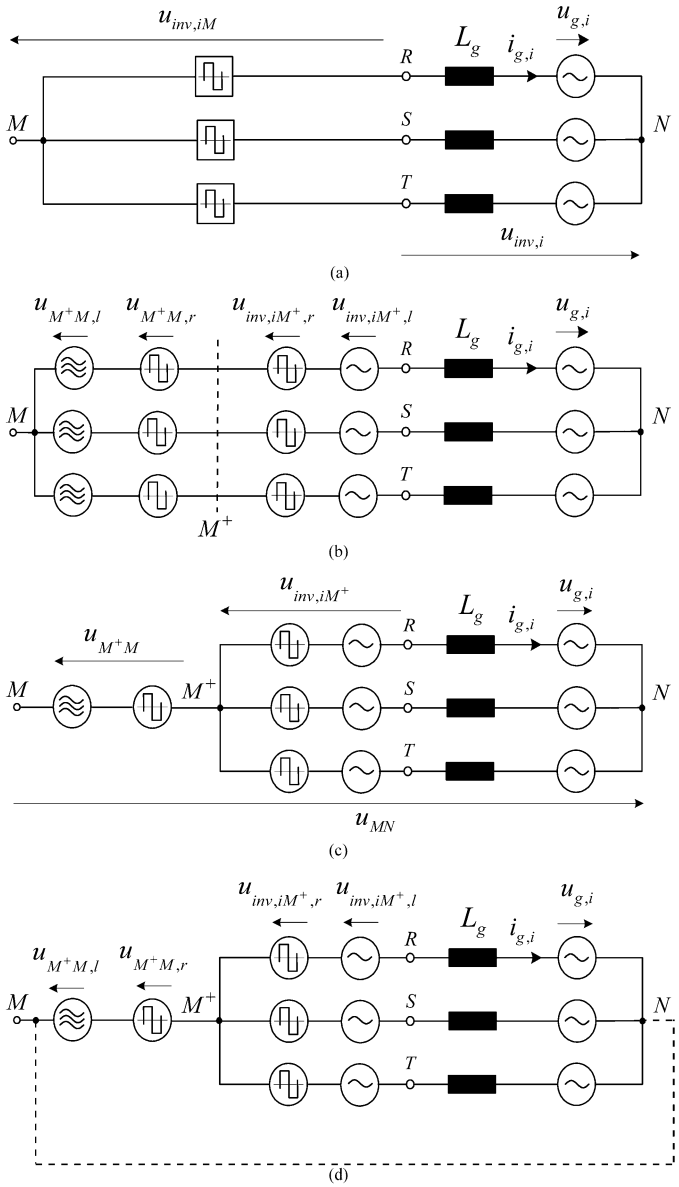

Fig. 6. Equivalent circuits of DHC implementation. (a) M and N are not connected. (b) Inverter output voltage divided in current forming component and zero sequence voltage. (c) Simplified model with the virtual potential M^+. (d) Virtual connection between M^+N allowing for the high frequency decoupling between phases.

or

$$u_{\mathrm{inv,RM}} = L_g \frac{di_{g,R}}{dt} + u_{g,R} + u_{\mathrm{NM}}$$
$$u_{\mathrm{inv,SM}} = L_g \frac{di_{g,S}}{dt} + u_{g,S} + u_{\mathrm{NM}}$$
$$u_{\mathrm{inv,TM}} = L_g \frac{di_{g,T}}{dt} + u_{g,T} + u_{\mathrm{NM}}. \quad (14)$$

Since symmetrical mains voltage is assumed, the influence of each phase on the zero sequence voltage is derived from (13)

$$u_{M^+M} = \frac{1}{3}(u_{\mathrm{inv,RM}} + u_{\mathrm{inv,SM}} + u_{\mathrm{inv,TM}}). \quad (15)$$

Considering the sum of the phase currents is zero and taking (13) and (14) into account, it follows:

$$u_{M^+M} = u_{\mathrm{NM}} = -u_{\mathrm{MN}}. \quad (16)$$

Therefore, combining (11), (12), (15), and (16), the coupling between the phases is clearly seen from

$$L_g \frac{di_{g,R}}{dt} = u_{\mathrm{inv,RM}} - u_{g,R} - \frac{1}{3}(u_{\mathrm{inv,RM}} + u_{\mathrm{inv,SM}} + u_{\mathrm{inv,TM}})$$
$$L_g \frac{di_{g,S}}{dt} = u_{\mathrm{inv,SM}} - u_{g,S} - \frac{1}{3}(u_{\mathrm{inv,RM}} + u_{\mathrm{inv,SM}} + u_{\mathrm{inv},TM})$$
$$L_g \frac{di_{g,T}}{dt} = u_{\mathrm{inv,TM}} - u_{g,T} - \frac{1}{3}(u_{\mathrm{inv,RM}} + u_{\mathrm{inv,SM}} + u_{\mathrm{inv,TM}}). \quad (17)$$

The current is not only dependent on the respective inverter output voltage but is also influenced by the zero sequence voltage, represented in the equivalent circuit [Fig. 6(b)] as a high frequency switching voltage component $u_{M^+M,r}$.

In the case where M, the midpoint of the dc capacitors is directly connected to the mains neutral N, $(u_{\mathrm{MN}} = 0)$ and/or $u_{\mathrm{inv},i} = u_{\mathrm{inv},iM}$, there is no mechanism for any interaction between the phases. This is because the current, $i_{g,i}$, that flows in each phase is only dependent on the total voltage measured to the midpoint, $u_{\mathrm{inv},iM}$ as shown in (11) and (12). The fundamental current is produced by the voltage difference of the mains voltage, $u_{g,i}$, and the fundamental voltage at the output of the inverter, $u_{\mathrm{inv},iM,l}$. The current ripple is created from the high frequency switching voltage at the output of the inverter $u_{\mathrm{inv},iM,r}$.

In order to eliminate the interaction between phases for the case when the midpoint M and the mains neutral N are not connected, an additional current term, i_0, is added into the current controller ($i'_{g,i} = i_{g,i} + i_0$, cf. Fig. 5). The current signal, i_0, is generated by integrating either the calculated voltage u_{M^+M} given by (15) or the measured zero sequence voltage u_{MN} as given by

$$i_0 = \frac{1}{L_g} \int u_{\mathrm{MN}}\, dt. \quad (18)$$

The addition of the decoupling controller now effectively makes the point M look like that it is connected to the mains neutral point [shown by dashed line in Fig. 6(d)]. Thus, the high frequency switching in each phase does not have any interaction with the other two phases.

Although DHC makes the switching frequency more uniform than a CHC [9], it is desirable to have the inverter operating with a constant switching frequency as this makes the design of the output filter task simpler. The harmonic performance can be substantially improved by varying the hysteresis band over each fundamental cycle, since the switching frequency is dependent on the voltage difference across the inductor, the inductor value, and the hysteresis band level.

In order to derive a relatively simple expression for the required hysteresis band, it is assumed that during one switching period that the fundamental voltage is constant. The switching of the inverter either impresses a $+1/2u_{\mathrm{dc}}$ (upper switch on) or a $-1/2u_{\mathrm{dc}}$ (lower switch on) voltage at the inverter's ac side

terminals. By combining the switching time equations and rearranging, the hysteresis band, h, required to produce a constant frequency is expressed as

$$h_i = \frac{\left(\frac{u_{\rm dc}}{2}\right)^2 - u_{{\rm inv},i}^2}{2 \cdot L_g \cdot f_s \cdot u_{\rm dc}}. \tag{19}$$

For a sinusoidal output inverter voltage, $u_{\rm inv,i}$, the shape of the hysteresis band for one mains period is shown in Fig. 7. The magnitude has been normalized by dividing by the peak value of the reference current.

The fundamental component of the inverter voltage $u_{{\rm inv},i}$ used in (19) is easily calculated from the output inverter flux ($\bar{\psi}_{\rm inv} = \int \bar{u}_{\rm inv} \cdot dt$) as follows:

$$\begin{aligned} u_{{\rm inv},\alpha} &= -k \cdot \psi_{{\rm inv},\beta} \\ u_{{\rm inv},\beta} &= k \cdot \psi_{{\rm inv},\alpha} \end{aligned} \tag{20}$$

where k is the gain to compensate for the integrator attenuation at fundamental frequency ($-$50 db at 50 Hz).

The advantages of the VF–DHC when compared with the conventional hysteresis can be observed in the Fig. 8. Adding the zero sequence current i_0 to the actual current reduces the interference between phases [Fig. 8(a)] and allows for a near constant switching frequency in one cycle period [Fig. 8(c)] due to the modulated hysteresis band. The switching becomes more centered around 4 kHz [Fig. 8(b)] rather than the wide frequency range for VF–CHC.

IV. Experimental Verification

In order to verify experimentally the proposed VF–DHC, it is implemented in a fully digital controller using an Analog Devices ADSP21991 16-b 160-MHz DSP interfaced to a 6-kW three-phase inverter [Fig. 9(a)]. The output inductance links between the inverter and the controlled 400-V three-phase ac power source. The inductor is designed to allow a current ripple of 20% of the peak phase current and to operate with an average switching frequency of 4 kHz. Due to this low switching frequency and low power rating the utilized inductor value is relatively large at 10 mH. The 750 V dc power is provided by a 10 kW, controlled dc power supply. The DSP implementation is divided into two loops with different sampling frequencies in order to optimize the process time. To avoid large current excursion outside the hysteresis band, the comparison between the error signal and the hysteresis boundaries is performed in a fast 200 kHz control loop. This control loop also reads the two phase currents and the dc voltage are sampled at the same rate using the DSP's internal 14-b ADC. During the ADC conversion time of 725 ns, the algorithm calculates the midpoint to neutral voltage using derived phase to midpoint voltages that are based on the switch state and previous sample instantaneous dc input voltage. The midpoint to neutral voltage is integrated and summed to the current reference. All six inverter switches are updated simultaneously at the end of the calculations. The calculation of the reference current and variable hysteresis band are updated at a rate of 30 kHz.

The static behavior of proposed VF–DHC is showed in Fig. 9(b). From that it can be seen that the grid virtual-fluxes are successfully estimated, since the α component of the virtual flux is 90° lagging the grid voltage (phase R). The phase current is in phase with the actual supply voltage since the reactive power is controlled to be zero.

The VF–DHC performance is better observed comparing the gate signals, switching frequency behavior and the current spectrum of the proposed method with the VF–CHC and VF–DHC

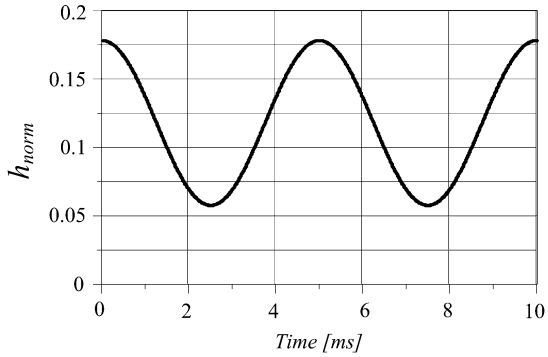

Fig. 7. Normalized hysteresis band shape for one mains period.

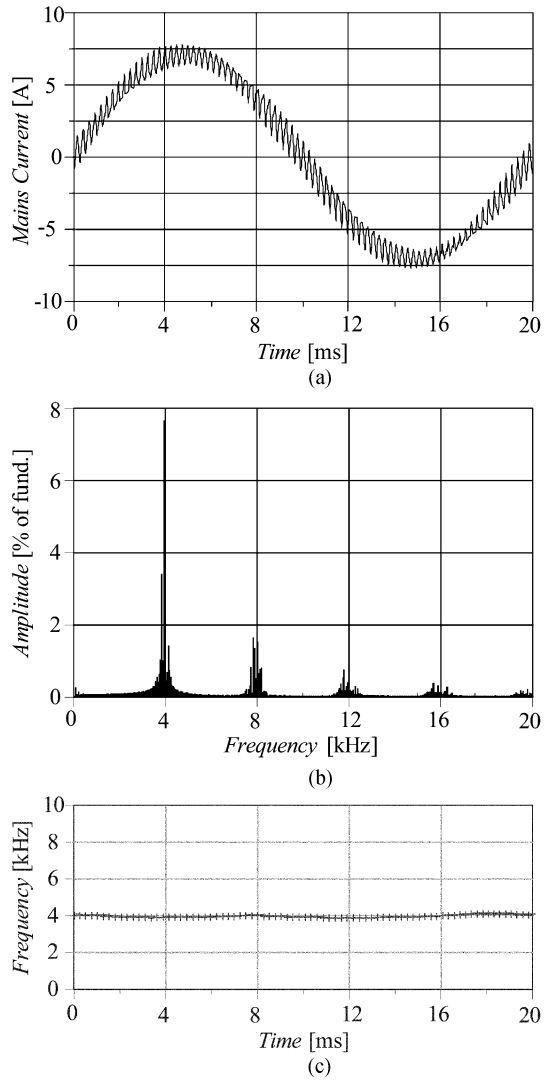

Fig. 8. Simulated performance of the proposed VF–DHC with switching frequency of 4 kHz. The (a) resulting mains current, (b) frequency spectrum, and (c) switching frequency behavior during one fundamental cycle.

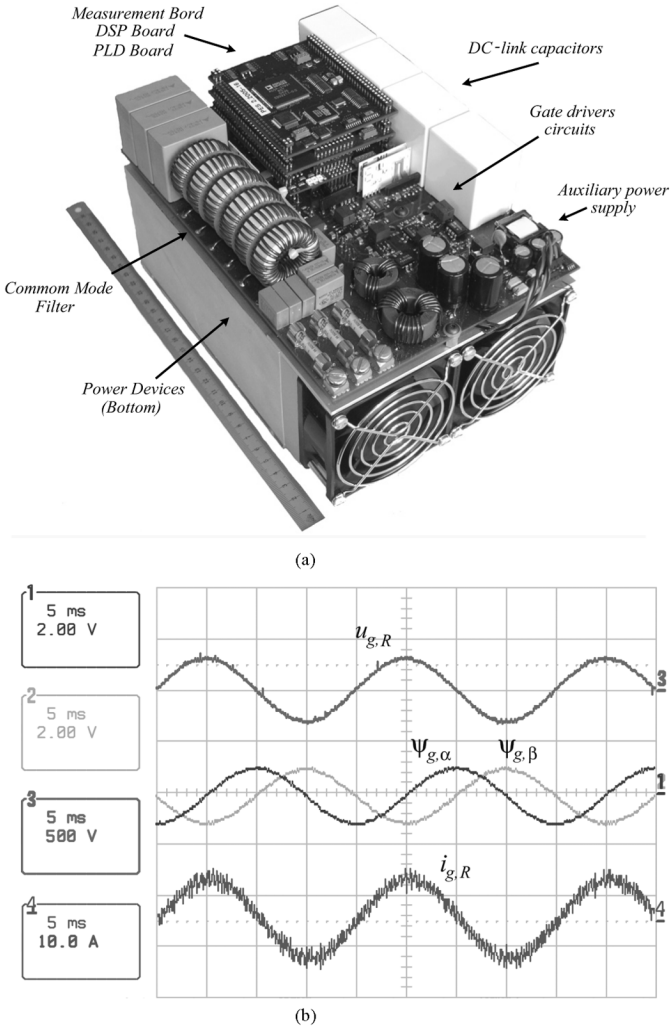

Fig. 9. (a) Prototype photo with L in the heatsink cavity and (b) mains phase voltage $u_{g,R}$, VF $\psi_{g,\alpha\beta}$ and phase-current of proposed VF–DHC.

with constant hysteresis band. For VF–CHC [Fig. 10(a)] it can be seen for the R phase switching signal that there are periods where no switching occurs due to the interaction of the phases. The variable switching frequency is observed through the measured instantaneous switching frequency behavior over one cycle period [Fig. 10(b)] and the current spectrum [Fig. 10(c)] shows that the switching is occurring over a relatively wide frequency range. Adding the zero sequence current to the measured currents the switching becomes more uniform, as can be observed in the phase current and gate signals [Fig. 10(d)], or directly by the instantaneous switching frequency [Fig. 10(e)] and the current spectrum [Fig. 10(f)] that becomes more uniform. Modulating the hysteresis band [Fig. 10(g)] the switching frequency becomes almost constant [Fig. 10(h)] and the spectrum is more centered around 4 kHz [Fig. 10(i)].

The decoupling does not affect the fast dynamic response inherent in the hysteresis controller as can be seen in the power reference step change (Fig. 11). Fig. 11(a) shows the estimated active power (p) quickly tracking the active power reference $(p_{\rm ref})$ during a step from 40% to 80%. The same behavior is observed in the negative step from 80% to 40% [Fig. 11(b)]. A rise time of 500 μs is observed in the positive step [Fig. 11(c)] while an even faster time response is noted in the negative step [Fig. 11(d)]. Both cases show that an active power step does not have any influence on the reactive power (q).

V. VF–DHC With LCL Filter

The VF–DHC concept can be extended for high power applications where it is very difficult to meet the IEEE519 without a third-order filter. The LCL filter attenuates the switching ripple substantially and the overall size of the LCL filter is reduced compared to only an L filter. However, systems incorporating an LCL filter require extra control effort in order to compensate some undesirable characteristics such as the filter resonance.

The modified VF–DHC showed in Fig. 12 maintains the core of the conventional approach and incorporates outer control loops which damp the filter resonance, reject the influence of grid voltage harmonics and compensate for the reactive power of the capacitor filter, since the active and reactive power are controlled on the inverter side.

A. Virtual-Flux Estimation

Another issue that has to be considered is the grid VF estimation, which differs from the concept with a series inductor as a filter. In this case, the grid side inductor (L_g) flux has to be considered and results in

$$\bar{\psi}_g = \int \bar{u}_{\rm inv} \cdot dt - L_{\rm inv} \cdot \bar{i}_{\rm inv} - L_g \cdot (\bar{i}_{\rm inv} - \bar{i}_c). \qquad (21)$$

A pure integrator used to estimate the inverter VF in practice brings some undesirable effects due to dc offset present in the voltage/current measurement. This dc component, no matter how small it is, can finally drive the pure integrator into saturation. A common solution to overcome this drawback is to replace the pure integrator by a first-order low-pass (LP) filter, however it reduces the performance of the system because of the phase and magnitude errors inherent in such filter. A method proposed in [11] to compensate the phase and magnitude errors is applied to the inverter VF estimation block, as shown in Fig. 13.

The main idea behind of such method is to provide low-pass filter behavior at all frequencies except at the operating frequency, thus avoiding integration drift problem while at the same time good system performance is maintained.

The corrected VF is calculated basically based on the ratio between the low-pass filter cutoff frequency (w_c) and the operating frequency (w_f)

$$\psi_{{\rm inv},\alpha} = \psi'_{{\rm inv},\alpha} + \psi'_{{\rm inv},\beta}\frac{w_c}{w_f} \qquad (22)$$

$$\psi_{{\rm inv},\beta} = \psi'_{{\rm inv},\beta} - \psi'_{{\rm inv},\alpha}\frac{w_c}{w_f}. \qquad (23)$$

B. Active Damping

The active damping strategy can be applied effectively because the resonance frequency of the output filter is usually inside the bandwidth of the inverter control loops. The active

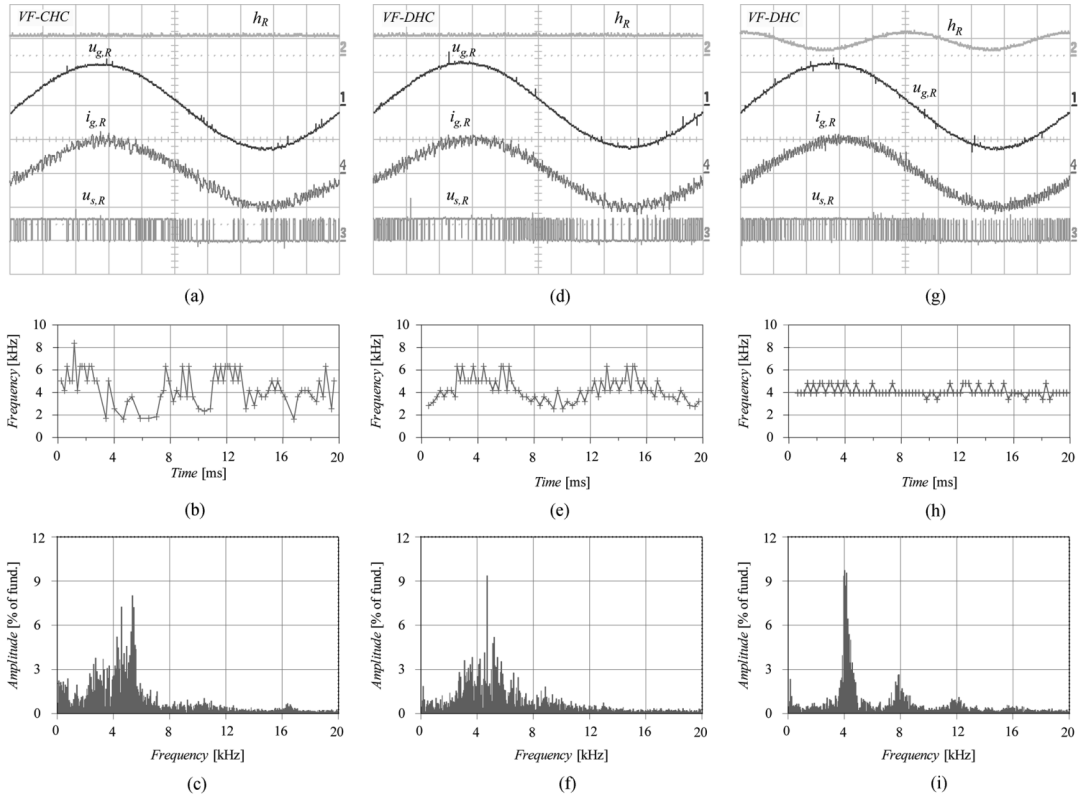

Fig. 10. Grid voltage $u_{g,R}$, grid current $i_{g,R}$, hysteresis band h and gate signals $u_{s,R}$ of (a) VF-CHC, (b) VF-DHC, (c) VF-DHC with modulated hysteresis band ($u_{g,R}$ trace is 200 V/div, $i_{g,R}$ is 10 A/div, $u_{s,R}$ is 20 V/div, time base is 2 ms/div). Switching frequency behavior during one fundamental cycle and frequency spectrum of the grid current (b)–(c) VF-CHC, (e)–(f) VF-DHC, and (h)–(i) VF-DHC with modulated hysteresis band.

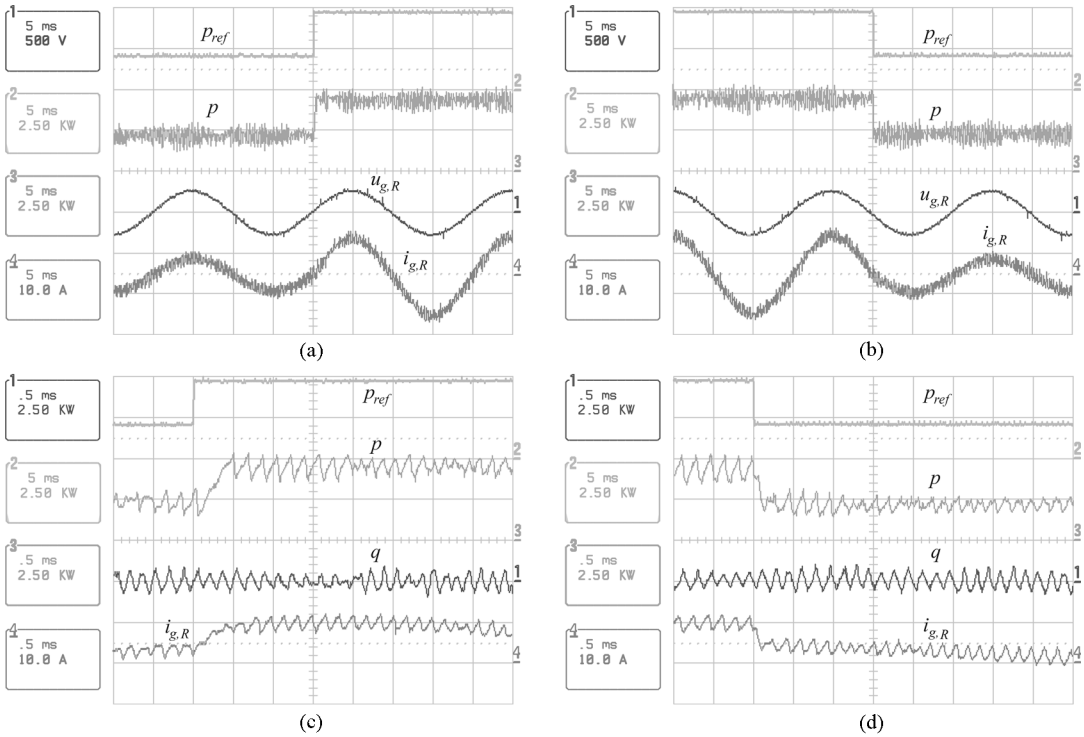

Fig. 11. Experimental results of step response for the VF–DHC with modulated hysteresis band (a) from 40% to 80% of active power; (b) from 80% to 40%; (c) detailed positive step; and (d) detailed negative step.

damping is achieved by emulating a resistor in parallel with the filter capacitor by creating a current source $(I_{d,dq})$ proportional to the capacitor voltage resonance component $(\tilde{u}_{C,\alpha\beta})$, as shown in the equivalent circuit of Fig. 14.

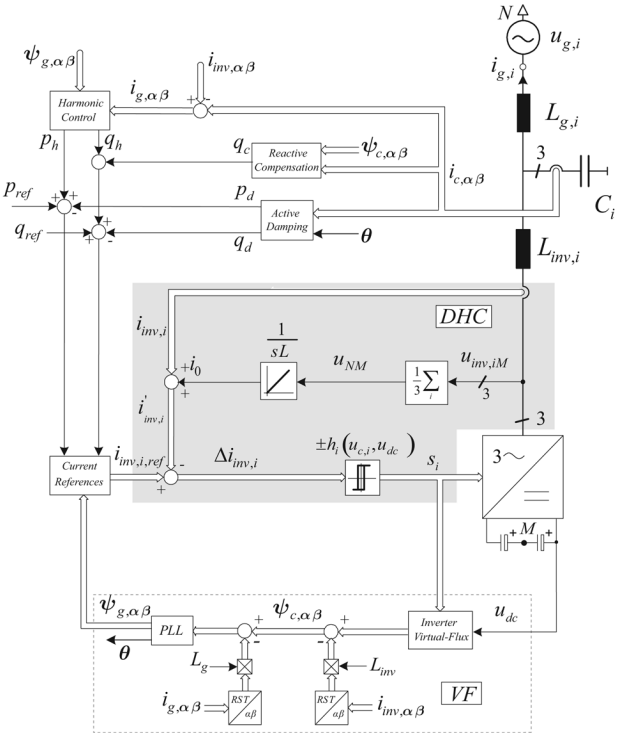

Fig. 12. Extension of the VF–DHC for high power application where LCL filter is usually employed.

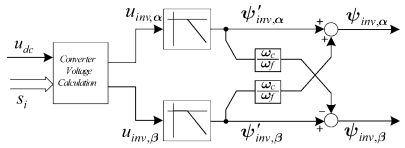

Fig. 13. Inverter VF calculation block with magnitude and phase errors compensation.

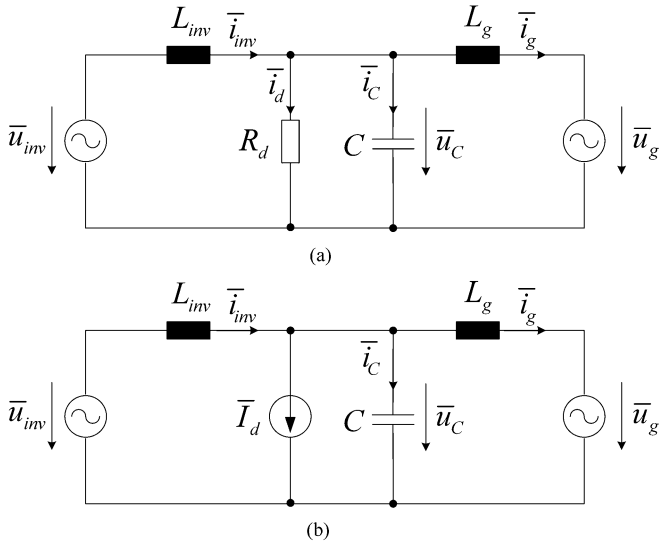

Fig. 14. Equivalent output stage with (a) passive damping and (b) active damping.

The active damping scheme is better explained through the block diagram of Fig. 15. The capacitor voltage $(u_{C,\alpha\beta})$ is calculated based on the capacitor current $(i_{C,\alpha\beta})$ and then converted to a d component by synchronous reference frame transformation, which is synchronously rotating in the same direction and speed as the capacitor voltage. The resonance component of the capacitor voltage $(\tilde{u}_{C,\alpha\beta})$ is extracted by eliminating the fundamental frequency component through a first-order notch filter with stopband between 40 and 60 Hz, for a 50-Hz mains frequency. The resonance part is transformed to dq components and then is multiplied by the damping factor (k_d) in order to obtain the proportional damping current source $(I_{d,dq})$.

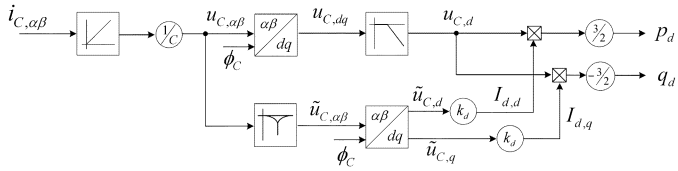

Fig. 15. Active damping block diagram.

Given that the control strategy is based on power quantities, the calculated current source is then multiplied by the capacitor voltage as follows:

$$p_d = \frac{3}{2}\mathrm{Re}\left\{u_{C,\mathrm{dq}} \cdot I^*_{d,\mathrm{dq}}\right\} \tag{24}$$

$$q_d = \frac{3}{2}\mathrm{Im}\left\{u_{C,\mathrm{dq}} \cdot I^*_{d,\mathrm{dq}}\right\}. \tag{25}$$

In order to decrease the effect of either low harmonics (fifth, seventh, 11th) or the resonance component on the d axis of the capacitor voltage $(u_{C,d})$, a first-order low-pass filter is implemented with a cutoff frequency at least one decade below the lowest frequency to be reduced.

The calculated damping components (26)–(27) are then subtracted from the active and reactive power references as illustrated in Fig. 12

$$p_d = \frac{3}{2}u_{C,d} \cdot k_d \cdot \tilde{u}_{C,d} \tag{26}$$

$$q_d = -\frac{3}{2}u_{C,d} \cdot k_d \cdot \tilde{u}_{C,q}. \tag{27}$$

The proposed controller (VF–DHC) when operating with a first-order output filter (L), provides a reasonable compensation of low-order harmonics (fifth, seventh), due to the low-pass filter characteristic of the estimated VF. However, by adding the third-order LCL filter and consequently the active damping loop, the harmonics present in the grid voltage are amplified through this feedback and therefore must be actively compensated.

C. Harmonic Control

The harmonic control block (Fig. 16) proposed in [12] and [13] regulates the harmonics individually in their respective individual synchronous reference frame. Each harmonic quantity to be controlled (h) is transformed into its own individual synchronous reference frame. The corresponding harmonic quantities appear as dc in their own reference frame, while all other harmonics will appear as harmonic of changed order. To extract only the dc component value, harmonic of interest, and consequently eliminate any other harmonic a first-order low-pass filter with a cutoff frequency of 10 Hz is implemented. This dc quantity is then controlled with a PI compensator, which tries to eliminate the steady state error.

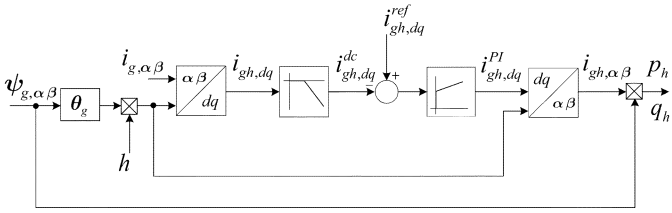

Fig. 16. Closed loop individual harmonic current control.

The PI controller output is transformed back to stationary reference frame and multiplied by the grid VF in order to obtain power quantities

$$p_h = \frac{3}{2}\omega \cdot (\psi_{g,h,\alpha} \cdot i_{h,\beta} - \psi_{g,h,\beta} \cdot i_{h,\alpha}) \tag{28}$$

$$q_h = \frac{3}{2}\omega \cdot (\psi_{g,h,\alpha} \cdot i_{h,\alpha} + \psi_{g,h,\beta} \cdot i_{h,\beta}). \tag{29}$$

Active $(p_{\rm hn})$ and reactive $(q_{\rm hn})$ components of each harmonic to be controlled are calculated separately and override either the active or reactive power references, as illustrated in Fig. 17. The number of harmonics to be compensated (fifth, seventh, 11th...) depend on the application, however they are limited by the LCL filter bandwidth.

D. Reactive Power Compensation

In the case where a third-order LCL filter is employed and the hysteresis controller is performed using the current feedback from the grid side current, the hysteresis band has to be reduced due to the very low ripple presented in the grid side current. It might end up by injecting more ripple into the grid due to measurement error.

To overcome this drawback the active and reactive power are controlled in the inverter side inductors as shown in Fig. 12. However, as the goal is to control the active and reactive power on the grid side, the capacitor reactive power has to be compensated.

Using the capacitor VF $(\psi_{c,\alpha\beta})$ and current $(i_{c,\alpha\beta})$ the capacitor reactive power is estimated (30) and added to the reactive power reference as shown in Fig. 12

$$q_c = \frac{3}{2}\omega \cdot (\psi_{c,\alpha} \cdot i_{c,\alpha} + \psi_{c,\beta} \cdot i_{c,\beta}). \tag{30}$$

E. Phase-Locked Loop

As the grid voltages are not always purely sinusoidal and balanced, a phase-locked loop (PLL) is used in order to extract the fundamental component, phase and frequency.

A PLL based on the VF stationary components was proposed in [14]. This method removes the influence of grid voltage distortion by extracting the magnitude value of the fundamental component and synchronizing the angle of the estimated grid VF, as shown in the block diagram of Fig. 18. A first-order low-pass filter is used to reject the ripple component present on the virtual flux magnitude value, while the angle synchronization is implemented by a PLL. This ripple is caused mainly by low-order harmonics on the grid voltage, therefore a cutoff frequency at least one decade below the second harmonic, the lowest to be suppressed, must be used.

The compensated radial $(\overline{\psi}_g)$ and angle (θ_g) polar components are transformed back to rectangular coordinate.

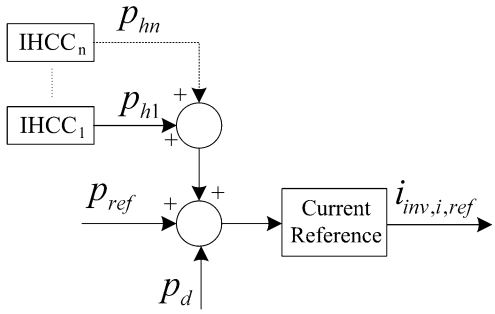

Fig. 17. Overriding harmonic power controllers.

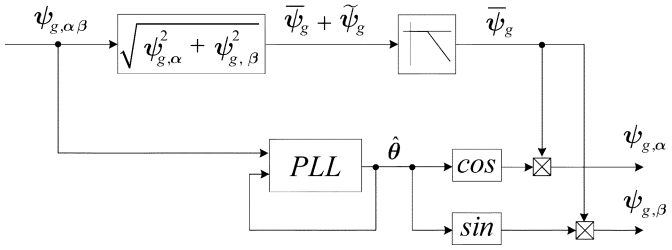

Fig. 18. Phase-locked loop scheme.

VI. Experimental Verification

The experimental verification of active damping, harmonic control and reactive power compensation schemes is performed using the 6 kW inverter setup described for the L filter VF–DHC approach, except the output filter that was replaced by a third-order LCL filter ($L_{\rm inv} = 7.9$ mH, $L_g = 3.5$ mH, and $C = 14.1\,\mu$F). The sample rate of the main loop was reduced to 140 kHz due to the limited computation time, since further calculations are required in the outer loops. The active damping calculation is included in the 30 kHz loop. Additionally, in order to calculate the fifth harmonic control and the PLL components a slower loop with sample rate of 10 kHz was included in the DSP code.

The effectiveness of the extended approach concerning the LCL resonance damping, the fifth harmonic reduction and the capacitor reactive power compensation is observed comparing phase current $(i_{g,R})$ and current spectrum of the conventional VF–DHC [Fig. 19(a)–(b)] with the proposed VF-DHC [Fig. 19(c)–(d)]. The resonance component presented in the current spectrum of the conventional scheme [Fig. 19(b)] is well damped in the extended method [Fig. 19(d)]. The same behavior is observed in the fifth harmonic component that is reduced from 3% to around 1.3%.

A correction in the reactive power is also observed when comparing the phase shift between grid voltage, $u_{g,R}$, and current, $i_{g,R}$, for the conventional approach [Fig. 19(a)] and the extend method [Fig. 19(c)].

Fig. 20 shows the experimental results of dynamic response when a step from 40% to 80% of total active power is given. A significant reduction of the resonance oscillation is noted comparing the VF–DHC [Fig. 20(a)–(b)] and the extended method [Fig. 20(c)–(d)]. It can be noted that even including the outer loops fast tracking (1 ms) of the active power reference $(p_{\rm ref})$ is maintained.

Since the control action is performed in the inverter side, the reactive power is compensated, as can be seen in Fig. 20(d),

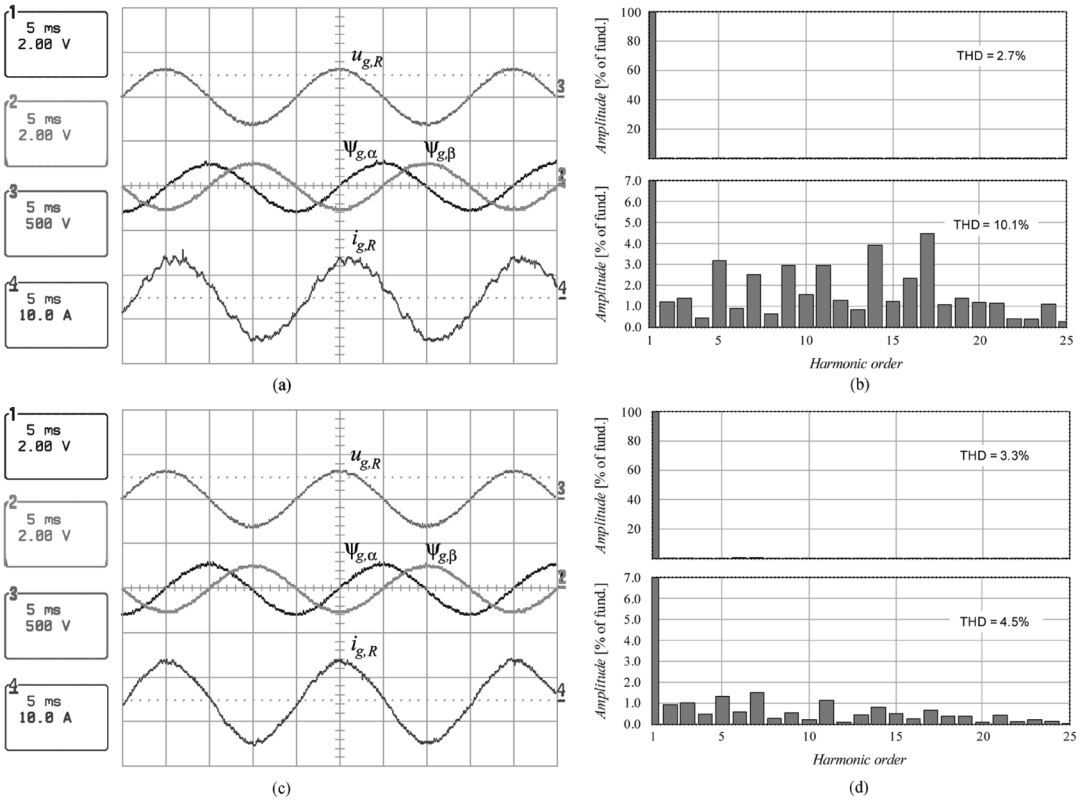

Fig. 19. Experimental result of grid phase voltage $u_{g,R}$, virtual-flux $\psi_{g,\alpha\beta}$ and phase current $i_{g,R}$ (a) for the conventional VF–DHC and (c) the extended strategy including the active damping, harmonic control and reactive power compensation. The respective grid voltage and current harmonic spectrums are shown in (b) and (d).

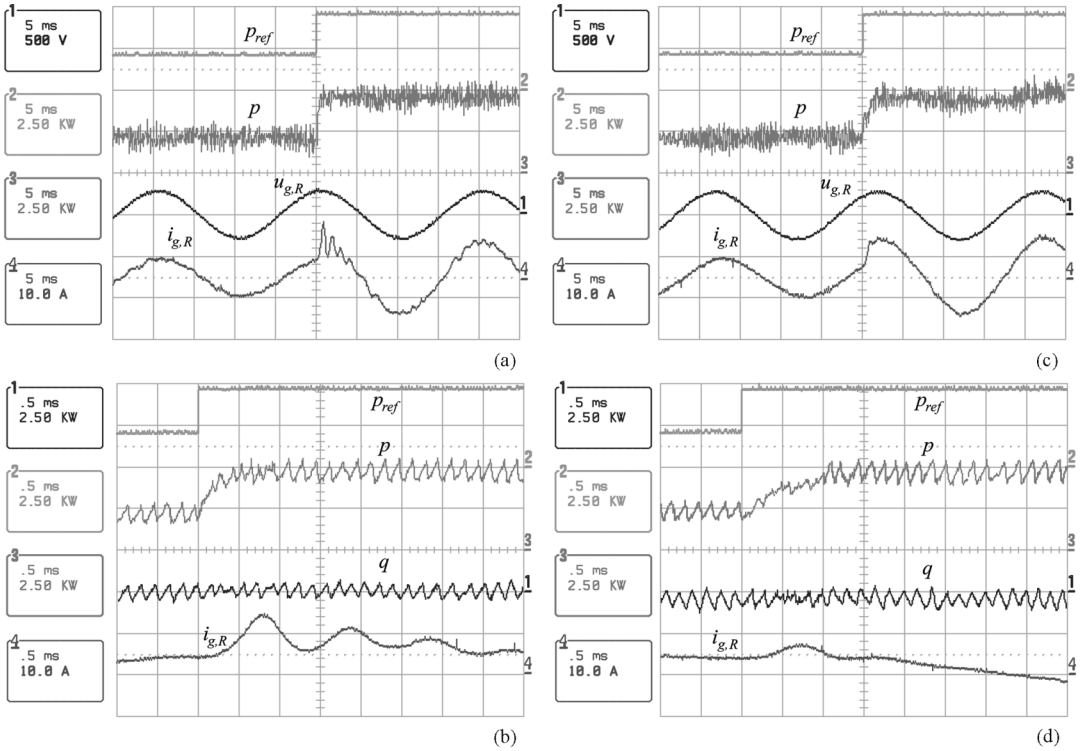

Fig. 20. Experimental results of a step in the active power reference of 40% with (a)–(b) the conventional VF-DHC and (c)–(d) the extended system. Active power reference $p_{\rm ref}$, actual active and reactive power p and q, respectively, grid phase voltage $u_{g,R}$ and current $i_{g,R}$.

by adding the estimated capacitor reactive power (30) to the reference and therefore to the controlled actual reactive power.

The performance of the system under unbalanced phase voltage (phase R+10% and phase S−10%) was also verified. Fig. 21(a) shows the unbalanced three phase voltages and the resulting grid phase current for the case without PLL. The distorted phase current is caused by the unbalanced estimated grid VF [Fig. 21(b)]. Balanced grid VF [Fig. 21(d)] and consequently

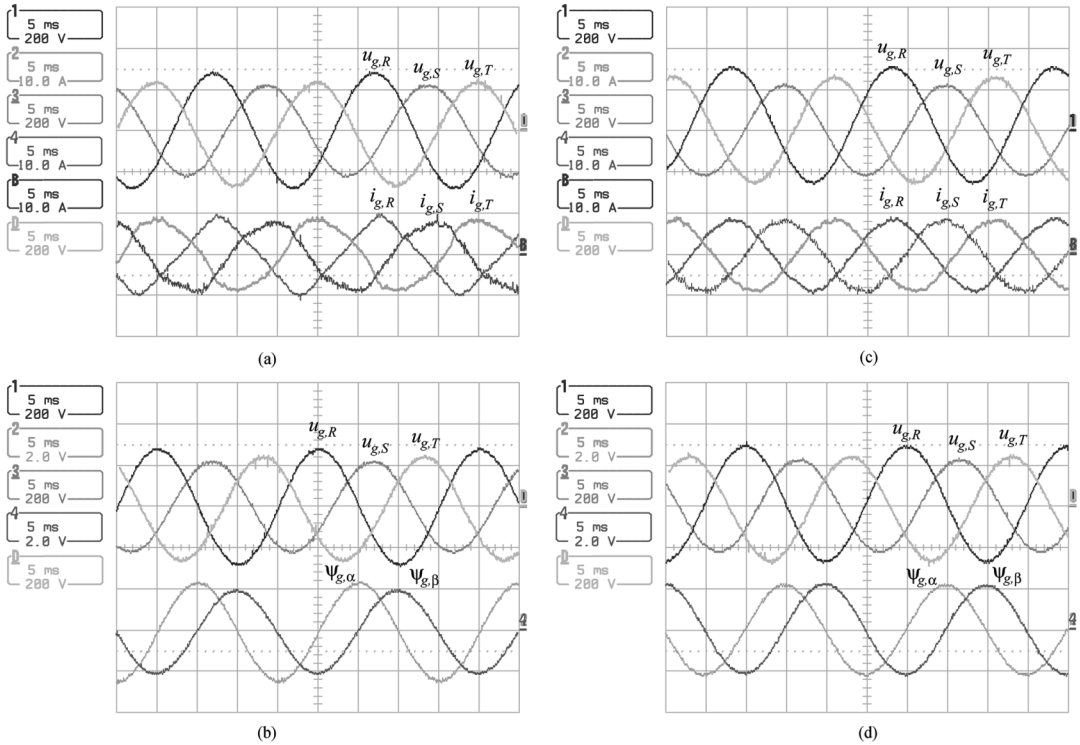

Fig. 21. Experimental results under unbalanced grid voltage (phase R with $+10\%$, phase S with -10% and phase T with 230 V rms). Grid phases current $i_{g,i}$ and grid virtual flux $\psi_{g,\alpha\beta}$ (a)–(b) without PLL and (c)–(d) with PLL, respectively.

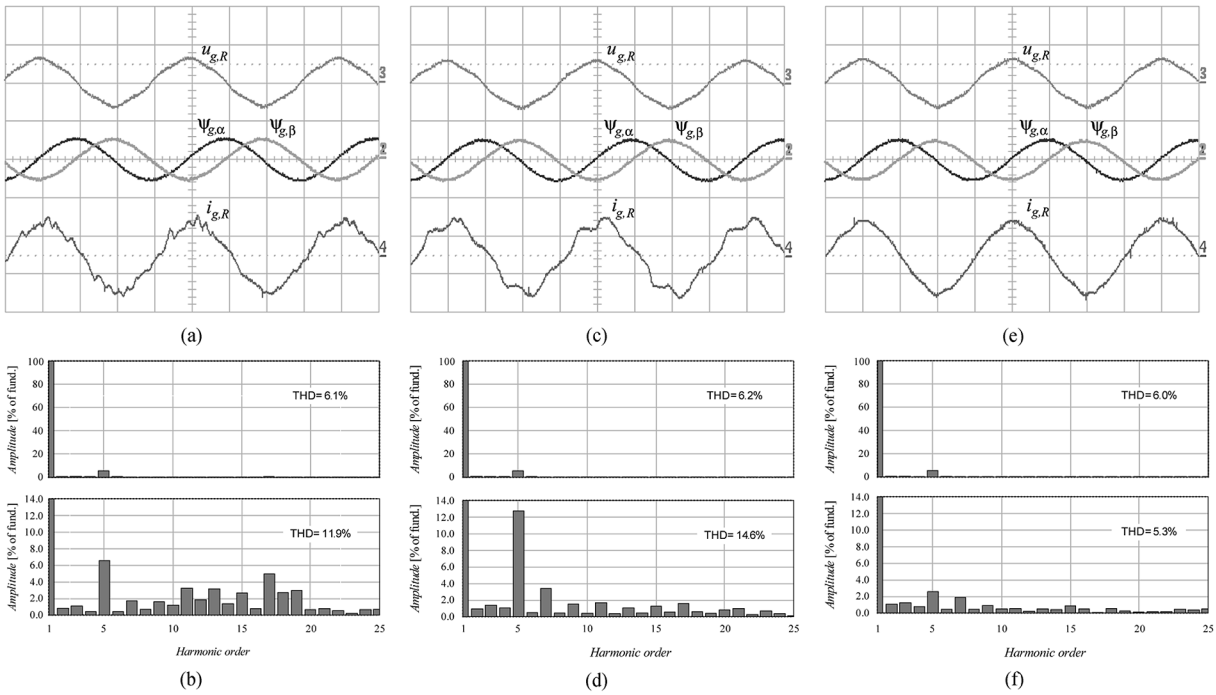

Fig. 22. Experimental results when 5% of the fifth harmonic is superposed the fundamental grid voltage band ($u_{g,R}$ trace is 500 V/div, $i_{g,R}$ is 10 A/div, time base is 5 ms/div). Grid phase voltage $u_{g,R}$, VF $\psi_{g,\alpha\beta}$, phase current $i_{g,R}$ and respective voltage and current spectrum (a)–(b) with the conventional VF–DHC and (c)–(d) adding the active damping and (e)–(f) enabling the fifth harmonic control.

reduction of low-order harmonics presented in the grid current [Fig. 21(c)] are achieved by including a PLL in the extend method.

Fig. 22 shows experimental results in which 5% of the fifth harmonic component was superposed on the fundamental grid voltage. High level of fifth harmonic component and the resonance frequency leads for a high total harmonic distortion for the case where a conventional VF–DHC is implemented as can be seen in Fig. 22(a)–(b). The resonance component is suppressed when the active damping is enabled. On the other hand, the fifth harmonic present in the capacitor voltage is feedback through the active damping loop amplifying the effect of such harmonic in the grid current as illustrated in Fig. 22(c)–(d). A significant reduction from 13% to around 2.5% of the fifth harmonic on the grid current is reached [Fig. 22(e)–(f)] by adding

the fifth harmonic control loop. The grid current total harmonic distortion is reduced to 5.3%.

VII. Conclusion

This paper has proposed a control concept for mains connected inverters applications that combines a DHC with VF and power estimation methods so that the advantages of a fast dynamic response and relatively simple implementation are maintained. The interference between phases for three-phase, three-wire inverters using conventional hysteresis control is avoided when DHC is used. By using a varying hysteresis band the switching frequency can be made almost constant. Both control strategies, VF–CHC, and VF–DHC, have been verified through simulation and experimental implementation.

An active damping, harmonic control, and PLL have been incorporated in the proposed concept in order to extend the method for high power applications, where usually a third-order filter is used as output filter. The performance of the extended method under several conditions such as unbalanced supply voltage and harmonic component superposing the grid voltage were also experimentally verified.

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