Balancing Circuit for a 5kV/50ns Pulsed Power Switch Based on SiC-JFET Super Cascode

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***Abstract*—In many pulse power applications there is a trend to modulators based on semiconductor technology. For these modulators high voltage and high current semiconductor switches are required in order to achieve a high pulsed power. Therefore, often high power IGBT modules or IGCT devices are used.**

Since these devices are based on bipolar technology the switching speed is limited and the switching losses are higher. In contrast to bipolar devices unipolar ones (e.g. SiC JFETs) basically offer a better switching performance. Moreover, these devices enable high blocking voltages in case wide band gap materials as for example SiC are used. At the moment SiC JFET devices with a blocking voltage of 1.2kV per JFET are available.

Alternatively, the operating voltage could be increased by connecting N JFETs and a low voltage MOSFET in series resulting in a Super Cascode switch with a blocking voltage N-times higher than the blocking voltage of a single JFET. For the Super Cascode auxiliary elements are required for achieving a statically and dynamically balanced voltage distribution in the Cascode. In this paper a new balancing circuit, which results in faster switching transients and higher possible operating pulse currents is presented and validated by measurement results.

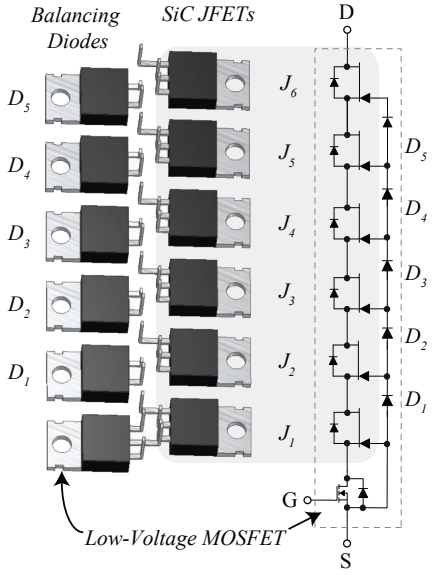

Fig. 1: Schematic of a Super Cascode consisting of 6 series connected SiC JFETs and a silicon low voltage MOSFET.

I. Introduction

In many pulse power applications such as accelerators, medical systems, or radar systems there is a general trend towards solid state modulators based on semiconductor technology, as these offer adjustable pulse parameters, turn off capabilities in case of failure and lower maintenance effort. There, high voltage, high current and fast semiconductor switches are required in order to achieve a high pulsed power and fast transients. Therefore, often high power IGBT modules or IGCT devices are used.

Since these devices are based on bipolar technology, the switching speed is limited and the switching losses are higher (e.g. due to the tail current), what could limit the pulse repetition rate and the converter efficiency and what increases the costs for cooling. Part of the switching speed limitation is caused by the parasitic elements of the power module packaging as has been shown in [1], [2]. There, standard 4.5kV IGBT chips for traction applications are mounted in a special low inductive housing, which allows significantly faster switching transitions than possible with standard high power modules.

In contrast to bipolar devices, unipolar ones (e.g. SiC JFETs) basically offer a much better switching performance since these utilise only majority carriers for conduction. In case wide band gap materials as e.g. SiC or GAN are used, these devices enable also a high blocking voltages. At the moment, normally on as well as normally off SiC JFETs with a blocking voltage of 1.2kV [4]–[6] and first test samples of 6.5kV devices are available.

In order to increase the blocking voltage capability the JFETs either can be connected in series, what requires either an active and/or passive control of the voltage distribution. Alternatively, a Super Cascode where JFETs are cascaded and connected in series with a low voltage MOSFET [7] could be used. The Super Cascode has the advantage of a simple control and very fast switching transients, but requires auxiliary elements for static and dynamic balancing of the voltage distribution.

In [3], [8] a first auxiliary circuit has been proposed and first results for the switching behaviour with resistive load have been presented. However, the turn on changed

from a very fast transient at the beginning to a kind of RC behaviour resulting in a slower turn on transient. Therefore, in this paper a new balancing network of the Super Cascode is presented, which allows a turn on exceeding a dv/dt of 100kV/μs and a 90% to 10% rise time below 50ns. First, the basic operation principle is explained shortly in **Section** II-A and then the auxiliary elements required for static and dynamic balancing are presented in **Section** II-B and **Section** II-C.

With the new balancing network, the transient voltage distribution is significantly improved compared to the previous balancing network. For validating the proposed circuit, measurement results are presented in **Section** III.

II. SiC JFET Super Cascode

For increasing the blocking voltage capability of a semiconductor switch, a series connection of the devices could be used. With a series connection, however, the voltage distribution must be either controlled actively and/or by passive snubber elements. The active control requires a large number of fast gate drives and measurement systems and with the passive snubber elements the overall switching losses are increased.

An alternative concept, which has just 1 control input/gate, is the JFET Super Cascode [7], which consists of a low voltage silicon MOSFET and series connected normally on JFETs as shown in Fig. 1. There, six 1.2kV SiC JFETs and a low voltage silicon MOSFET are utilised, what results in a total blocking voltage of 7.2kV. Due to the limited die size the current rating of the SiC-JFETs is limited to 5A for continuous operation at the moment, but will soon increase to 20A and more as announced by SiCED [5].

The key element for balancing the voltage distribution of the series connected JFETs are 5 low power avalanche rated Si-diodes [7] with an avalanche voltage of approximately 800V. For a reliable operation under static and transient conditions, however, additional elements are required as will be discussed in the following sections by enhancing the Super Cascode of Fig. 1 step by step after the basic operating principle is shortly explained.

A. Basic Operation Principle

The Super Cascode in Fig. 1 is controlled only via the gate of the low voltage MOSFET and for turning the switch on, a positive gate voltage is applied to this gate. With a turned on MOSFET also the bottom JFET J_1 (cf. Fig. 1) is conducting, since its gate is connected to its source via the MOSFET, i.e. $V_{gs,J_1} = 0$, and the JFET is a normally on device. Also the second JFET J_2 is conducting since the potential of the cathode of D_1, which is connected to the gate of J_2, could not be lower than the forward voltage drop V_F of D_1 with respect to the anode and the source of J_2 is connected to the anode of diode D_1 via the turned on J_1 and the MOSFET. Consequently, the gate voltage of J_2 must be higher than -V_F, which is above the threshold voltage of J_2 ($V_{th} \approx -20V$), so that J_2 is definitely turned on, assuming a zero voltage drop across J_1 and the MOSFET.

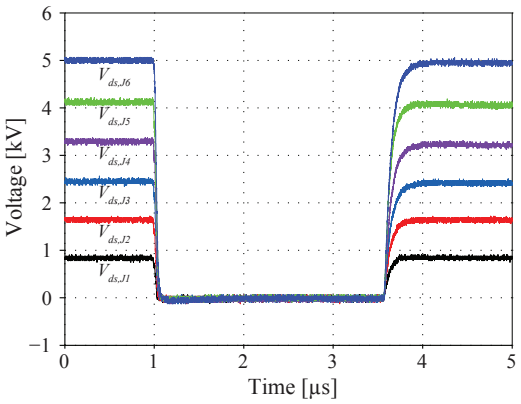

Fig. 2: Voltage distribution across the JFETs of the Super Cascode caused by the avalanche voltage of the gate diodes.

In the real circuit, the gate voltage of J_2 is in between $-V_F$ and V_{F,J_G}, which is the forward voltage of the gate diode of the JFET, depending on the leakage current distribution in the JFETs and diodes. In order to reduce the dependency of the gate voltage on the leakage currents additional elements are needed as discussed in the next section.

The gate of the third JFET J_3 is connected via D_1 and D_2 to the source of the MOSFET, so the lower limit of the gate voltage is given by $2 \times V_F$ and the upper limit by the forward voltage of the gate diode V_{F,J_G} assuming again that there is no voltage drop across the MOSFET, J_1 and J_2. Similar considerations can be performed for the upper JFETs.

For turning the cascaded switch off, first the MOSFET is turned off via its gate and the drain-source voltage of the MOSFET rises until the pinch-off voltage of J_1 is reached. Then, J_1 turns off and blocks the rising drain source voltage of the Super Cascode until the avalanche voltage of diode D_1 is reached. Due to the avalanche of diode D_1, the potential of the gate of J_2 is fixed with respect to the source of the Super Cascode and does not rise any more. However, the potential of the source of J_2 continues to rise with the increasing drain-source voltage of J_1, so that the gate source voltage of J_2 becomes negative and turns off as soon as its pinch-off voltage is reached. This sequential turn off, which could be seen in Fig. 2, continues with the next JFETs until the blocking voltage is reached.

B. Static Off Behaviour

After the sequential turn off the static voltage distribution in the off-state (cf. Fig. 2) is mainly determined by the avalanche voltage of diodes $D_1 \dots D_5$. For a controlled and stable avalanche, i.e. for a controlled static voltage

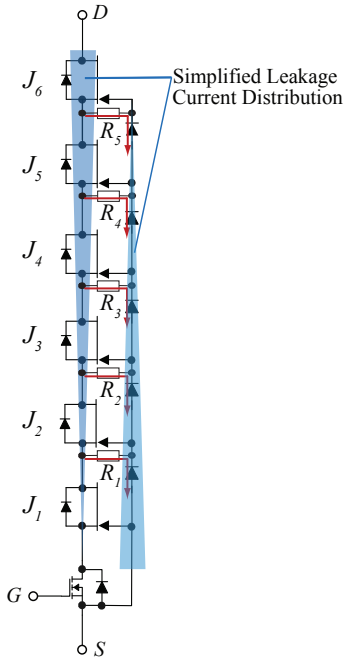

Fig. 3: Leakage current distribution in the SiC Super Cascode with additional balancing resistors for static off behaviour.

distribution, a certain leakage current through the diodes is required [7]. In order to guarantee this leakage current independently of the JFET parameters, resistors must be connected between the gate and the source of the upper JFETs as shown in Fig. 3. With the resistors, the leakage current is mainly defined by the resistance value and the JFET's pinch off voltage, which is equal to the voltage drop across the resistor in the off-state [8].

By inserting the resistor also a kind of control loop of the voltage distribution in the off-state is initiated (cf. Fig. 3): In case for example J_2 tends to turn off a bit more, i.e. increasing its drain-source voltage and/or resistance, the leakage current through J_2 would decrease. With the reduced leakage current through J_2 also the current through resistor R_1, which flows via the voltage balancing diodes to ground, would decrease if it is assumed that the leakage current through J_1 is constant. This results in a reduced voltage drop across resistor R_1. Consequently, the gate-source voltage of J_2 decreases, so that J_2 is turning on a bit, which increases the leakage current through J_2 and stabilises the gate-source voltage as well as the drain-source voltage of J_2. This control mechanism leads to a stable leakage current through the resistors and the diodes, so that the voltage sharing between the devices is stabilised by the avalanche voltage of the diodes, which determine the gate potentials of the JFETs.

The leakage current for the lower JFETs flows via the upper JFETs, so that the current in the JFETs decreases from the upper to the lower one and the current in the voltage balancing diodes increases from the upper to the lower one as symbolised by the triangular arrows in Fig. 3. Additionally, with the resistors an operation could be achieved, where the lowest diode reaches its avalanche voltage first and therefore the blocking voltage is built up from the lower to the upper JFET, since the lower diode must always conduct the leakage current of the upper ones. This also stabilises the turn off switching transition.

C. Transient Behaviour

In **Section** II-A about the basic operation principle a sequential turn on process of the JFETs in the Super Cascode has been described. Such a sequential turn on could result in overvoltages of the upper JFETs, especially for example in case of a hard commutation of a diode in a bridge leg. There, first the current must be commutated from the diode to the Super Cascode before the voltage could decrease, so that in a sequential turn on, the most upper JFET would have to take the full blocking voltage for a short period of time. In order to avoid the overvoltages and achieve a synchronisation of the JFETs during the switching transients, capacitors $C_{D,1} \dots C_{D,5}$ and resistors $R_{D,1} \dots R_{D,5}$ are added as shown in Fig. 4.

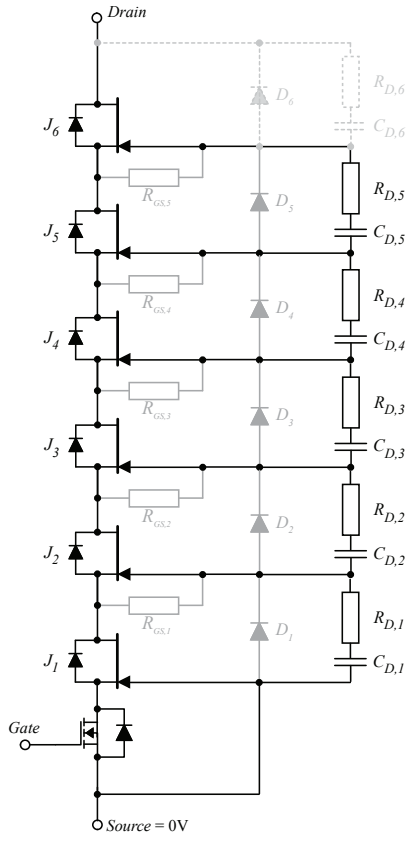

Fig. 4: Auxiliary resistors $R_{D,1} \dots R_{D,6}$ and capacitors $C_{D,1} \dots C_{D,6}$ for dynamically balancing the voltage distribution of the JFETs.

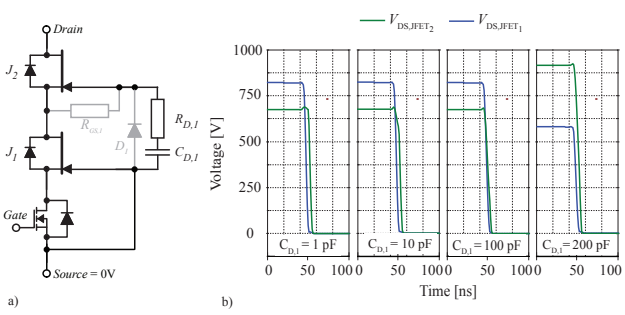

Fig. 5: Drain-source voltages b) of the JFETs in a Super Cascode a) consisting of 2 JFETs for different values of the auxiliary capacitors $C_{D,1}$ ranging from 10pF to 200pF ($R_{D,1}$=50Ω, $R_{GS,1}$=240kΩ, V_{DC}=1.5kV). With $C_{D,1} \geq$ 100pF the both JFETs turn at the same time as could be seen in b).

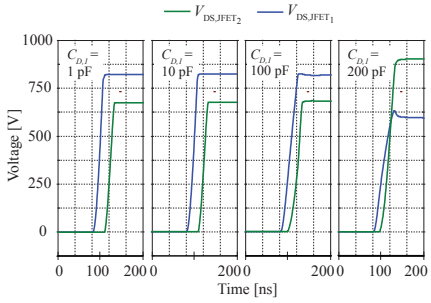

Fig. 6: Drain-source voltages of the JFETs in a Super Cascode consisting of 2 JFETs for different values of the auxiliary capacitors $C_{D,1}$ and $C_{D,2}$ ranging from 10pF to 200pF ($R_{D,1}$=50Ω, $R_{GS,1}$=240kΩ, V_{DC}=1.5kV). With increasing $C_{D,\nu}$ first the turn off becomes more synchronously and then J_2 tends to take a much large share of the voltage than J_1.

Starting in the off state and assuming a relatively small resistance value for $R_{D,1} \ldots R_{D,5}$ as well as that capacitors $C_{D,1} \ldots C_{D,5}$ are equally charged up, the MOSFET is turned on by a positive gate voltage. As described earlier, the potential of the source of J_1 and the gate voltage of J_1 is decreasing, so that J_1 starts to conduct when the gate voltage is close enough to 0V. As soon as J_1 starts to conduct, the potential of the source of J_2 decreases. However, due to capacitor $C_{D,1}$, the potential of the gate of J_2 is fixed for a limited time, so that the gate voltage of J_2 starts to increase as soon as the potential of the source starts to decrease. This means that J_2 starts to turn on as soon as J_1 is turning on, resulting in a synchronous switching of both JFETs. Analogue considerations can be performed for the upper JFETs.

In Fig. 5 a simulation of the drain source voltages of a Super Cascode consisting of 1 MOSFET and 2 JFETs for different values of capacitor $C_{D,1}$ ranging from 10pF to 200pF are shown. There, it could be seen that with increasing capacitance value, both JFETs tend to turn on more synchronously. The resistor $R_{D,1}$ in series to $C_{D,1}$ is added for damping oscillations during the switching transients.

Looking at Fig. 5 it seems that a larger capacitance value for $C_{D,\nu}$ results in more synchronous switching transients. However, at turn off a too large value for $C_{D,\nu}$ results in an asynchron switching operation and an unbalanced voltage distribution as could be seen in Fig. 6. The reason for this is that at the beginning of the turn off the capacitors are discharged, so that they hold the gate potential of J_2 down. When J_1 now starts to turn off, the gate voltage of J_2 immediately becomes negative and turns off J_2 faster than J_1, so that J_2 is blocking the largest share of the voltage.

The parasitic capacitances of the balancing diodes $D_1 \ldots D_5$ have a similar influence on the switching transients as capacitors $C_{D,1} \ldots C_{D,5}$. However, the value of the capacitance changes with the voltage across the diode and it is the smallest, when the diode is in avalanche. Thus, the effect on turn on is much smaller (where a large capacitance value is advantageous) than the effect on turn off, where the capacitance value is maximal, but a small capacitance would be good. Therefore, it is difficult to achieve an optimal transient performance just with the parasitic capacitance of the diodes and adding $C_{D,1} \ldots C_{D,5}$ as well as $R_{D,1} \ldots R_{D,5}$ is proposed in order to fully utilise the performance of the JFETs. For achieving an optimal transient behaviour, i.e. fast and synchronous turn on and off, a tuning of the capacitors/resistors is required. This results in decreasing capacitance values from $C_{D,1}$ to $C_{D,5}$ as also the leakage current is smaller for the upper JFETs.

In order to make the Super Cascode more robust against tolerances, diode D_6 and/or capacitor $C_{D,6}$ and resistor $R_{D,6}$ as shown grey shaded in Fig. 4 can be added. The upper capacitor $C_{D,6}$ mainly leads to a more balanced voltage distribution for capacitors $C_{D,1}$ to $C_{D,5}$ as the circuit acts as dynamic voltage divider. With diode D_6 a similar stabilisation could be achieved, but also the maximal blocking voltage of the Super Cascode is fixed to $6 \times V_{Avalanche}$.

III. Measurement Results

For investigating the switching behaviour of the Super Cascode in detail, a half bridge with two switches consisting of a MOSFET and 6 cascaded SiC JFETs as shown in the schematic Fig. 7 has been designed (cf. Fig. 8). In the following shortly the test platform and the utilised components and then the measurement results are discussed.

A. Testplatform

For the gate drive of the Super Cascode, a standard 9A gate driver from IXYS is used to drive the MOSFET with a gate voltage of +12V/-12V. The gate signal is transferred via fibre optics and the gate power via a small

HV transformer. For minimising the stray inductance of the setup ceramic capacitors mounted closely to the JFETs are applied besides the film capacitors. The load consisted of 8 series connected pulse resistors made by Vishay.

For the voltage balancing diodes, which require a stable avalanche voltage in order to guarantee a well defined static and dynamic voltage distribution of the Super Cascode, a series connection of 3 fast recovery rectifier diodes BZT03C270 made by Vishay are used. These diodes show a stable avalanche behaviour at 270 kV. In oder to simplify the design a single diode with an avalanche voltage of $\approx$ 0.8 kV would be required, but unfortunately such devices were not available. Moreover, one has to consider, that the parasitic capacitance of the single diode would be higher than the one of the series connection.

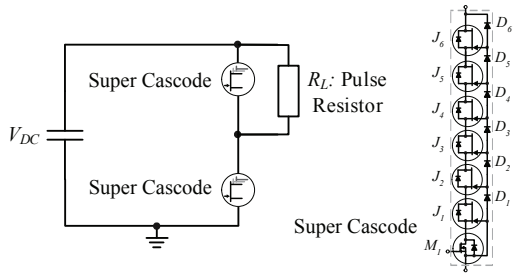

Fig. 7: Schematic of the measurement setup for the SiC Super Cascode, where the auxiliary components are not shown for sake of simplicity.

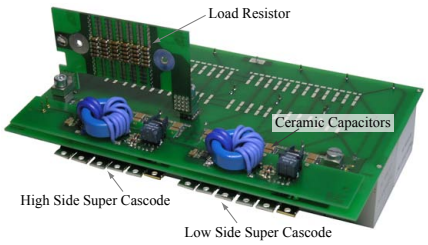

Fig. 8: Photo of the measurement setup for the SiC Super Cascode. (Size: 155mm×170mm×50mm / Load: 90mm×50mm×5mm)

TABLE I: Components and system parameters of the test bench for the Super Cascode with a DC link voltage of 5kV.

SiC JFETs	1.2kV / 5A (TO220/SiCED)
Si-MOSFET	IRLR024N / 55V (D^2-Pak)
Balancing Diodes	3×BZT03C270 / 3×270V
Load Resistors	CMB0207 100Ω (Vishay)
DC-Link capacitor	ICEL 8μF/800V_{DC} (7×2) Syfer 500V/560nF/X7R (12×2)
DC-Link Voltage	5000V
Gate Driver	IXYS IXDI 9A / 35V
Pulsed Power	5kV × 6A = 30kW

B. Measurements

With the test benches for the Super Cascode measurements of the switch voltage and the load current for a purely resistive load have been performed. The maximal load current for the Super Cascode is limited to approximately 6A due to the relatively small chips, which are available at the moment, and due to the unipolar device characteristic. This characteristic leads to a pinch off of the conducting channel as known from the MOSFET, if the

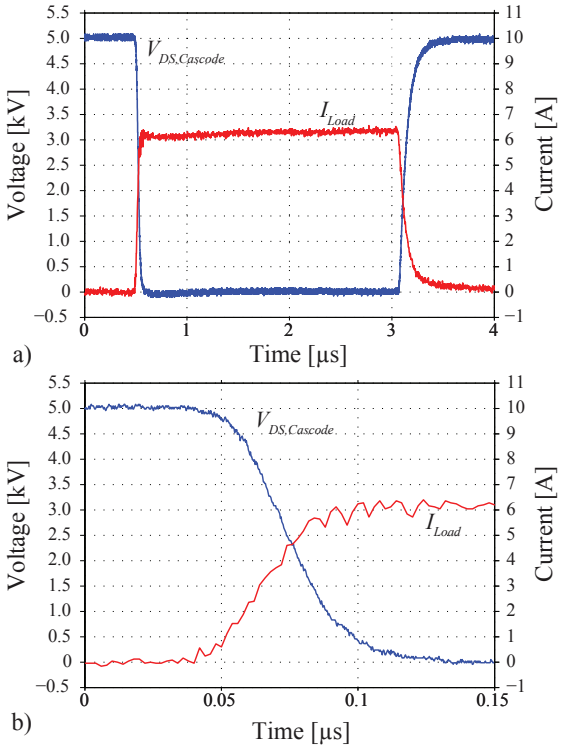

Fig. 9: a) Measurement results for the Super Cascode with a gate voltage of 12V and 800Ω purely resistive load. b) Zoomed view around turn on.

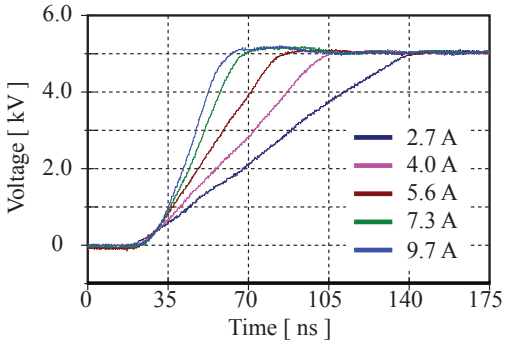

Fig. 10: Rising edge of the voltage pulse during turn off of the Super Cascode for different load currents from 2.7A to 9.7A and inductive load.

current is too high.

The results for the Super Cascode are shown in Fig. 9, where it could be seen, that the 90%-10% rise time of the voltage is significantly smaller than 50ns. The fall time is also in the range of 100ns, but depending significantly on the load current as shown in Fig. 10, since the cascode turns off very fast and then the dv/dt is only determined by the output capacitance and the load current charging the capacitor.

IV. Conclusion

In this paper the basic operating principle of a Super Cascode based on 1.2kV SiC JFETs and a low voltage Si-MOSFET is presented. There, also the requirement for additional gate-source resistors/capacitors for guaranteeing a stable static voltage distribution and damping internal oscillations is explained. Furthermore, a R-C network for improving the dynamic behaviour and the voltage balancing of the Super Cascode are presented.

For evaluating the switching performance of the Super Cascode measurements for resistive load with a pulse voltage of 5kV and a load current of 6A have been performed. The rise time of the switch voltage is significantly below 50ns, what is very fast. The falling edge of the output pulse is also in the range of 100ns, but depends significantly on the load current/load resistor, which charges the output capacitor of the Super Cascode.

Acknowledgment

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