Advanced Setup for Thermal Cycling of Power Modules following Definable Junction Temperature Profiles

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***Abstract*-- In this paper a setup for performing power cycling tests of IGBT modules for the purpose of reliability analysis is presented. The main purpose of the setup is to provide experimental data for the parameterization and verification of a newly developed physical model of solder deformation leading to the failure of power electronic devices. The design procedure, including considerations of reliability, measurement, and cooling, for a 5 kW flexible power cycling system is presented. Experimental results of a sub-1 kW prototype setup are shown, demonstrating the ability of the system to force the junction temperature of the device under test to follow an arbitrary temperature profile.**

***Index Terms*-- power cycling tests, reliability, test system.**

I. INTRODUCTION

Manufacturers seek to estimate the lifetime of their power electronic modules and the conditions under which they fail. Such lifetime estimation and reliability testing is usually done through accelerated power cycling tests [1-6]. By submitting a device to repeated current load cycles, a junction temperature swing ΔT_j is induced, creating a corresponding temperature cycle. The device is composed of several layers of different materials with differing coefficients of thermal expansion. This causes power modules to experience shear stresses within their composition, causing deformations and eventually leading to device failure, such as cracking of a solder layer [7]. The key output of all power cycling tests is the number of cycles to failure, N_f, which is then used in models for lifetime estimation.

Analytical models for lifetime estimation, in which N_f and other power cycle parameters are fitted to a function of choice, are widespread, most notably the Coffin-Manson model [8]. A major drawback of this model is that it considers only the parameters N_f, ΔT_j, and the maximum junction temperature T_{jmax}, whereas it has been proven that other factors (e.g. power cycle frequency) also affect lifetime significantly. This can lead to errors as high as a factor of 12 when the Coffin-Manson model is used to calculate lifetime [2]. Other models [9-10] have been developed but have their own deficiencies [11]. Therefore a new physical model [11-12] describing the deformation mechanisms due to temperature stresses based on [13-14] has been developed that takes into account the effect of elastic strain, plastic strain, and creep occurring in the solder layer of a power semiconductor module. All three components have an effect on device lifetime, but how much of each deformation type occurs is strongly dependent on the characteristics of the temperature profile the device is submitted to [11-12]. For example, the longer the dwell time of the device at a certain temperature, the more creep occurs, while during fast temperature changes, more inelastic and plastic strain occurs. Thus in order to correctly parameterize and robustly verify this model, a power cycling test setup that is able to produce precisely defined temperature cycles is required.

The issue of designing and building power cycling test setups is not discussed in great detail in existing literature. The proliferation of the Coffin-Manson model has led to the use of relatively simple setups [3-5] designed simply to produce a certain ΔT_j and T_{jmax}. A typical circuit is given in Fig. 1. Such circuits often have 50% load current duty ratios, designed to cycle two sets of devices intermittently with a constant input current, or are designed to simply load the device with various current pulses [15-17]. Such configurations are not suitable for the creation of power cycles required for the parameterization and verification of the model of [11-12].

A suitable reliability testing setup is the topic of this paper. **Section 2** discusses in more detail the requirements for such a system and explores two possible converter topologies for its realization. Measurement and cooling are also discussed. **Section 3** presents experimental results of a prototype power cycling setup based on the considerations of the previous Section. The ability to produce arbitrary temperature profiles is demonstrated. **Section 4** presents conclusions.

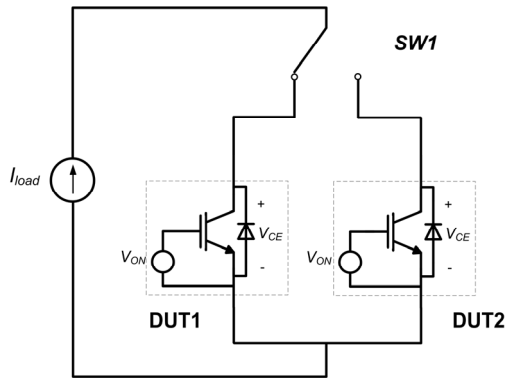

Fig. 1 – A typical power cycling circuit used for reliability testing. A constant load current is switched between two devices under test (DUTs). Each DUT is loaded equally, i.e. *SW1* is operated with a 50% duty ratio.

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II. Power Cycling System Design

The number of cycles to failure due to solder degradation N_f is defined as the number of cycles after which the junction-to-case thermal resistance, $R_{th,j\text{-}c}$, rises to 20% above its initial value [1-2]. The resistance is defined as

$$R_{th,j-c} = \frac{T_j - T_c}{P} \quad (1)$$

where P is the electrical power dissipated, T_j the device junction temperature, and T_c the case temperature. According to the model of [11-12], the lifetime of an IGBT will depend on the junction temperature swing ΔT_j, power cycle frequency, and the rate of change of T_j, i.e. its slope. Therefore the basic requirement of the power cycling system is the ability to produce a T_j profile i.e. waveform for which the aforementioned parameters can be precisely specified.

The model of [11-12] has two parameters which are module-dependent and must be determined on the basis of cycling tests. Temperature cycles used for parameterization should ideally cause all types of possible deformations, so that the parameterized model best reflects the underlying physical reality of the solder layer. With the model unparameterized, it is not possible to specify exactly where the transition, in terms of thermal cycle characteristics, between one type of deformation to another is. Therefore the setup must be designed to be as flexible as possible, producing temperature changes in the range of tens of degrees per second down to fractions of degrees per second, as well as constant high temperatures. As far as cycle frequency is concerned, temperature cycles used for exploring solder layer degradation and failure typically have periods on the minute timescale [18]. Shorter cycles – on the second timescale – are generally used for stressing chip bond wires [18], which are not the subject of the mentioned model [12]. Generally the larger the ΔT_j, the shorter the test. Typically, for the device to fail within several weeks to one year, ΔT_j should be 50-80°C [2], [18]. The maximum allowable junction temperature T_{jmax} and the maximum load current are defined by the ratings of the device under test; otherwise the device will be outside of its safe operating area. Operating up to T_{jmax} shortens the device lifetime [19] and thus the test.

A. Measurements

The power dissipated through the device P can be easily obtained from measurements of the load current I and the IGBT collector-emitter voltage V_{ce}. The case temperature T_c can be measured via a thermal sensor i.e. thermocouple glued to the base plate of the device under test (DUT). There are several methods of measuring the junction temperature T_j. If a closed, off-the-shelf module is used as a DUT, the only way to measure T_j is via the measurement of thermo-sensitive parameters, such as V_{ce} [1]. In the case an open module (with accessible die) can be obtained, T_j can be determined via the measurement of the chip surface temperature, for which there are several methods [20]. The most accurate results are achieved with a high resolution infrared camera [20], with measurement samples less than 2 ms apart. However such a fine resolution is not required, since as noted the temperature cycles are on the seconds and minutes timescale. Lower cost alternatives are infrared sensors and thermocouples, with time constants of 50 ms and 200 ms, respectively [20], being therefore fast enough for measuring the required temperature cycles. At the required timescale both produce measurements in good agreement with the infrared camera [20].

The junction temperature can be approximated as the surface temperature of the device centre point [21]. It should be noted of course that there exists a certain temperature gradient across the active chip area as noted in [22-23], where it is shown that a more precise method of T_j determination would be to take a current- or area-weighted average of the chip surface temperature. In the aforementioned studies it was found that such a value corresponds well to temperatures determined from simulation and from the V_{ce} method, while the chip centre was found to be approximately 10% hotter. This suggests that measurements of the chip centre temperature should be reduced by this fraction to arrive at the actual T_j.

B. Converter Configuration

In order to achieve maximum flexibility in terms of temperature profile characteristics, the power cycling setup should be able to deliver the maximum rated current of the DUT. In this paper, the DUT is a 3300 V, 1200 A IGBT with a typical saturation collector-emitter voltage of 3.85 V at T_{jmax}, giving a dissipated power of 4.6 kW at full load. Hence the maximum output rating for the power cycling setup is set to be 5 kW. At this power level a three phase supply must be used, and therefore the voltage needs to be stepped down. Two approaches are

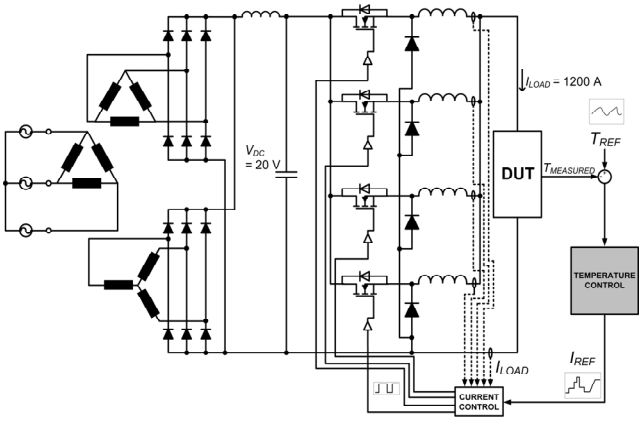


Fig. 2 – Topology I: Low frequency transformer power cycling setup.

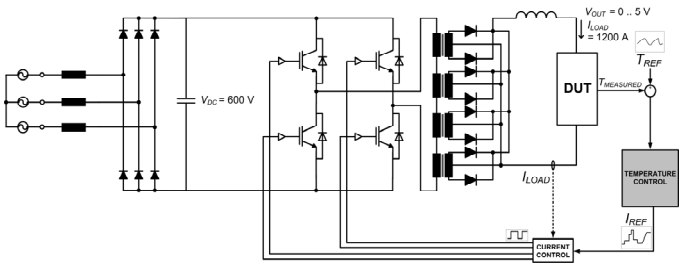


Fig. 3 – Topology II: High frequency transformer power cycling setup.

possible – a low frequency transformer solution and high-frequency transformer solution.

The low-frequency solution, Topology I, is given in Fig. 2. It consists of a 50 Hz 12-pulse transformer and rectifiers followed by a multiphase buck converter with an input voltage of 20 V. Due to the low voltage, power MOSFETs are used. At full load each of the phases carries 300 A.

The high-frequency solution, Topology II, is given in Fig. 3. It consists of a 3-phase rectifier followed by an isolated full-bridge converter with an input voltage of 600 V. IGBTs are used for the full bridge. There are four secondary windings i.e. phases, again each carrying 300 A at full load. Topology II is more compact than Topology I but the transformer design is more challenging to realize.

In both approaches, a sensor measures the current I_{LOAD} through the DUT. A current controller regulates the load current so that it is equal to the reference current I_{REF}. The DUT junction temperature T_j is measured and sent to the temperature controller which calculates the I_{REF} required in order to match T_j to the reference temperature T_{REF}, i.e. a temperature feedback control loop is established. T_{REF} is a desired time-varying temperature profile which the DUT junction temperature follows.

C. Test Setup Reliability

The cycling test setup obviously must not fail itself prior to the DUT failing, and it must be reliable enough to perform several cycling tests. To ensure this and to compare Topology I to Topology II in terms of reliability, each is analyzed using the well-known procedure of MIL-HDBK-217F [19]. The Mean Time Between Failures (MTBF) of a system is defined as

$$MTBF = \frac{1}{\sum \lambda_i} \quad (2)$$

where λ_i is the failure rate of component i and is defined as

$$\lambda_i = \lambda_b \pi_T \pi_A \pi_S \pi_Q \pi_E \quad (3)$$

where λ_b is the base component failure rate given in MIL-HDBK-217F, and the remaining terms are scaling factors accounting for junction temperature (π_T), type of application including power rating (π_A), voltage stress i.e. derating (π_S= 1.0 denotes operation at max. rated voltage), part quality (π_Q) and operating environment (π_E). It should be noted that not all scaling factors are given for each component; for example, no π_S is given for MOSFETs, while no π_A is given for diodes. Since the control, measurement, and data storage components are essentially the same in both topologies, only the power circuit itself is analyzed. As magnetic components are generally very reliable and have failure rates an order of magnitude lower than that of the power switches [24], the inductors and transformers are also not considered in the analysis. The same can be done for capacitors if film capacitors, with much lower failure rates than both switches and electrolytic capacitors [19], are used; hence for the comparison only the MTBF of the MOSFETs, IGBTs, and diodes is considered.

To improve reliability, the power components are all derated. For Topology I, 100 V, 1220 A MOSFETs (IXYS VMO 1200-01F) and 45 V, 400 A diodes (Vishay 400CNQ045P6F) are used for both the converter and rectifier. For Topology II, the same 400 A diodes are used for the secondary side of the converter, while 800 V, 20 A diodes are used for the rectifier, and 1700 V, 400 A IGBTs (Semikron SKM series) for the full-bridge. As IGBTs are not listed in MIL-HDBK-217F, the standard approach is to assume that the π factors listed in MIL-HDBK-217F for bipolar transistors are valid for IGBTs, with λ_b obtained from manufacturer warranty data [25]. When this data is not available, another approach is to use the base failure rate given in MIL-HDBK-217F for MOSFETs [26], and this is the approach taken here.

TABLE I
FAILURE RATE AND MTBF ANALYSIS OF TOPOLOGY I

Failure rate λ (failures/10^6 hours)	
MOSFET	0.9504
Diode (buck converter)	0.0383
Single converter phase	0.9887
MTBF (years)	
4 phases and rectifier (full system)	27.67

TABLE II
FAILURE RATE AND MTBF ANALYSIS OF TOPOLOGY II

Failure rate λ (failures/10^6 hours)	
IGBT (derated 65%)	0.2265
IGBT (derated 50%)	0.2973
IGBT (no derating)	1.4156
Diode (secondary side)	0.0071
Full-bridge converter (derated 65%)	0.9623
Full-bridge converter (derated 50%)	1.2462
Full-bridge converter (no derating)	5.7193
MTBF (years) – converter and rectifier (full system)	
IGBTs derated 65%	111.56
IGBTs derated 50%	87.84
IGBTs not derated	20.16

For a worst-case analysis, all component factors are considered for peak load. All peak junction temperatures for the devices were selected to be the minimum achievable with air-cooling at this load, and were well below their rated maximum.

Results for Topology I are given in Table I. Results for Topology II are given in Table II. The first conclusion is that both setups have high enough MTBFs, over 20 years, to be suitable for power cycling applications, where the longest test typically takes 1-2 years. Second, it would appear that the whole of Topology II is much more reliable than just one phase of Topology I. However it must be taken into account that MIL-HDBK-217F provides no derating factor for MOSFETs, while giving one for bipolar transistors. As IGBTs can operate at very high voltages, it is easy to derate the IGBTs of Topology II – as long as switching frequency requirements can be met – until a desired MTBF is achieved; however it is not clear if this then results in a fair comparison with the MOSFETs

of Topology I. For this reason Table II shows also the results of the reliability analysis if 1200 V (50% derating) and 600 V (no derating) IGBTs are used. As can be seen, when the derating factor is eliminated, Topology I has a higher MTBF. Furthermore, the MIL-HDBK-217F approach ignores the effect of junction temperature swings and the converter switching losses. Therefore, while the MTBF analysis shows that either topology is reliable enough to be used, its results cannot really be used to judge which one is the better choice.

Another factor to consider is redundancy i.e. the ability of the system to continue functioning if a component fails. The phases of Topology I are derated enough to allow the system to function at full load with only 3 phases, so redundancy can be easily built into Topology I by adding output ORing i.e. isolation diodes [27] after the inductor in each phase. Furthermore by adding extra phases, additional redundancy can be achieved. On the other hand Topology II fails entirely if one IGBT fails, and to add redundancy the entire full bridge must be replicated. Further redundancy can be achieved with Topology I by using several separate controllers, e.g one for two of the phases and another for the remaining two phases. For these reasons, and due to simpler transformer design, the low-frequency Topology I is selected for the power cycling system.

D. Temperature Controller

In order to design the temperature controller which completes the feedback loop in Fig. 2 and 3, the DUT's thermal characteristics must be known. Data sheets of power devices typically state the junction-to-case thermal resistance $R_{th,j\text{-}c}$ and the case-to-heat sink thermal resistance $R_{th,c\text{-}h}$. Often thermal impedance curves are also given, so the thermal characteristic of an IGBT for example can be represented as a thermal RC circuit, as seen in Fig. 4. Sometimes the values of the elements are given directly in the datasheet, which is the case for the DUT used in this paper. Otherwise, if the structure of the device is known, this thermal RC network can be derived from 3D-FEM simulations or by using the finite-difference method [28]. The DUT is placed on a heat sink, so this must also be characterized. The thermal resistance of an air-cooled heat sink $R_{th,HS}$ is typically given in datasheets, and it can also be derived from 3D simulations or from analytical expressions [29]. The thermal capacitance $C_{th,HS}$ of the heat sink can be roughly calculated knowing the density ρ and specific heat capacity C_p of the heat sink material and the sink's dimensions i.e. volume V, as shown by (4). Then the thermal time constant of the heat sink τ_{HS} can be calculated as in (5).

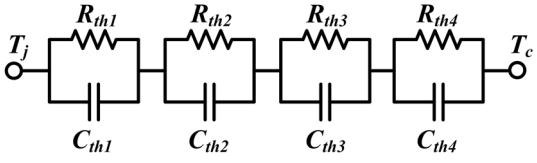


Fig. 4 – Thermal RC network of an IGBT module representing its transient thermal behaviour. $R_{th1} + Rt_{h2} + R_{th3} + R_{th4} = R_{th,j\text{-}c.}$

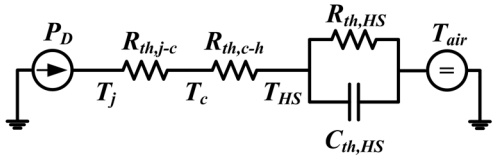


Fig. 5 – Simplified thermal network of the DUT and air-cooled heat sink, neglecting DUT capacitance. $R_{th,c\text{-}h}$ represents the resistance of the thermal grease or paste applied between the module and sink. P_D is the power dissipated in the DUT.

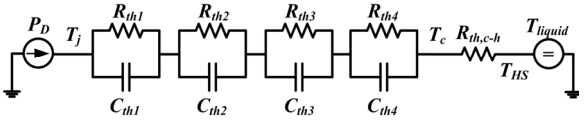


Fig. 6 – RC thermal network model for liquid cooling: DUT thermal network followed by the thermal grease resistance $R_{th,c\text{-}h}$ and a constant cold plate temperature.

$$C_{th,HS} = \rho C_p V \quad (4)$$

$$\tau_{HS} = C_{th,HS} R_{th,HS} \quad (5)$$

As the time constant of the heat sink is on the order of tens or hundreds of seconds, and as $C_{th,HS}$ is much larger than the capacitance of a power module, for air cooling the DUT capacitance can be ignored and the simple RC model of Fig. 5 used. Although representing the heat sink with a single resistor and capacitor is only a rough approximation, it was found to give results within 10-20% of those obtainable through 3D simulations. For liquid cooling, where the DUT is placed on a cold plate, it is assumed that the cold plate surface is kept at a constant temperature by the coolant. This results in the RC model of Fig. 6, where the DUT capacitance cannot be ignored as it is the dominant factor of the overall time constant.

Closed-loop temperature controllers have been developed previously [30-31]. In [30] the thermal characteristics of a device are modeled in a manner similar to that described here and included in the control loop in order to achieve over-temperature protection during converter operation. In [31] a PI controller for thermal cycling purposes was developed where the system was characterized experimentally using step response and a relatively simple cooling model. In this paper, with the system fully characterized electrically and thermally, a PI controller was designed in a manner similar to the approach of [30]. For verification, the full closed loop, electrical and thermal characteristics included, was modeled in the power electronics simulator GeckoCIRCUITS [32], which allows the coupling of circuit and thermal models.

To ensure reliability, precise timing, and to ease experimental tuning of the coefficients, the temperature controller should be implemented on a DSP board. DSP chips are extremely reliable [33] while industrial-grade DSP boards, with data acquisition circuitry included, having a MTBF of well over 100,000 hours can be constructed [34].

E. Cooling

The ability of the DUT junction temperature to follow a particular temperature profile is greatly influenced by the manner in which it is cooled. Air cooling is preferable, in order to avoid dealing with liquid, pumps,

pipes, requirements for the regulation of coolant flow, and so forth. High performance DC fans for heat sinks have lifetimes of e.g. 40,000 hours [35] (about four and a half years), enough to perform several cycling tests. However the time constant τ_{HS} of the heat sink limits the temperature cycle characteristics and therefore an air-cooled system must be analyzed to determine whether it is suitable for the parameterization of the model of [12].

To compare air and liquid cooling, the models of Figs. 5 and 6 are used. The ambient temperature of air is assumed to be 25°C. The temperature of the liquid coolant is assumed to be 40°C. The maximum junction temperature of the DUT is 125°C.

A low τ_{HS} is desired so that a wider range of temperature shapes and slopes is possible. Commercial air-cooled heat sinks [36] have time constants in the range of 100-200 seconds or more. To test the limits of air cooling, an optimization procedure [29] which produces the minimum-resistance design of a protruded fin heat sink for a given fan, was slightly modified to produce instead a heat sink with a minimum time constant: heat sink channel number and fin thickness was varied until a minimum τ_{HS} was arrived at. A heat sink with $R_{th,HS}$ = 0.048 K/W and τ_{HS} = 47 s resulted. For the DUT, $R_{th,j\text{-}c}$ = 0.0085 K/W and $R_{th,c\text{-}h}$ = 0.009 K/W. The heat sink dimensions are defined by the DUT baseplate area and fan size.

First, the air-cooled system was simulated with triangular temperature profiles with 25%, 50%, and 75% duty ratio, as shown in Fig. 7. The maximum achievable frequency f for a particular junction temperature swing ΔT_j is defined as the frequency at which the given amplitude can be achieved with a constant defined slope. The results for the three profiles for air cooling, as well as for the 50% duty cycle triangular profile for liquid cooling, are plotted in Fig. 8. Table III summarizes the data in terms of minimum cycle period and maximum temperature change rate i.e. slope dT/dt for the 25% and

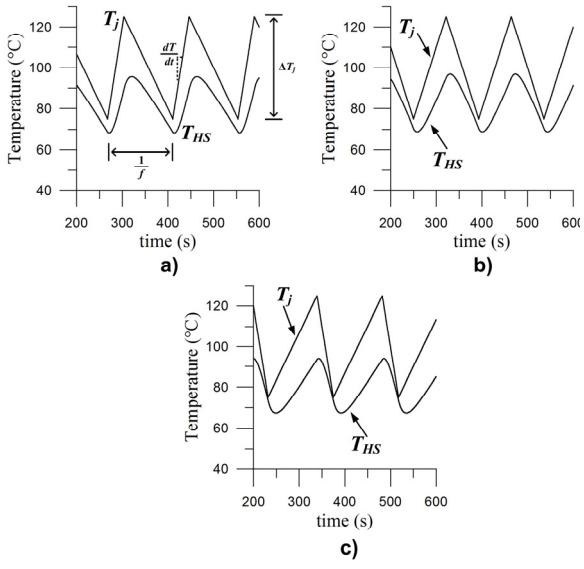


Fig. 7 – Simulated triangular profiles of the junction temperature T_j with a) 25% duty ratio b) 50% duty ratio and c) 75% duty ratio, also showing air-cooled heat sink surface temperature T_{HS}.

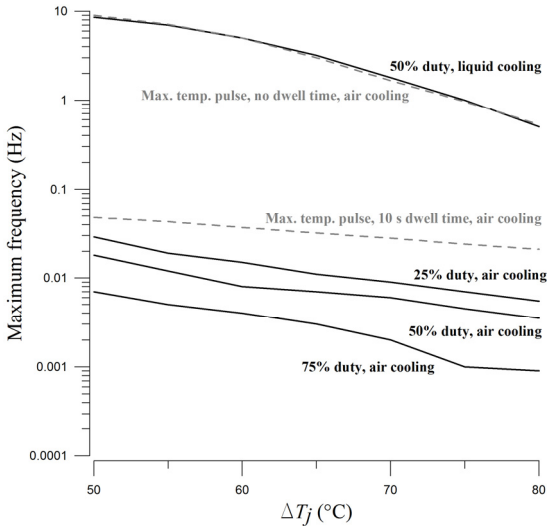


Fig. 8 – Maximum achievable temperature cycle frequency with air-cooling for a given junction temperature swing ΔT_j for air-cooling: triangular waveforms with 25%, 50%, 75% duty ratio; and for liquid cooling: triangular waveform with 50% duty ratio. Dashed lines show results for the non-triangular profiles of Fig. 9, where the heat sink has less time to heat up, allowing higher cycle frequencies.

TABLE III
MINIMUM ACHIEVABLE CYCLE PERIOD FOR A GIVEN ΔT_j FOR TRIANGULAR TEMPERATURE PROFILES

ΔT_j (°C)	Duty cycle	Min. period (s)	Max. pos. dT/dt (°C/s)	Max. neg. dT/dt (°C/s)
50	25%	34.5	5.8	1.93
	50%	55.6	1.8	
55	25%	52.6	4.2	1.39
	50%	83.3	1.32	
60	25%	66.7	3.6	1.2
	50%	125	0.96	
65	25%	90.9	2.86	0.95
	50%	143	0.91	
70	25%	111	2.52	0.84
	50%	167	0.84	
75	25%	143	2.1	0.7
	50%	222	0.675	
80	25%	182	1.76	0.59
	50%	286	0.56	

50% duty cycle profiles with air cooling. The maximum f for a certain ΔT_j can be thought of as the maximum frequency at which the temperature change rate can be freely controlled at that ΔT_j. As can be seen, the air-cooled heat sink limits the maximum cycle frequency to hundredths of a Hertz or less, i.e. periods ranging from tens to hundreds of seconds. With water cooling, where the DUT time constant is the limiting factor, much higher frequencies, from 0.5 to 8.5 Hz, can be achieved. As noted however for the testing of the solder layer cycles with periods in minutes are required, and the air cooled system can fulfil this requirement. The maximum achievable change rate with air cooling in these cycles is

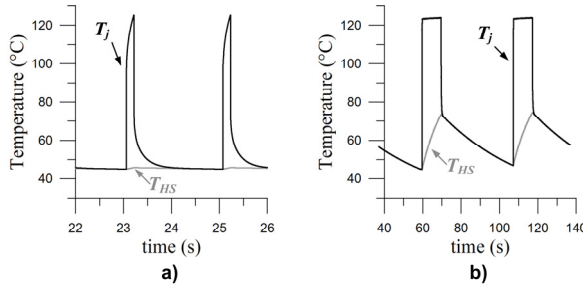


Fig. 9 – Simulated step profiles of the junction temperature T_j, also showing air-cooled heat sink surface temperature T_{HS}: a) turn off right after T_{jmax} b) 10 s of dwell time at T_{jmax}.

however at most several degrees per second, while it is as mentioned desirable to achieve rates of tens of degrees per second. This can be achieved with liquid cooling or by applying a different temperature profile to the air cooled system. First, a cycle was simulated where maximum current is applied to the DUT until it reaches 125°C, and then no current is applied until the DUT cools down by a certain ΔT_j. This is shown in Fig. 9(a), with the results summarized in Table IV. The DUT heats up quickly and the current is on for a very short time; the heat sink, with its large τ_{HS}, therefore has much less time to heat up than with the triangular cycles and the difference between the junction temperature and heat sink temperature is greater, allowing for faster cooling. With this cycle, much greater cycling frequencies can be obtained; more importantly, T_{jmax} is reached in less than one second, giving a very high temperature change rate. The drawback with this type of profile is that the change rate is not controlled precisely. For this reason another profile, shown in Fig. 9(b), was simulated, where the temperature change rate is partly controlled: maximum current is applied to quickly reach T_{jmax}, and then the temperature is maintained at T_{jmax} for 10 seconds. This cycle combines a very fast change rate at the beginning, inducing plastic and elastic strain, and then an almost flat temperature afterwards, inducing creep. The maximum achievable frequencies for this profile are shown in Table V.

Another parameter to consider is the power required to produce the simulated cycles. For the triangular profile with 50% duty cycle, f = 0.018 Hz, ΔT_j = 50°C and using air cooling, a peak power of 2.4 kW was needed, with the average power per cycle period being 1.2 kW.

TABLE IV
MAXIMUM ACHIEVABLE CYCLE FREQUENCY FOR A GIVEN ΔT_J
FOR THE PROFILE OF FIG. 9 (A): TURN ON-T_{MAX}-TURN OFF

ΔT_j (°C)	Max. f (Hz)	Min. period (s)	Rise time to T_{jmax} (s)
50	9	0.11	0.013
55	7	0.14	0.015
60	5	0.20	0.022
65	3	0.33	0.040
70	1.66	0.60	0.065
75	0.96	1.04	0.098
80	0.53	1.88	0.146

TABLE V
MAXIMUM ACHIEVABLE CYCLE FREQUENCY FOR A GIVEN ΔT_J
FOR THE PROFILE OF FIG. 9 (B): 10 S DWELL TIME AT T_{MAX}

ΔT_j (°C)	Max. f (Hz)	Min. period (s)
50	0.048	20.8
55	0.043	23.3
60	0.037	27.0
65	0.032	31.0
70	0.028	35.7
75	0.024	41.7
80	0.021	47.6

To produce the same cycle with water cooling, an average of 3.3 kW per cycle with a peak of 4.8 kW was required. This is explained by the fact that the air-cooled heat sink has a higher thermal resistance and is therefore easier to heat up. So while liquid cooling increases the system's flexibility in terms of thermal cycling, it also increases the power consumption.

In conclusion, although liquid cooling allows the setup to be more flexible and produce the widest range of frequencies, amplitudes and change rates, with air-cooling it is possible to design a set of temperature profiles that have wide varying slopes, amplitudes and frequencies - although there are limits and tradeoffs must be made, i.e. it is not possible to specify freely e.g. the frequency and the slope in a particular cycle. Nonetheless, the range of variation that can be achieved with air cooling over different cycles is sufficient to parameterize the model of [11-12], which is the primary goal of this power cycling system. For that reason, and because an air cooled system shows greatly reduced complexity compared to a liquid cooled setup, as well as lower power consumption, air cooling is selected for the power cycling system of this paper.

F. Data Storage

During a cycling test that may last weeks or months, a large amount of collected data needs to be stored, upwards of 1 GB per day. Reliability of the data storage system can be improved by using a redundant array of independent disks (RAID), a known technology widely applied for servers and data centers and other data-critical applications.

III. EXPERIMENTAL RESULTS

To demonstrate the concept of an air-cooled temperature-controlled power cycling test setup, a prototype system consisting of one phase of Topology I was constructed. One phase alone cannot deliver enough current to effectively cycle the whole 1200 A, 3300 V IGBT. An open module with the die accessible was obtained, consisting of six separate dies, each with 4 IGBT chips and 2 diodes in parallel. The connections between the dies were cut, allowing for the power cycling of a single die, making T_j = 125°C obtainable with the use of only 250 A. This also allowed the use of a commercial 8V, 220 A DC power supply instead of a

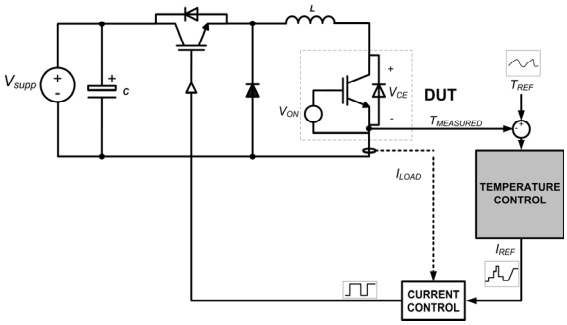


Fig. 10 – The prototype power cycling test setup.

three-phase transformer.

The schematic of the prototype power cycling system is given in Fig. 10. The DUT, placed on a commercial off-the-shelf heat sink, is kept always on (closed). A sensor measures the current I_{LOAD} through the DUT. The control loop contains a hysteretic-band current controller and a PI temperature controller setting I_{REF} based on the measured T_j and reference temperature curve T_{REF}. The acquisition and storage of measurements and the generation of control signals is done with the use of LabVIEW software and peripherals [37]. To speed up the development time, the temperature controller is also implemented in LabVIEW and runs on a PC.

Standard thermocouples, glued to the power module case and the top of the die to measure T_c and T_j, respectively, were chosen because of their low cost, adequate response time and wide measuring range (from below 0°C to more than 500°C). As discussed earlier, T_j is approximated by measuring the temperature of the chip centre point.

Over-current and over-voltage protection circuits are implemented as part of the current controller. An over-temperature sensor and smoke detector are also connected to a master switch (not shown) that can shut down all power in case of overheating or fire. As the setup operates non-stop until device failure, it is enclosed in a safety cage.

Initially all measurements are recorded on the PC's hard disk. The system is configured so that at a set instance every 24 hours, the day's recorded data is moved to an external 1TB hard drive. This also allows the data to be examined externally at any other time without having to stop system operation.

Tests of the built system, shown in Fig. 11, have

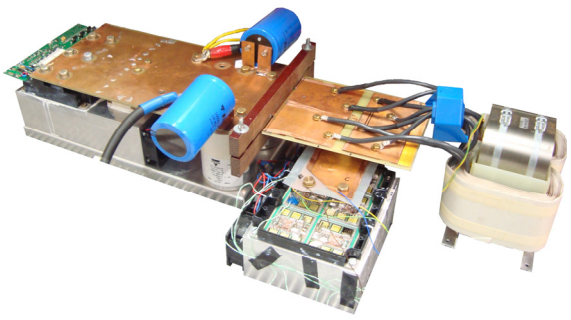
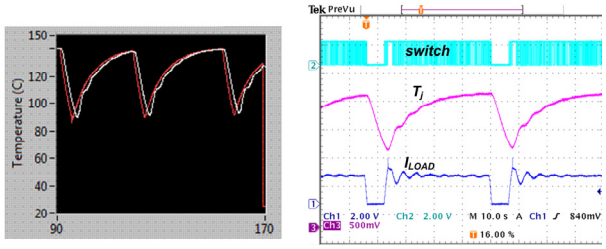
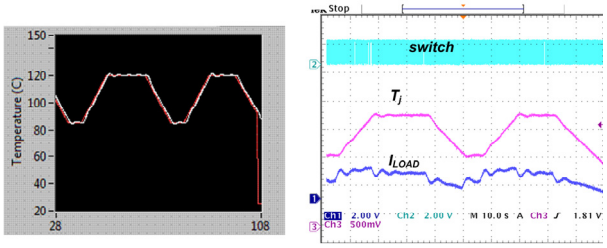


Fig. 11 – The built prototype setup, showing the test circuit and DUT (open module) on heat sink, with attached sensors.



a) b)

Fig. 12 – Experimental results in closed-loop demonstrating the functioning of the temperature controller. T_{REF} consists of two consecutive 35 s and 40 s cycles respectively, ΔT_j = 53°C, T_{jmax} = 138°C: a) LabVIEW window; T_{REF} in red, measured T_j in white; b) oscilloscope waveform: Ch. 1: DUT current, 2 V/div, 83 A/V; Ch. 3: T_j, 500 mV/div, 49°C/V (offset = 25°C); 10 s/div.



a) b)

Fig. 13 – Experimental results in closed-loop. T_{REF} consists of two 45 s cycles with 20 s and 15 s of dwell time, respectively. ΔT_j = 40°C, T_{jmax} = 120°C: a) LabVIEW window; T_{REF} in red, measured T_j in white; b) oscilloscope waveform: Ch. 1: DUT current, 2 V/div, 83 A/V; Ch. 3: T_j, 500 mV/div, 49°C/V (offset = 25°C); 10 s/div.

demonstrated its ability to produce the temperature cycles required for the parameterization and verification of the model of [11-12]. Figs. 12 and 13 show the results of closed-loop tests with two different temperature cycles, demonstrating that the temperature controller can produce an arbitrary temperature profile of the DUT. Fig. 12 shows a cycle where almost constant current is applied to get a slow, exponential rise to a high temperature, creating a temperature curve with varying slope. Fig. 13 is essentially a combination of the profiles of Figs. 7 and 9(b) – constant up and down slope, but with dwell time. Controller performance suffers due to the inability to specify a deterministic sampling rate in LabVIEW running on a PC. This underlines the need for a DSP-based controller in the full system.

The prototype system is currently performing a long-term cycling test. With the concept verified, the next step will be the construction of the full converter of Topology I with the three-phase transformer.

IV. Conclusions

The design procedure for an advanced power cycling setup that can force the junction temperature of a power module to follow a defined temperature profile was presented, the main purpose of which is to perform cycling tests for the parameterization and verification of a newly developed model of the solder layer deformation. It was demonstrated that the system can be sufficiently reliable to withstand several long-term cycling tests.

Although cooling the DUT with air limits the types of temperature profiles that can be applied to the device, cycles with varied enough characteristics, sufficient for the parameterization of the model, can be produced.

A scaled-down prototype system consisting of one phase of the proposed full-power setup was constructed, and the ability to create a defined temperature profile of the DUT was demonstrated. This system is currently being used for a long-term power cycling test, the results of which will be reported in a future publication.

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