Modeling and Robust Control of a Three-Phase Buck+Boost PWM Rectifier (VRX-4)

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***Abstract*—The modeling and control of a three-phase three-switch buck-type rectifier system with integrated boost output stage (Voltage Range Extended 4-Switch Rectifier) is analyzed in this paper. A cascaded multiloop control structure is presented that has the following features: constant output voltage for a wide input voltage range and stepwise changes of load; sinusoidal input currents in phase with the mains voltages that also remain sinusoidal in case of unbalanced mains conditions; and active damping of the input filter resonance. For the control design, an equivalent dc–dc small-signal model of the converter is derived and verified by simulations and measurements. Based on this and on the identification of the critical operating point, the controllers for the inner dc current and outer voltage control loops are selected. The stability of the closed loop system is discussed and the robust operation of the system is verified by measurements on a 5-kW prototype.**

***Index Terms*—Robust control, small-signal model, three-phase pulsewidth modulation (PWM) rectifier, unbalanced mains conditions.**

I. Introduction

A THREE-PHASE pulsewidth modulation (PWM) rectifier formed by integration of a three-phase three-switch buck-type front end and a dc–dc boost-type output stage has been proposed in [1]. This topology gives the possibility of controlling the output voltage to 400 V for a wide input voltage range of $208\ V_{rms}, \ldots, 480\ V_{rms}$ at unity power factor by only employing four power transistors (cf., Fig. 1); therefore, it is called as the Voltage Range Extended 4-Switch Rectifier (**VRX-4**).

The control aim of this rectifier is to provide a stable operation, a constant output voltage and an ohmic input behavior within the whole operating range, i.e., within the specified wide input voltage range. In particular, input currents being in phase with the mains voltages have to be guaranteed also in case of mains phase failure or a short circuit between two phases. Furthermore, disturbances from the load side (such as sudden load changes) must not provoke a change of the output voltage.

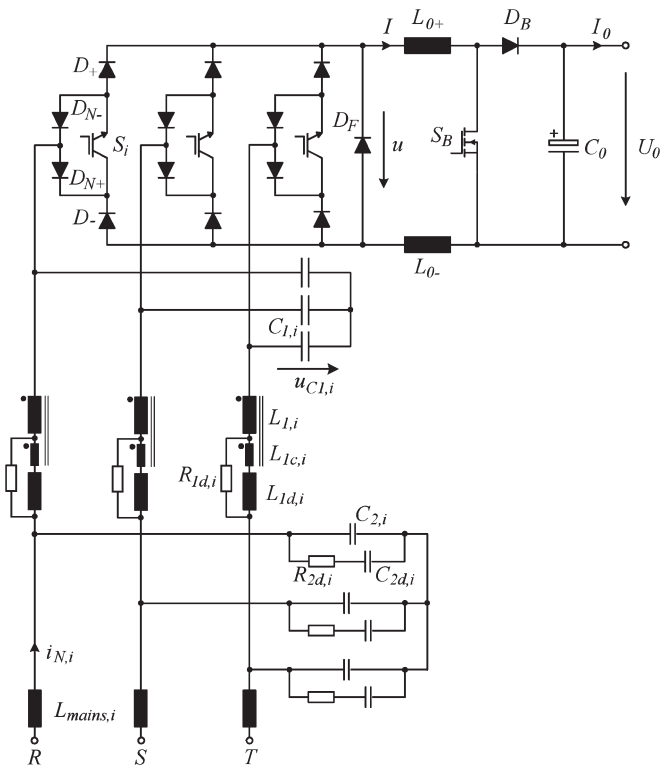

Fig. 1. Topology of the VRX-4 including input filter [4], three-phase buck-type rectifier input part and boost-type output part.

In [2], a cascaded control scheme has been developed for a boost-type rectifier system that has the aforementioned control features. Generally, buck-derived topologies cannot perform this operation due to their incapacity to step-up input voltages (being lower than the output voltages during mains failures). As shown in [1], the VRX-4 rectifier can solve this problem due to its integrated boost operation capability. The basic control structure that is required to maintain sinusoidal mains currents in case of mains unbalances has been presented in [3]. However, until now, no research has been done in the field of modeling and control design of this rectifier, such as the investigation of a dynamic model for all operating points or the influence of the input filter and its passive and active damping. As the following points indicate, the derivation of a thorough model is involved

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but important for achieving a good control performance within the whole operating range.

1) First, depending on the mains voltage, the system is operating in a purely step-down (buck) mode or in a step-up (buck+boost[1]) mode. Between these two modes, the dynamics of the system to be controlled changes. Therefore, the worst case operating point within the whole operating range has to be identified and controllers have to be designed that enable stable operation with good reference tracking and disturbance rejection behavior for all operating points.
2) Second, the input filter shown in Fig. 1, which has been developed in [4] for compliance of the electromagnetic compatibility (EMC) standards [5], takes a major influence on the control stability by significantly increasing the system order. In [6], a sufficient condition for a separate design of the control and the input filter was given, whose fulfillment, however, leads to oversized filters and/or poor control bandwidth [7]. Thus, for achieving a good control performance, the dynamics of the filter has to be directly considered in the control design.
3) Furthermore, an active damping of the input filter resonance takes substantial influence on the stability of the inner control loop and therefore should not be neglected in the controller design.
4) And finally, the losses of the power semiconductors (switching and conduction losses) also influence the dynamics as they provide additional passive damping to the system. This fact is often neglected in conventional converter modeling [8], [9].

In literature, some approaches for the modeling of three-phase systems have already been undertaken. Because of the fact that in a three-phase system without neutral line the sum of the phase currents and voltages is always equal to zero, a three-phase system (R, S, T) can be unambiguously transformed into a rotating two-phase system (d, q). With this, a d- and a q-component are obtained by projection of the R, S, T components on a rotating d- and a 90° phase-shifted q-axis [10], [11]. This greatly reduces the control effort from three ac quantities [12] to two dc quantities [13] for the control of the mains currents. A key paper [14] proved that the q-component has practically no relevance for the system control stability and dynamics due to its higher stability and low coupling with the d-component. Hence, a reduced single-phase dc–dc model can be derived based only on the dynamics of the d-component. Furthermore, it has been shown in [14] that all relevant transfer functions in the dq-system and in the reduced single-phase dc–dc model are nearly identical, wherefore the validity of the model reduction could be proved.

With this, the three-phase ac–dc buck input part of the VRX-4 can be modeled as a simple dc–dc buck converter with equivalent dc input parameters (input voltage and filter parameters). These equivalent parameters are derived in this paper based on the equity of input and output power, whereas the power losses and their influence on the dynamics are modeled afterward explicitly. This paper is structured as follows:

After a short description of the basic operating behavior of the rectifier in Section II, the control-oriented modeling of the topology is presented and verified in Section III and the dynamically critical operating point of the system is identified in Section IV. In Section V, the proposed control structure that features robustness against disturbances from the mains and/or load side and ensures sinusoidal mains currents under unbalanced mains conditions is discussed. In particular, four important issues for the control are the matter of discussion, namely: a feedforward of the load facilitating an optimum disturbance rejection and/or minimum output voltage drop for load variations; a dc current shaping to enable sinusoidal mains currents also for asymmetric mains condition; a common current controller allowing a smooth transition between the operation modes, i.e., the pure buck mode for high input voltages and the buck+boost mode for low input voltages; and an effective and easy-to-realize active damping scheme and its influence on the input filter stability. In Section VI, controllers for the inner and outer control loop are designed, and the control performance is shown by measurements on a 5 kW prototype in Section VII.

II. Basic Operating Behavior

For the VRX-4, there are two operation modes. First, the pure buck mode, where only the switching functions of the three transistors S_i of the buck-type rectifier input stage are controlled and the boost switch is turned off. Second, the buck+boost mode, where due to low mains voltages and/or high reference output voltage, the boost stage is additionally activated by controlling the boost switch S_{B}, and the buck stage is operated in open-loop. In the following, the equations for these two operating modes are derived, whereby all forthcoming considerations are based on these operating parameters:

$$\begin{aligned} U_{N,\mathrm{rms}} &= (120, \ldots, 280)\ \mathrm{V} & L_0 &= L_{0+} + L_{0-} = 2\ \mathrm{mH} \\ U_0 &= 400\ \mathrm{V} & C_0 &= 750\ \mu\mathrm{F} \\ P_0 &= 5\ \mathrm{kW} & C_{1,i} &= 6.8\ \mu\mathrm{F} \\ f_S &= 28\ \mathrm{kHz} & L_{1,i} &= 240\ \mu\mathrm{H}. \end{aligned}$$

A. Buck Operation Mode

The modulation index of the VRX-4 input part is defined as

$$M = \frac{\hat{I}_N}{I} = 0, \ldots, M_{\max}. \tag{1}$$

Because of the equity of input and output power

$$P_0 = \frac{3}{2}\hat{U}_N\hat{I}_N = UI \tag{2}$$

the maximum dc-link voltage $U_{\max}$ is given by

$$U_{\max} = \frac{3}{2}M_{\max} \cdot \hat{U}_N. \tag{3}$$

[1]Because of the system topology, the input part of the rectifier is always working in a buck mode. Therefore, the operation mode with additional step-up (boost) functionality is called buck+boost mode.

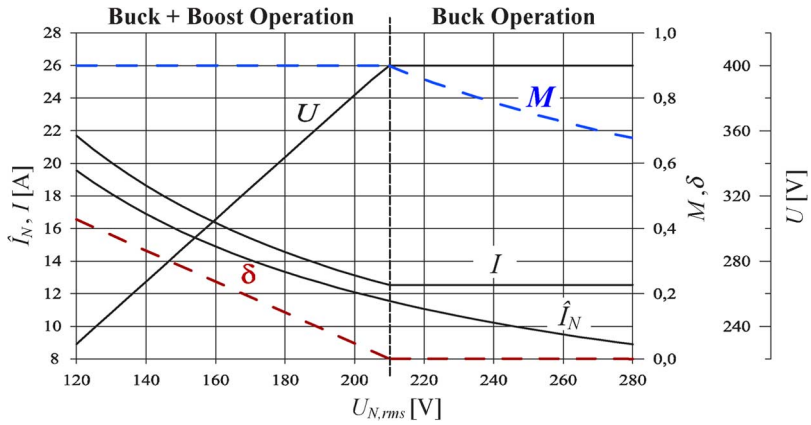

Fig. 2. Operating areas of the buck+boost rectifier: in the buck operating mode the modulation index M of the buck-type rectifier input stage is reduced with increasing input voltage and the relative on-time δ of the boost switch is equal to zero, while in the buck+boost operating mode the modulation index M is set to $M_{\max} = 0.9$ and the boost switch is activated according to (10).

for symmetric mains conditions

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\omega_N t) \\ u_{N,S} &= \hat{U}_N \cos(\omega_N t - 2\pi/3) \\ u_{N,T} &= \hat{U}_N \cos(\omega_N t + 2\pi/3). \end{aligned} \tag{4}$$

As for dc–dc buck converters, the modulation index M can vary within the range $M = (0, \ldots, 1)$. However, to reserve some modulation margin $m_{\text{damp}} = (0, \ldots, 0.1)$ for active damping, which will be discussed later in Section V, M is limited to

$$M_{\max} = 0.9. \tag{5}$$

With (3) and (5) the input voltage limit for the pure buck operating mode can be calculated by

$$U_{N,\text{rms}}|_{U_{\max}=U_0} = \frac{\sqrt{2}}{3}\frac{U_0}{M_{\max}} = 210 \text{ V}. \tag{6}$$

Above this input voltage, the modulation index M changes according to

$$M = \frac{\sqrt{2}}{3}\frac{U_0}{U_{N,\text{rms}}} = (0.67, \ldots, 0.9). \tag{7}$$

While the dc link current is constant in the buck operating range ($I = 12.5$ A), the mains current is given by

$$\hat{I}_N = \frac{I}{M} = (8.4, \ldots, 11.2) \text{ A}. \tag{8}$$

The dependence of the operating variables on the input voltage for symmetric mains conditions is depicted in Fig. 2.

B. Buck+Boost Operation Mode

For lower input voltages than $U_{N,\text{rms}} = 210$ V the dc-link voltage U decreases according to

$$U = \frac{3}{\sqrt{2}} M_{\max} \cdot U_{N,\text{rms}} = (230, \ldots, 400) \text{ V} \tag{9}$$

and therefore is lower than the required output voltage U_0. Hence, the on-time of the boost converter has to be set according to

$$\delta = 1 - \frac{U}{U_0} = (0, \ldots, 0.43) \tag{10}$$

to maintain $U_0 = 400$ V. Because of (2) and (9), the dc link current I increases for decreasing input voltages

$$I = \frac{P_0}{U} = (12.5, \ldots, 21.7) \text{ A}. \tag{11}$$

Consequently, also the input current amplitude $\hat{I}_N$ is increasing

$$\hat{I}_N = M \cdot I = (11.3, \ldots, 19.5) \text{ A} \tag{12}$$

due to the constant modulation index M of the buck rectifier part.

It has to be noted that these dependencies (cf., Fig. 2) are only valid for symmetric mains conditions. For asymmetric mains, such as loss of one phase, the control structure presented in Section V has to be applied to maintain sinusoidal input current shapes and the modulation index of the buck converter M and the duty cycle of the boost converter δ are then both changing during the mains period.

III. Control-Oriented Converter Modeling

As explained in the introduction, the main idea of the modeling is that the three-phase ac-to-dc buck-type rectifier stage shows similar dynamic behavior as an equivalent dc-to-dc buck converter with a suitable dc input voltage and appropriate values of the passive filter components [cf., Fig. 3(a)]. In the following, the parameters of the equivalent system are calculated.

If for the equivalent model the same modulation range as for the three-phase system is chosen

$$M_{\text{eq}} = M = 0, \ldots, M_{\max} \tag{13}$$

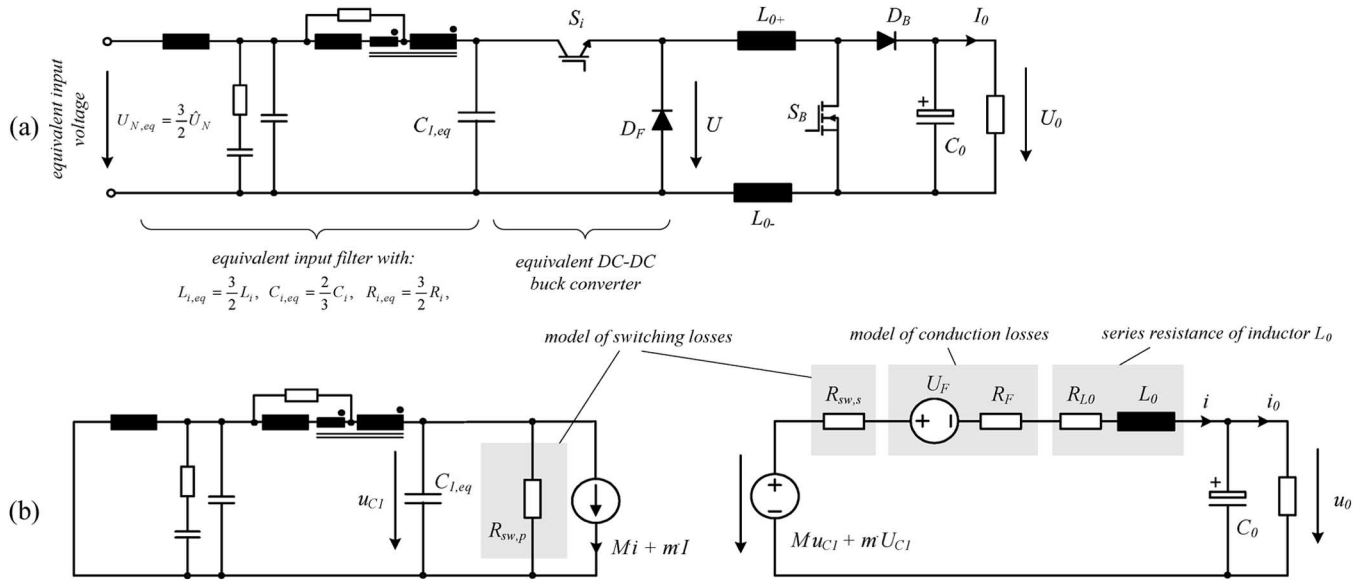

Fig. 3. (a) DC–DC model of the VRX-4 rectifier system with equivalent input parameters and (b) linearized small-signal model of the converter for $U_{N,l-l,\mathrm{rms}} = 400$ V ($M = 0.82$) containing damping elements such as the series resistor of the dc inductor and equivalent resistors modeling switching and conduction losses.

the equivalent input current $i_{N,\mathrm{eq}}$ exactly corresponds to the amplitude $\hat{I}_N$ of the mains current of the three-phase system

$$i_{N,\mathrm{eq}} = \hat{I}_N. \tag{14}$$

Since the equivalent system has the same input power as the original system

$$u_{N,\mathrm{eq}} \cdot i_{N,\mathrm{eq}} = \frac{3}{2}\hat{U}_N \cdot \hat{I}_N \tag{15}$$

the equivalent input voltage is given by

$$u_{N,\mathrm{eq}} = \frac{3}{2}\hat{U}_N. \tag{16}$$

This voltage exactly corresponds to the value of the two line-to-line input voltages that are used for the formation of the dc link voltage at $\omega_N t = n \cdot \pi/3$, i.e., in the middle of the interval, in which these voltages are used [1].

For the determination of the equivalent filter parameters, the stored energies in the components can be compared for the three-phase system and the equivalent system. That is, the sum of the energy in the filter inductors $L_{1,i}$ can be derived by

$$\begin{aligned} E_{L_{1,3\mathrm{ph}}} &= \frac{1}{2}L_{1,R} \cdot \left(\hat{I}_N \cos(\omega_N t)\right)^2 \\ &\quad + \frac{1}{2}L_{1,S} \cdot \left(\hat{I}_N \cos\left(\omega_N t - \frac{2\pi}{3}\right)\right)^2 \\ &\quad + \frac{1}{2}L_{1,T} \cdot \left(\hat{I}_N \cos\left(\omega_N t + \frac{2\pi}{3}\right)\right)^2 \\ &= \frac{3}{4}L_{1,i}\hat{I}_N^2 \end{aligned} \tag{17}$$

while the stored energy in the filter inductor $L_{1,\mathrm{eq}}$ in the equivalent system is

$$E_{L_{1,\mathrm{eq}}} = \frac{1}{2}L_{1,\mathrm{eq}}i_{N,\mathrm{eq}}^2. \tag{18}$$

With $E_{L_{1,3\mathrm{ph}}} = E_{L_{1,\mathrm{eq}}}$ and (14), the equivalent inductor value is given by

$$L_{1,\mathrm{eq}} = \frac{3}{2}L_{1,i}. \tag{19}$$

Analogously, the sum of the filter capacitor energies is

$$E_{C_{1,3\mathrm{ph}}} = \frac{3}{4}C_{1,i}\hat{U}_N^2 \tag{20}$$

for the three-phase system and

$$E_{C_{1,\mathrm{eq}}} = \frac{1}{2}C_{1,\mathrm{eq}}u_{N,\mathrm{eq}}^2 \tag{21}$$

for the equivalent system, respectively. Therefore, with $E_{C_{1,3\mathrm{ph}}} = E_{C_{1,\mathrm{eq}}}$ and (16), the equivalent capacitor value is given by

$$C_{1,\mathrm{eq}} = \frac{2}{3}C_{1,i}. \tag{22}$$

With this, the filter resonance frequencies stay the same in both systems

$$f_{\mathrm{res,eq}} = \frac{1}{2\pi\sqrt{L_{1,\mathrm{eq}} \cdot C_{1,\mathrm{eq}}}} = \frac{1}{2\pi\sqrt{L_{1,i} \cdot C_{1,i}}} = f_{\mathrm{res,3ph}}. \tag{23}$$

In the same way, all filter inductors and capacitors can be transformed with the factor 3/2 or 2/3, respectively. Finally, the filter damping resistors can be transformed in an analogous

manner as the filter inductors with a factor 3/2. The complete equivalent input filter is shown in Fig. 3(a).

To develop a small signal model of the equivalent dc–dc converter, an average model can be derived based on the well-known state space averaging method [8]. For system dynamics being significantly slower than the switching frequency, this technique transforms the switches and diodes into a system of controlled voltage and current sources. However, to enable the calculation of transfer functions, the system has to be linearized in an operating point, which has been done in Fig. 3(b) for the pure buck operating mode. As will be shown in the next section, this is the worst case operating mode, therefore the controller design will be carried out for this mode and the boost switch does not have to be considered.

However, the equivalent system does not result in exactly the same dynamic behavior due to the negligence of the power losses in the real system. The switching and conduction losses of the rectifier provide considerable damping that can be modeled by equivalent series resistors $R_{\mathrm{sw,s}}$ and equivalent parallel resistors $R_{\mathrm{sw,p}}$ [cf., Fig. 3(b)].

To ascertain the equivalent resistor values, first the switching losses of the converter at the operating point of interest have to be determined as it was done for the system at hand in [15]. The turn-on, turn-off, reverse and forward recovery losses are dependent on the switched voltage and the switched current according to the function given by (1) in [15]. However, to derive a linear model the function has to be simplified to a linear dependence on the equivalent capacitor voltage U_{C_1} [cf., Fig. 3(a)] and the dc current I

$$P_{\mathrm{sw}} \approx k_{\mathrm{sw}} \cdot U_{C_1} \cdot I. \tag{24}$$

The losses occurring in the equivalent resistors $R_{\mathrm{sw,p}}$ and $R_{\mathrm{sw,s}}$ [cf., Fig. 3(b)] are given by

$$P_{\mathrm{sw}} \approx \frac{U_{C_1}^2}{R_{\mathrm{sw,p}}} + I^2 \cdot R_{\mathrm{sw,s}}. \tag{25}$$

By taking the derivative of (24) and (25)

$$\frac{\partial}{\partial U_{C_1}}(P_{\mathrm{sw}}) = k_{\mathrm{sw}} \cdot I = \frac{2 \cdot U_{C_1}}{R_{\mathrm{sw,p}}} \tag{26}$$

$$\frac{\partial}{\partial I}(P_{\mathrm{sw}}) = k_{\mathrm{sw}} \cdot U_{C_1} = 2 \cdot I \cdot R_{\mathrm{sw,s}} \tag{27}$$

the values of the resistors can be ascertained

$$R_{\mathrm{sw,p}} = \frac{2 \cdot U_{C_1}}{k \cdot I} \tag{28}$$

$$R_{\mathrm{sw,s}} = \frac{k \cdot U_{C_1}}{2 \cdot I}. \tag{29}$$

That is, for $U_{N,l-l,\mathrm{rms}} = 400$ V, the operating parameters given in Section II ($I = 12.5$ A) and the loss calculation in [15] ($k_{\mathrm{sw}} = 0.013$), the equivalent damping resistors $R_{\mathrm{sw,p}} = 5.9$ kΩ and $R_{\mathrm{sw,s}} = 260$ mΩ are derived. The separation into a parallel and a series resistor represents a separation into a purely voltage-dependent and a purely current-dependent part of the switching losses. It should be noted that an equivalent model with a series resistor at the input side and a parallel resistor on the dc side would also be possible. This would, however, lead to resistor values that are then dependent on the actual modulation index.

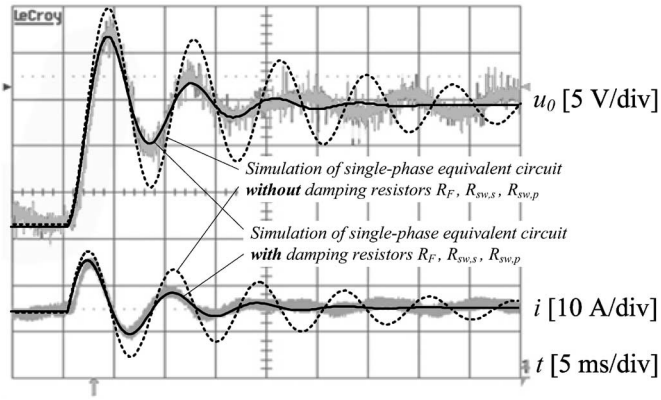

Fig. 4. Response of the measured output voltage for a stepwise change of the modulation index ($M = 0.82 \rightarrow 0.84$) in open-loop operation for the three-phase system and simulation of the single-phase equivalent dc–dc circuit with and without consideration of the switching and conduction losses in the model.

The conduction losses of the insulated gate bipolar transistors ($U_{\mathrm{CE},0}$, r_{CE}), the module diodes ($U_{\mathrm{F,DM}}$, r_{DM}), the freewheeling diode ($U_{\mathrm{F,DF}}$, r_{DF}), and the boost diode ($U_{\mathrm{F,DB}}$, r_{DB}) can be modeled by a total forward voltage drop U_{F}, which is not influencing the dynamics of the system but is altering the operating point

$$U_{\mathrm{F}} = M \cdot (2U_{\mathrm{CE},0} + 4U_{\mathrm{F,DM}} + U_{\mathrm{F,DB}}) + (1 - M) \cdot (U_{\mathrm{F,DF}} + U_{\mathrm{F,DB}}) \tag{30}$$

and a total forward resistance R_{F}

$$R_{\mathrm{F}} = M \cdot (2r_{\mathrm{CE}} + 4r_{\mathrm{DM}} + r_{\mathrm{DB}}) + (1 - M) \cdot (r_{\mathrm{DF}} + r_{\mathrm{DB}}). \tag{31}$$

Together with the series resistance R_{L_0} of the dc inductor $L_0 = L_{0+} + L_{0-}$ the damping provided by the equivalent resistors R_{F}, $R_{\mathrm{sw,p}}$ and $R_{\mathrm{sw,s}}$ precisely corresponds with the damping appearing in the real system, which is verified in Fig. 4 for a small signal step response of the output voltage for open loop operation of the system.[2] On the contrary, without consideration of switching and conduction losses in the model, the damping is considerably lower.

However, the waveforms in Fig. 4 are mainly dominated by the output filter dynamics of the output filter (the oscillation frequency in Fig. 4 corresponds with the output filter resonance frequency), wherefore the equivalent model of the input parameters cannot be verified directly by this test.

Hence, a step of the input voltage for impressed output current was additionally simulated. As can be seen in Fig. 5, the time behavior of the local averaged value of the dc link voltage u at the freewheeling diode D_{F} perfectly coincides with the time response of the equivalent linearized single phase model for a small-signal step of the input voltage. Both the overshoot

[2]The 100-Hz component that can be observed in the hardware measurement is originating from small asymmetries in the hardware setup but is not caused by a resonance in the system.

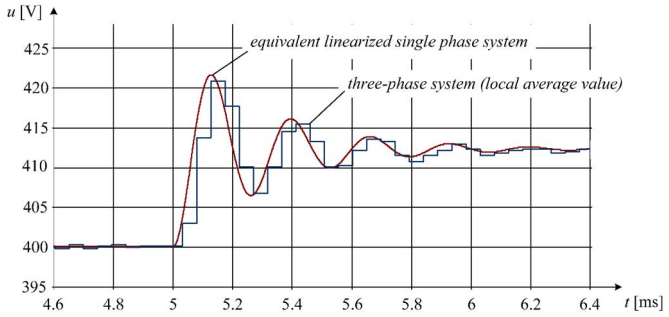

Fig. 5. Simulated response of the dc link voltage u at the freewheeling diode D_{F} for a stepwise change of the amplitude of the input voltage ($\Delta\hat{U} = 10$ V) and for constantly impressed output current $I = 12.5$ A in open-loop operation for the three-phase system and the single-phase equivalent dc–dc circuit.

amplitude and the resonance frequency match accurately, from which it can be concluded that the modeling of the rectifier is successful.

IV. Critical Operating Point

The system is operating in two operation modes, namely: the pure buck mode, where the control variable is the duty cycle of the buck-type input part of the converter; and the buck+boost mode, where the duty cycle of the buck part is set to a constant value and the on-time of the boost transistor is the control variable (cf., Section II).

As will be explained in Section V, one common controller for both operating modes is utilized, therefore the critical operating condition within the whole operating range has to be identified. The controllers will then be designed for this worst case condition.

For both operation modes, the plant that is seen by the inner current loop controller mainly shows integral behavior with a conjugated complex pole-pair and a conjugated complex zero-pair. These zeros/poles that originate from the first section of the input filter define the stability of the inner loop, while the output filter, due to the significantly lower resonance frequency and the slow output voltage controller, has no influence. Therefore, the identification of the critical operating point can be restricted to an analysis of the dominant zero-pole combination.

In Fig. 6 the root locus diagram is shown for several operating conditions. It can be seen that for higher output power (dashed lines) the system is less stable than for low output power[3] (solid lines). The position of the poles of the open loop system is not changed, while the zeros move toward the right half-plane. Also, with decreasing input voltage (higher modulation index M) the stability margin decreases. The worst case condition in the buck operating mode is therefore full power $P_0 = 5$ kW and minimum voltage $U_{N,l-l} = 363\ \mathrm{V_{rms}}$ at the border of the buck+boost mode. If the input voltage is further lowered, the control variable then becomes the duty cycle of the boost transistor and therefore the plant is changed. From Fig. 6, it can be seen that the system is always stable in the buck+boost operating mode (dot and dash line) and that the dynamics are not influenced by the output power.

This fact can be explained by deriving the open-loop transfer functions of the two operation modes. For sake of clarity, only a single-stage input filter without passive damping is considered and the output voltage is assumed to be constant. Then, the open-loop transfer function for the pure buck operation is equal to

$$G_{\mathrm{Buck}}(s) = \frac{i}{m} = \frac{U_{N,\mathrm{eq}}}{L_0} \cdot \frac{\left(1+s^2 L_{1,\mathrm{eq}} C_{1,\mathrm{eq}}\right) - \frac{M^2}{C_{1,\mathrm{eq}}} \cdot \frac{I_0}{U_0} s}{s \cdot \left(1+M^2 \cdot \frac{L_{1,\mathrm{eq}}}{L_0} + s^2 L_{1,\mathrm{eq}} C_{1,\mathrm{eq}}\right)}. \tag{32}$$

It can be seen that in (32) a zero in the right half-plane occurs due to the negative s-coefficient in the numerator. If the passive damping of the filter is added, the zero will move toward the left and potentially enter the left half-plane for decreasing loads [I_0 in (32)] and increasing input voltages [decreasing M in (32)], as already described above for Fig. 5.

For the buck+boost operating mode it can be shown that the negative s-coefficient in the numerator disappears, therefore also the dependence of the position of the zero on the load and the input voltage

$$G_{\mathrm{Boost}}(s) = \frac{i}{\delta} = \frac{U_0}{L_0} \cdot \frac{1 + s^2 L_{1,\mathrm{eq}} C_{1,\mathrm{eq}}}{s \cdot \left(1 + M^2 \cdot \frac{L_{1,\mathrm{eq}}}{L_0} + s^2 L_{1,\mathrm{eq}} C_{1,\mathrm{eq}}\right)}. \tag{33}$$

Hence, the converter always has higher stability in the buck+boost operation mode compared to the pure buck operation mode.

Based on these considerations, for the forthcoming controller design, the aforementioned operating point ($P_0 = 5$ kW, $M = 0.9$) is considered.

V. Control Structure

In Fig. 7, the basic control structure of the buck+boost rectifier is depicted. A slow outer control loop regulates the output voltage to a constant reference voltage U_0^* and sets the reference value for the fast inner dc current loop. A feedforward of the load current (cf., Section V-A) decreases the variation of the output voltage in case of sudden load changes. A current shaping circuit, which will be discussed in Section V-B, provides sinusoidal input currents also in case of asymmetric mains phase conditions such as phase loss or short-circuit between two phases. The output of the inner current controller u_{L}^* has a precontrol of the rate-limited reference output voltage $U_{0,\mathrm{lim}}^*$ to improve the large-signal behavior of the controller in case of a start-up. The output of the current controller is the required inductor voltage so that the dc current follows the reference current and is used for the calculation of the relative on-times of the transistors of the buck input part as well as the boost output part (cf., Section V-C). An active damping scheme (cf., Section V-D) is additionally employed to damp the resonance of the input filter.

[3]Here, a minimum load of 10% was chosen in order to maintain continuous mode operation.

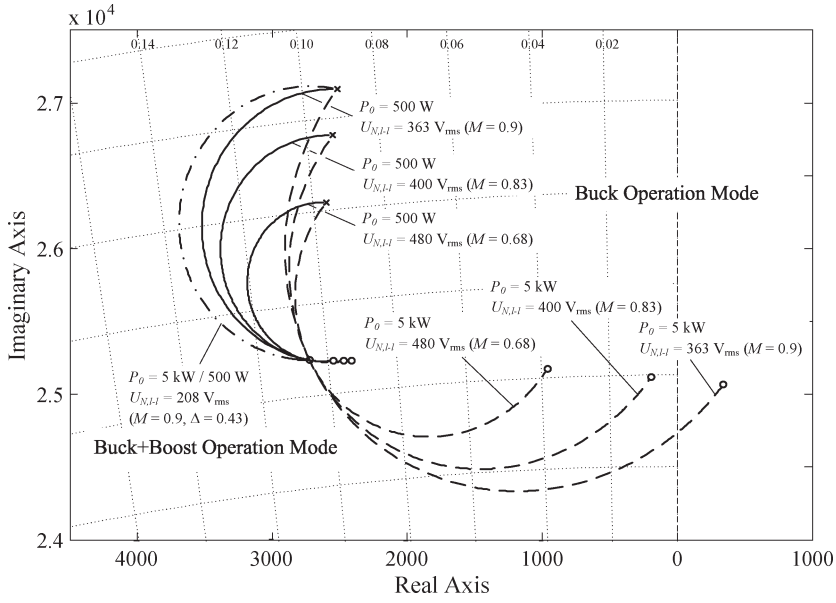

Fig. 6. Zoom of the root locus diagram showing the dominant poles of the inner control loop for different operating points. The input line-to-line voltage is varied within the specified voltage range and the output power varied between rated load and 10% of the rated load.

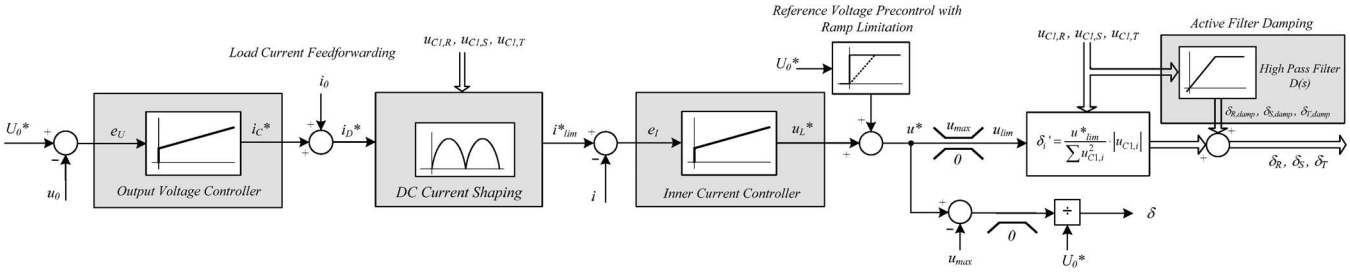

Fig. 7. Complete control structure enabling sinusoidal input currents under unbalanced mains conditions including a feedforward of the load current and active damping of the input filter.

A. Load Current Feedforward

A load current feedforward scheme is added to the output of the output voltage controller, which can be viewed as the reference capacitor current i_C^*. This gives a direct reference step for the underlying dc current control loop and enables an immediate change of the relative on-times of the power transistors for sudden steps of the load current. Hence, the reference value for the underlying current control loop is changed instantly without causing significant involvement of the (very slow) outer voltage loop. The effect of this disturbance feedforward method is proved experimentally in Section VII. However, it is necessary to include the dynamics of the feedforward in the design of the output voltage controller as done in Section VI.

B. DC Current Shaping

For a constant output voltage reference value U_0^*, a slow output voltage controller and no variation of the load ($i_0 = \text{const.}$), the current reference value i_D^* (cf., Fig. 7) will be a constant value according to the power demand of the load. However, for asymmetric mains conditions, the power that is drawn from the mains is varying over the mains periods if sinusoidal input currents are maintained. Hence, the current reference then has to be accordingly changed [16], [17] as depicted in Fig. 8.

The average power demand of the output voltage controller is calculated by

$$P^* = U_0^* \cdot i_D^*. \tag{34}$$

To achieve sinusoidal mains currents in phase with the input voltages, the three phases of the converter must show resistive behavior, i.e., the rectifier inputs look from the mains side as three resistors with resistance and/or conductance values

$$G^* = \frac{1}{R^*} = \frac{\bar{i}_{\text{rec}}}{u_{C_1}} \tag{35}$$

being constant over one mains period. The conductance values can be calculated by summation of the average power drawn from the three phases

$$P^* = \left(\frac{\hat{U}_{C_{1,R}}}{\sqrt{2}}\right)^2 \cdot G^* + \left(\frac{\hat{U}_{C_{1,S}}}{\sqrt{2}}\right)^2 \cdot G^* + \left(\frac{\hat{U}_{C_{1,T}}}{\sqrt{2}}\right)^2 \cdot G^*$$
$$= \frac{\hat{U}_{C_{1,R}}^2 + \hat{U}_{C_{1,S}}^2 + \hat{U}_{C_{1,T}}^2}{2} \cdot G^* \tag{36}$$

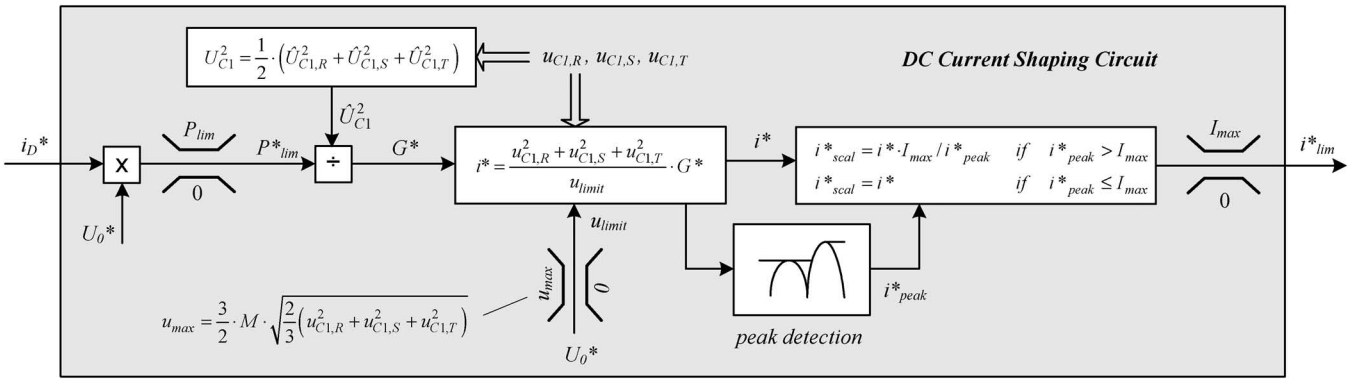

Fig. 8. DC current-shaping circuit enabling sinusoidal input currents under unbalanced mains conditions.

where the peak values of the phase voltages have to be detected by a peak detection circuit. The instantaneous power at the input of the rectifier has to equal the instantaneous power at the output side of the rectifier

$$p = \left(u_{C_{1,R}}^2 + u_{C_{1,S}}^2 + u_{C_{1,T}}^2\right) \cdot G^* = u_{0,\lim} \cdot i^* \qquad (37)$$

where $u_{0,\lim}$ is the reference output voltage that is limited to the maximum instantaneous dc-link voltage $u_{\max}$

$$\begin{aligned} u_{0,\lim} &= U_0^* \qquad \text{for} \qquad U_0^* \le u_{\max} \\ u_{0,\lim} &= u_{\max} \qquad \text{for} \qquad U_0^* > u_{\max}. \end{aligned} \qquad (38)$$

The maximum dc-link voltage $u_{\max}$ at the output of the buck-type rectifier input stage in the case of asymmetric mains conditions is not given by (3) anymore, but is dependent on the three rectifier input voltages

$$u_{\max} = \frac{3}{2} \cdot M_{\max} \cdot \sqrt{\frac{2}{3}\left(u_{C_{1,R}}^2(t) + u_{C_{1,S}}^2(t) + u_{C_{1,T}}^2(t)\right)}. \qquad (39)$$

Using (37), the reference current can be calculated

$$i^* = \frac{u_{C_{1,R}}^2 + u_{C_{1,S}}^2 + u_{C_{1,T}}^2}{u_{0,\lim}} \cdot G^*. \qquad (40)$$

As stated before, for the case of asymmetric mains conditions, the dc-link current is then shaped by the inner controller according to the power demand with double mains frequency. The peak values can then potentially exceed the maximum allowable current values $I_{\max}$. Therefore, the current reference value i^* has to be limited to $I_{\max}$, or—if the sinusoidal shape of the mains currents has to be maintained also in this case—i^* has to be rescaled according to

$$\begin{aligned} i_{\text{scal}}^* &= i^* \qquad \text{for} \qquad i_{\text{peak}}^* \le I_{\max} \\ i_{\text{scal}}^* &= i^* \cdot \frac{I_{\max}}{i_{\text{peak}}^*} \qquad \text{for} \qquad i_{\text{peak}}^* > I_{\max} \end{aligned} \qquad (41)$$

where i_{peak}^* is the peak value of i^* during a half mains period.

Experimental waveforms in Section VII prove the working principle of the dc current shaping circuit, i.e., that resistive input behavior of the VRX-4 is maintained also during asymmetric mains conditions.

C. Common Current Controller for Smooth Transition Between Operation Modes

To prevent oscillations at the boundary between the pure buck operation mode and the buck+boost operation mode, a common controller is employed (cf., Fig. 7). The output of the current controller is then utilized for the calculation of the relative on-times of the buck-type input part as well as for the boost output stage.

If different controller types and/or gains would be employed, the boundary between the operation modes would have to be detected accurately and without any time delay to switch exactly between the two control modes and to enable a smooth transition. Since measurements in reality contain noise and/or delay times, the robustness of the control is significantly improved with a common controller.

For the case that the reference voltage u^* is lower than the maximum output voltage of the buck input part $u_{\max}$, the duty cycle of the boost transistor is set to zero and the relative on-times of the three buck transistors are derived by

$$\delta_i' = \frac{u^*}{\sum u_{C_{1,i}}^2} \cdot |u_{C_{1,i}}|. \qquad (42)$$

If u^* exceeds $u_{\max}$, the on-times of the buck transistors are set to

$$\delta_i' = \frac{u_{\max}}{\sum u_{C_{1,i}}^2} \cdot |u_{C_{1,i}}| \qquad (43)$$

and additionally the boost converter has to be turned on

$$\delta = \frac{u^* - u_{\max}}{U_0^*}. \qquad (44)$$

The smooth transition between these two operation modes will be verified experimentally in Section VII.

D. Active Damping of the Input Filter

Generally, passive damping is a strict requirement for input filters in any case for open-loop operation of the rectifier (see damping resistors $R_{1\text{d},i}$ and $R_{2\text{d},i}$ in Fig. 1). However, since passive damping is always related with the loss of high frequency attenuation and/or bigger filter volume [4], it is usually kept at a minimum level to maintain high power density.

To provide a good filter damping during closed-loop operation, an active damping can be added. In literature, various methods for an active input filter damping have been proposed, such as the feedback of the mains voltage [18] or the input filter inductor voltage [19], the introduction of an input filter capacitor voltage control [20], the limitation of the maximum possible rate of rise of the current reference values [21], or the feedback of the high-pass filtered input capacitor voltages [22]. Both in terms of effectiveness and low realization effort, the latter method seems to be most promising and will therefore be used for the following design of the active filter damping.

Because of the input filter characteristic, the filter can possibly be excited by harmonics contained in the feeding mains voltages mainly at the resonance frequency of the first filter stage $(L_1 - C_1)$ at $f_{\mathrm{res},1} = 3.4$ kHz (for $L_{\mathrm{mains}} = 50\ \mu$H). To provide active damping, the resonant frequency components of the filter capacitor voltages are fed back to the control system by bandpass filtering around $f_{\mathrm{res},1}$. As the control block diagram in Fig. 7 of [22] shows, this method works like a damping resistor that is only valid for frequencies located inside the bandpass and therefore does not cause losses in the mains frequency area. The gain of this feedback has to be selected very carefully, since the amount of damping has substantial impact on the stability of the system. Compared to other active damping methods, this technique does not require any additional measurements such as mains voltages or filter inductor voltages [18], [19] that are usually not available and is not only restricted to oscillations originating from the rectifier itself [21].

In the design step, the considerations can be limited to one phase due to the equivalent dc-to-dc model resulting in a change of the duty cycle by

$$m = m' + m_{\mathrm{damp}}. \tag{45}$$

However, for a three-phase system, resonances normally cause ringing in the amplitude and phase of the capacitor voltage space vector; hence, the relative on-times of the switches of all phases have to be adapted to

$$\delta_i = \delta_i' + \delta_{i,\mathrm{damp}}, \qquad i = R, S, T. \tag{46}$$

Because of phase symmetry, it is sufficient to calculate only two damping coefficients

$$\begin{aligned} \delta_{R,\mathrm{damp}} &= D(s) \cdot u_{C_{1,R}} \\ \delta_{S,\mathrm{damp}} &= D(s) \cdot u_{C_{1,S}} \end{aligned} \tag{47}$$

and derive the third one by

$$\delta_{T,\mathrm{damp}} = -(\delta_{R,\mathrm{damp}} + \delta_{S,\mathrm{damp}}). \tag{48}$$

For the design of the active damping filtering function

$$D(s) = \frac{m_{\mathrm{damp}}}{u_{C_1}} = k \cdot F(s) \tag{49}$$

the filter type $F(\mathrm{s})$ and the active damping factor k have to be selected. An important requirement for the filter is the sufficient suppression of the fundamental component of the filter capacitor voltage $u_{C_{1,50\,\mathrm{Hz}}}$ in order not to introduce an additional 50 Hz component to the duty cycle. Here, a digital Bessel high-pass filter of third order with a cutoff frequency of 1 kHz and an attenuation of -78 dB at 50 Hz was selected. It can be shown that due to the characteristic shape of the Bessel filter, it manipulates the phase of the open loop inner control path less compared to other filter structures such as Chebyshev, Cauer, or Butterworth filters. Since the digital high-pass filter is only working until the switching frequency, it performs the required bandpass filtering function.

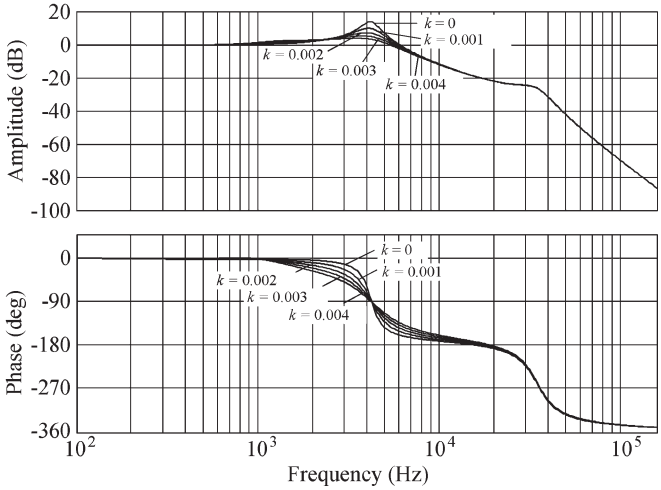

Fig. 9. Bode diagram of the transfer function $G(s) = u_{C_1}/u_N$ for different damping factors k (with $L_{\mathrm{mains}} = 50\ \mu$H).

The damping effect can be observed in the transfer functions that are plotted in Fig. 9 for different k-factors. Obviously, the resonant peak at the resonance frequency is lowered with increasing damping factors. However, the damping should not be chosen too high. One reason is the loss of phase margin and/or decrease of bandwidth of the inner current control loop. Second, the amplitudes of the damping coefficients (47), (48) should not exceed considerably the reserved modulation space of $|\delta_{i,\mathrm{damp}}| \leq 0.1$ for practical cases of mains voltage disturbances. With this, the damping factor of $k = 0.002$ is selected as a good compromise.

The effect of the active damping scheme will be proved by experimental measurements in Section VII.

VI. Controller Design

Based on the small-signal model derived in Section III, the appropriate controllers for the inner current loop and the outer voltage loop have to be selected for the critical operating point.

A. Inner DC Current Control Loop

Once a model of the system is found and verified (cf., Section III), the critical operating condition is identified (cf., Section IV), the control structure is decided, and the active damping function $D(s)$ is determined (cf., Section V), the ultimate task is the controller design, where all of the aforementioned issues have to be considered. A control-oriented block diagram for the inner control loop is depicted in Fig. 10.

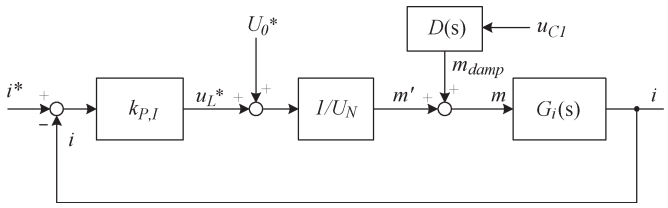

Fig. 10. Block diagram of the inner current control loop.

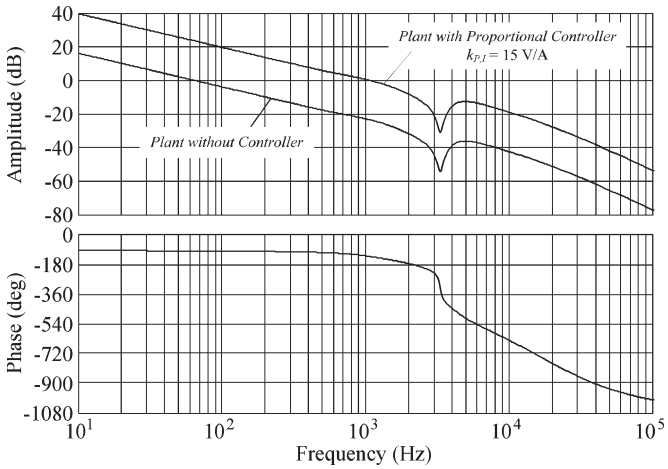

Fig. 11. Open loop bode diagram of the inner dc current control loop without controller and with the selected controller ($k_{P,I} = 15$ V/A).

The bode diagram in Fig. 11 shows that a purely proportional controller

$$K_I(s) = k_{P,I} \tag{50}$$

is sufficient due to the integral behavior of the plant below the input filter resonance frequency.[4] The selection of the appropriate controller gain is naturally a tradeoff between dynamics and stability. For the case at hand, a gain of

$$k_{P,I} = 15 \text{ V/A} \tag{51}$$

was selected.

B. Outer Output Voltage Control Loop

For the design of the output voltage controller, the whole dynamics of the plant including the load current feedforwarding (cf., Section V-A) and the closed inner control loop (cf., Section VI-A) have to be considered.

Generally, the bandwidth and therefore the gain of the output voltage loop has to be much lower than twice the mains frequency to suppress the 100 Hz component of the output voltage for a mains phase failure and keep the reference power P^* and the reference conductance G^* constant over one mains period. To achieve a bandwidth of $f_{\mathrm{BW}} = 1$ Hz and a sufficient phase margin for ensuring an overshoot-free step response ($\varphi_M > 70°$) a purely integral controller with

$$k_{I,U} = 0.43 \text{ A} \cdot \text{rad}/(\text{V} \cdot \text{s}) \tag{52}$$

[4]Because of the low dynamics of the outer output voltage control loop, the output voltage can be regarded as constant for the inner loop.

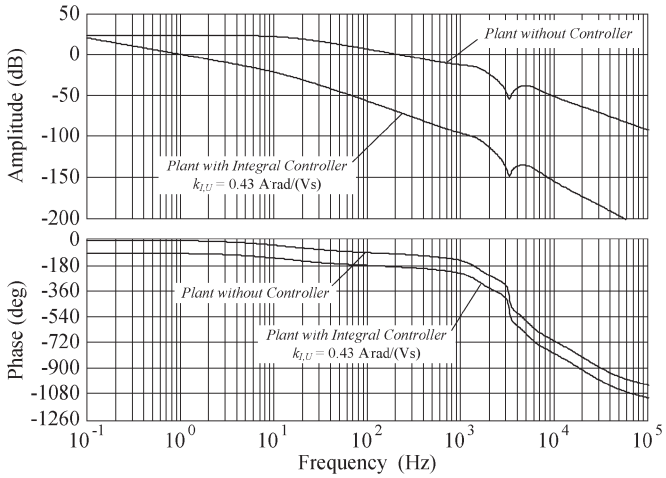

Fig. 12. Open-loop Bode diagram of the outer output voltage control without controller and with the selected controller [$k_{I,U} = 0.43$ A · rad/(V · s)].

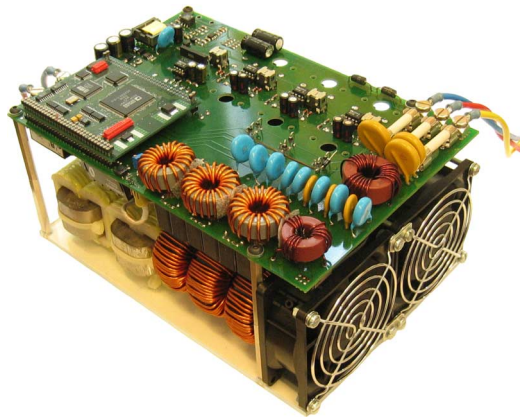

Fig. 13. 5-kW prototype of the VRX-4 rectifier including DSP control board and EMC input filter. Overall, dimensions: 240 mm × 160 mm × 120 mm.

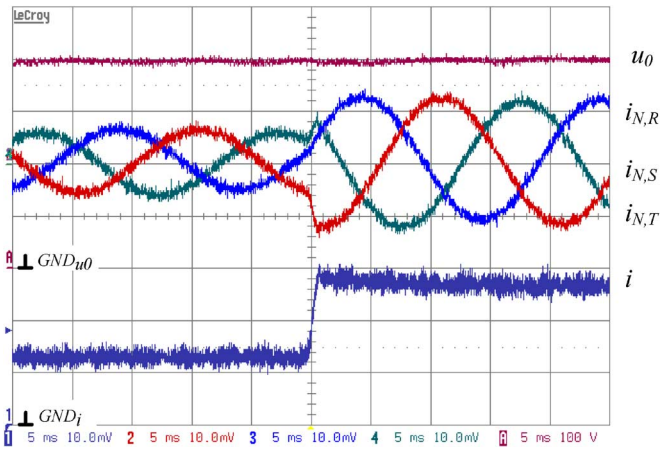

Fig. 14. Voltage and current waveforms for a sudden load step (2.76 kW → 5.52 kW) (voltage scale: 100 V/div, current scale: 5 A/div, time scale: 5 ms/div).

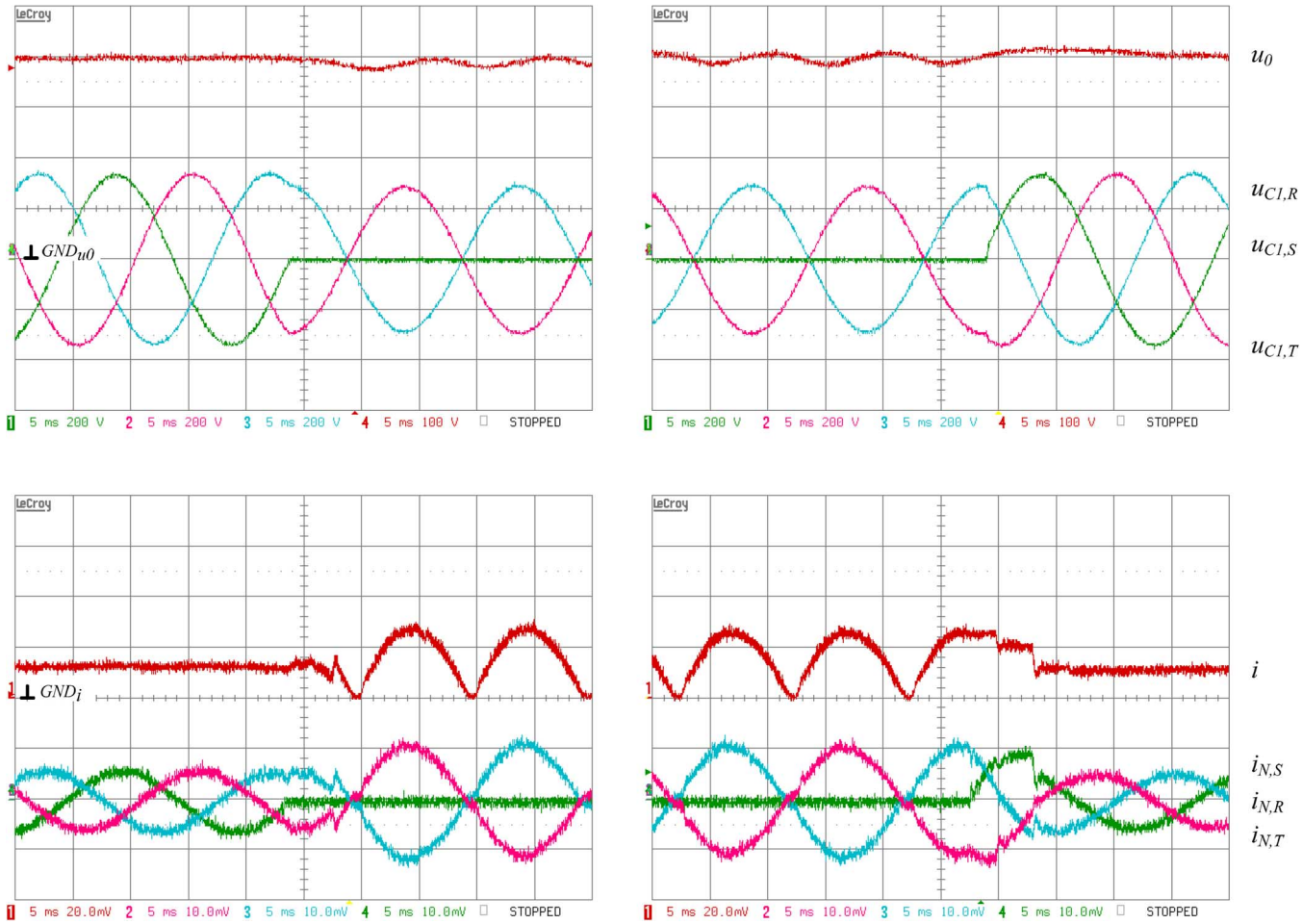

Fig. 15. Experimental results for a phase loss and a reconnection of phase S. Time behavior of output voltage u_0, input filter capacitor voltages $u_{C_{1,i}}$, dc link current i, and mains phase currents $i_{N,i}$. Voltage scales: u_0: 100 V/div, $u_{C_{1,i}}$: 200 V/div, current scales: i, $i_{N,i}$: 10 A/div, time scale: 5 ms/div.

is selected. The Bode diagram of the plants with and without the voltage controller is shown in Fig. 12.

For the loss of one phase, which represents the worst case, the capacitor voltage ripple (peak-to-peak value) according to

$$e_{U,p-p} = \Delta u_{p-p,100\,\mathrm{Hz}} = 2 \cdot \frac{P_0}{U_0} \frac{1}{2\omega C_0} = 53\ \mathrm{V} \tag{53}$$

would cause with this controller (52) a reference power ripple (peak-to-peak value) of

$$\Delta P^*_{p-p} = e_{U,p-p} \cdot \frac{k_{I,U}}{2\pi \cdot 100\ \mathrm{Hz}} \cdot U^*_0 = 14.5\ \mathrm{W} \tag{54}$$

which is less than 0.3% of the rated output power.

VII. Experimental Verification

The proposed control structure has been implemented on a DSP board and tested on a 5-kW hardware prototype of the VRX-4 rectifier system (cf., Fig. 13). In the following, the features of the robust control scheme that were discussed in Section V will be verified by measurement results.

First, to show the robustness of the control to load variations, a load step from half load to full load was performed. The waveforms in Fig. 14 prove that the dc link current and therefore also the mains currents immediately change their amplitude due to the load current feedforward (cf., Section V-A), while the output voltage remains on a constant level.

For a loss of one mains phase the measurement results are shown in Fig. 15. It can be seen that the two remaining phases maintain with sinusoidal input currents in phase with the input voltages, while the dc-link current then also has sinusoidal shape due to the dc current-shaping circuit (cf., Section V-B) and the output voltage shows a 100-Hz ripple. For the phase loss as well as the reconnection of the phase the new peak values of the filter capacitor voltages are detected after a quarter mains period and therefore the power reference and the current reference for the underlying control loop are adapted without affecting the output voltage significantly.

In Fig. 16, the effect of the active damping technique (presented in Section V-D) is shown. The reaction of the input filter capacitor voltage $u_{C_{1,R}}$ was observed for a sudden step of the mains voltage amplitude appearing at the moment of the maximum value of $u_{C_{1,R}}$. Apparently, the active damping scheme exhibits a great improvement in the time behavior of the capacitor voltage. While the amplitude of the overshoot cannot

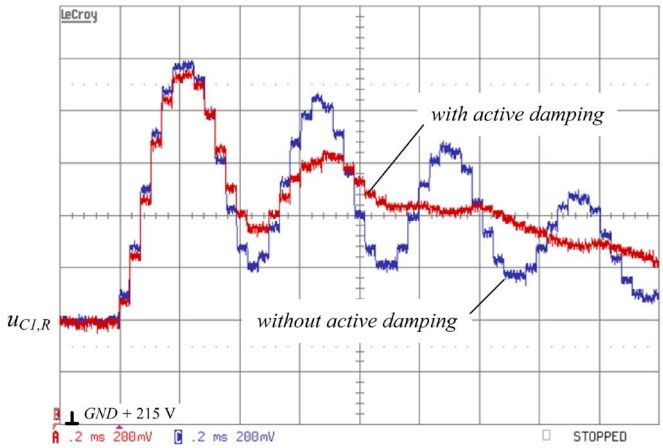

Fig. 16. Filter capacitor voltage waveforms $u_{C_{1,R}}$ (local averaged values) for a sudden step of the mains voltage amplitude $\hat{U}_N$ of 70 V (from 255 to 325 V) (voltage scale: 20 V/div, time scale: 200 μs/div).

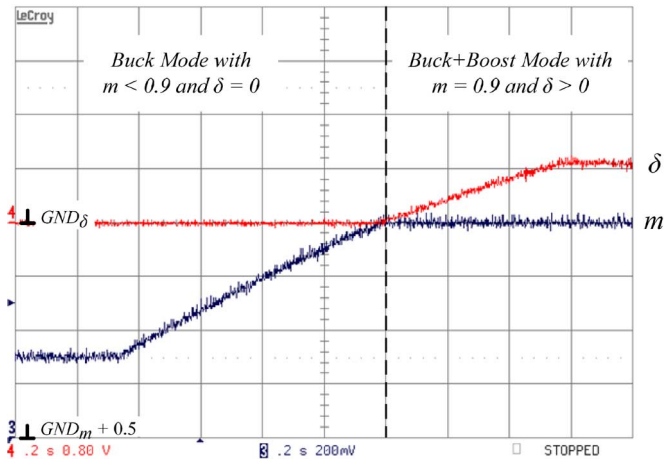

Fig. 17. Time behavior of the modulation index m of the buck-type rectifier input stage and the duty cycle δ of the boost output stage for a stepwise change of the voltage reference u_0^* from pure buck operation ($m = 0.65$, $\delta = 0$) to buck+boost operation ($m = 0.9$, $\delta = 0.1$). Duty cycle scales (m, δ): 0.1/div, time scale: 200 ms/div).

be reduced notably with this measure, the input filter capacitor voltage shows a well-damped time behavior compared to the operation without active damping scheme.

Finally, the smooth transition between buck mode and buck+boost mode due to the common current controller (cf., Section V-C) is illustrated in Fig. 17. Because of a sudden change of the voltage reference u_0^* from a value below the maximum buck rectifier output voltage $u_{\max}$ to a value $u_0^* > u_{\max}$ the converter has to perform a transition from pure buck mode ($m = 0.65$, $\delta = 0$) to buck+boost mode ($m = 0.9$, $\delta = 0.1$). According to the proposed control scheme, at the boundary between these two operation modes, the modulation index m of the buck rectifier input stage is simply limited to its maximum value ($m = 0.9$) and the output of the current controller is then used for controlling the duty cycle of the boost converter. Since the controller was designed for the critical operating point of the system (cf., Section IV), stable operation is ensured in both control modes and the transition between the modes is performed in the predicted smooth way.

VIII. Conclusion

The control of the VRX-4 was investigated in this paper. With the proposed robust control scheme the output voltage can be kept constant ($U_0 = 400$ V) and sinusoidal input currents are guaranteed for a wide input voltage range ($U_{N,l-l} = 208$ V, ..., 480 V), for extensive load variations as well as heavily unbalanced mains conditions such as loss of one phase or short-circuit between two phases.

In the course of the control design, a detailed modeling of the system was undertaken, where it was found that the damping effect of switching and conduction losses of the converter has to be considered in the model. Since the system has to operate in two dynamically different control modes due to the wide input voltage range, the worst case operating condition was identified and a common controller for both operation modes was utilized to achieve a smooth transition between the two modes. Furthermore, an active damping scheme for additional damping of the input filter resonance was designed.

All theoretical considerations have been verified by experimental results on a hardware prototype of the system. With the proposed control scheme, the topology is of high interest for rectifiers, where a wide input voltage and/or wide output voltage range is required, e.g., for telecom power supplies or future applications in the More Electric Aircraft area.

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