Design and Experimental Analysis of a Three-Phase Single-Stage 8.5kW Buck-Derived PWM-Rectifier System (VIENNA Rectifier III)

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Abstract

In this paper a practical investigation of a VIENNA Rectifier III is presented. The stresses on the power components are calculated in analytical form based on the analysis of an equivalent DC/DC converter system. This gives the basis for the dimensioning and practical realization of a 8.5kW $400V_{AC}/48V_{DC}$ prototype of the system. There, for system control an outer output voltage control loop and an inner output inductor current control loop are provided and implemented on a digital signal processor (ADSP 21061) which transfers the relative on-times of the power transistors to an EPLD for generation of the gating signals of the power transistors. Finally, the dependency of the efficiency, of the power factor and of the THD of the mains current on the output power as gained from measurements on the prototype are given.

1 Introduction

In [1] a single-stage three-phase PWM rectifier system (VIENNA Rectifier III, cf. Fig.1) with sinusoidal input currents and high-frequency isolated and controlled output voltage has been introduced. The main advantage of this rectifier system is the low realization effort (only five switches) and the buck-derived structure which ensures lower voltage stress on the power semiconductors as compared to a boost-derived system [2]. The design and experimental investigation of this rectifier system is the subject of this paper.

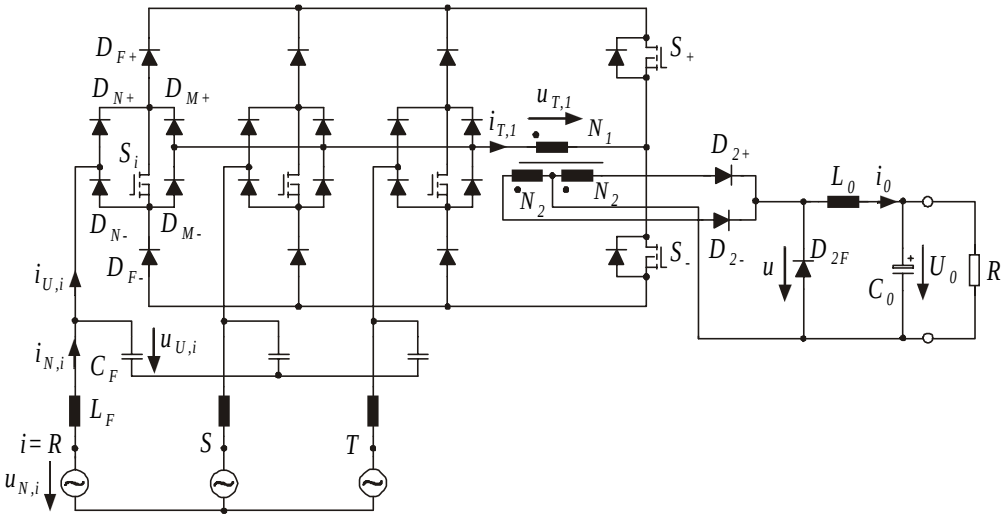

Fig.1: Power circuit of the VIENNA Rectifier III.

In the following, in **section 2** the basic principle of operation of the VIENNA Rectifier III is discussed briefly. Based on this the stresses on the power components are calculated in **section 3** using a simplified DC/DC-model. In **section 4** a 8.5kW laboratory prototype of the rectifier is designed and a breakdown of the total system losses to the individual components is performed. The basic control concept of the rectifier system using an output current controller and an outer output voltage controller is shown in **section 5**. In **section 6** the experimental results, i.e. the measured input current waveform, power factor, and efficiency are compiled. Finally, the advantages and drawbacks of the system are discussed and the scope of future research is given.

1.1 Definitions

The transfer of the constant output inductor current I_O into the input phase currents $i_{U,i}$ (i=R,S,T) is characterized according to [1] by a modulation index

$$M = \frac{\hat{I}_{U,(1)}}{\frac{\sqrt{3}}{2} \cdot \frac{N_2}{N_1} \cdot I_O} \tag{1}$$

where $\hat{I}_{U,(1)}$ denotes the amplitude of the fundamental of an input phase current $i_{U,i}$. N_1 and N_2 denote the number of turns of the high-frequency transformer primary and secondary windings.

The mains voltages are defined by:

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cdot \cos(\varphi_N) \\ u_{N,S} &= \hat{U}_N \cdot \cos(\varphi_N - \tfrac{2\pi}{3}) \\ u_{N,T} &= \hat{U}_N \cdot \cos(\varphi_N + \tfrac{2\pi}{3}) \end{aligned} \tag{2}$$

with

$$\varphi_N = \omega_N \cdot t \tag{3}$$

The switching states are denoted by $j=(s_R,s_S,s_T)_{s+,s-}^{sign(u_{T,1})}$. Thereby s_i=1, i=*R,S,T,+,-*, denotes the turn-on state of a power transistor S_i. Accordingly, the turn-off state of S_i is denoted by s_i=0.

2 Principle of Operation

In analogy to a basic buck converter, the input currents of the rectifier $i_{U,i}$ are composed of pulse width modulated segments of the output current I_0 being impressed by the output inductor. Describing the function in detail, the mains period T_N has to be divided in six mains intervals as defined by the different combinations of signs of the input phase voltages [1]. Fore example in $\varphi_N \in \left[-\frac{\pi}{6},\frac{\pi}{6}\right]$ the switching sequence shown in **Fig.2** is applied. In this mains interval, the input voltage of phase R, $u_{U,R}$, is positive and the input voltages of phase S, $u_{U,S}$, and phase T, $u_{U,T}$, are negative.

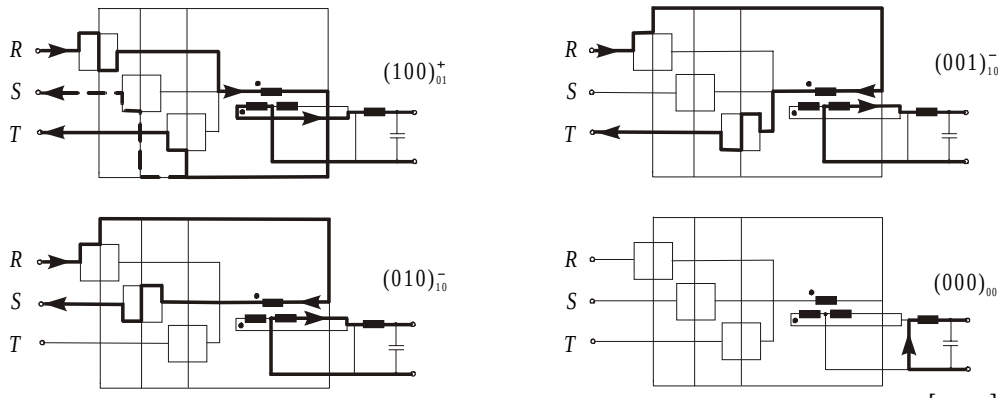

Fig.2: Conduction states for the switching state sequence $(100)_{01}^{+}-(000)_{00}-(001)_{10}^{-}-(010)_{10}^{-}$ in $\varphi_N \in \left[-\frac{\pi}{6},\frac{\pi}{6}\right]$. For the sake of clearness the components are not shown in detail and the current flow is shown by a bold line. The dashed line for $j=(100)_{01}^{+}$ shows the current flow for $u_{U,S}<u_{U,T}$ ($\varphi_N \in \left[-\frac{\pi}{6},0\right]$).

Employing the switching state $j=(100)_{01}^{+}$ the sign of the primary transformer voltage $u_{T,1}$ is positive and the output inductor current is transformed to the input current of phase R and S/T (depending on which phase voltage shows a higher instantaneous value). For $j=(010)_{10}^{-}$ and $j=(001)_{10}^{-}$ the sign of $u_{T,1}$ is negative and the output inductor current is transformed to the input current of phase R and phase S or T. For $j=(000)_{00}$ the output inductor current flows through the freewheeling diode D_{2F}. By proper calculation of the on-times of this four switching states a magnetization of the transformer only with pulse frequency could be achieved besides guiding the local average value of the input current proportional to the input voltage. Furthermore, the output voltage is controlled to a constant value.

The current flow and the sign of the primary transformer voltage in the other mains intervals can be investigated in an analogue manner.

3 Stress on the Power Components

In order to calculate the stresses on the power components in a simplified way, a purely ohmic mains behavior is assumed and/or the capacitive loading of the mains due to the filter capacitors C_F is neglected. As already mentioned and as shown in **Fig.3**(a), the mains period T_N is divided in six intervals as defined by the different combinations of signs of the input phase voltages.

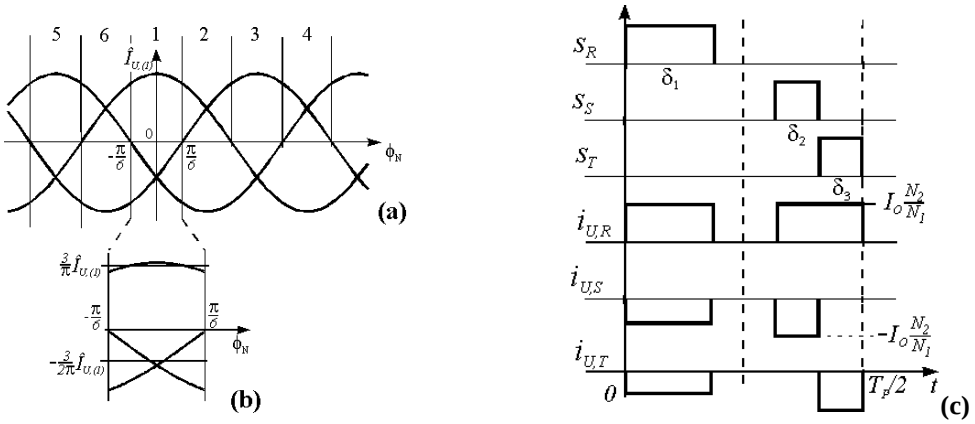

Fig.3: Partition of the mains period in six 60°-wide intervals **(a)** and local averaging of the fundamental of the input phase currents over a 60°-interval **(b)**. Furthermore shown are the gating signals of the switches S_R, S_S, S_T and the formation of the input phase currents $i_{U,R}$, $i_{U,S}$, $i_{U,T}$ from segments of the transformed output current I_O **(c)**.

Within each mains interval the sinusoidal input currents are replaced by the average values over the 60°-interval (cf. (4) and (5), Fig. 3(b)) and/or the system is considered as a basic DC/DC-converter.

$$\bar{I}_{N,R}=\frac{3}{\pi}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\hat{I}_{U,(1)}\cdot\cos\varphi_N\cdot d\varphi_N=\frac{3}{\pi}\hat{I}_{U,(1)} \tag{4}$$

$$\bar{I}_{N,S}=\bar{I}_{N,T}=\frac{3}{\pi}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\hat{I}_{U,(1)}\cdot\cos\left(\varphi_N\pm\tfrac{2\pi}{3}\right)\cdot d\varphi_N=-\frac{3}{2\pi}\hat{I}_{U,(1)}=-\frac{\bar{I}_{N,R}}{2}\ . \tag{5}$$

The formation of the input currents according to the switching stages in $\varphi_N\in\left[-\frac{\pi}{6},\frac{\pi}{6}\right]$ (c.f. Fig.2) is given in Fig.3(c). In order to achieve the desired average values of the input currents $\bar{I}_{i,R}$ the duty cycles δ_i have to be set as

$$\delta_1=\frac{1}{2}\cdot\frac{\bar{I}_{N,R}}{I_O\cdot\frac{N_2}{N_1}}=\frac{3}{2\pi}\cdot\frac{N_1}{N_2}\cdot\frac{\hat{I}_{U,(1)}}{I_O}, \tag{6}$$

$$\delta_2=\frac{1}{2}\cdot\frac{-\bar{I}_{N,S}}{I_O\cdot\frac{N_2}{N_1}}=\frac{3}{4\pi}\cdot\frac{N_1}{N_2}\cdot\frac{\hat{I}_{U,(1)}}{I_O}=\frac{\delta_1}{2}, \tag{7}$$

$$\delta_3 = \frac{1}{2} \cdot \frac{-\bar{I}_{N,T}}{I_O \cdot \frac{N_2}{N_1}} = \frac{\delta_1}{2}. \tag{8}$$

Calculating the current stress of the switch S_R, one can see in Fig.2 that the transformed output inductor current flows through the switch S_R only for $j=(000)_{00}$. Therefore, the average current of S_R in the mains interval 1 results to

$$I_{SR,avg[1]} = \frac{N_2}{N_1} \cdot I_0 \cdot \delta_1 = \frac{3}{2\pi} \cdot \hat{I}_{U,(1)}, \tag{9}$$

and the square of the rms value results to

$$I^2_{SR,rms[1]} = \left(\frac{N_2}{N_1} \cdot I_0\right)^2 \cdot \delta_1 = \frac{\sqrt{3}}{\pi \cdot M} \cdot \hat{I}^2_{U(1)}. \tag{10}$$

Applying this algorithm to all 6 mains intervals, the current stress of the switch S_R results to

$$I_{SR,avg} = \frac{1}{6}\sum_{i=1}^{6} I_{SR,avg[i]} = \frac{1}{\pi} \cdot \hat{I}_{U,(1)}, \tag{11}$$

$$I^2_{SR,rms} = \frac{1}{6}\sum_{i=1}^{6} I^2_{SR,rms[i]} = \frac{2}{\sqrt{3} \cdot \pi \cdot M} \cdot \hat{I}^2_{U,(1)}. \tag{12}$$

The equations describing the current stresses on the power components are compiled in **Tab.I**.

Table I: Current stress on the power components

	S_i	S_+, S_-	D_{N+}, D_{N-},	D_{F+}, D_{F-}, D_{M+}, D_{M-}	D_{2+}, D_{2-}	D_{2F}	C_F	N_1
I_{avg}	$\frac{1}{\pi} \cdot \hat{I}_{U,(1)}$	$\frac{3}{2\pi} \cdot \hat{I}_{U,(1)}$	$\frac{1}{\pi} \cdot \hat{I}_{U,(1)}$	$\frac{1}{2\pi} \cdot \hat{I}_{U,(1)}$	$\frac{3}{2\pi} \cdot \hat{I}_{U,(1)} \cdot \frac{N_1}{N_2}$	$I_O - \frac{3}{\pi} \cdot \frac{N_1}{N_2} \hat{I}_{U,(1)}$		
I^2_{rms}	$\frac{2}{\sqrt{3} \cdot \pi \cdot M} \cdot \hat{I}^2_{U,(1)}$	$\frac{\sqrt{3}}{\pi \cdot M} \cdot \hat{I}^2_{U,(1)}$	$\frac{2}{\sqrt{3} \cdot \pi \cdot M} \cdot \hat{I}^2_{U,(1)}$	$\frac{1}{\sqrt{3} \cdot \pi \cdot M} \cdot \hat{I}^2_{U,(1)}$	$\frac{\sqrt{3}}{\pi \cdot M} \cdot \hat{I}^2_{U,(1)} \cdot \frac{N_1^2}{N_2^2}$		$\left(\frac{4 \cdot \sqrt{3}}{3 \cdot \pi \cdot M} - \frac{1}{2}\right) \cdot \hat{I}^2_{U,(1)}$	$\frac{2 \cdot \sqrt{3}}{\pi \cdot M} \cdot \hat{I}^2_{U,(1)}$

4 System Design

The laboratory prototype of the PWM rectifier is designed based on the following specifications:

Input voltage (line to line)	U_N	=	$400V_{rms}$
Output voltage	U_0	=	48V
Output power	P_0	=	8.5kW
Output current	I_0	=	177A
Switching frequency	f_P	=	32kHz.

Assuming a worst-case efficiency of η= 85% the amplitude of the input current fundamental $\hat{I}_{U,(1)}$ has to be

$$\hat{I}_{U,(1)} = \frac{P_0}{\eta \cdot U_N \cdot \sqrt{3}} \cdot \sqrt{2} = 20.4\text{A}. \tag{13}$$

Taking into account voltage spikes of about 150V amplitude as caused by the stray inductance of the transformer and an amplitude of the input voltage of 400*√2 =566V the blocking capability of the primary side power semiconductors should be higher than 800V. For a peak input voltage of 566V and a transformer turns ratio of N_1:N_2=12:2 the blocking capability of the secondary side diodes has to be at least 200V.

In order to avoid a resonant condition at the system input, proper damping of the input filter has to be provided. As shown in **Fig.4** the input filter is formed by a capacitor C_F=13µF, two inductors L_{F1}=100µH, L_{F2} =700µH and a damping resistor of R_D=2.0 Ω per phase [3]. Due to the inductor L_{F2},

the damping resistor R_D is not active for the fundamental component of the input current. Therefore, the power losses of the damping resistor remain at low levels. Hence, the size of the input filter is increased by ≈30% as compared to a filter realization without damping.

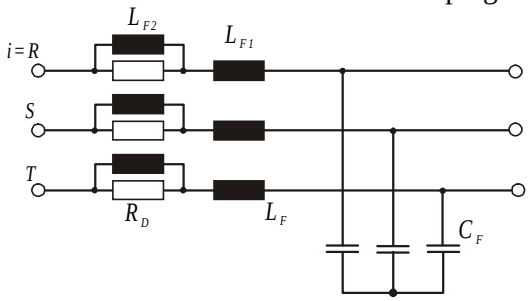

Fig.4: Damped input filter

The characteristic values and types of the components employed for the practical realization of the laboratory prototype are listed in **Tab.II**.

Table II: Employed power components

	S_i, S_+, S_-	D_{N+}, D_{N-},D_{F+}, D_{F-}, D_{M+}, D_{M-}	D_{2+}, D_{2-}, D_{2F}	C_F	L_{F1}	L_{F2}	Transformer	L_O
Type	APT10025JVFR	RURG75120	DSEI 2x121	AVX FFV36	Micrometals T184-40	Micrometals T184-40	4 * E65	AMCC-25
	1000V	1200V	200V	13µF, 900V	N=26, L=100µH	N=68, L=700µH	$\frac{N_1}{N_2}=\frac{12}{2}$	N=8,L=12.8µH @200A

4.1 Loss breakdown

The distribution of the total losses to the individual power components at nominal operation (U_N=400V, U_0=48V, P_0=8500W) is given in the following. Thereby, the input current fundamental is assumed to be $\hat{I}_{U,(1)}$=20.4A and the modulation index results to M=0.8. The current stresses and the power losses resulting for these parameters are compiled in **Fig.5**.

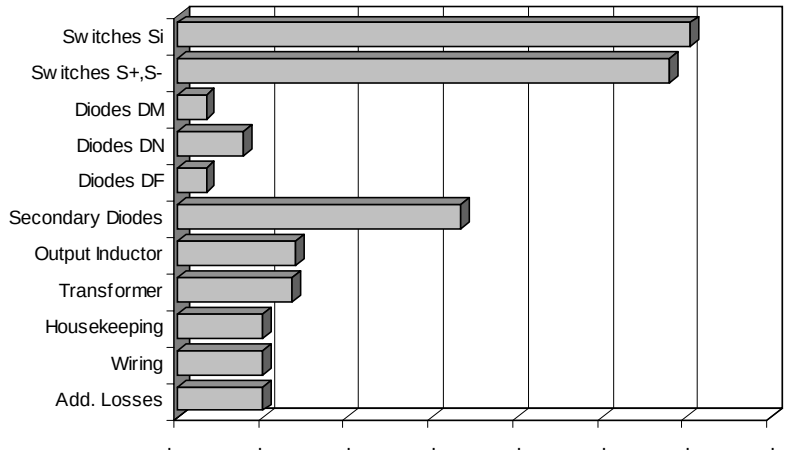

Fig.5: Loss breakdown to the individual power components in Watts at U_N=400V, U_0=48V, P_0=8500W. The values for housekeeping, wiring and additional losses are estimations.

The overall losses of the rectifier are P_L =1121W which results in a efficiency of

$$\eta = \frac{P_0}{P_0 + P_L} = 88{,}3\%. \qquad (14)$$

As shown in Fig.5, the main losses are caused by the switches S_i (i=R,S,T) , S_+, S_- and by the output diodes. Using two power MOSFETs in parallel one could save 144W at S_i and 98W at S_+ and S_- and would achieve an efficiency of 90.6%.

5 Control Structure

The structure of the implemented control is shown in **Fig.6.** The output voltage controller *F(s)* defines the reference value of the current i_0 in the output inductor L_0. The output current controller *G(s)* outputs a reference value u^* for the rectified transformer secondary voltage. A signal processor (ADSP-21061) calculates the relative on-times of the power transistors S_i under consideration of the actual input voltages $u_{U,i}$ and of the reference value u^*.

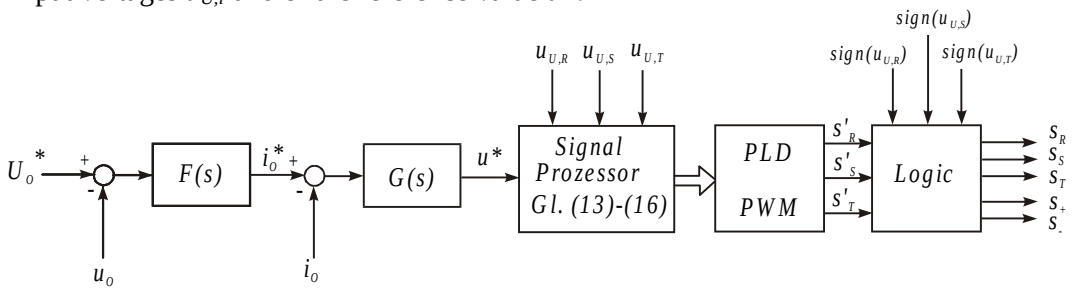

Fig.6: Structure of the implemented control of the VIENNA Rectifier III; output voltage controller *F(s)*, output current controller *G(s)*, digital signal processor (ADSP21061) calculating the relative on-times of the power transistors according to (15) – (18). Based on this PWM-signals s_R‘, s_S‘, s_T‘ are generated by a PLD (Programmable Logic Device – Altera EPM7128) and are decoded into the gating signals s_R, s_S, s_T, s_+, s_- for the power transistors by a combinatorial logic [1].

For the generation of the pulse pattern a PLD (ALTERA EPM7128) is employed which outputs three auxiliary switching functions s_R‘, s_S‘, s_T‘ showing a symmetry to the center of a pulse period (the on-times of the auxiliary switching functions s_i´ are defined by adding relative on-times δ_j). The actual switching pattern s_R, s_S, s_T then is derived by a decoding combinatorial logic which considers the signs of the input phase voltages and/or the input voltage sector number (cf. Fig.3(a)).

For the calculation of the on-times of the switching states, e.g., the following equations are used for $\varphi_N \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$ and/or sector 1 (for the sake of clarity only the switching state combination (s_R,s_S,s_T) is used for the denomination of the relative on-times instead of $j=(s_R, s_S, s_T)_{s+,s-}^{sign(u_T,1)}$.

$$u_{U,RS} \cdot \delta_{(100)} - u_{U,RT} \cdot \delta_{(001)} - u_{U,RS} \cdot \delta_{(010)} = 0 \tag{15}$$

$$u_{U,RS} \cdot \delta_{(100)} + u_{U,RT} \cdot \delta_{(001)} + u_{U,RS} \cdot \delta_{(010)} = \frac{N_1}{N_2} \cdot u^* \tag{16}$$

$$\frac{i_R}{i_T} = \frac{u_{U,R}}{u_{U,T}} \tag{17}$$

$$\delta_{(100)} + \delta_{(000)} + \delta_{(001)} + \delta_{(010)} = 1 \tag{18}$$

Equation (15) assures, that the volt seconds which are applied to the transformer primary winding equal zero in the average over a pulse-period and/or that the transformer magnetization is only with pulse frequency. Equation (16) describes the formation of the desired rectified transformer secondary voltage u^*. Equation (17) defines an ohmic fundamental mains behavior of the rectifier (i_R and i_T denote local average values of the corresponding input phase currents $i_{U,R}$ and $i_{U,T}$) and (18) ensures that the sum of the individual duty cycles equals one. The system of equations shows only a single solution for regular mains conditions (balanced mains, no zero-sequence component) and is implemented in the digital signal processor for each mains interval.

Subsequently, the calculated duty cycles are modified in order to achieve an active volt second balancing of the transformer which is discussed in [4]. There, the magnetizing current is measured by a trough-hole current transducer with 6 windings carrying the transformer primary current and one winding carrying the transformer secondary current in the opposite direction. The resulting signal is

sampled and used for a correction of the transformer volt seconds and/or transistor on-times in the following pulse interval.

5.1 Output Inductor Current Control Loop

Due to parasitic effects such as voltage drops, different characteristics of the gate drive circuits, non sinusoidal input voltages and the low value of the output inductance (12µH@200A) the inductor current would differ in practice from the theoretical constant value. This would result in heavily disturbed input current and a high current stress on the input and output capacitors. Therefore, the current through the output inductor has to be controlled to a constant value.

Considering the input filter in connection with an inner mains inductance of about 20µH-100µH the resonant frequency of the input filter is in between 3.1 - 4.0kHz. In order to avoid oscillations of the input filter due to the constant power input characteristic (negative incremental input impedance of the system) the cut-off frequency of the output current controller should be lower than 500Hz.

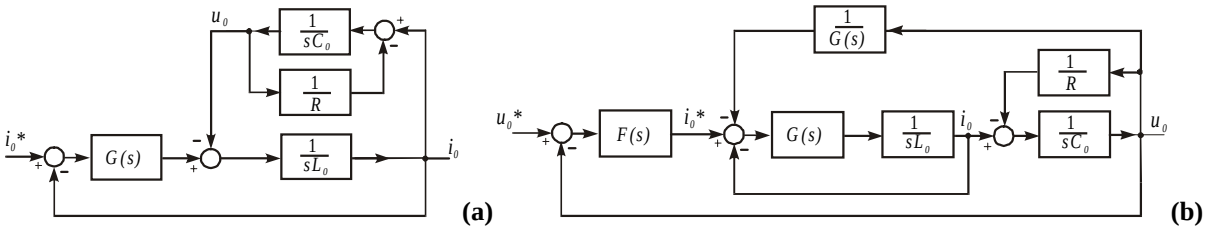

Fig.7: Low-frequency estimation (with reference to the resonant frequency of the input filter) of the current control loop (a) and output voltage control loop (b).

Employing a current controller *G(s)* as defined by (19) with T_1 =47µs and K_I=0.057V/A the inner current control loop can be approximated by a second order delay (poles of the characteristic polynom: $p_{1,2}$ =2350±j1350[s^{-1}] @ P_0 =8.5kW and $p_{1,2}$ =2230±j1120[s^{-1}] @ P_0 =1000W) which results in a current controller bandwidth of about 370Hz.

$$G(s) = \frac{K_I}{(1 + s \cdot T_1)} \tag{19}$$

5.2 Output voltage control loop

Because the outer output voltage control loop has to show a lower bandwidth than the inner current control loop, the cut-off frequency of the voltage controller has been chosen as 200Hz. This is achieved with a PI-type controller with K_P=5A/*V* and T_N=0.28ms.

$$F(s) = \frac{K_P}{T_N} \frac{1 + sT_N}{s} \tag{20}$$

A detailed analysis of both control loops should be omitted here for the sake of brevity.

6 Experimental Results

The experimental results given in the following are gained from a laboratory prototype of the rectifier system at 400V input voltage, 48V output voltage and an output power of 3.8kW (I_O=80A) using the output inductor current control loop shown in Fig7(a). There, the system shows an efficiency of 90% and a power factor of 0.987.

The input voltage $u_{U,R}$ and the corresponding mains current $i_{N,R}$ are shown in **Fig.8**. Due to the input filter capacitor a minor phase leg of the input current with reference to the input voltage does occur.

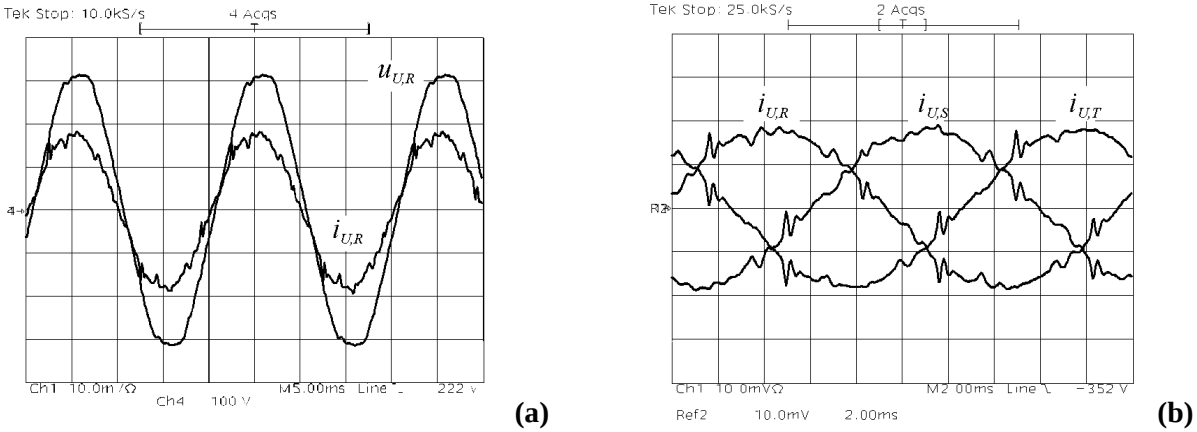

Fig.8: Input voltage $u_{U,R}$ (100V/div) and corresponding mains current $i_{N,R}$ (5A/div) **(a)** and input currents of all three phases **(b).**

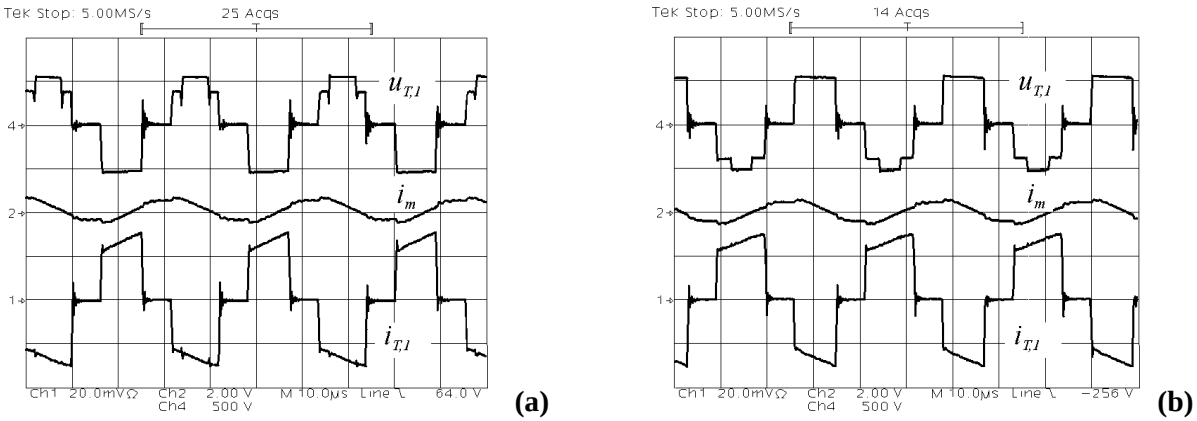

Fig.9: Voltage across the primary windings of the transformer $u_{T,1}$ (500V/div), magnetizing current i_m (3.33A/div) and current through the primary winding of the transformer $i_{T,1}$ (10A/div) in mains interval 1 **(a)** and interval 2 **(b)** (cf. Fig.3(a)).

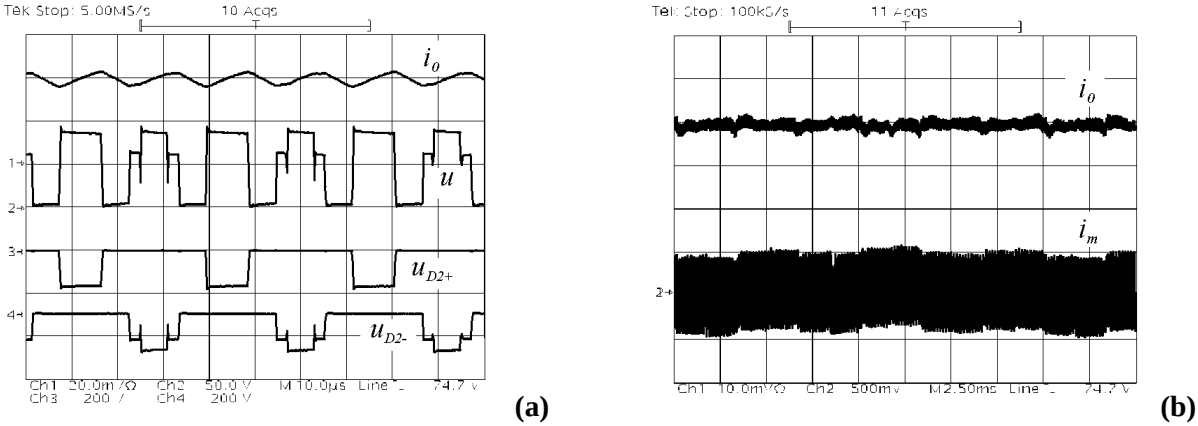

Fig.10: Output inductor current i_0 (40A/div), rectified secondary side voltage u (50V/div) and blocking voltage of the secondary side diodes D_{2+} and D_{2-} (200V/div) **(a)**. Furthermore shown are the output inductor current (20A/div) and the magnetizing current (0.83A/div) within one mains period **(b)**.

The time behavior of the voltage at the primary windings of the transformer $u_{T,1}$, the magnetizing current i_m and the current through the transformer primary winding $i_{T,1}$ are shown in **Fig.9** for mains interval 1 and 2. The magnetizing current is measured by a through-hole current transducer with 6 windings carrying the transformer primary current and one winding carrying the transformer secondary current in the opposite direction. [4].

In **Fig.10**(a) the output current i_0 and the rectified secondary side voltage u are given. Furthermore, the blocking voltages of the secondary side diodes D_{2+} and D_{2-} are shown. Figure 10(b) shows the output current i_0, which is controlled by the output current controller and the measured magnetizing current i_m; the local average value of the magnetizing current is controlled by active transformer volt seconds balancing.

The drain-to-source voltage of the power transistors S_R, S_S, S_T and S_+, S_- is given in **Fig.11** in combination with the current through the primary winding of the transformer $i_{T,1}$.

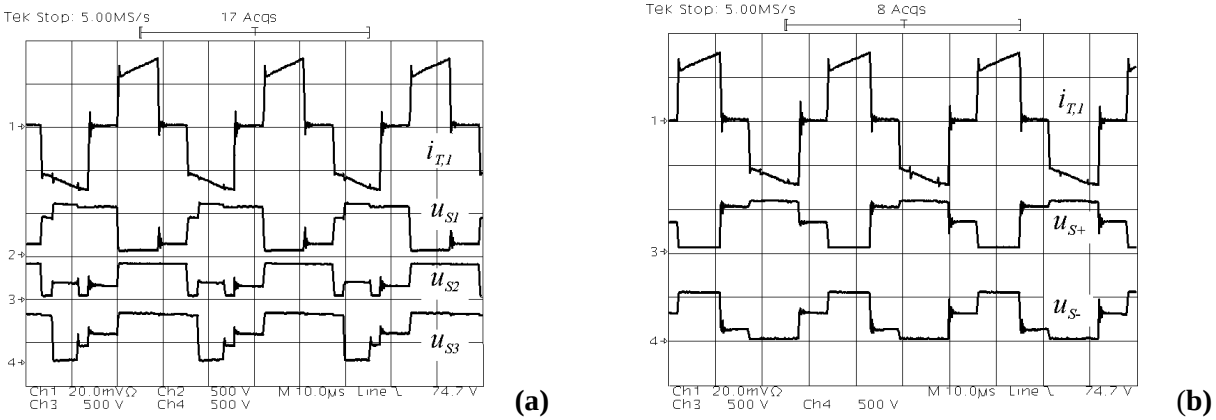

Fig.11: Current through the primary winding of the transformer $i_{T,1}$ (10A/div) and drain-to-source voltage of the switches S_R, S_S, S_T **(a)** and S_+, S_- **(b)** at (500V/div).

Characteristic parameters of the rectifier system, i.e. efficiency, power factor and total harmonic distortion as determined experimentally at 400V input and 48V output voltage are listed in **Tab.III** in dependency on the output power and shown graphically in **Fig.12**.

Table III: Measured rectifier behavior

P_0	480	960	1920	2880	3864	4872	5856	6696	7680	8472	[W]
I_0	10	20	40	60	80.5	101.5	122	139.5	160	176.5	[A]
P_I	630	1128	2163	3195	4264	5400	6492	7521	8730	9673	[W]
Efficiency	72.7	82.9	87.6	89.3	90.0	89.7	89.8	88.7	87.7	87.3	[%]
THD_V	2.5	2.5	2.6	2.6	2.5	2.6	2.6	2.6	2.6	2.6	[%]
THD_A	19.7	14.0	8.3	6.8	7.1	7.3	7.5	7.9	8.5	9.0	[%]
PF	0.667	0.853	0.954	0.979	0.987	0.991	0.994	0.994	0.994	0.994	

According to Fig.12 the rectifier system shows a high efficiency, a good power factor and a low THD_A of the input current in a wide output power range:

- Efficiency >87% @ P_0=[2000W..8500W]
- Power Factor >0.98 @ P_0=[3000W..8500W]
- THD_A <9% @ P_0=[2000W..8500W]

A photo of the 8.5kW prototype of the VIENNA Rectifier III as used for the experimental analysis is shown in **Fig.13**. The overall dimensions (width ∗ length ∗ height) of the power stage are 33cm ∗34cm ∗14cm (13in ∗13.4in ∗5.5in).

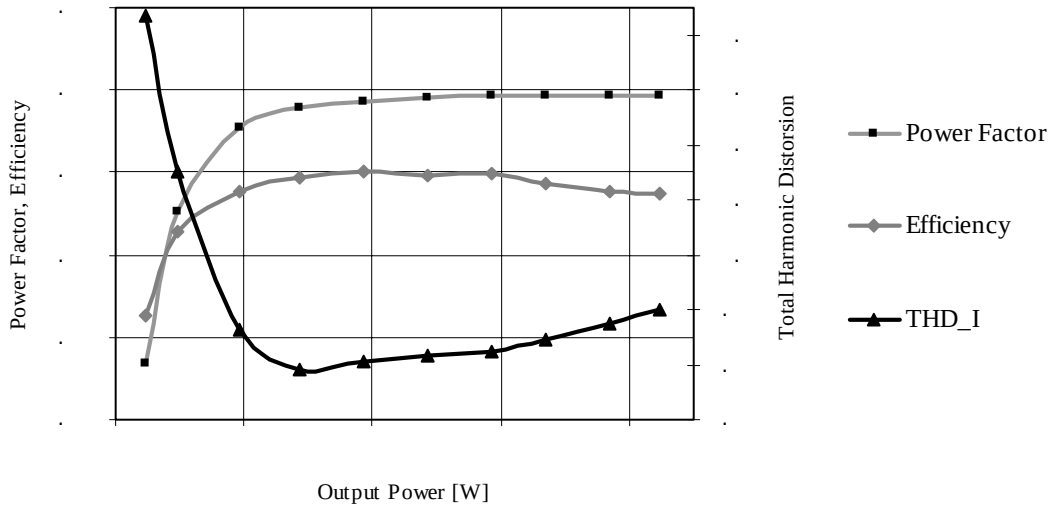

Fig.12: Dependency of power factor λ, efficiency and total harmonic distortion (THD_A) of the input current on the output power at 400V input voltage and 48V output voltage.

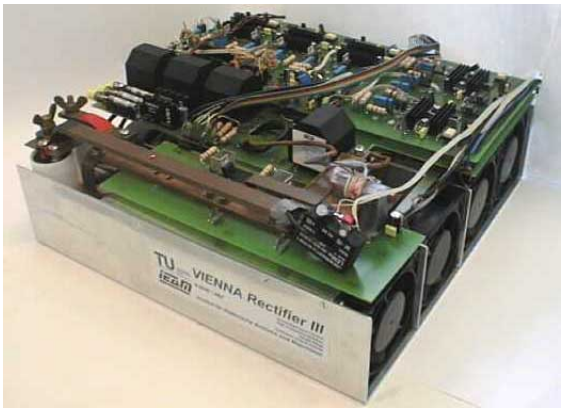

Fig.13: Power stage of the 8.5kW prototype.

7 Conclusions

As shown in this paper, the concept of the VIENNA Rectifier III is verified experimentally. The single-stage, buck-derived rectifier system includes a high-frequency transformer and provides a controlled DC output voltage, a high power factor and high efficiency. Besides an output inductor current control and an output voltage control, the volt seconds applied to the transformer are balanced actively by a magnetizing current controller. The control of the converter is realized using a digital signal processor (ASDP 21061 from Analog Devices) and two programmable logic devices (PLD from Altera) .

Due to the low resonance frequency of the input filter and due to the wide range of variation of the inner mains inductance the bandwidth of the output voltage control employed in the proposed control structure is limited to a few 100Hz in order to avoid a resonance condition of the input filter. An improved control structure which does include an active damping of the input filter [5], [6] is currently under consideration and will be published at a future conference.

The limited bandwidth of the output voltage control, does make the rectifier system more suitable for the realization of high power industrial process power supplies rather than for telecommunications applications.

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