Multi-objective Optimization and Comparative Evaluation of Si Soft-switched and SiC Hard-switched Automotive DC-DC Converters

S. Waffler and M. Preindl and J.W. Kolar
Power Electronic Systems Laboratory
ETH Zurich
8092 Zurich, Switzerland
Email: waffler@lem.ee.ethz.ch

***Abstract*—The application of soft-switching concepts or Silicon Carbide (SiC) devices are two enabling technologies to further push the efficiency, power density or specific weight of power electronics converters. For an automotive application, such as a dc-dc converter that interconnects the high voltage battery or ultra-capacitor in a hybrid electrical vehicle (HEV) or a fuel cell vehicle (FCV) to the dc-link, costs and failure rate are likewise of importance. Due to increasing requirements on multiple of these converter characteristics the comprehensive multi-objective optimization of the entire converter system gains importance.**

Thereto, this paper proposes an optimization method to explore the limits of power density as a function of the switching frequency and the number of phases of non-isolated bi-directional multi-phase dc-dc converters operated with soft-switching and Silicon devices and hard-switched converters that take advantage of SiC devices. In addition, the optimization includes an algorithm to determine the chip size required for the semiconductor devices under consideration of the thermal characteristics and efficiency requirements. Based on detailed analytical volume, loss and cost models of the converter components as well as on measurements demonstrative results on the optimum converter designs are provided and evaluated comparatively for the different converter concepts.

***Index Terms*—dc-dc converter, multi-phase, optimization, soft-switching, Silicon-Carbide**

I. Introduction

Hybrid Electrical Vehicles (HEV) and Fuel Cell Vehicles (FCV) typically take advantage of a second power source in addition the combustion engine or the fuel cell (FC) to improve the overall drive train efficiency [1]. That is because the additional power momentarily provided by the energy storage elements such as a high voltage battery or an ultra-capacitor, e.g. in case of acceleration, allows the main power source to be designed for a tighter load range and thus to be operated at a better efficiency. Additionally, the battery or ultra-capacitor is used for regenerative braking.

That is why the dc-dc converter that interfaces the storage element to the dc-link needs to be designed for a bi-directional operation. Furthermore, depending on the drive train design, the battery voltage range may overlap with the dc-link voltage, which requires both a buck and a boost functionality of the dc-dc converter.

One commonly used converter topology for this application is the hard-switched, cascaded, buck+boost converter [2] shown in Fig. 1. When operated in continuous conduction mode (CCM) and with conventional pulse width modulation (PWM) as indicated in Fig. 2 b), the significant switching losses caused by the reverse recovery of Silicon diodes result in a low efficiency.

The alternatives to improve efficiency that have been proposed include a constant-frequency soft-switching modulation strategy (cf. Fig. 2 a)) that allows a Zero Voltage Switching (ZVS) of the switches S_1 to S_4 by a negative offset current I_0 at the beginning of the pulse period [3] and the application of Silicon Carbide (SiC) diodes. It has been shown that with SiC diodes, the switch turn-on losses caused by reverse recovery are reduced by approximately 67% [4].

Besides efficiency, major concerns in the converter design are a low volume, i.e. a high power density ρ_p, and low costs. Since these quantities are influenced by multiple parameters such as the chosen converter topology, the switching frequency f_{sw} or the number of phases N of a multi-phase converter, a

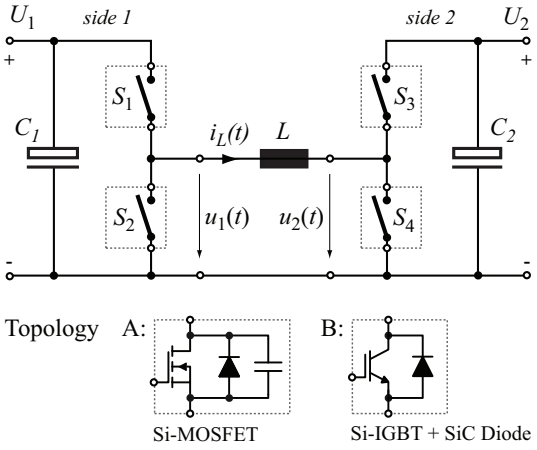

Fig. 1. Topology variants for converter optimization: Topology A using Silicon MOSFET switches S_i and ZVS modulation and Topology B using Silicon IGBTs with anti-parallel SiC diodes and standard PWM modulation in DCM or CCM.

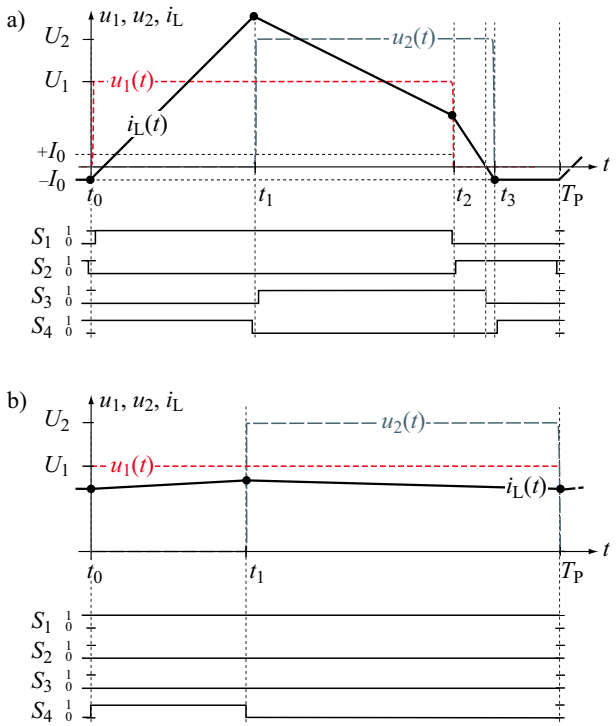

Fig. 2. Half-bridge voltages $u_1(t)$, $u_2(t)$, inductor current $i_L(t)$ and switch S_1 to S_4 gating signals for both topology variants and the same voltage transfer ratio of $U_1/U_2 = 2/3$ and power P.

comprehensive multi-objective system optimization is essential.

For this reason, a optimization algorithm is proposed in section II that identifies the optimum converter design regarding power density for the two candidate topologies shown in Fig. 1: Topology A using ZVS modulation with Silicon MOSFETs and topology B using PWM modulation with Silicon IGBTs and anti-parallel SiC diodes. The basis for the calculations are detailed volume, loss and cost models of the passive components C_1, C_2, L and switches S_i given in section III, section IV and section V and a secondary efficiency-based semiconductor chip size optimizer (cf. section VI). The results of the optimization are given section VII in the form of a comparison, stating the characteristics, advantages and drawbacks of both the topologies.

II. Design Procedure and Parameters

There are several design constraints that affect the converter characteristics such as power density, efficiency, costs and weight. Firstly, besides the specification on the voltage ranges U_1, U_2 at the battery and the dc link side of the converter, there are limits on the ripple amplitudes $\hat{\tilde{u}}_1$ and $\hat{\tilde{u}}_2$ of these voltages. Secondly, there exists a requirement on the overall converter efficiency η such as $\eta > 95\%$ for an transfered power of $P > 0.1P_{\max}$. The maximum power $P_{\max}$ is typically derated by an upper limit $I_{\max}$ that applies to the battery current I_1 and the dc link current I_2. The detailed converter specification applied for the optimization is listed in table I.

TABLE I
Converter Specification

Parameter	Value
Voltage range U_1	150 V .. 450 V
Voltage range U_2	150 V .. 450 V
Ripple amplitude $\hat{\tilde{u}}_1$	1 V
Ripple amplitude $\hat{\tilde{u}}_2$	1 V
Peak power $P_{\max}$	70 kW
Maximum current $I_{\max} = I_1 = I_2$	250 A
Required efficiency η_{req}	95 % for $P > 0.1P_{\max}$

However, there are several degrees of freedom for a converter that meets the electrical specification. Principally, these are the choice of the converter topology, the type of semiconductors and the junction temperature T_j, the cooling concept, the switching frequency f_{sw}, the inductor design and others.

Additionally, with a multi-phase converter design, the ripple quantities and thus also the total volume claimed by the passive components is reduced [3][5] and for a low power P the efficiency is improved by partial operation of N_{on} out of N converter phases that are connected in parallel [6][4].

Taking the degrees of freedom into account, an optimization based on loss, volume and cost models of the converter components is deployed, to identify the optimum converter design. Thereto, under assumption the of additional constraints listed in table II, the topology, N and f_{sw} are varied and power density and semiconductor costs are determined as a result of the step by step converter design procedure as shown in Fig. 3.

In a first step, analytical functions for the voltage and current time functions for each component in the converter phases of the intended converter topology are gathered in dependence on the operating point $\boldsymbol{O} = \{U_1, U_2, P_n\}$, the direction of power conversion and the component values. Identical phases with $P_{n,max} = P_{max}/N$ are assumed.

Secondly, the required inductance L and the capacitors C_1 and C_2 are are determined. In case of topology B, L is found by optimization considering the voltage ranges U_1, U_2, the derated phase power $P_n(U_1, U_2, P_n(U_1, U_2, P_{n,\max}, I_{\max}))$ and an upper limit of the relative current ripple of 5%. A design rule for the inductor L in topology A is presented in [3]. It is assumed that the N converter phases share the capacitors C_1 and C_2, whereas e.g. the capacitor C_1 current is the sum the phase-shifted switch $S_{1,n}$ currents minus the *side 1* DC current I_1:

$$i_{C1}(t) = \sum_{i=n}^{N} i_{S1,n}\left(t - \frac{i-1}{N f_{sw}}\right) - I_1. \tag{1}$$

Then, the charge difference

$$Q_1 = \frac{1}{2}\int_0^{1/f_{sw}} |i_{C1}(t)|\, dt \tag{2}$$

determines the necessary capacitance

$$C_1 = \frac{Q_1}{2\hat{\tilde{u}}_1} \tag{3}$$

to keep the voltage ripple $\hat{\tilde{u}}_1$ within its limits. Similar to L, the value of C_1 is found by optimization considering the given voltage and power ranges and a minimum number of $N_{\mathrm{on,min}}$ phases in operation.

Afterward, the inductor and capacitor volumes are determined as well as the miscellaneous losses

$$P_{\mathrm{misc}} = P_{\mathrm{ind}} + P_{\mathrm{aux}} \tag{4}$$

in the inductor L and the auxiliary circuits neglecting the losses in the capacitors C_1 and C_2, whereas the same models (cf. section IV and section III) for both topologies guarantee a fair comparison. The efficiency requirement η_{req} and P_{misc} limit the permitted semiconductor losses $P_{\mathrm{semi}} = P_{\mathrm{co}} + P_{\mathrm{sw}}$ of the converter phase:

$$P_{\mathrm{semi}} = \left(\frac{1}{\eta_{\mathrm{req}}} - 1\right) P_n - P_{\mathrm{misc}}. \tag{5}$$

Knowing P_{semi}, an optimization of the chip size size of each switch or diode of the converter is carried out to satisfy the efficiency requirement.

Finally, the volume of the cooling system and the auxiliary volumes for gate drivers, controller and measurement circuits are estimated and the overall converter volume is calculated.

TABLE II
OPTIMIZER CONSTRAINTS

Parameter	Value
Converter Topology	A or B
Switching frequency f_{sw}	10 kHz .. 250 kHz
Number of phases N	1 .. 20
Minimum phases active $N_{\mathrm{on,min}}$	2
Inductor type	cf. section III
Capacitor type	cf. section IV
Maximum junction temperature $T_{\mathrm{j,max}}$	150°C
Cooling concept	liquid cooler @ T_{s} = 80°C

III. INDUCTOR MODEL

To keep the optimization simple and applicable over a wide range of inductance L and switching frequency, a standard design approach for an inductor built of an air-gapped ferrite E-core is chosen that relies on the area product

$$A_{\mathrm{w}} A_{\mathrm{c}} = \frac{L \hat{I}_{\mathrm{L}} I_{\mathrm{L,rms}}}{k_{\mathrm{w}} J_{\mathrm{rms}} \hat{B}} \tag{6}$$

to give an indication on the required core size [7]. A Litz wire winding and the Epcos N87 ferrite material ensure an adequate HF loss behavior throughout the entire considered switching frequency range. In (6) $\hat{I}_{\mathrm{L}}$ and $I_{\mathrm{L,rms}}$ are the peak and RMS values of the inductor current $i_{\mathrm{L}}(t)$, A_{c} the core cross section and a copper fill factor of k_{w} = 0.44, a peak induction of $\hat{B}$ = 300 mT, a maximum current density J_{rms} = 500 A/cm^2 in the window area A_{w} and a operation temperature of T_{ind} = 100°C are assumed.

A. Inductor Volume

The inductor volume V_{L} can be expressed in dependence of the area product and is given by

$$V_{\mathrm{L}} = k_{\mathrm{L}} \left(A_{\mathrm{w}} A_{\mathrm{c}}\right)^{3/4}, \tag{7}$$

whereas a value of

$$k_{\mathrm{L}} = 4 \left(\sqrt{q_{\mathrm{A}}} + \sqrt{\frac{1}{q_{\mathrm{A}}}}\right) \cdot \left(\sqrt{\frac{1}{2\sqrt{q_{\mathrm{A}}} + \sqrt{\frac{1}{q_{\mathrm{A}}}}}} + \sqrt{\frac{1}{\sqrt{q_{\mathrm{A}}} + \sqrt{\frac{1}{q_{\mathrm{A}}}}}}\right) = 10.223 \tag{8}$$

is found when the overall inductor volume including the E-core and winding volume is expressed as a functions of A_{w} and A_{c}. The area quotient $q_{\mathrm{A}} = A_{\mathrm{w}}/A_{\mathrm{c}} = 1.362$ for a minimum inductor volume results from an analytical optimization, which is not shown for the sake of brevity. Then, V_{L} can be expressed as a function of the energy stored in the inductor:

$$V_{\mathrm{L}} = 438\ \mathrm{cm}^3 \cdot \left(\frac{L \hat{I}_{\mathrm{L}} I_{\mathrm{L,rms}}}{1\ \mathrm{Ws}}\right)^{3/4} \tag{9}$$

B. Inductor Losses

The inductor losses P_{ind} include Skin losses P_{sk} and Proximity losses P_{pr} of the winding and the core losses P_{c}:

$$P_{\mathrm{ind}} = P_{\mathrm{sk}} + P_{\mathrm{pr}} + P_{\mathrm{c}} \tag{10}$$

The skin losses for a Litz wire winding with diameter d_{c} and N_{S} straints are given by

$$P_{\mathrm{sk}} = N_{\mathrm{S}} R_{\mathrm{DC}} F_{\mathrm{R}} \left(\frac{\hat{I}_{\mathrm{L}}}{N_{\mathrm{S}}}\right)^2 \tag{11}$$

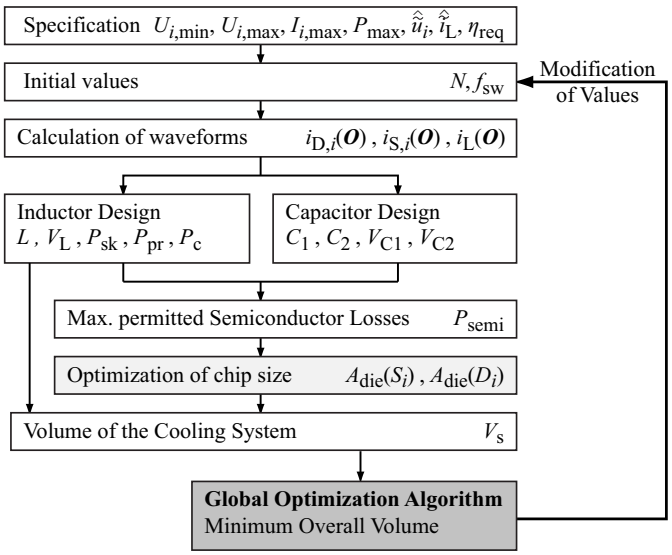

Fig. 3. Flow chart of the optimization algorithm.

and the losses due to internal Proximity effect and the external magnetic field H_e are given by

$$P_{pr} = N_S R_{DC} G_R \left(H_e^2 + \frac{\hat{I}_L^2}{2\pi^2 d_c^2} \right) \tag{12}$$

where R_{DC} is the dc resistance of the winding and F_R and G_R are factors that model geometry and frequency dependence of the losses and are given in [8].

Furthermore, for a given magnitude of induction ΔB and known voltages $U_{L,j}$ applied to the inductor L during the time intervals Δt_j, the core losses P_c are calculated by

$$P_c = k_c f_{sw} (\Delta B)^{\beta-\alpha} \sum_j \left| \frac{U_{L,j}}{N_{turns} A_c} \right|^{\alpha} (\Delta t_j) \tag{13}$$

where

$$k_c = \frac{k}{2^{\beta+1}\pi^{\alpha-1}\left(0.2761 + \frac{1.7061}{\alpha+1.354}\right)} \tag{14}$$

is a constant depending on the Steinmetz Parameters k, α, β of the magnetic material [9].

IV. Capacitor Model

A. Capacitor Volume

Film capacitors are preferred for C_1 and C_2 instead of ceramic capacitors or electrolyte capacitors, since the latter either show a strong dependence of the capacitance on the applied dc voltage and are prone to mechanical stress or are limited in lifetime. Therefore, with the fit function

$$V_C = k_{C1} + k_{C2} C U_R \tag{15}$$

the volume of Epcos high density B3277x MKP dc link capacitors is determined to

$$V_C = 6.76\ \text{cm}^3 + 0.00206\ \text{cm}^3/\text{As} \cdot C U_R, \tag{16}$$

where U_R is the rated capacitor voltage. Fig. 4 approves a low error of the volume equation.

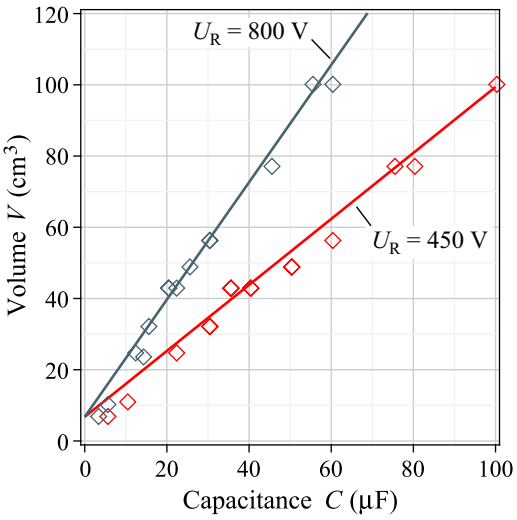

Fig. 4. Volume of Epcos high desity series MKP dc link capacitors shown along with the fit function (16).

V. Semiconductor Model

A. Semiconductor Losses

There are two different switch configurations to be modeled in terms of conduction, switching and gate losses $P_{co} + P_{sw} + P_g = P_{semi}$, which are Silicon MOSFETs for topology A and Silicon IGBTs with anti-parallel SiC diodes for topology B. The P_{co} models discussed in the following are based on semiconductor parameters extracted from the datasheets of a IXYS IXFB82N60P MOSFET, a ST STGP30NC60W IGBT and a Cree CSD20060D SiC diode as a function of junction temperature T_j, conducted current and applied voltage. In case of the MOSFET system the overall conduction losses of the four switches S_i are given by

$$P_{co} = \sum_{i=1}^{4} r_{DS,on}(T_j, I_{S,i,rms}) I_{S,i,rms}^2, \tag{17}$$

where $I_{S,i,rms}$ are the calculated switch RMS currents and $r_{DS,on}$ is the temperature dependent drain-source resistance. On the other hand, in case of the IGBT system and depending on the mode of operation, the conduction losses are either generated by the IGBT or the diode D_i and are given by

$$\begin{aligned} P_{co} = \sum_{i=1}^{4} \big(& U_{CE0}(T_j) I_{S,i,avg} + r_{CE}(T_j) I_{S,i,rms}^2 + \\ & + U_{D0}(T_j) I_{D,i,avg} + r_D(T_j) I_{D,i,rms}^2 \big), \end{aligned} \tag{18}$$

where U_{CE0}, r_{CE}, U_{D0} and r_D are the temperature dependent values of on-state forward voltage drop and differential resistance of IGBT and diode, respectively.

Since the switching losses cannot be extracted from the datasheets, these are measured when switching an inductive load with two switches in a half-bridge configuration for different voltages, load currents and junction temperature. In case of the Si IGBT, SiC diode combination the switching losses are calculated by $P_{sw} = f_{sw} \cdot (E_{on} + E_{off})$ whereas the switching energies E_{on} and E_{off} are fitted by

$$\begin{aligned} E = (& c_1 + c_2 \cdot U_{CE} + c_3 \cdot I_C + \\ & + c_4 \cdot U_{CE}^2 + c_5 \cdot I_C^2 + c_6 \cdot U_{CE} I_C) \end{aligned} \tag{19}$$

and results of the measurements. The MOSFET switching losses $P_{sw} = f_{sw} \cdot E_{sw}$ are determined by a fit of measurements with the polynom

$$E_{sw} = U_{DS} \sum_{i=0}^{3} c_{i+1} \cdot I_D^i + \sum_{i=0}^{3} c_{i+5} \cdot I_D^i. \tag{20}$$

As a last semiconductor loss component, the gate driver losses $P_g = f_{sw} \cdot Q U_g$ are calculated. To take the influence of the chip size A_{die} on the three loss components into account, these are scaled relative to the chip size A_{ref} of the reference devices.

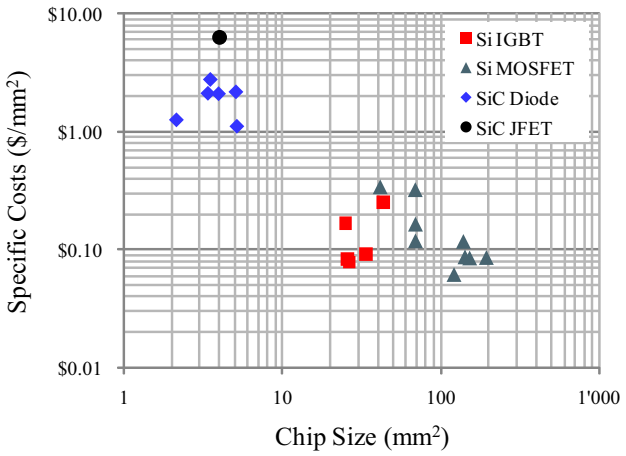

Fig. 5. Specific costs of different semiconductor device technologies.

TABLE III
AVERAGE COSTS PER CHIP SIZE

Device	Costs
Si IGBT	0.08 $/mm^2
Si MOSFET	0.10 $/mm^2
SiC Diode	1.20 $/mm^2
SiC JFET	6.25 $/mm^2

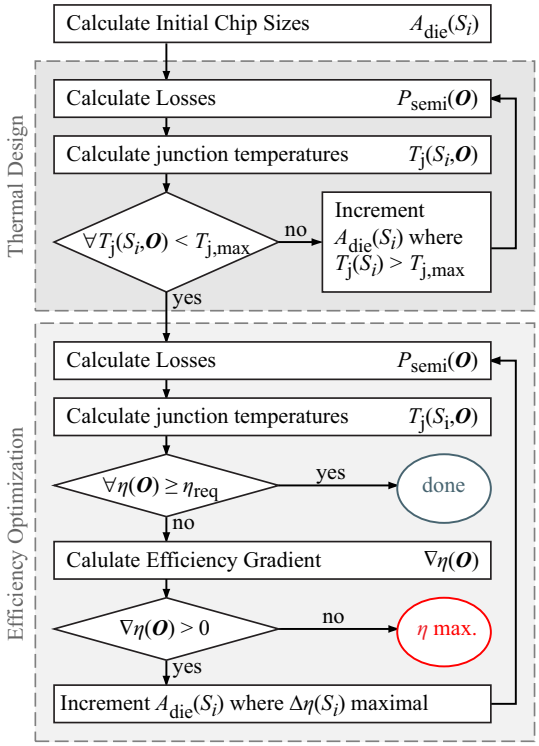

Fig. 6. Flow chart of the chip size optimization algorithm.

B. Semiconductor Costs and Volume

Another important property are the semiconductor costs, which are approximately proportional to the chip size A_{die}. To determine a specific costs per mm^2 chip area, the distributor prices and die sizes of multiple 600V MOSFETs, IGBTs and SiC diodes have been evaluated. The specific costs are shown in Fig. 5 and yield the average costs listed in table III.

Similar to costs, also the semiconductor volume $V_{\text{semi}} = k_{\text{semi}} \cdot A_{\text{die}}$ is approximated to be directly proportional to the chip size A_{die} with the constant k_{semi} extracted from the package dimensions of the IXYS IXFB82N60P MOSFET.

VI. SEMICONDUCTOR CHIP SIZE OPTIMIZATION

The minimum required chip size A_{die} is affected by the allowed semiconductor losses $P_{\text{semi}}(A_{\text{die}})$. On the one hand these losses must be low enough that the junction temperature

$$T_{\text{j}} = T_{\text{s}} + R_{\text{th,js}} P_{\text{semi}} \tag{21}$$

does not exceed its limits for a given heatsink temperature T_{s} and the chip area dependent thermal resistance that is approximated by

$$R_{\text{th,js}} = 23.94 \text{ K/W} \cdot \left(\frac{A_{\text{die}}}{1\text{mm}^2} \right)^{-0.88} \tag{22}$$

as proposed in [10]. A maximum junction temperature of $T_{\text{j,max}}$ = 150°C for both Si and SiC devices is assumed due to aspects of reliability. Furthermore, the thermal capacitances are neglected since a optimization for continuous operation instead of a mission profile based optimization is aimed for reasons of simplicity in a first step. On the other hand, it might be necessary to deploy larger chip sizes than required for thermal stability to fulfill the efficiency target η_{req}. Both aspects are considered in the implementation of the chip size optimization algorithm depicted in Fig. 6.

The chip sizes A_{die} of the switches S_i and/or the diodes D_i are initialized with a fraction of their actual required values. Then the semiconductor losses $P_{\text{semi}}(\boldsymbol{O})$ and the junction temperature $T_{\text{j}}(S_i, \boldsymbol{O})$ is calculated for multiple operation points $\boldsymbol{O}$ (different voltage transfer ratio U_1/U_2 and power P_n, 16 in total). The chip size of those of the switches or diodes with $T_{\text{j}} > T_{\text{j,max}}$ is incremented iteratively by a factor $k_{\text{A}} = A'_{\text{die}}/A_{\text{die}} = 1.25\%$ until the junction temperature of each device and operation point remains below $T_{\text{j,max}}$.

In a second iteration loop the chip sizes are optimized for efficiency. Thereto, the efficiency

$$\eta(\boldsymbol{O}) = \frac{P(\boldsymbol{O})}{P(\boldsymbol{O}) + P_{\text{semi}}(\boldsymbol{O}) + P_{\text{misc}}(\boldsymbol{O})} \tag{23}$$

for each operation point $\boldsymbol{O}$ is checked against the requirement η_{req}, whereas the optimization procedure finishes when $\forall \eta(\boldsymbol{O}) \geq \eta_{\text{req}}$. Otherwise the efficiency gradient

$$\nabla\eta(\boldsymbol{O}) = \sum_{\boldsymbol{O}} \Delta\eta(\boldsymbol{O}) = \sum_{\boldsymbol{O}} \eta(\boldsymbol{O}, A'_{\text{die}}) - \eta(\boldsymbol{O}, A_{\text{die}}) \tag{24}$$

is calculated. For a $\nabla\eta(\boldsymbol{O}) < 0$ no further improvement of the average efficiency $\bar{\eta}$ is achievable by an area increment and the solver exits discarding the converter design out of specification.

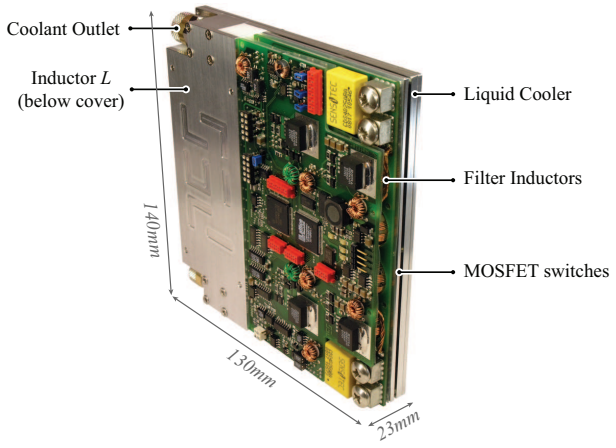

Fig. 7. Photo of a converter phase module for topology A with a power density of ρ_p = 30 kW/l at a maximum output power of $P_{n,\max}$ = 12 kW and a switching frequency of f_sw = 100 kHz.

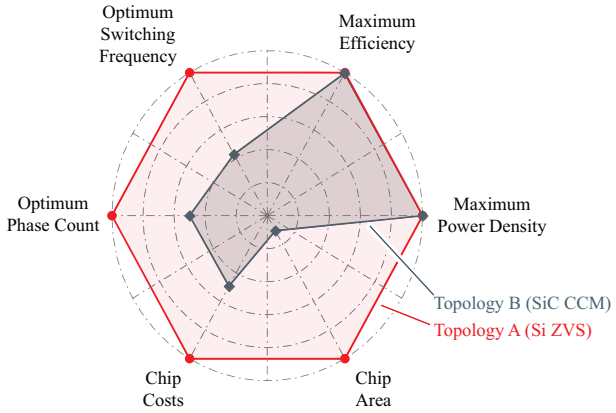

Fig. 8. Comparison of converter characteristics shown with the parameters normalized to their maximum values for both topologies.

VII. Optimization Results

Additionally to the component models given in section III to section V, the volume of the cooling system V_s and the auxiliary losses P_aux are taken into account to calculate the overall power density ρ_p. These numbers are found by comparison with a converter already realized in hardware that is shown in Fig. 7. In the optimization results the mark indicates the numbers of the converter depicted in Fig. 7. It should be noted that this system shows a reduced power density because additional differential mode filter inductors and an inductor built of planar cores instead of an E-core are utilized.

The results of the power density optimization are depicted in Fig. 9 for topology A and in Fig. 10 for topology B, respectively for all valid converter designs ($\eta \geq \eta_\mathrm{req}$ = 95%) and the switching frequency in a 10 kHz grid. A maximum power density of 47.9 kW/l is expected for topology A at N = 4 and f_sw = 220 kHz and a maximum power density of 45.9 kW/l for topology B at N = 2 and f_sw = 250 kHz.

Based on the optimization results for $\eta \geq \eta_\mathrm{req}$ = 95% provided in Fig. 9 to Fig. 12 the two converter designs listed in table IV are suggested for a hardware realization. For topology A, the optimum phase count is N = 4 and a switching frequency of 150 kHz is sufficient to achieve a high power density of 47.3 kW/l. At the same switching frequency and the optimum phase count of N = 2, topology B shows a lower power density of 36.6 kW/l.

TABLE IV
Reference Designs

Parameter	**Topology A**	**Topology B**
Phase Properties		
Inductance L	2.1 µH	60.0 µH
Inductor Peak Current $\hat{I}_\mathrm{L}$	202 A	125 A
Capacitor C_1, C_2	6.13 µF	26.0 µF
Total Volume	0.37 l	0.94 l
Chip Size S_1, S_3 (each)	1940 mm^2	214 mm^2
Chip Size S_2, S_4 (each)	785 mm^2	164 mm^2
Chip Size D_1, D_3 (each)	-	115 mm2
Chip Size D_2, D_4 (each)	-	80 mm2
Max. junction temperature	95.5 °C	150 °C
Converter Properties		
Switching frequency f_sw	150 kHz	150 kHz
Number of phases N	4	2
Total Capacitor Energy	4.9 Ws	10.5 Ws
Total Inductor Energy	0.17 Ws	0.94 Ws
Semiconductor Costs	$ 2196	$ 1083
Total Volume	1.48 l	1.88 l
Power Density ρ_p	47.3 kW/l	36.6 kW/l
Average Efficiency η_avg	96.6%	97.8%

However, both topologies could either be designed for best power density ρ_p or best efficiency η, depending on the application requirement. The maximum average efficiency (average converter efficiency of 16 operating points $\boldsymbol{O}$ including part load and full load conditions) is calculated based on the provided loss models and the chip size optimization algorithm given in section VI with an efficiency target of 100% and is given in Fig. 11 and Fig. 12. With the soft-switching topology A, the efficiency drops linearly with increasing switching frequency, mainly due to the high frequency losses in the inductor but also due to a small share of switching losses that cannot be avoided even with a ZVS mode of operation. For the hard-switching SiC topology B, there exists an optimum switching frequency of approximately 60 kHz. Below that frequency the inductor conduction losses are reason for the efficiency to drop, since the required inductance increases and therefore also the winding losses. As can be seen from the η-ρ_p-pareto-front depicted in Fig. 13 and Fig. 14, with both topologies ultra-compact converter realizations with a promising ρ_p in the range of 48 kW/l and a comparable

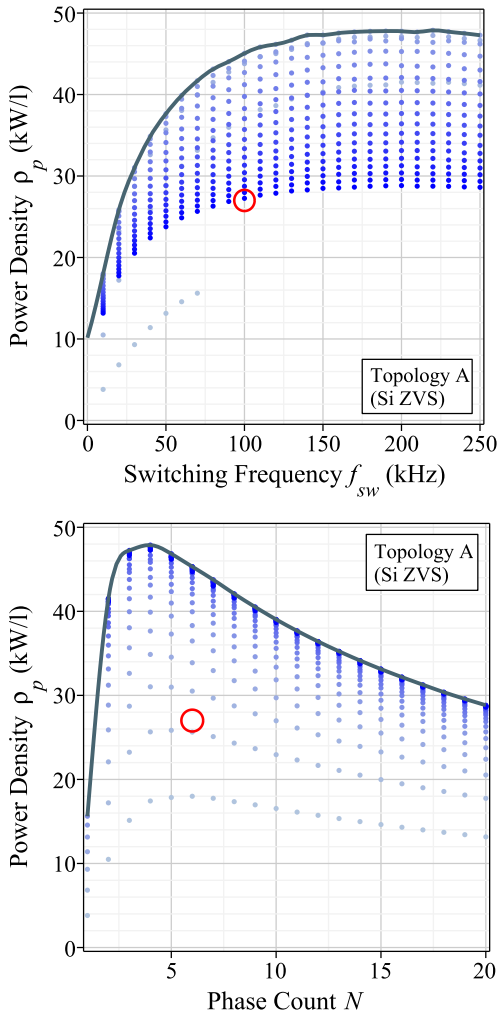

Fig. 9. Power density optimization results for topology A built with Silicon MOSFETs and ZVS operation. The red mark indicates the characteristics of the realized hardware depicted in Fig. 7.

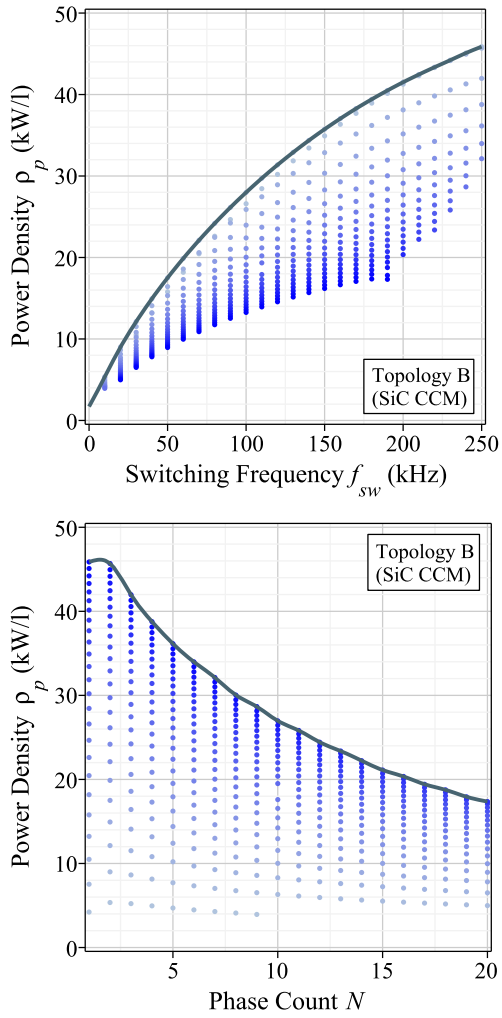

Fig. 10. Power density optimization results for topology B built with Silicon IGBTs and anti-parallel SiC diodes and operated with PWM modulation in DCM/CCM.

maximum average efficiency greater than 98.5% are expected.

The converter data listed in table IV, however, indicates that the ZVS topology A requires a 9.5 times larger total chip area. Thus, in spite of the 12 times higher specific costs for SiC diodes compared to the Si MOSFETs, the total semiconductor costs of topology A are approximatly two times higher. On the other hand, topology A has the advantage of a 5.5 times lower total energy stored in the inductors L resulting in lower costs for these inductors. Furthermore, due to the lower inductance value, higher system dynamics are achievable with topology A. The characteristics of the two topologies are summarized and visualized comparative in Fig. 8.

VIII. Conclusion

In this paper a multi-objective power density optimization algorithm for dc-dc converters that includes an secondary optimizer to determine the required chip size of the semiconductors is proposed and applied to find the optimum converter designs of two different non-isolated bi-directional multi-phase converter concepts applicable to interconnect the high voltage battery of a HEV of FCV to the dc link. Furthermore, the volume, losses and costs models of the converter components such as inductors, capacitors and semiconductors that provide the basis of the optimization are given in the form of comprehensive analytical models.

It is found as a result of the optimization that for both the soft-switching converter topology built with Silicon MOSFETs and the hard-switched topology built with Silicon IGBTs and Silicon Carbide diodes, the efficiency target of $\eta > 95\%$ for $P > 0.1P_{\max}$ is met and ultra-compact designs with a power density of approximately 48 kW/l could be realized. A comparison of semiconductor chip costs identifies the hard-switched system to be more cost-efficient in spite the application of Silicon Carbide devices, as the chip size required for the soft-switching topology to keep the conduction losses low is significantly higher.

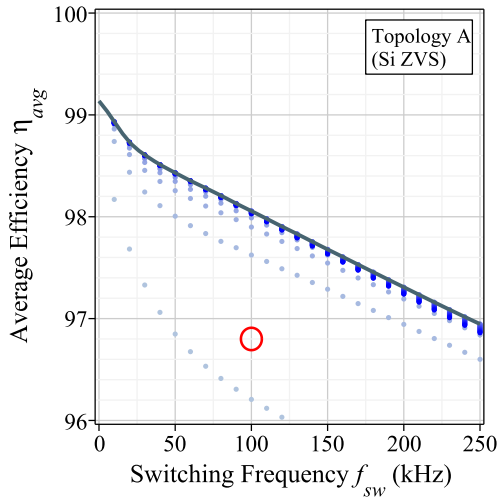

Fig. 11. Efficiency optimization results for topology A built with Silicon MOSFETs and ZVS operation. The red mark indicates the characteristics of the realized hardware depicted in Fig. 7.

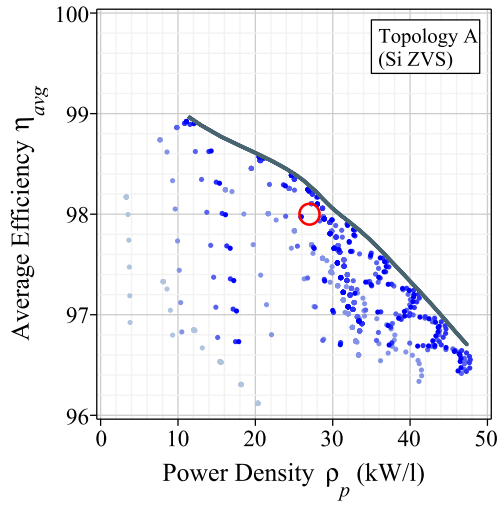

Fig. 13. η-ρ_p-pareto-front for topology A built with Silicon MOSFETs and ZVS operation. The red mark indicates the characteristics of the realized hardware depicted in Fig. 7.

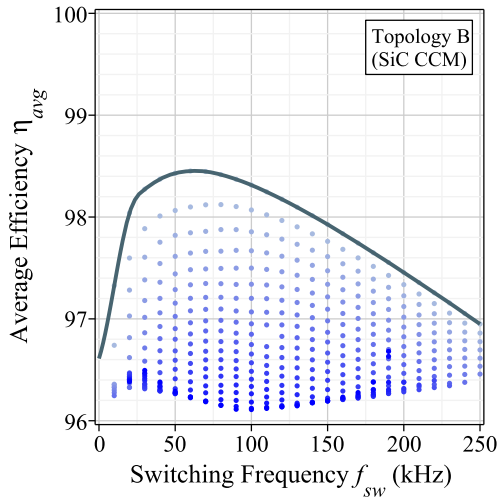

Fig. 12. Efficiency optimization results for topology B built with Silicon IGBTs and anti-parallel SiC diodes.

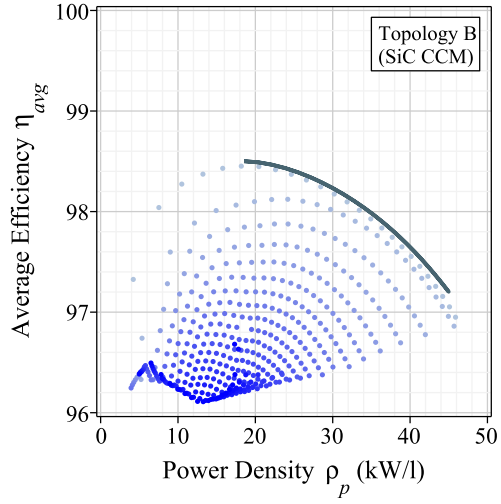

Fig. 14. η-ρ_p-pareto-front for topology B built with Silicon IGBTs and anti-parallel SiC diodes.

References

[1] A. Emadi, S. S. Williamson, and A. Khaligh, "Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 567–577, May 2006.

[2] R. M. Schupbach and J. C. Balda, "Comparing dc-dc converters for power management in hybrid electric vehicles," in *Proc. IEMDC'03 Electric Machines and Drives Conference IEEE International*, vol. 3, 1–4 June 2003, pp. 1369–1374.

[3] S. Waffler and J. W. Kolar, "A novel low-loss modulation strategy for high-power bi-directional buck+boost converters," in *Proc. 7th Internatonal Conference on Power Electronics ICPE '07*, 22–26 Oct. 2007, pp. 889–894.

[4] B. Eckardt and M. Mrz, "A 100kw automotive powertrain dc/dc converter with 25kw/dm^3 by using sic," in *Power Conversion Intelligent Motion (PCIM)*, 2006.

[5] O. Garcia, P. Zumel, A. de Castro, and A. Cobos, "Automotive dc-dc bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 578–586, May 2006.

[6] S. Waffler and J. W. Kolar, "Efficiency optimization of an automotive multi-phase bi-directional dc-dc converter," in *Proc. 6th International Power Electronics and Motion Control Conference - ECCE Asia IPEMC '09*, 17–20 May 2009.

[7] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. Wiley, 2003.

[8] J. A. Ferreira, "Analytical computation of ac resistance of round and rectangular litz wire windings," *IEE Proceedings B Electric Power Applications*, vol. 139, no. 1, pp. 21–25, Jan. 1992.

[9] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. IEEE Workshop on Computers in Power Electronics*, 3–4 June 2002, pp. 36–41.

[10] T. Friedli and J. W. Kolar, "A semiconductor area based assessment of ac motor drive converter topologies," in *Proc. Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition APEC 2009*, 15–19 Feb. 2009, pp. 336–342.