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CIPS 2018

Google Little-Box Reloaded

Johann W. Kolar et al.

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Outline

- Google Little Box Challenge
- *Requirements*
- *Little Box 1.0*
- Further Analysis & *New Approach*
- *Adv. Measurement Techniques*
- *New Circuit Topology*
- *Little Box 2.0*
- Conclusions

fraza
Fraunhofer IZM
Acknowledgement M. Kasper
O. Knecht
F. Krismer

Google

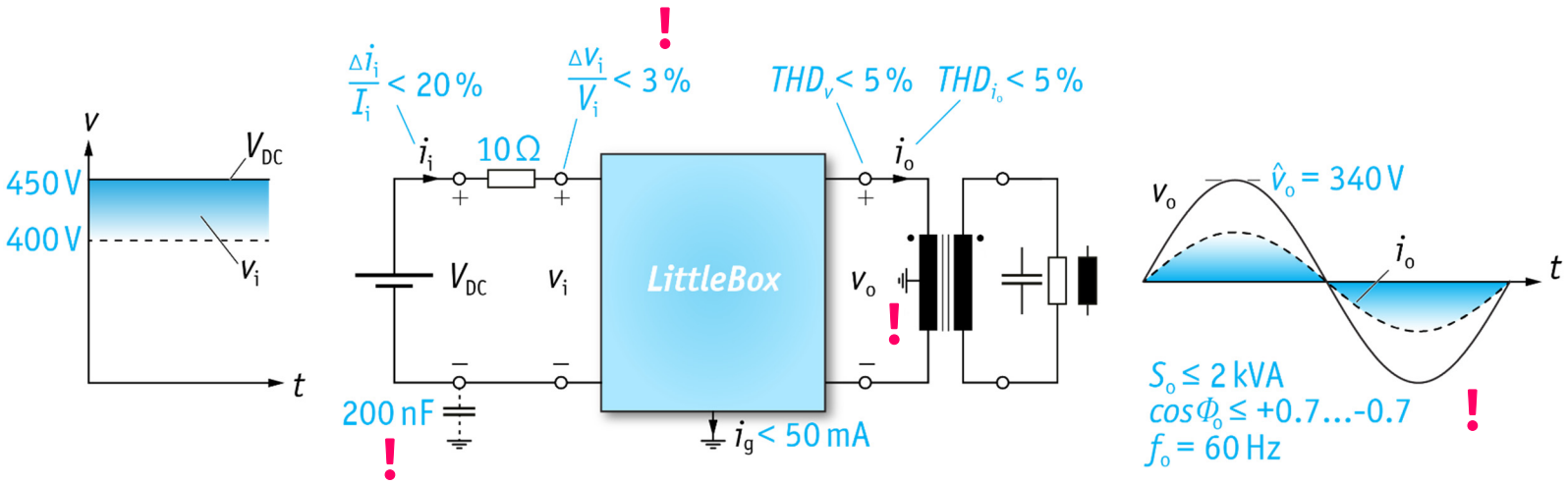
Little Box Challenge

Requirements
Little Box 1.0
Other Finalists

LITTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-ΦSolar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B



- Push the Forefront of New Technologies in R&D of High Power Density Inverters

The Grand Prize

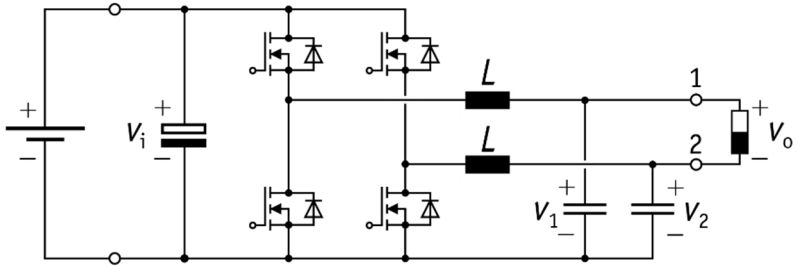
- Highest Power Density (> 50W/in^3)
- Highest Level of Innovation

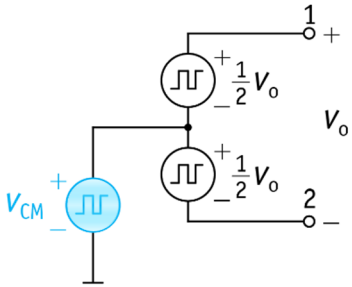
$1,000,000

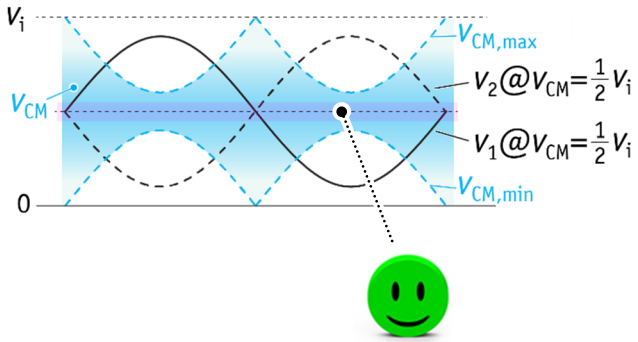
- Timeline
  - Challenge Announced in Summer 2014
  - **2000+ Teams Registered** Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - **18 Finalists (3 No-Shows)**

Selected Converter Topology

- Full-Bridge Output Stage
- Modulation of Both Bridge Legs



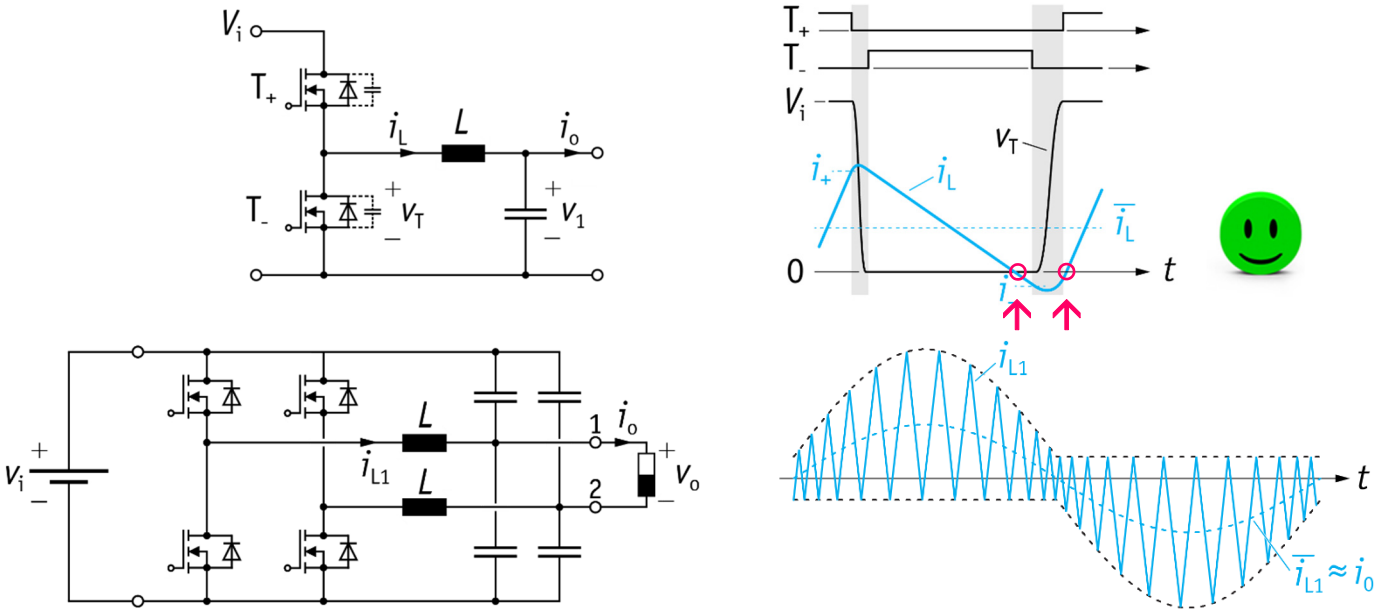




- DM Component of u_1 and u_2 Defines Output Voltage u_0
- No Low-Frequency CM Component of u_1 and u_2 (Different to e.g. 1-Φ PFC Rectifier Systems !)

Triangular Current Mode (TCM) ZVS Operation

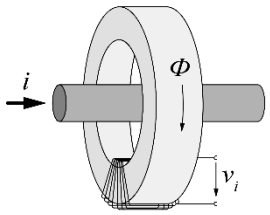
- TCM Operation for Resonant Voltage Transition @ Turn-On/Turn-Off

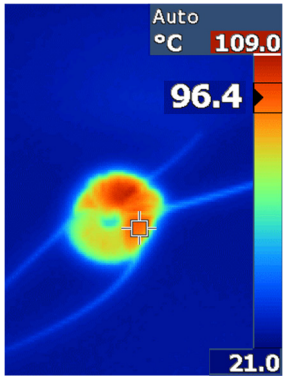


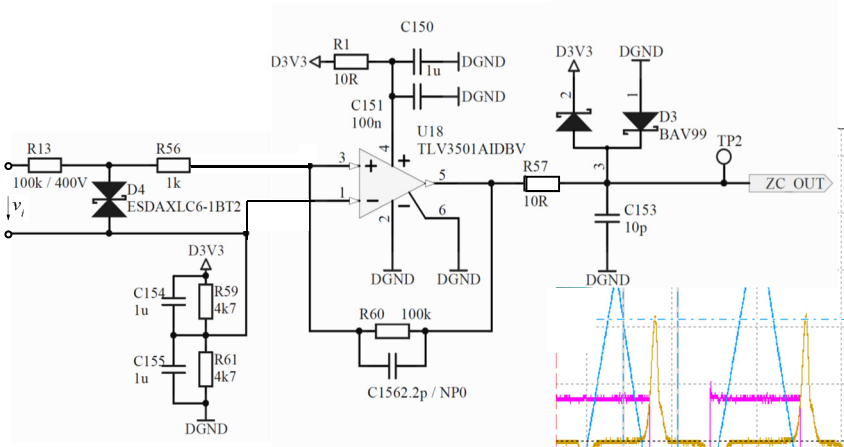
- Requires Only Measurement of Current Zero Crossings, $i = 0$
- High f_S Around $i = 0$ Challenging for Digital Control
- Variable Sw. Freq. f_S Lowers EMI

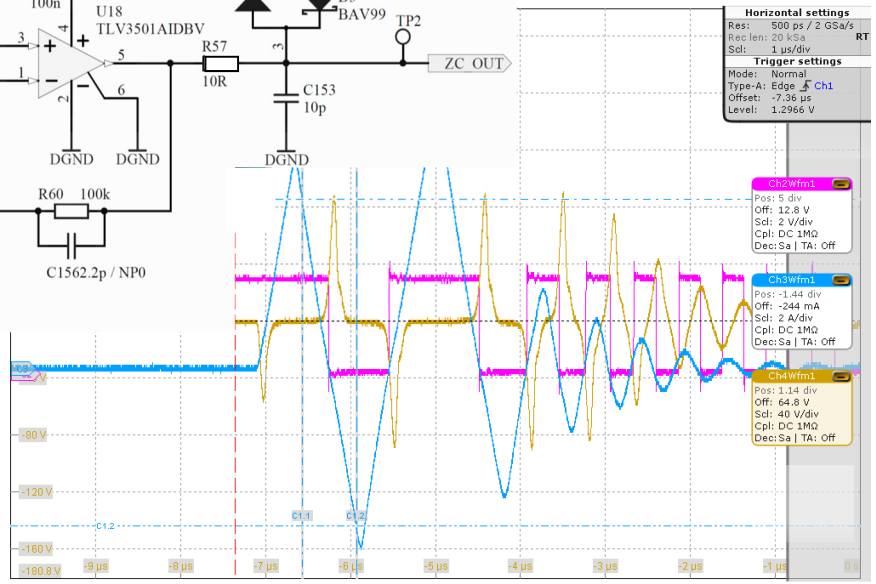
i=0 Detection

- Saturable Inductor – Toroidal Core R4 x 2.4 x 1.6, EPCOS (4mm Diameter)
  – Core Material N30, EPCOS





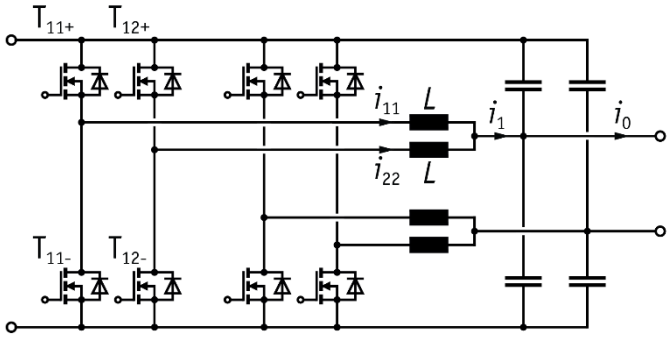


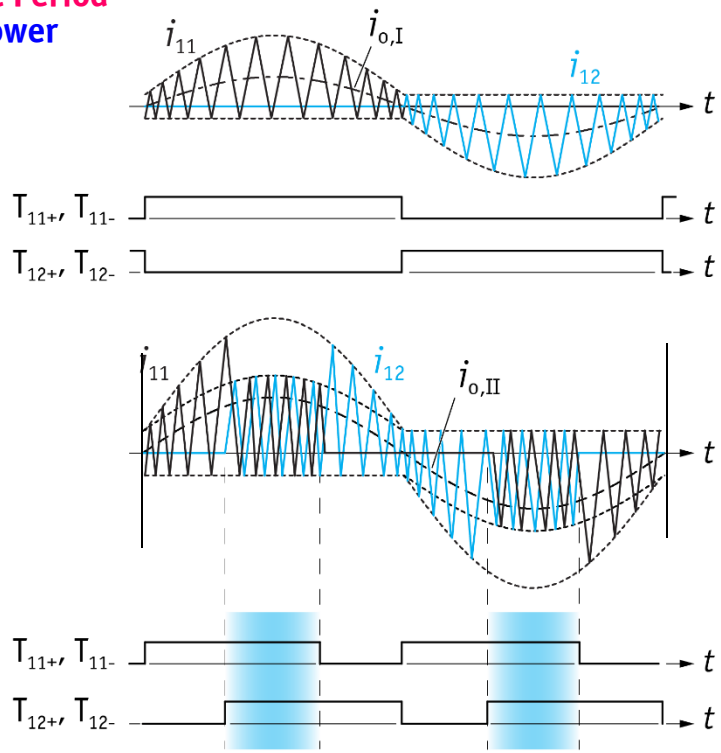


- Operation Tested up to 2.5MHz Switching Frequency

4D-Interleaving

- Interleaving of 2 Bridge Legs per Phase - Volume / Filtering / Efficiency Optimum
- Interleaving in Space & Time – Within Output Period
- Alternate Operation of Bridge Legs @ Low Power
- Overlapping Operation @ High Power

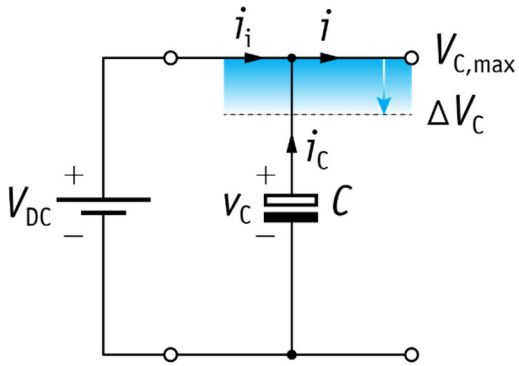


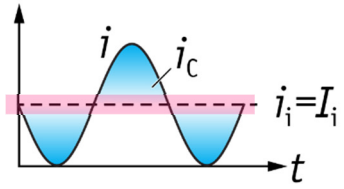


- Opt. Trade-Off of Conduction & Switching Losses / Opt. Distribution of Losses

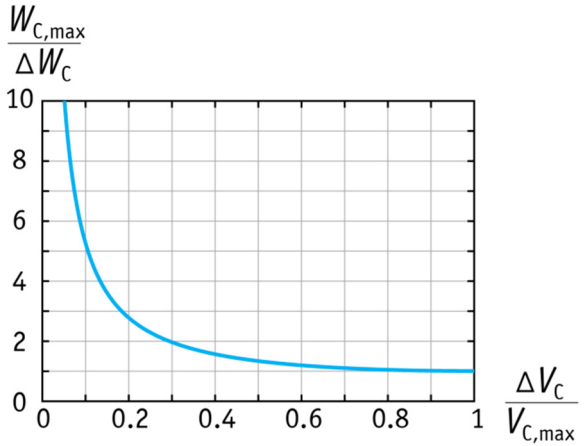
DC-Side Passive Power Pulsation Buffer

- Electrolytic Capacitor





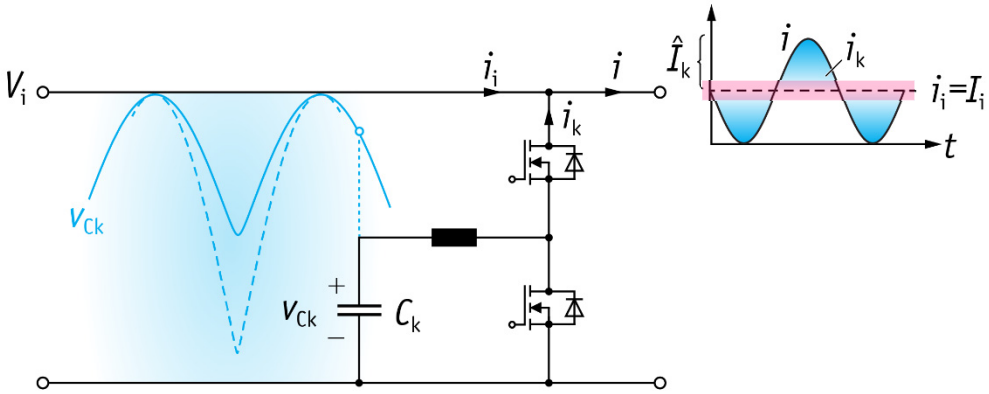
S_0 = 2.0 kVA
$\cos \Phi_0$ = 0.7
$V_{C,max}$ = 450 V
$\Delta V_C / V_{C,max}$=3 %



- C > 2.2mF / 166 cm^3 → Consumes 1/4 of Allowed Total Allowed Volume !

DC-Side Active Power Pulsation Buffer

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck-Type (Lower Voltage Levels) or Boost-Type DC/DC Interface Converter



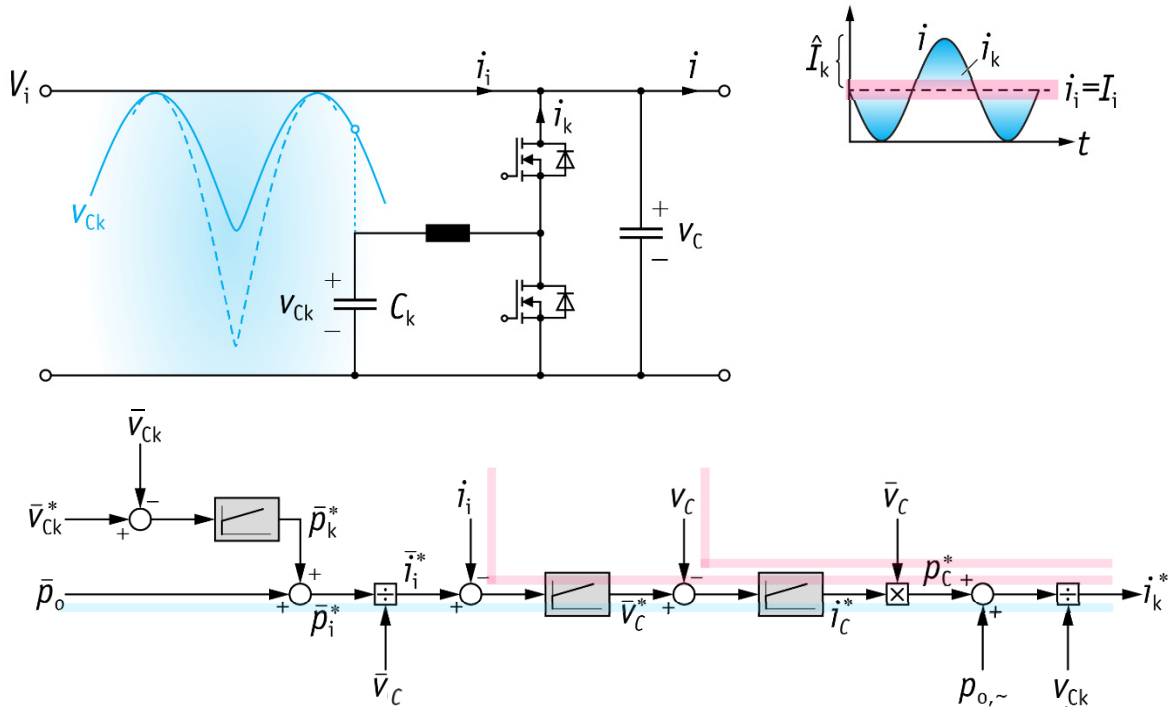
CeraLink™ TDK

108 x 1.2µF /400 V
$C_k \approx 140\mu F$
$V_{ck} = 23.7cm^3$

- Significantly Lower Overall Volume Compared to Electrolytic Capacitor

DC-Side Active Power Pulsation Buffer

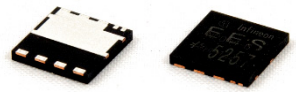
- Cascaded Control Structure



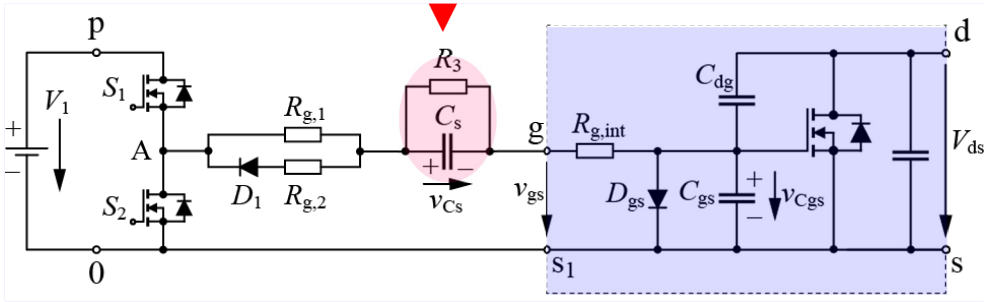
- P-Type Resonant Controller
- Feedforward of Output Power Fluctuation
- Outer Input Current (i_i) / Underlying DC Link Voltage (v_C) Control

Selected Power Semiconductors

- 600V IFX Normally-Off GaN GIT - ThinPAK8x8
- State-of-the-Art Gate Drive

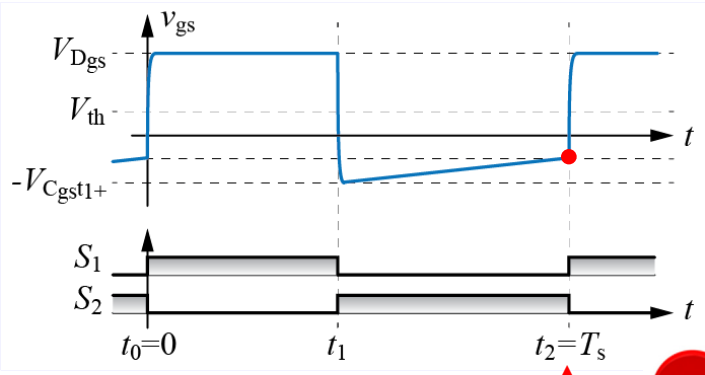


$V_{gs,th}$ = 1.2V
$R_{ds,on}$ = 55 mΩ @ 25°C
$R_{g,int}$ = 5Ω



– C_s Enables High Gate Current for Fast Turn-On

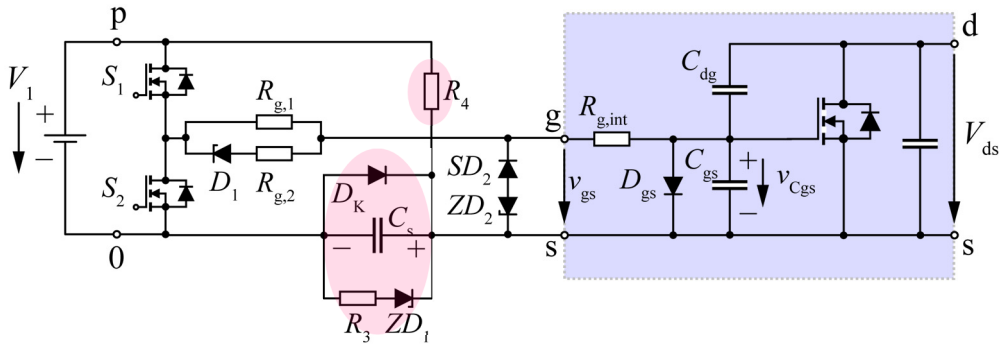
– R_3 Discharges C_s During Off-State



- Duty Cycle & Frequency Dependent Gate Voltage

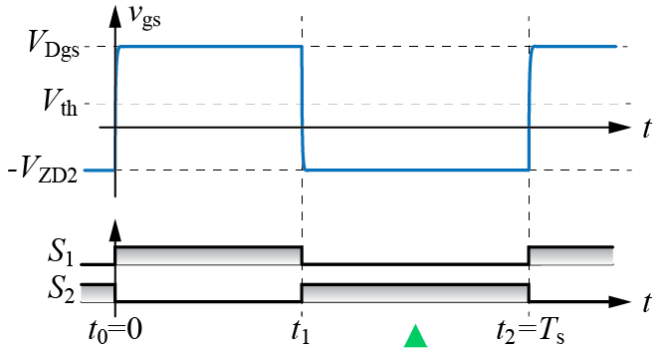
High dv/dt-Immunity Gate Drive

- Fixed Negative Turn-Off Gate Voltage - Independent of Sw. Frequency and Duty Cycle
- Extreme d*v*/d*t*-Immunity (500 kV/µs) - Due to CM Choke at Signal Isolator Input
- < 30ns Overall Prop. Delay



– Diode ZD_2 Quickly Discharges C_s to V_{ZD2} @ Turn-Off

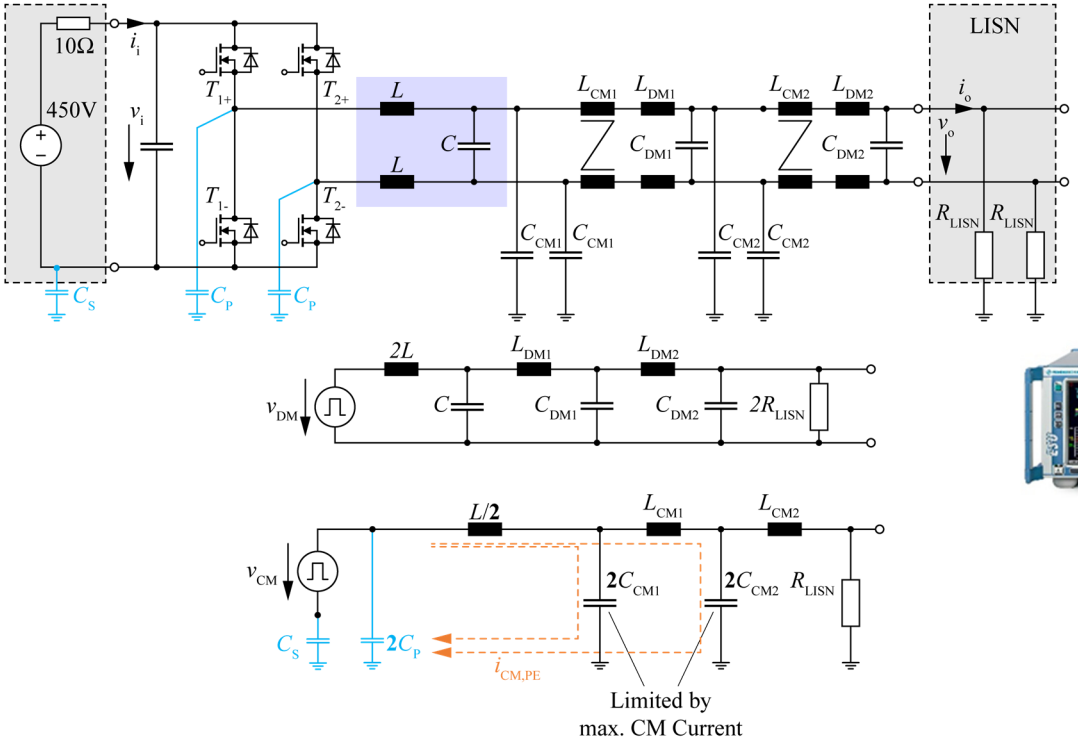
– Diode ZD_1 Prevents Complete Discharge of C_s During Off-State



- R_4 Ensures Precharge of C_s → Neg. Gate Voltage @ Start-Up

EMI Filter Topology (1)

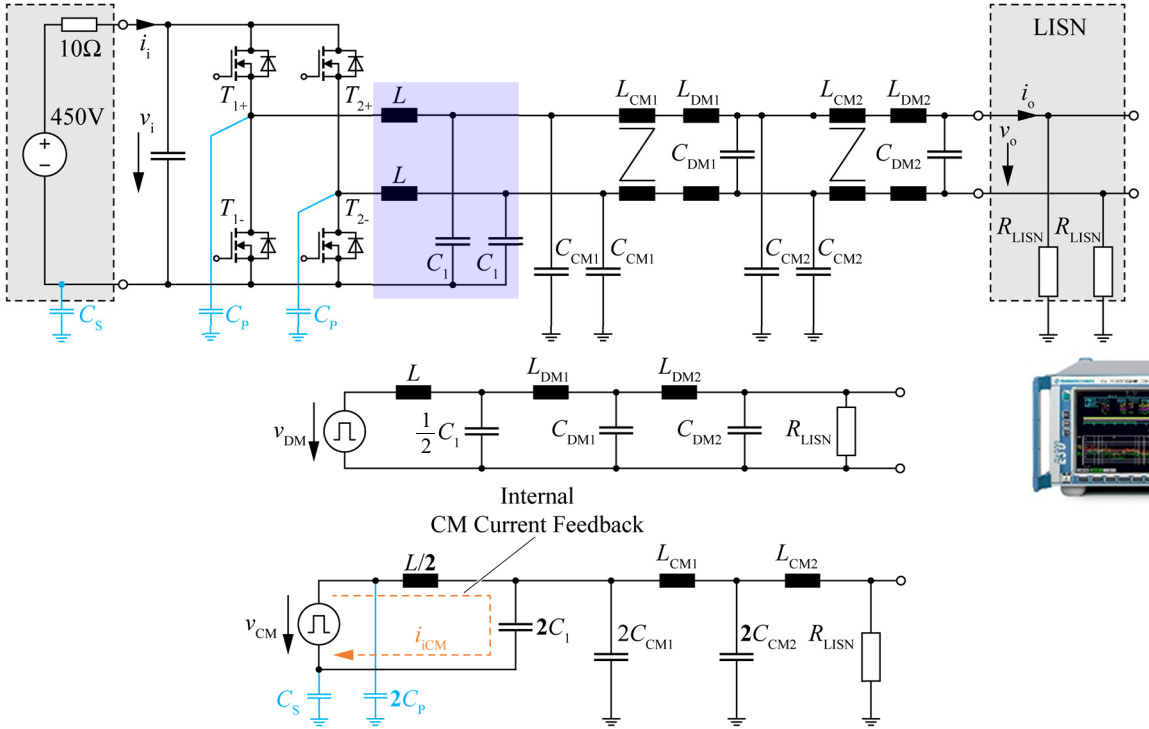
- Conventional Filter Structure
  - DM Filtering Between the Phases
  - CM Filtering Between Phases and PE



- CM Cap. Limited by Earth Current Limit – Typ. 3.5mA for PFC Rectifiers (GLBC: 5mA, later 50mA !)
- Large CM Inductor Needed – Filter Volume Mainly Defined by CM Inductors

EMI Filter Topology (2)

- Filter Structure with Internal CM Capacitor Feedback
- Filtering to DC- (and Optional to DC+)

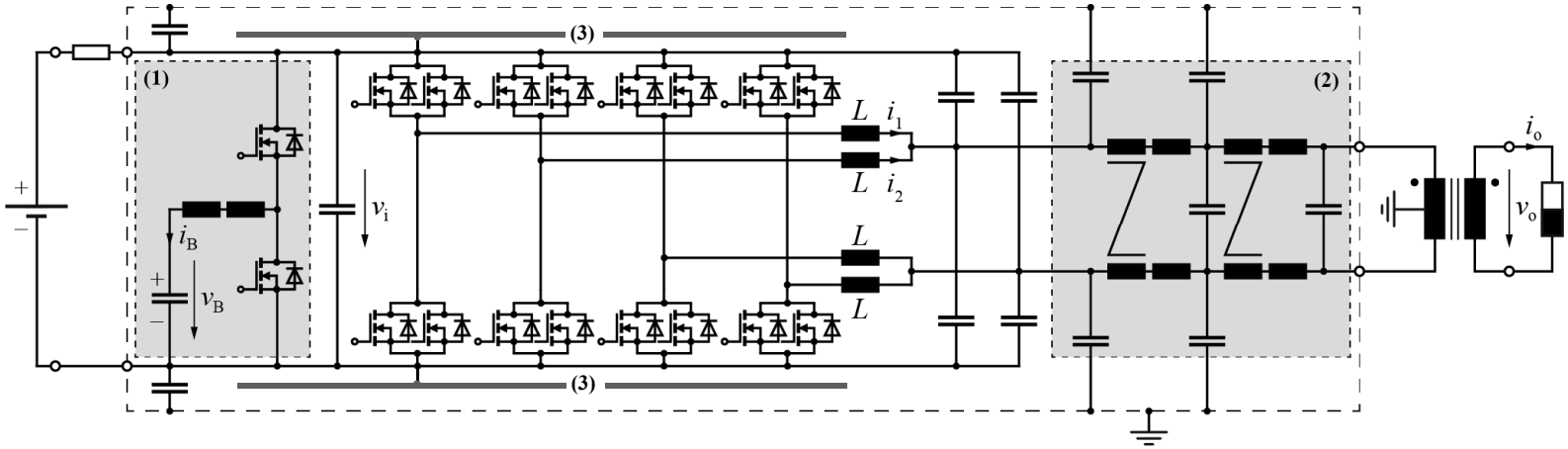


- No Limitation of CM Capacitor C_1 Due to Earth Current Limit → µF Instead of nF Can be Employed
- Allows Downsizing of CM Inductor and/or Total Filter Volume

Final Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- First Stage AC Filter Caps Connected to DC-
- 2-Stage EMI AC Output Filter

(1) Power Pulsation Buffer
(2) EMI Output Filter
(3) Heatsink



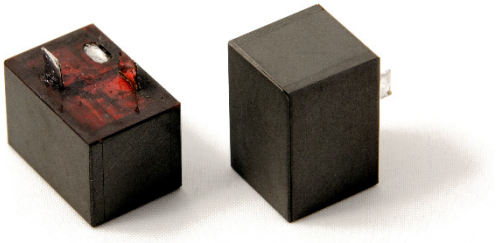
- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

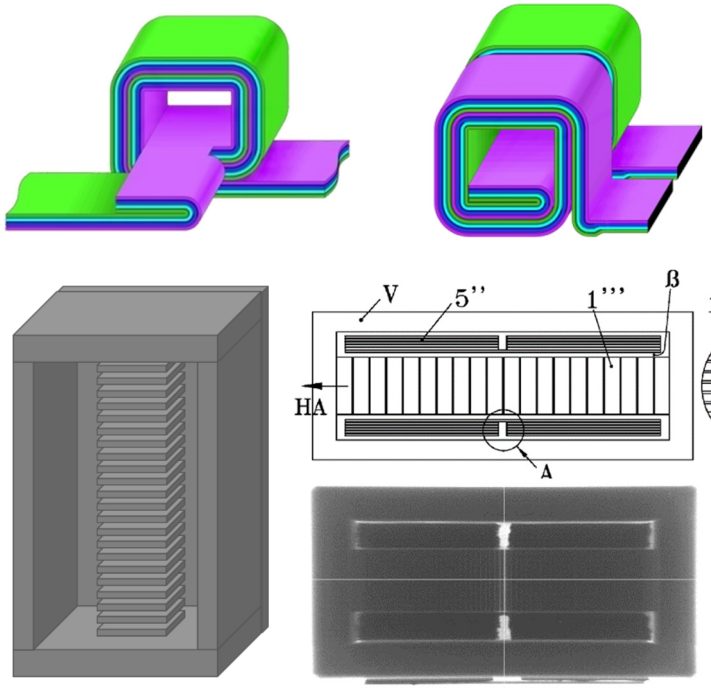
High Frequency Inductors (1)

fraza

- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- L= 10.5µH
- 2 x 8 Turns
- 24 x 80µm Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 µm Copper Foil / 4 in Parallel
- 7 µm Kapton Layer Isolation
- 20mΩ Winding Resistance / Q≈600
- Terminals in No-Leakage Flux Area



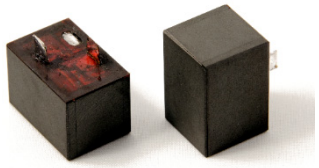


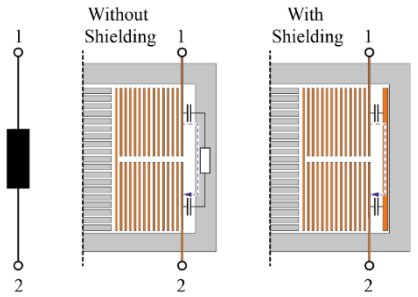
- Dimensions - 14.5 x 14.5 x 22mm³

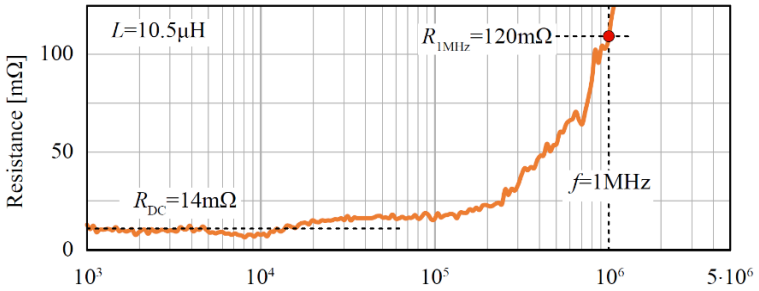
High Frequency Inductors (2)

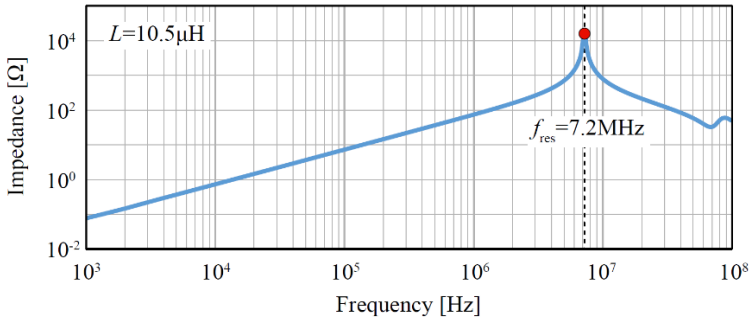
TDK

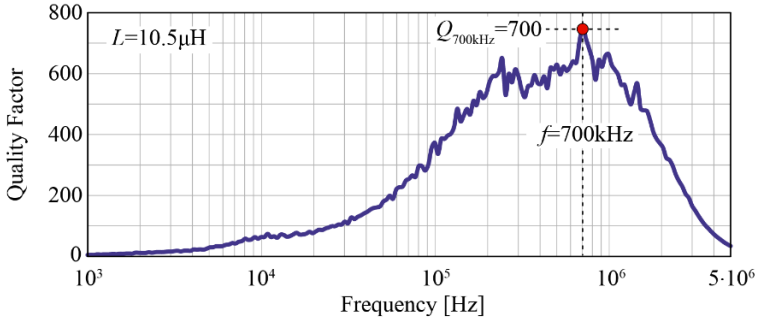
- High Resonance Frequency → Inductive Behavior up to High Frequencies
- Extremely Low AC-Resistance → Low Conduction Losses up to High Frequencies
- High Quality Factor









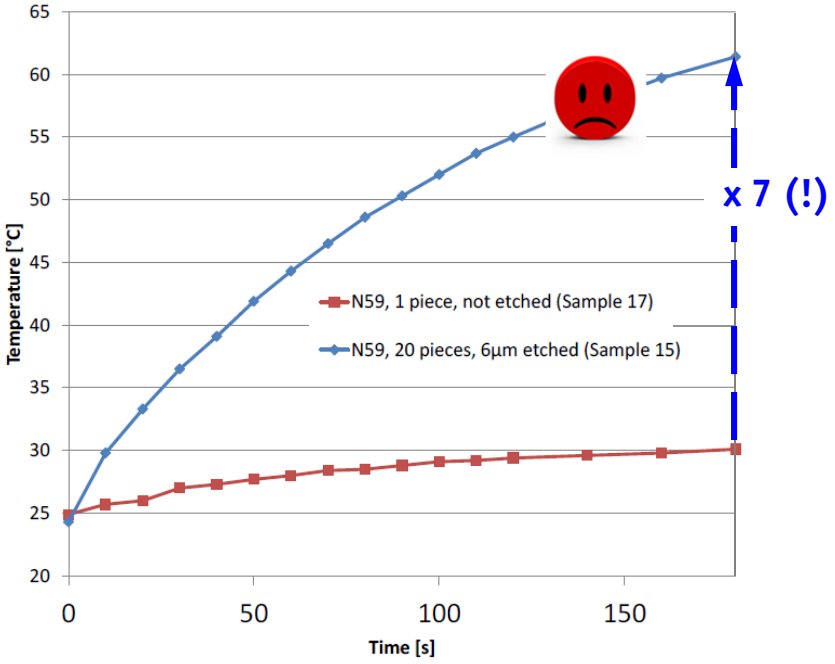


- Shielding Eliminates HF Current through the Ferrite → Avoids High Core Losses
- Shielding Increases the Parasitic Capacitance

High Frequency Inductors (3)

- Comparison of Temp. Increase of a Bulk and a Sliced Ferrite Sample @ 70mT / 800kHz

* Knowles (1975!)

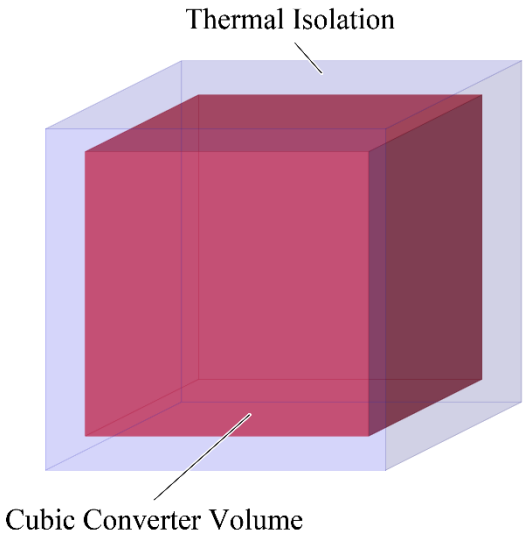


- Cutting of Ferrite Introduces Mech. Stress
- Significant Increase of the Loss Factor
- Further Treatment Still to be Clarified

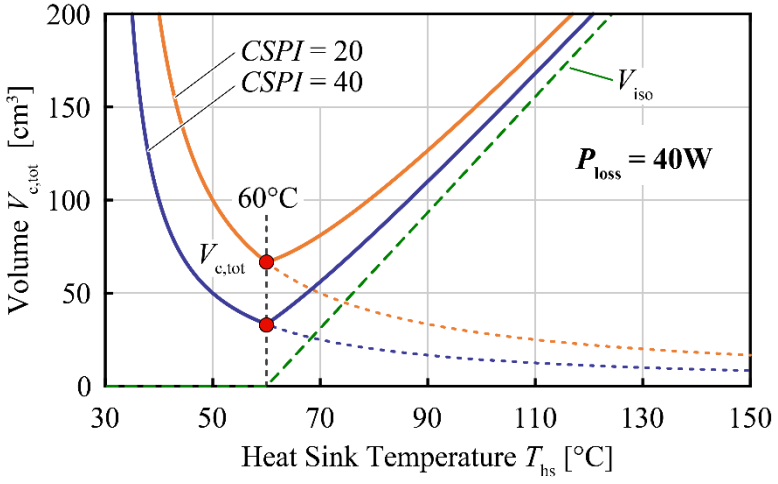
Thermal Management (1)

- 30°C max. Ambient Temperature
- 60°C max. Allowed Surface and Air Outlet Temperature

- Evaluation of Optimum Heatsink Temp. for Thermal Isolation of Converter



$$CSPI\left[\frac{W}{K\cdot liter}\right] = \frac{G_{th,S-a}^{(HS)}\left[\frac{W}{K}\right]}{Vol_{CS}\left[liter\right]} = \frac{1}{R_{th,S-a}^{(HS)}\left[\frac{K}{W}\right]\cdot Vol_{CS}\left[liter\right]}$$



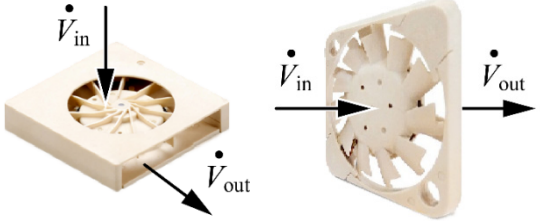
- Minimum Volume Achieved w/o Thermal Isolation with Heatsink @ max. Allowed Surface Temp.

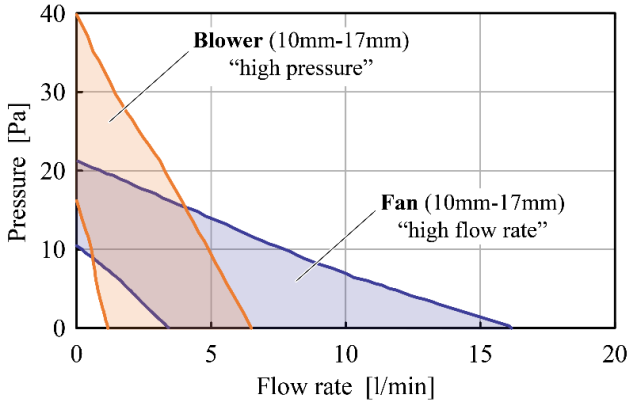
Thermal Management (2)

- Overall Cooling Performance Defined by Selected Fan Type and Heatsink

– Radial Blower

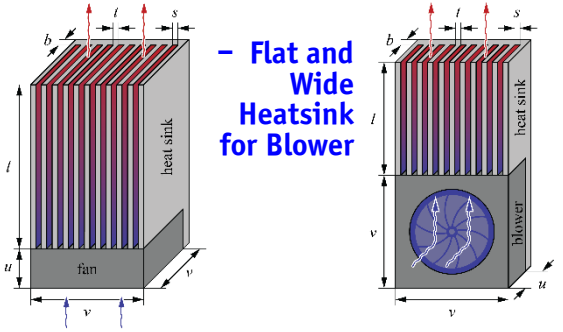
– Axial Fan

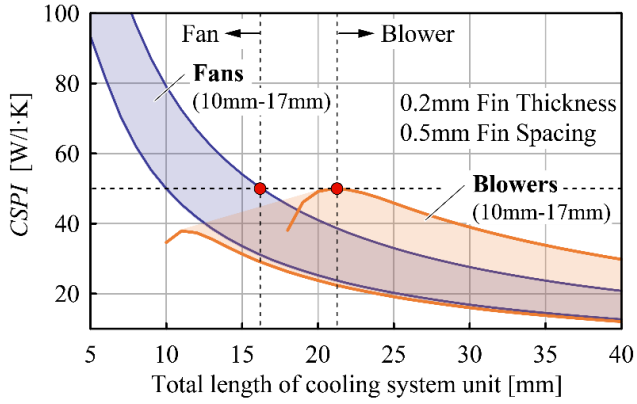




– Square Cross Section of Heatsink for Using a Fan

– Flat and Wide Heatsink for Blower



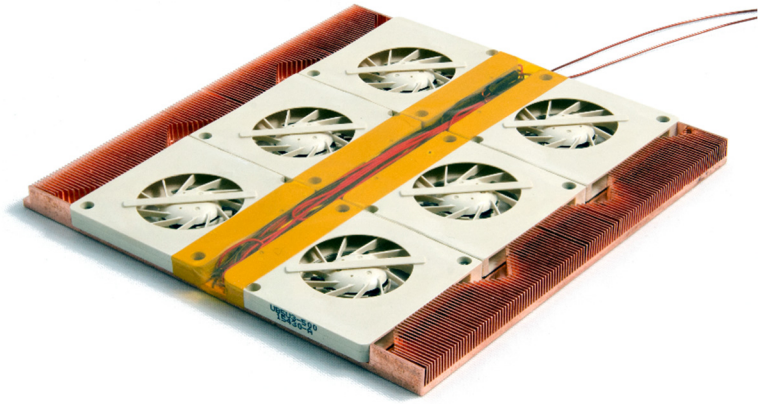


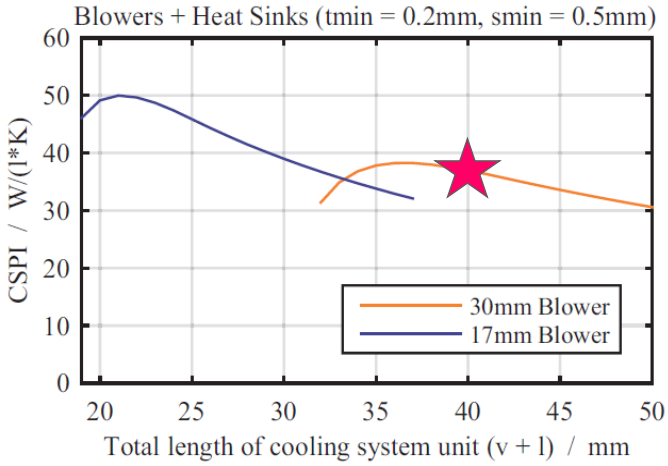
- Optimal Fan and Heat Sink Configuration Defined by Total Cooling System Length
- Cooling Concept with Blower Selected → Higher *CSPI* for Larger Mounting Surface

Thermal Management (3)

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters

- 200um Fin Thickness
- 500um Fin Spacing
- 3mm Fin Height
- 10mm Fin Length
- CSPI = 37 W/(dm³.K)
- 1.5mm Baseplate





- $CSPI_{eff}$= 25 W/(dm³.K) Considering Heat Distribution Elements
- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)

Little Box 1.0

★ 135 W/in³

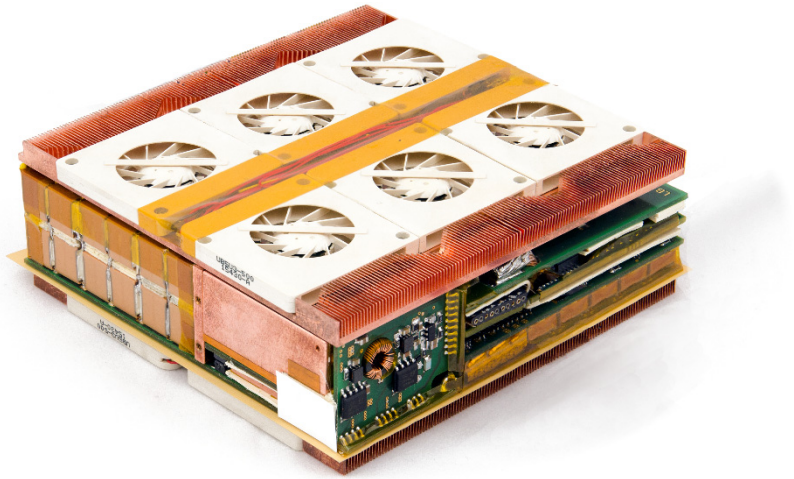
- System Employing Active CeraLink™ 1-Φ Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- f_S = 250kHz ... 1MHz
- 96,3% Efficiency @ 2kW
- T_c=58°C @ 2kW

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%

■ Compliant to All "Original" Specifications (!)

- i_{gnd} < 5mA (!)
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents



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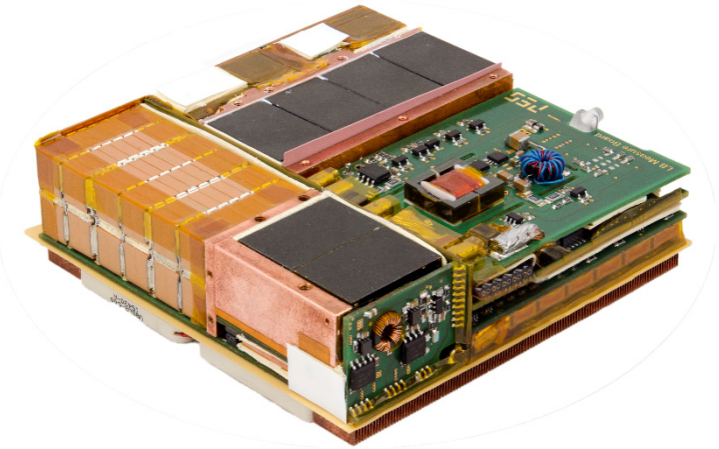
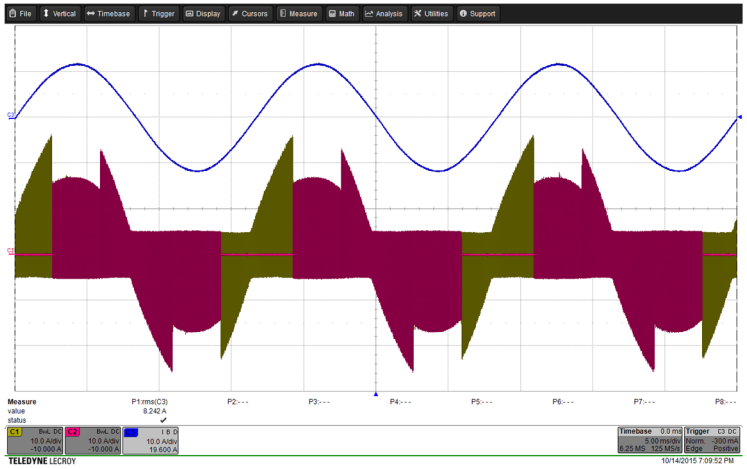


Measurement Results (1)

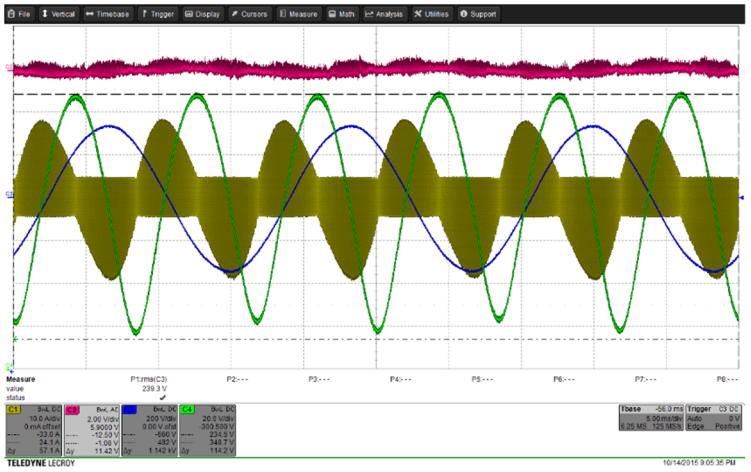
- System Employing Active CeraLink™ 1-Φ Power Pulsation Buffer

  - Ohmic Load / 2kW

Output Current (10 A/div)
Inductor Current Bridge Leg 1-1 (10 A/div)
Inductor Current Bridge Leg 1-2 (10 A/div)



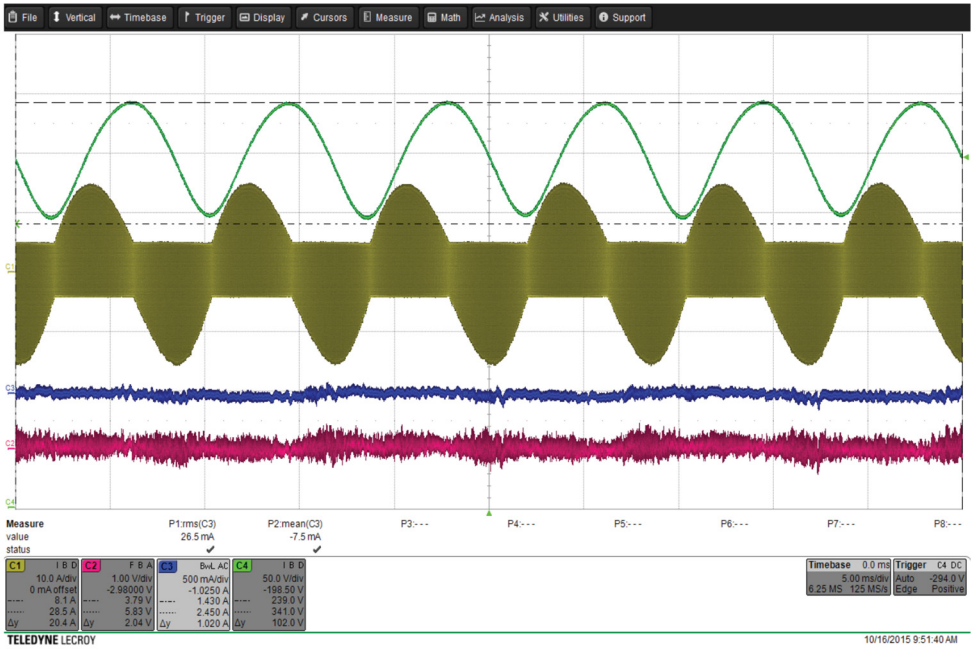
DC Link Voltage (AC-Coupl., 2 V/div)
Buffer Cap. Voltage (20 V/div)
Buffer Cap. Current (10 A/div)
Output Voltage (200 V/div)



- Compliant to All Specifications

Measurement Results (2)

- System Employing Active CeraLink™ 1-Φ Power Pulsation Buffer



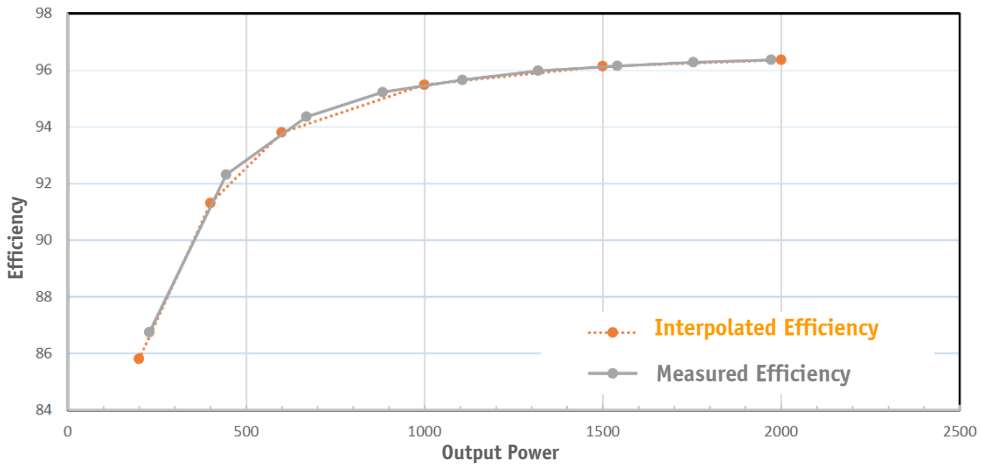
Buffer Cap. Voltage (50 V/div)
Buffer Cap. Current (10 A/div)
DC Inp. Curr. (AC Coupl. 500 mA/div)
DC Link Voltage (AC Coupl. 1 V/div)

- Stationary Operation @ 2kW Output Power

Measurement Results (3)

- System Employing Active CeraLink™ 1-Φ Power Pulsation Buffer

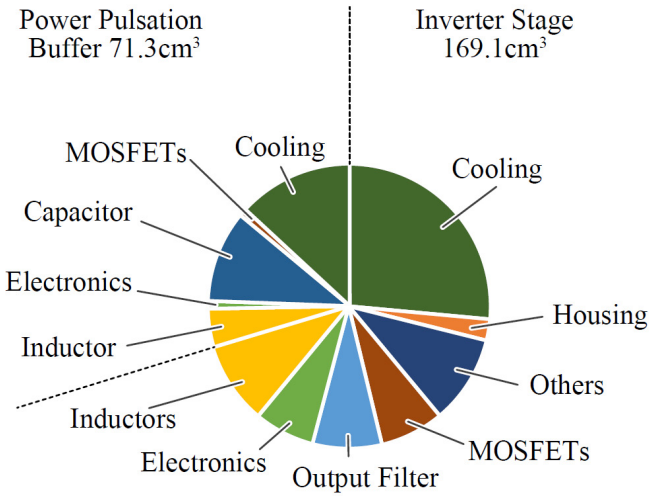
★ η_w=95.07% Weighted Efficiency



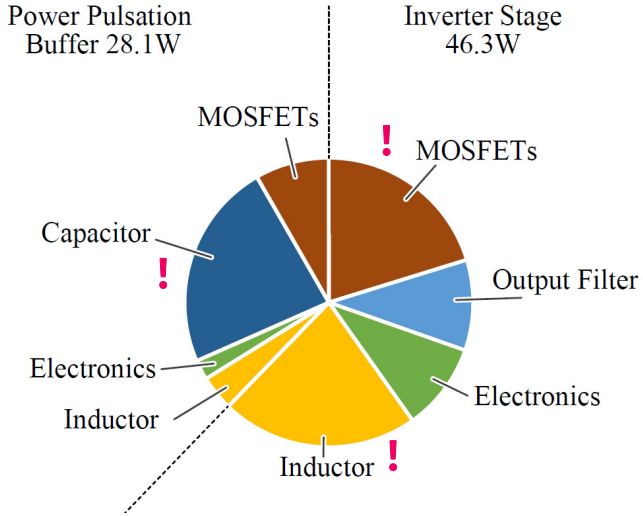
- Rel. Low Part Load Efficiency → Rel. High Output Power Independent Loss Components

Volume & Loss Distribution

- Volume Distribution (240cm³)



- Loss Distribution (75W)

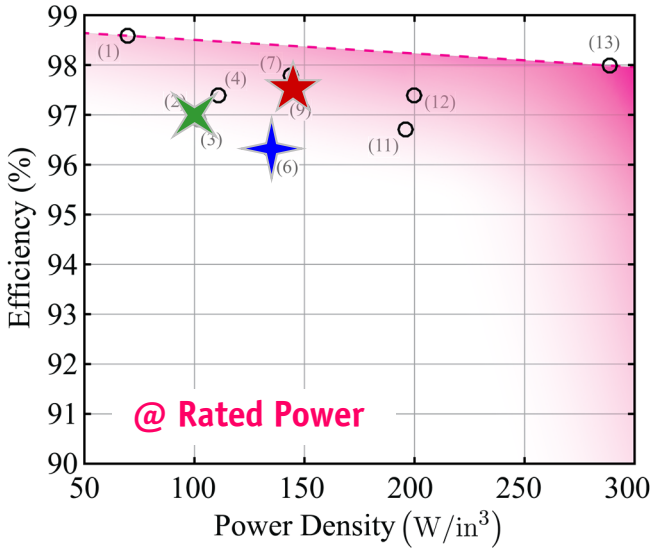


- Large Heatsink (incl. Heat Conduction Layers)
- Large Losses in Power Fluctuation Buffer Capacitor (!)
- TCM Causes Relatively High Conduction & Switching Losses @ Low Power
- Relatively Low Switching Frequency @ High Power – Determines EMI Filter Volume

Finalists - Performance Overview

- 18 Finalists (3 No-Shows)
- 7 Groups of Consultants / 7 Companies / 4 Universities

Note: Numbering of Teams is Arbitrary



(1) Virginia Tech
(2) Schneider Electric
(3) EPRI (Univ. of Tennessee)
(4) Venderbosch
(5) Energy Layer
(6) ETH Zurich
(7) Rompower
(8) Tommasi-Bailly
(9) Red Electric Devils
(10) AHED
(11) FH IISB
(12) Univ. of Illinois
(13) AMR

- 70 ... 300 W/in³
- 35 kHz ... 500kHz ... 1 MHz (up to 1MHz: 3 Teams)
- Full-Bridge or DC/|AC|Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- GaN (11 Teams) / SiC (2 Teams) / Si (2 Teams)

Google

Little Box Challenge Grand Prize Winner

Dr. Paul Bleus
Directeur R&D

CET POWER

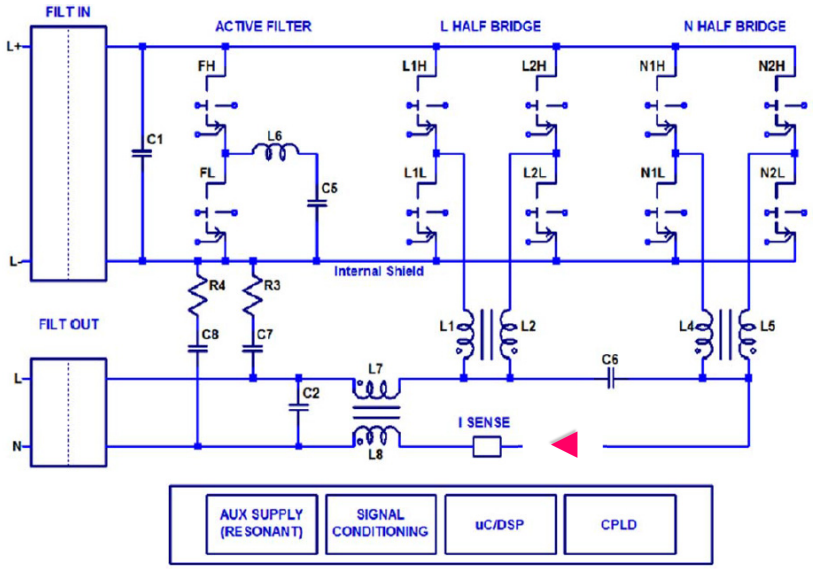
Red Electric Devils

Olivier Bomboir, Paul Bleus, Fabrice Frebel, Thierry Joannes, Francois Milstein, Pierre Stassain, Christophe Geuzaine, Carl Emmerechts, Philippe Laurent

Red Electric Devils

★ 145 W/in³

- No Low-Frequ. Common-Mode Output Voltage Comp. → i_{gnd} < 5mA (!)
- Buck-Type DC-Side Active Power Pulsation Filter (MLCC Cap. <150µF, 200V_{pp})



- 2 x Interleaved Bridge Legs for Each Half-Bridge
- DM Inductors (L_1/L_2 and L_4/L_5) and Series Connected CM Inductor (L_7/L_8)
- Single Open-Loop Hall Sensor Outp. Curr. Measurement + Observer-Based Curr. Reconstruction

Red Electric Devils

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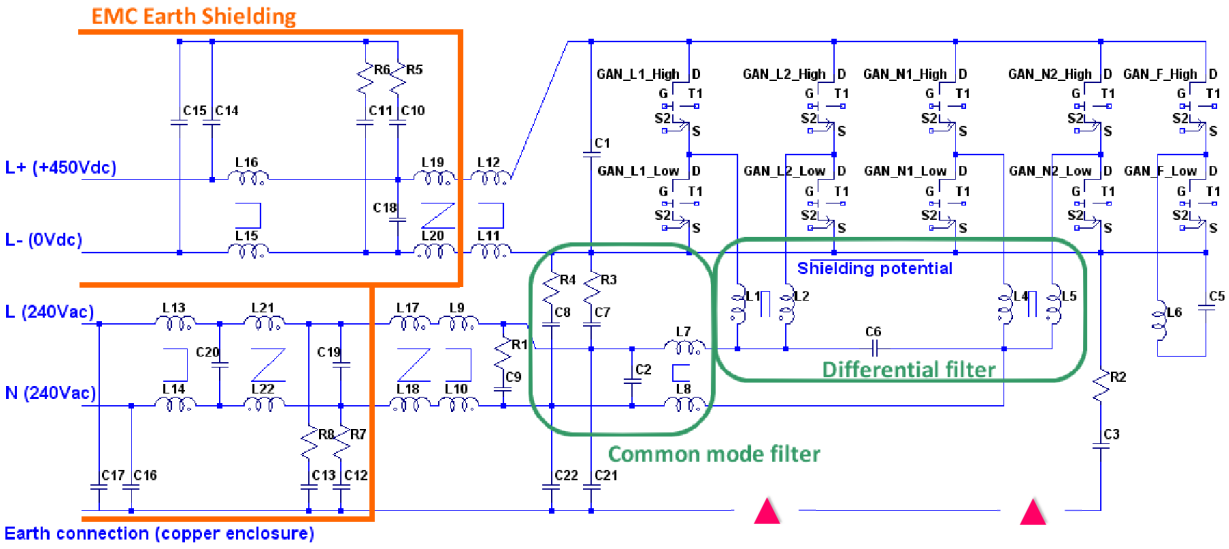
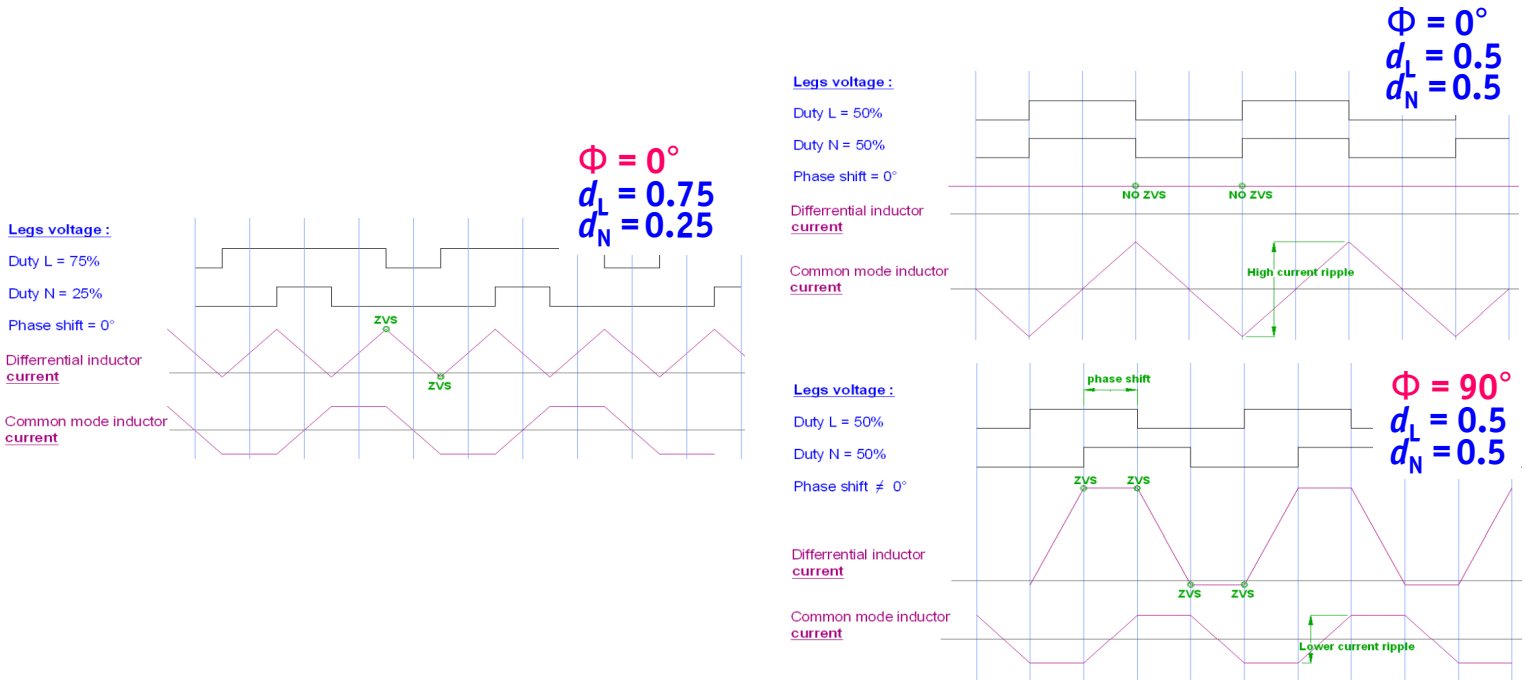


- DSP & CPLD Control
- GaN Systems @ ZVS (35kHz ... 240kHz)
- Shielded Multi-Stage EMI Filter @ DC Input & AC Output

Red Electric Devils

★ 145 W/in³

- Variable Phase-Shift of the Half-Bridges (0° or 90°) Dep. on Duty Cycle

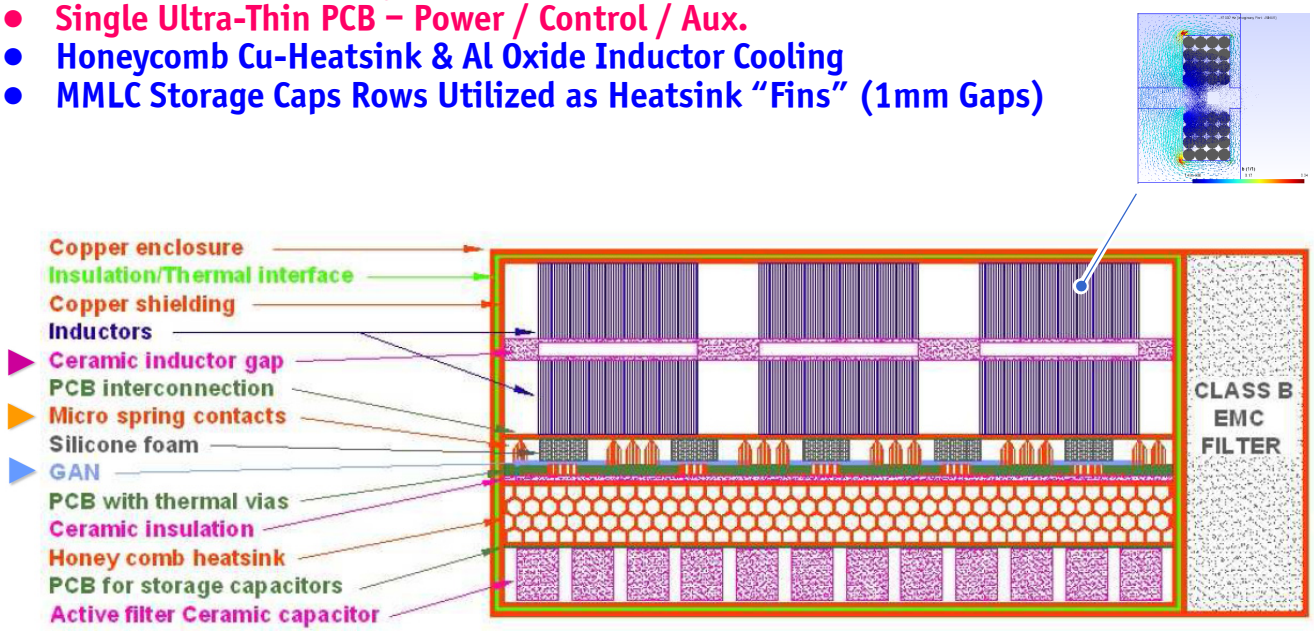


- Selection of Opt. Phase Shift & Sw. Frequency for ZVS & Min. Size of Filter Ind. L_{CM} & L_{DM}

Red Electric Devils

★ 145 W/in³

- 3D Sandwich Assembly
- Single Ultra-Thin PCB – Power / Control / Aux.
- Honeycomb Cu-Heatsink & Al Oxide Inductor Cooling
- MMLC Storage Caps Rows Utilized as Heatsink "Fins" (1mm Gaps)



- 145 W/in³
- 95.4 % CEC Efficiency
- i_{gnd} < 5mA (!)
- CSPI = 22.6 W/(dm³.K) - Heatsink & Axial Fan

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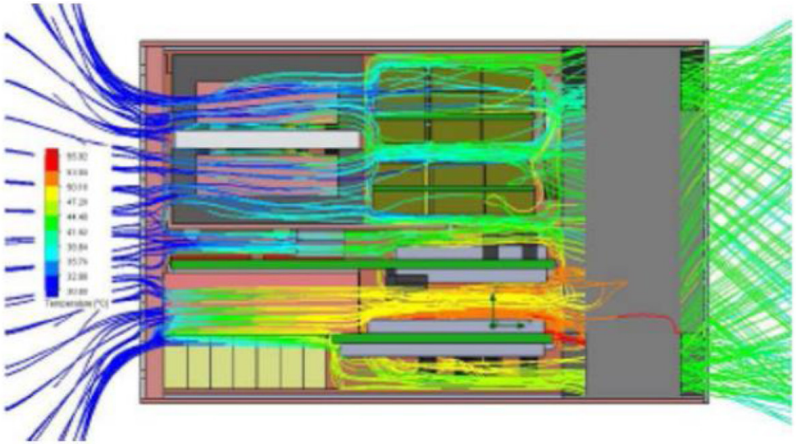
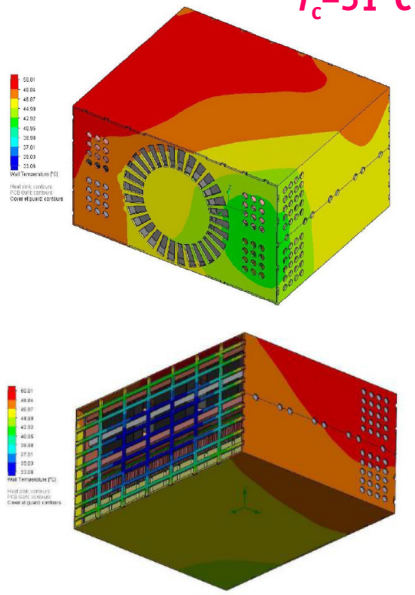


T_c=51°C



- 145 W/in³
- 95.4 % CEC Efficiency
- i_{gnd} < 5mA (!)
- CSPI = 22.6 W/(dm³.K) - Heatsink & Axial Fan

Google

Little Box Challenge
Top 3 Finalist

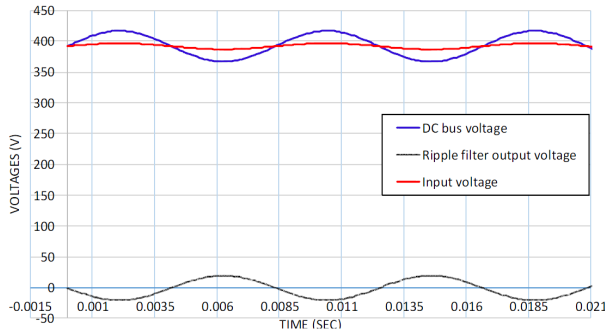
Schneider Electric *Team*

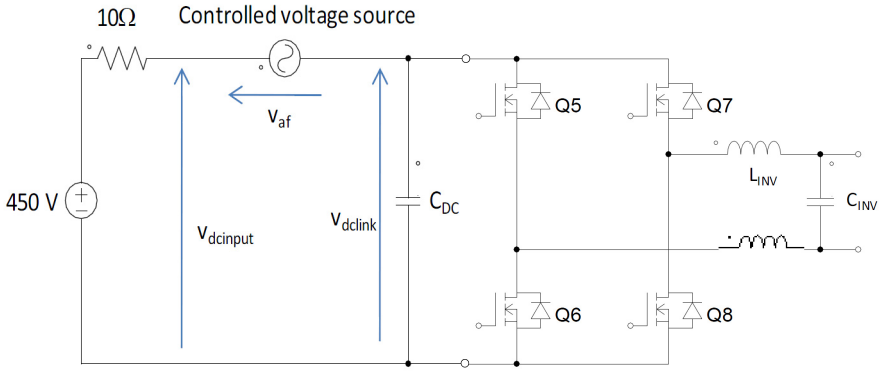
Miao-xin Wang, Rajesh Ghosh, Srikanth Mudiyula, Radoslava Mitova, David Reilly, Milind Dighrasker, Sajeesh Sulaiman, Alain Dentella, Damir Klikic, Michael Hartmann

Schneider Electric Global Team

★ 100 W/in³

- High Efficiency & Robustness Preferred → Larger Size
- PWM of Both Legs of Output Full-Bridge → No Low. Frequ. CM Output Voltage Comp.
- DC-Side Series (!) Active Power Puls. Filter → Compensates 120Hz DC Link Volt. Variation





- C_{DC} = 400uF / 450V
- 1/5 Volume Comp. to only Bulk Capacitors
- $V_{dcinput}$ Ripple <10% (<30V_{pp}) @ Full Load

- Nanocrystalline CM Choke
- DC-Side & AC-Side EMI/RF Filter
- $Q_{5...8}$ – TO247 SiC MOSFETs, 45kHz of Both Legs

Schneider Electric Global Team

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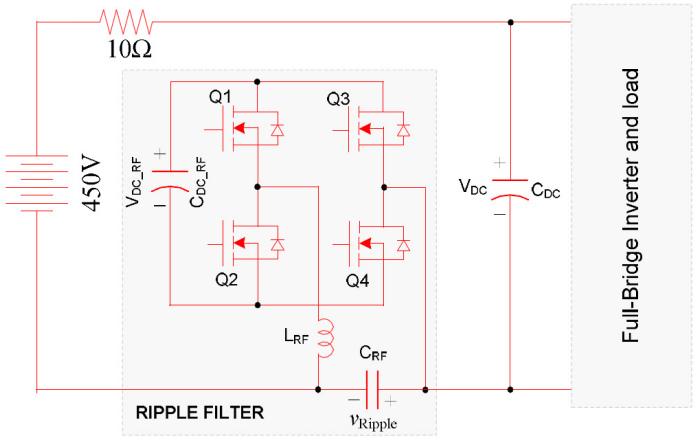
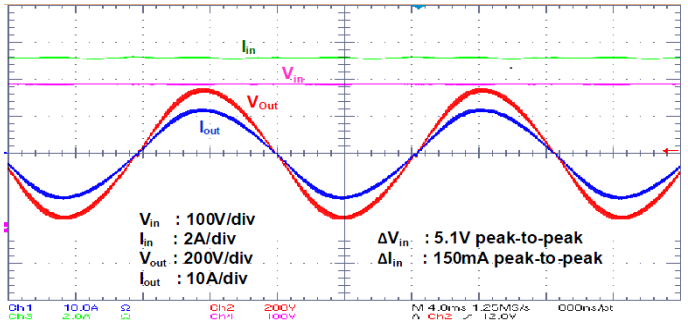


- i_{gnd} < 25mA (!)
- 97.2 % CEC Efficiency



- C_{DC_RF}=2 x 1500uF/25V, U_{DC_RF}=15V
- Only 52VA Processed Ripple Filter Power @ Rated Output (!)
- Q_1/Q_2 & Q_3/Q_4 - $R_{ds,on}$= 2.2mΩ MOSFETs (40V, 100A), w/o Heatsink, f_S= 130kHz of Both Legs
- TI Piccolo DSP Control of Entire System / Open Loop Control of 120Hz Comp. Filter

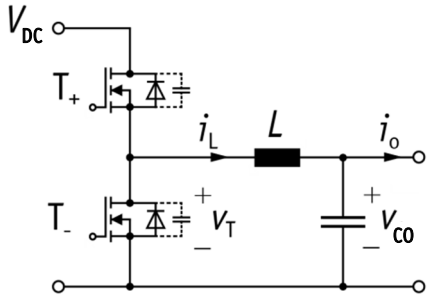
Optimization of Little-Box 1.0

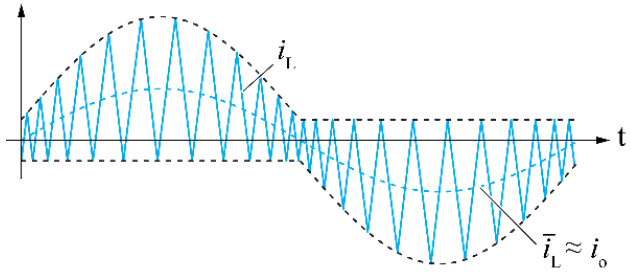
Adv. Modulation / Circuit Concepts
Measurement of Buffer Cap. Performance
Measurement of GaN ZVS & On-State Losses
Measurement of Multi-Aircap Core Losses
ηρ-Pareto Optimization

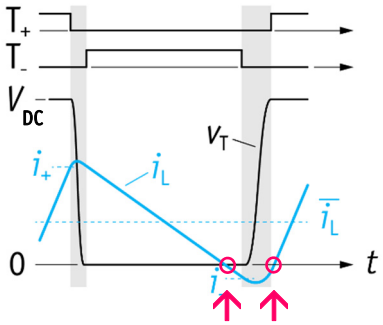
Eff. Optimal f_S-Modulation

- TCM → ZVS but Large Current Ripple & Wide Frequency Variation
- PWM → Const. Sw. Frequency but Hard Sw. @ Current Maximum

- Opt. Combination of TCM & PWM → Optim. Variation of Local Sw. Frequ. Over Output Period
- Exp. Determination of Loss-Opt. Local Sw. Frequency f_{OFM} Considering DC/DC Conv. Stage







- Loss-Optimal Local Sw. Frequ. f_{OFM} for Given V_{DC} & Local i_o & v_{CO}
- DC/AC Properties Calculated Assuming Local DC/DC Operation

Eff. Optimal f_S-Modulation

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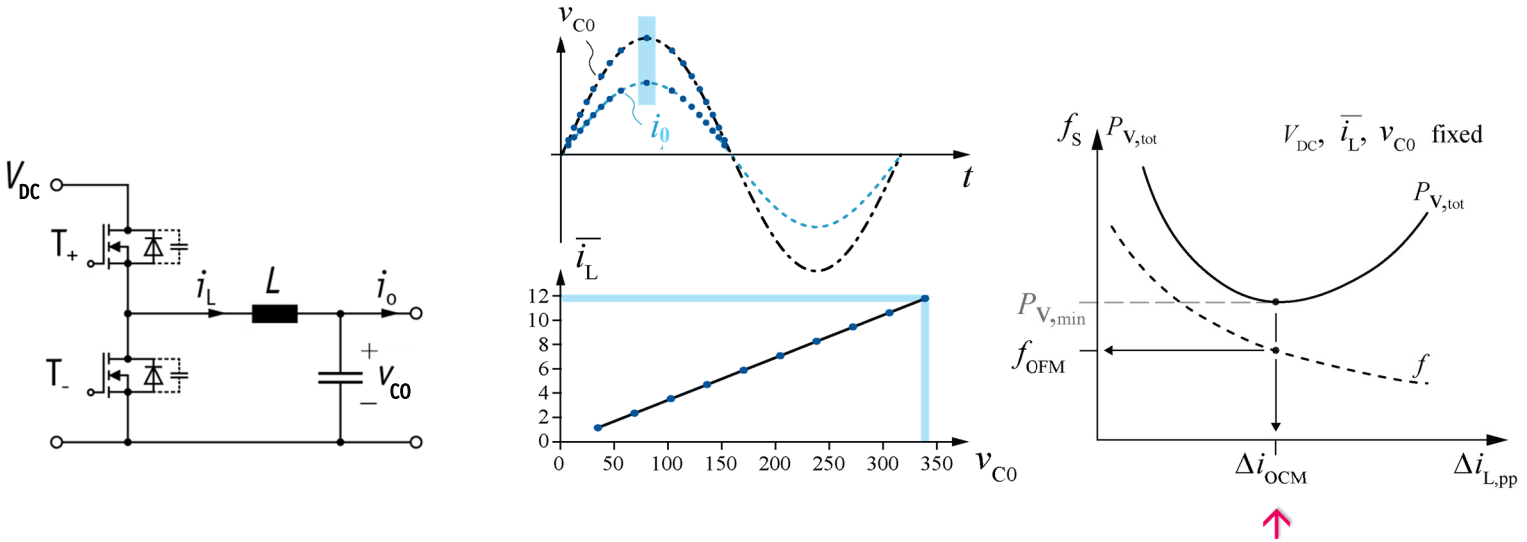
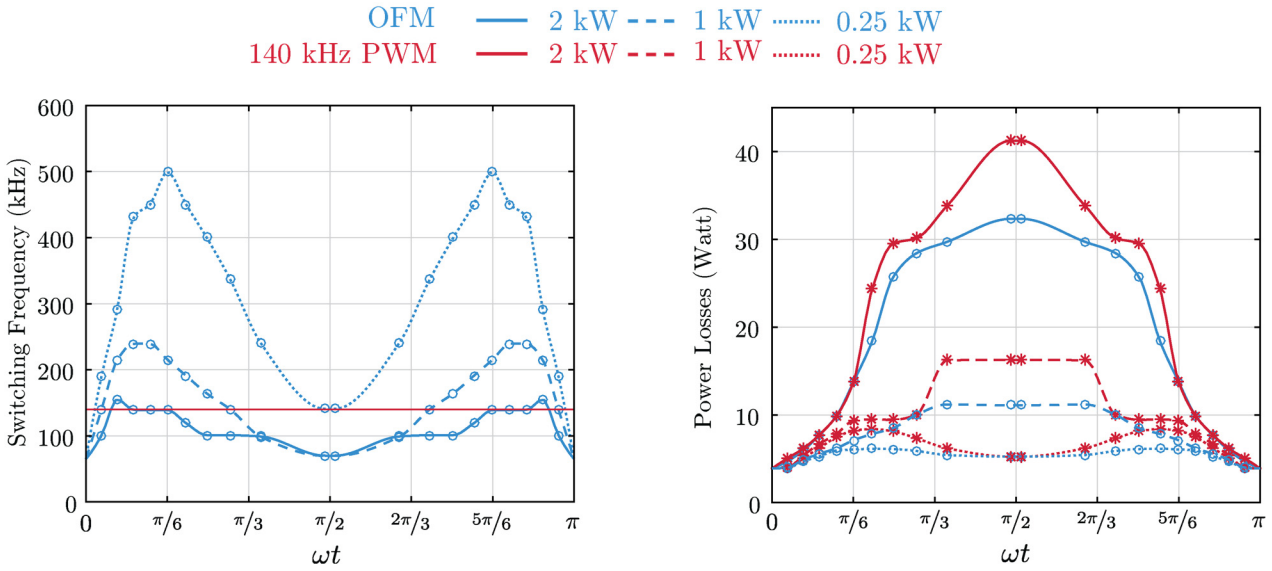


- DC/AC Properties Calculated Assuming Local DC/DC Operation
- Loss-Optimal Local Sw. Frequ. f_{OFM} for Given V_{DC} & Local i_0 & v_{C0}

Eff. Optimal f_S-Modulation

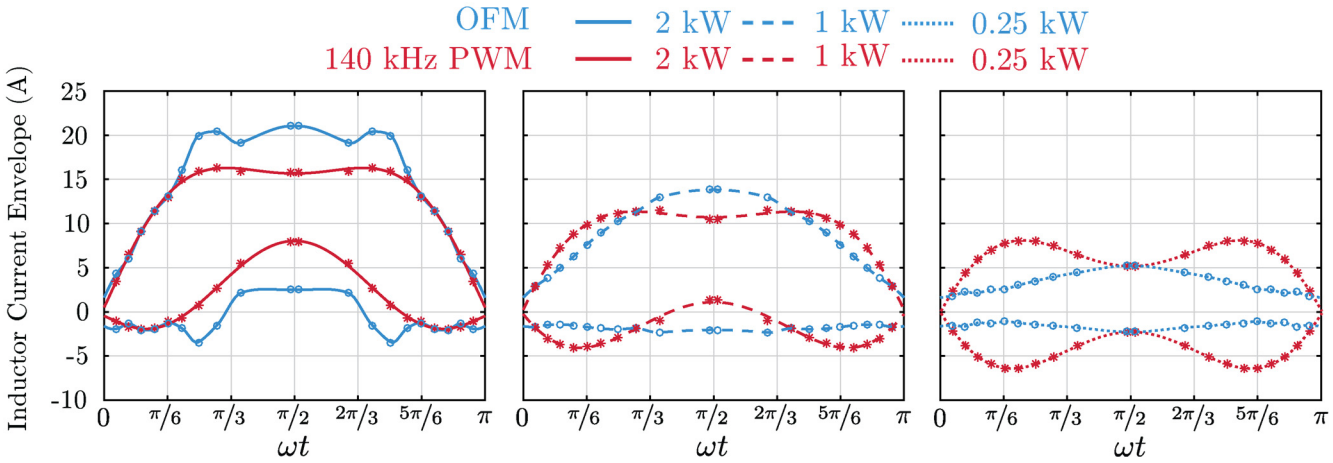
- Resulting Time-Dependency of Optimal Sw. Frequ. & Power Loss
- Comparison with 140 kHz Const. Sw. Frequency PWM



- Higher Average Switching Frequency f_s @ Light Loads
- Reduction of f_s @ Mains Voltage Peak (for Ohmic Load) for Sustaining ZVS

Eff. Optimal f_S-Modulation

- **Optimal Inductor Current Envelope for Diff. Output Power Levels**

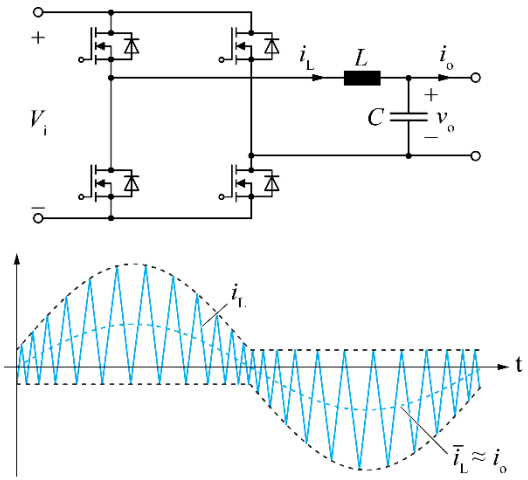


- **Higher Average Switching Frequency f_s @ Light Loads**
- **Reduction of f_s @ Mains Voltage Peak (for Ohmic Load) for Sustaining ZVS**

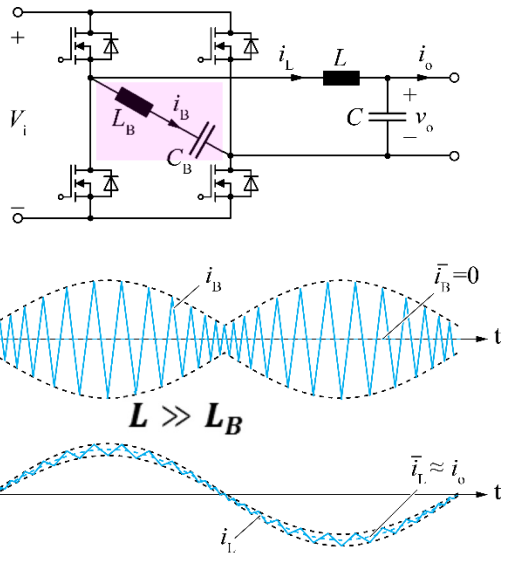
iTCM Inverter Topology

- TCM → Challenging Inductor Design → HF & LF Currents
- iTCM → Add. LC-Circuit / Separation of LF & HF Currents → $L >> L_B$ (P. Jain, 2015)

– TCM



– iTCM



– iTCM :

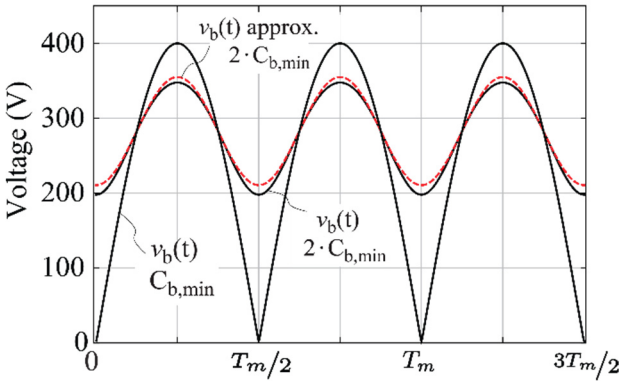
- Low Output Curr. Ripple / Noise → Reduced Filtering Effort
- Variable f_S PWM Applicable, No i=0 Detect. → Simple Control Strategy (DSP)
- Dedicated LF and HF Inductor Designs Possible → Improved Conv. Efficiency

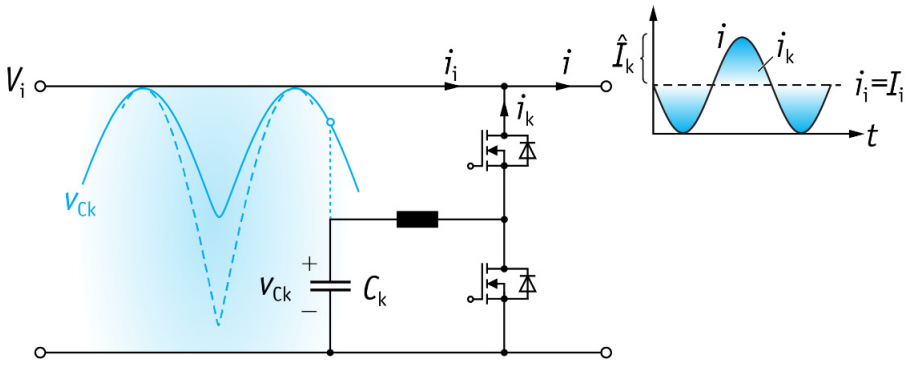
Measurements

Buffer Capacitor Losses / Cap.
Power Semicond. ZVS & On-State Losses
Ferrite Multi-Airgap Core Losses

CeraLink™ vs. X6S (1)

- Electrolytic Capacitors → Limited by Lifetime Current Limit
- X6S MLCC, 2.2µF, 450 V Class II → Highest Energy Density but Low Cap. @ High DC Bias
- CeraLink™,1µF /2µF, 650 V → PLZT Ceramic, High Cap. @ High DC Bias
- CeraLink™ Allows Op. @ 125°C → Very Low ESR @ High Frequencies

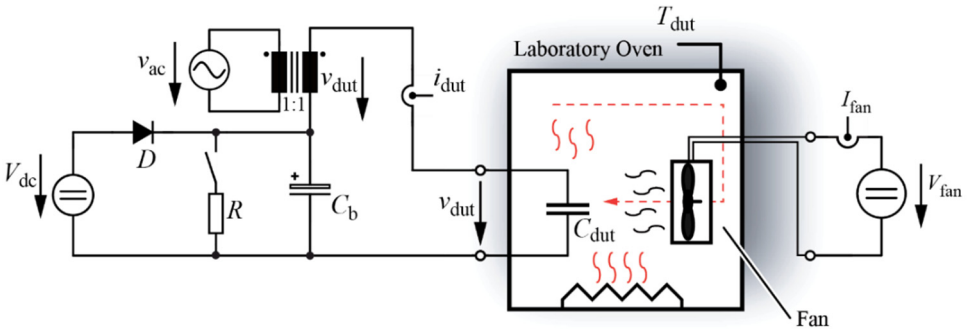


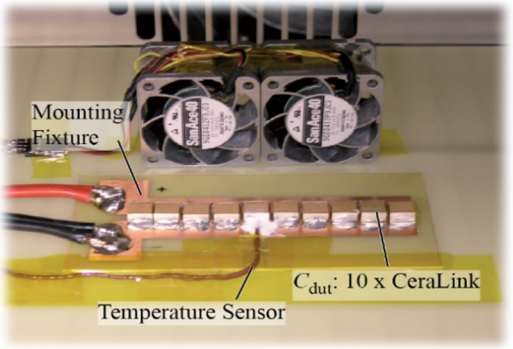


- PPB Design Optimiz. Requires Large-Signal Capacitance and Power Loss Data in All Operating Points

CeraLink™ vs. X6S (2)

- Electrolytic Capacitors → Limited by Lifetime Current Limit
- X6S MLCC, 2.2µF, 450 V Class II → Highest Energy Density but Low Cap. @ High DC Bias
- CeraLink™,1µF /2µF, 650 V → PLZT Ceramic, High Cap. @ High DC Bias
- CeraLink™ Allows Op. @ 125°C → Very Low ESR @ High Frequencies

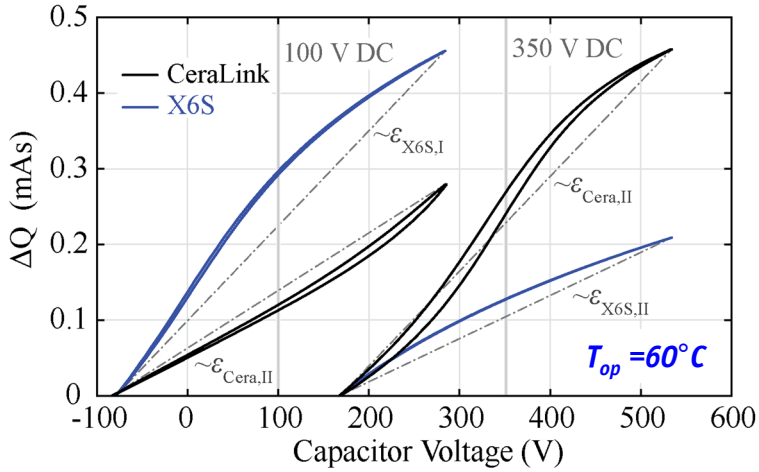


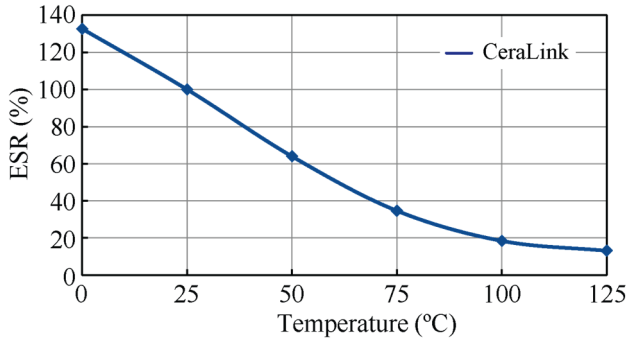


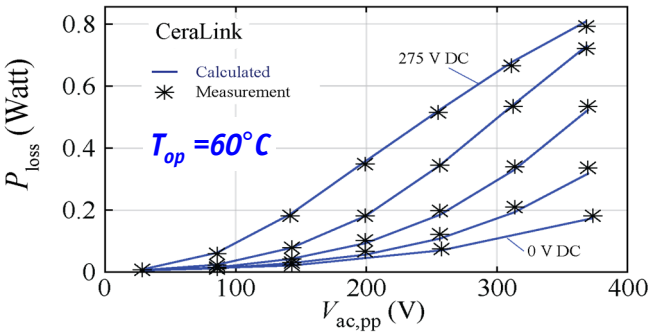
- Experimental Setup for Generation of DC Bias & Superimposed AC Voltage

CeraLink™ vs. X6S (3)

- CeraLink™
  - Large-Signal 120Hz Excitation Reveals Large Hysteresis
  - Significantly Higher Losses @ 120Hz Comp. to X6S MLCC
  - ESR Drops Significantly @ Higher Temp.
  - 36µF (27µF) Blocks of Prepackaged Single Chips
  - Reliable Mech. Construction
- X6S MMLC
  - Only Available as Single Chips
  - Complicated Packaging







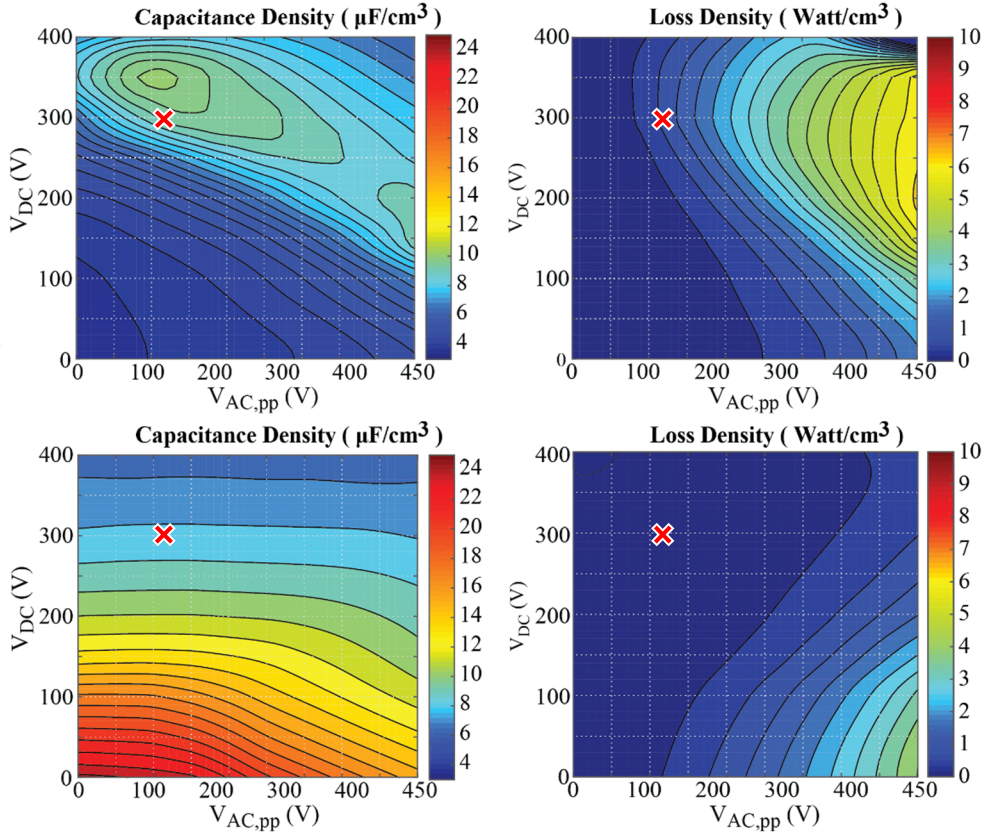
CeraLink™ vs. X6S (4)

- Variation of DC Bias and Superimposed AC Voltage @ 60°C Operating Temp.

× Designed Op. Point

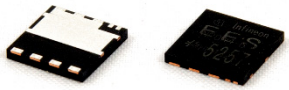
EPCOS/TDK CeraLink™ 2µF, 600V ▶

TDK Class II X6S MLCC 2.2µF, 450V ▶



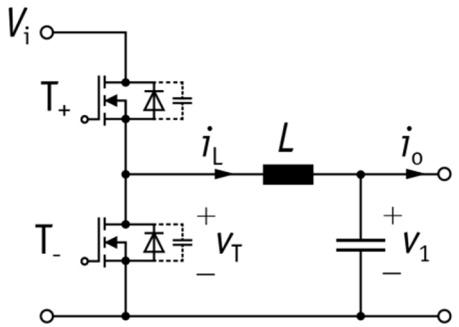
- PPB Design Optimiz. Requires Large-Signal Capacitance and Power Loss Data in All Operating Points

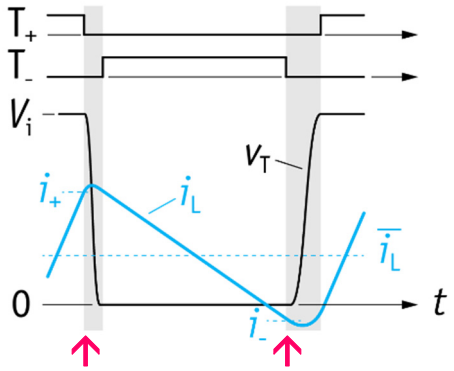
Measurement of GaN ZVS & On-State Losses →



Analysis of GaN Power Transistor *ZVS Losses*

- Little-Box 1.0 Experiments Indicated *Residual ZVS Losses of GaN Power Transistors*
- Losses Cannot be Explained by Remaining i_D, u_{DS} Overlap / Non-Ideal Gate Drive etc.





- Potentially Large Measurement Error for Electric Double-Pulse Sw. Loss Measurement
- Accuracy only Guaranteed by Direct Loss Measurement → Calorimetric Approach

Analysis of GaN Power Transistor *ZVS Losses*

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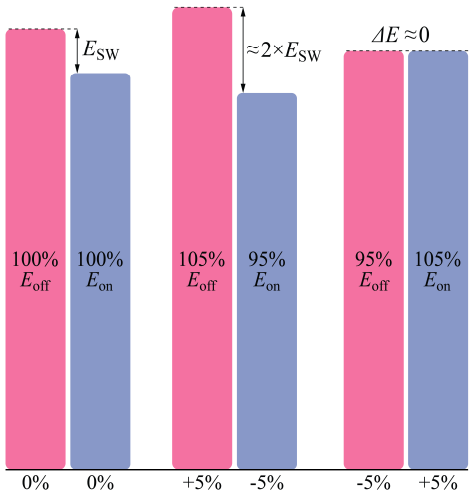
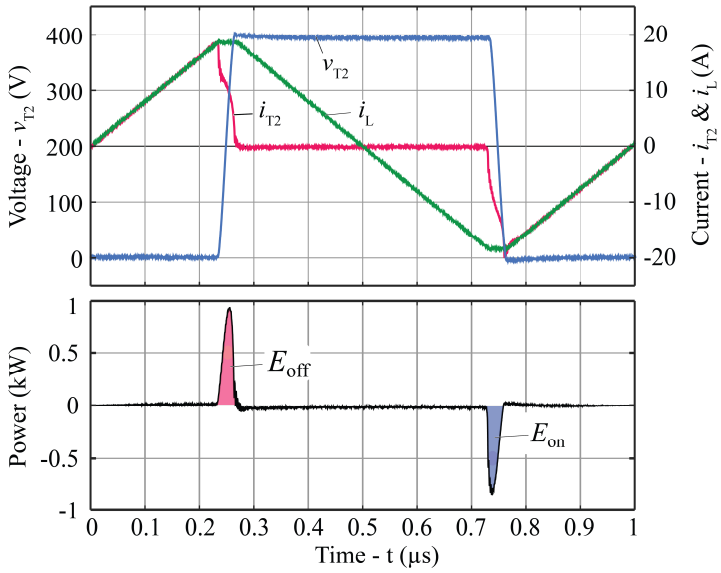
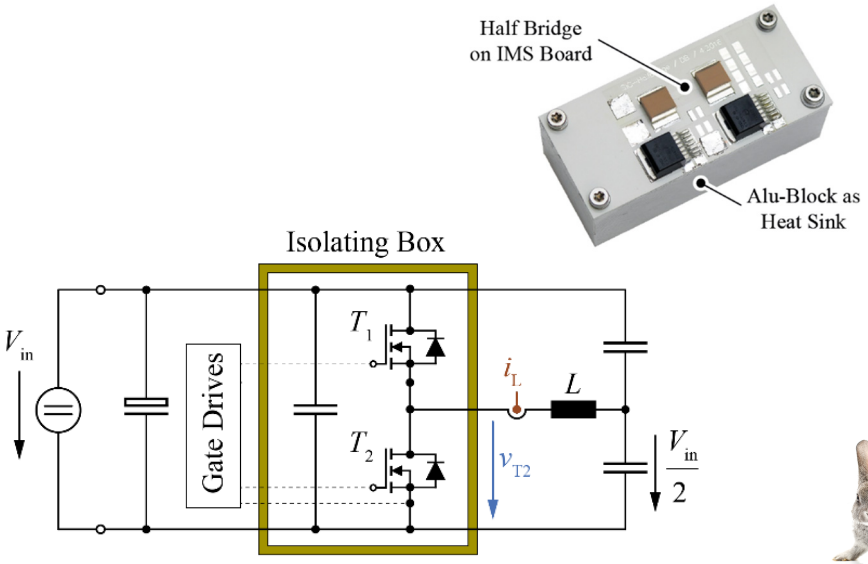


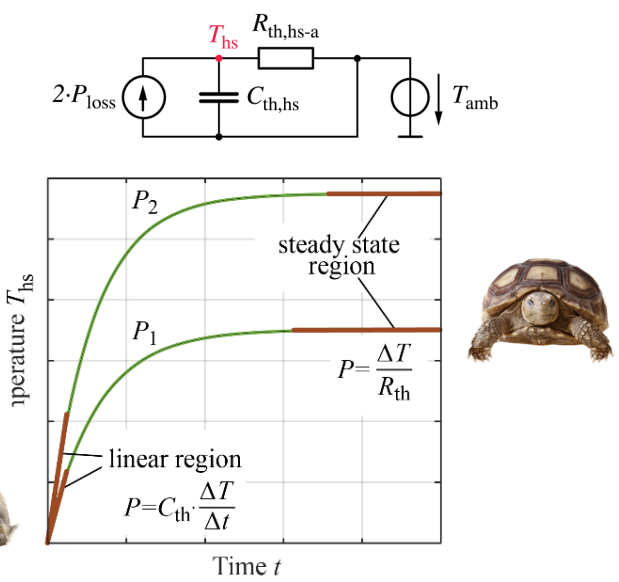


- Potentially Large Measurement Error for Electrical Double-Pulse Sw. Loss Measurement
- Accuracy only Guaranteed by Direct Loss Measurement → *Calorimetric Approach*

Calorimetric Measurement of *ZVS Losses*

- "Inductor in the Box" → Accurate DC Inp. & Outp. Power Measurement, Subtr. of Ind. Losses
- "Bridge Leg in the Box" → Direct Measurement of the Sum of Cond. & Sw. Losses





- "Bridge Leg in the Box" & Fast Measurement by $C_{th}.\Delta T/\Delta t$ Evaluation
- DC/DC Operation @ High Sw. Frequency for Large Ratio of Sw. and Conduction Losses
- Subtraction of the Cond. Losses from Datasheet or Dir. Measurement

Calorimetric Measurement of *ZVS Losses*

- "Bridge Leg in the Box" & Fast Measurement by $C_{th}.\Delta T/\Delta t$ Evaluation
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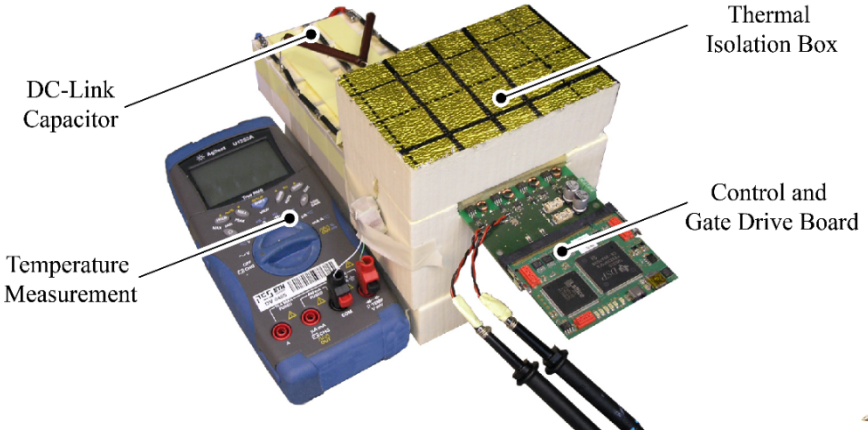
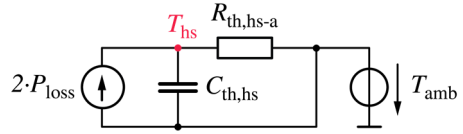
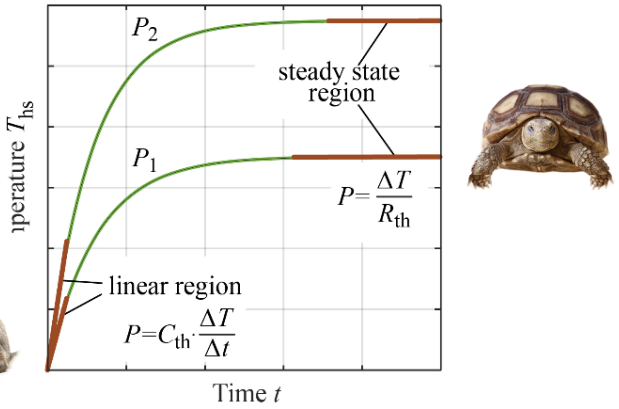




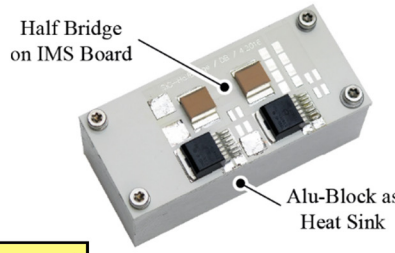


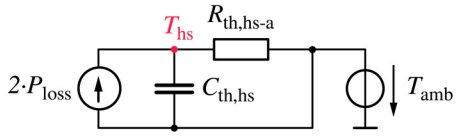
OPTOCON® OPTICAL SENSORS AND SYSTEMS

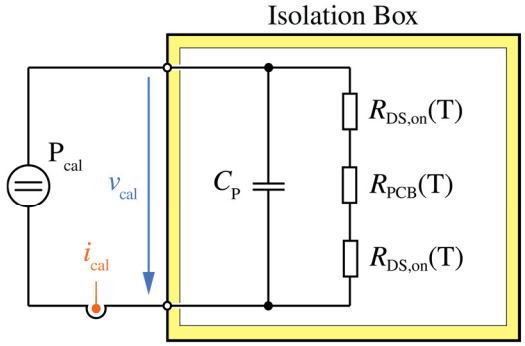
- Isolated Temp. Measurement with Optical Fiber (GaAs Crystal) Instead of Thermocouple
- Calibration by On-State of T_1 and T_2 & DC Current Operation / DC Power Loss Measurement

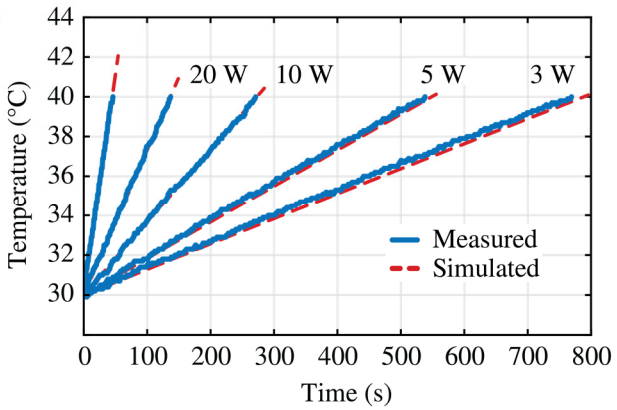
Calibration of "Bridge Leg in the Box" Setup

- Calibration by On-State of T_1 and T_2 & DC Current Operation / DC Power Loss Measurement
- Identification of Thermal Cap. C_{th} and Thermal Resistance R_{th}





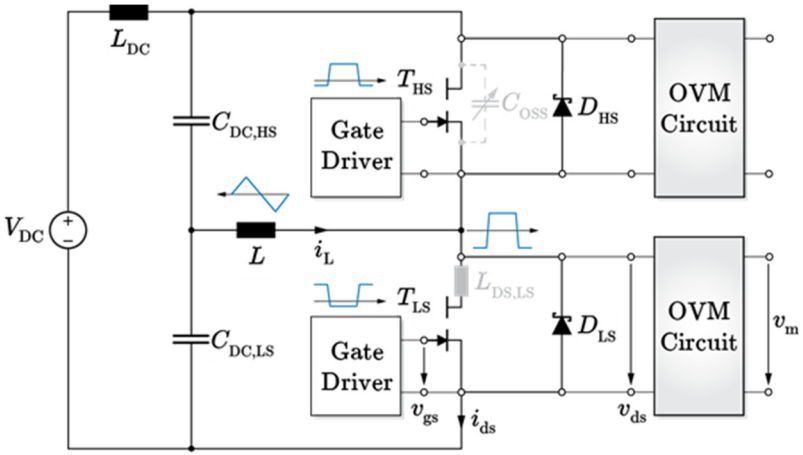


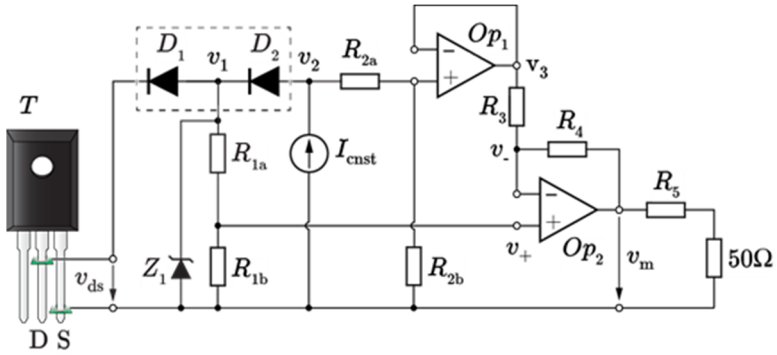


- DC Power Loss Measurement Ensures High Accuracy
- Thermal Behavior for Short Measurement Times Mainly Determined by C_{th}

Accurate On-State Voltage Measurement

- Clamping Diode for Limiting the On-State Voltage Measurement (OVM) Range to a Few Volts
- Subtraction of the SiC Diode Forward Voltage Drop for High Accuracy (2mV)





- Only 50ns Blanking Time – OVM Circuit Can also be Used for Dynamic $R_{DS,on}$ Measurement

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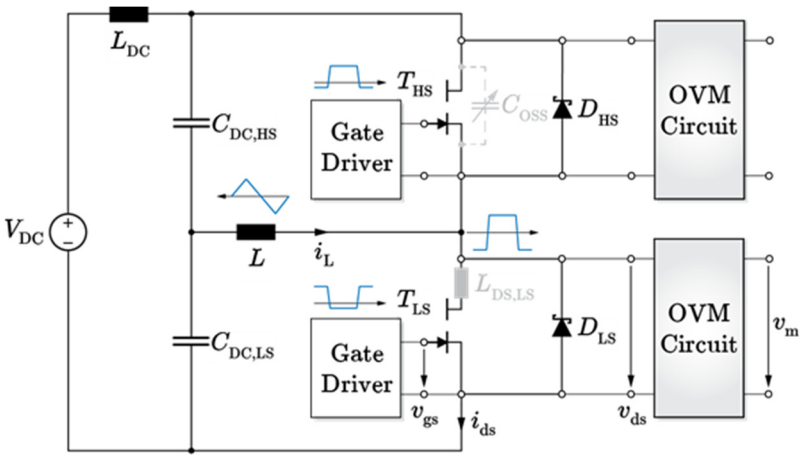
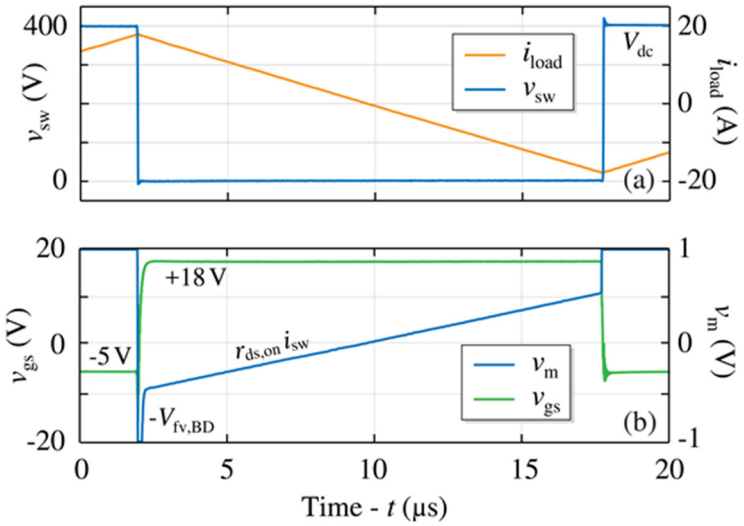
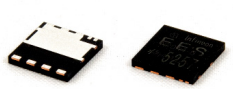


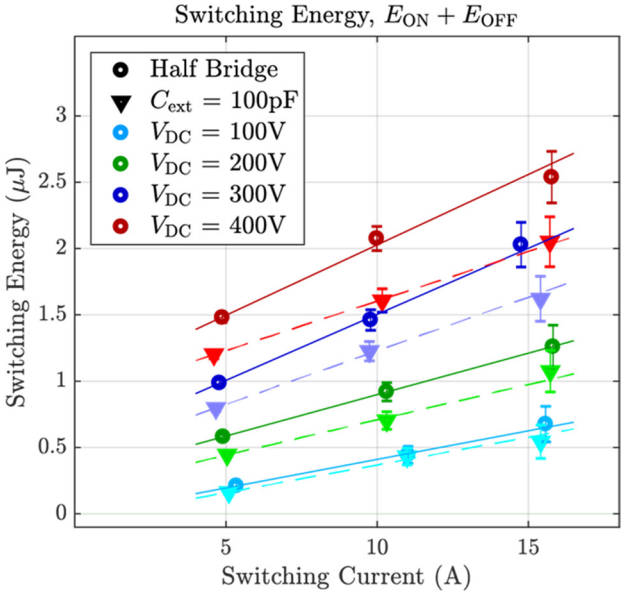


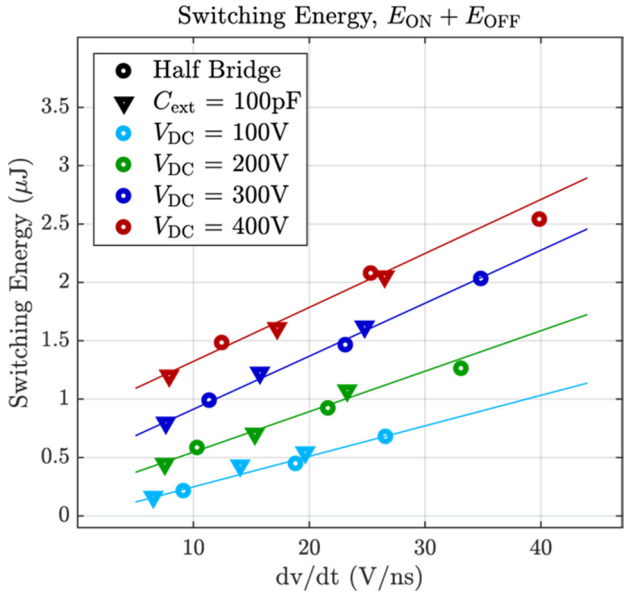
- Only *50ns* Blanking Time – OVM Circuit Can also be Used for Dynamic $R_{DS,on}$ Measurement

ZVS Loss Measurement Results (1)

- Measurement of Energy Loss per Switch and Switching Period
- GaN Enhancement Mode Power Transistor (600V, 70mΩ@25°C)
- Antiparallel CREE SiC Schottky Freewheeling Diode (600V, 3.3A)



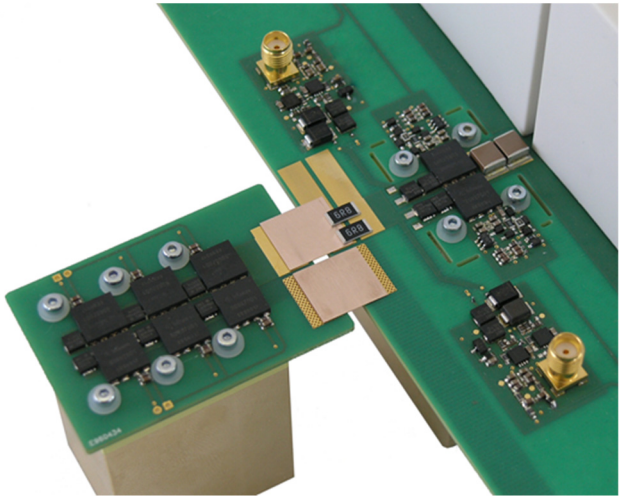


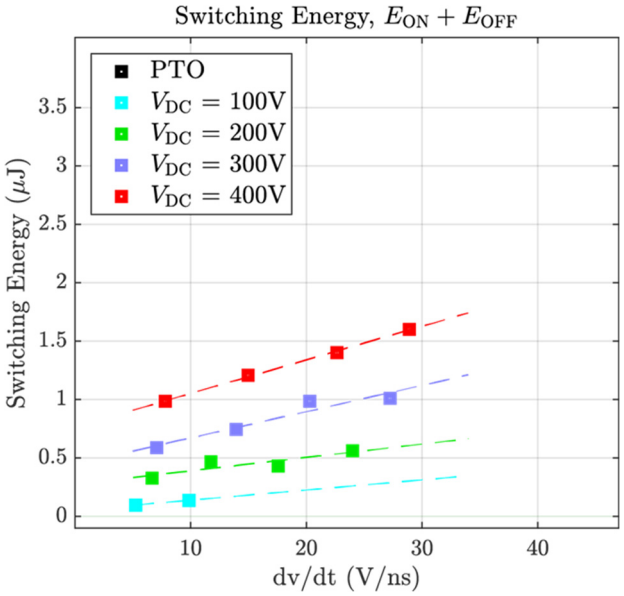


- Switching w/ and w/o 100pF Parallel Low-Loss SMD Multilayer Ceramic Chip Capacitor (450V)
- *dv/dt* Measured in 10%...90% of Turn-off Voltage, Behavior @ at Low *dv/dt* Still to be Clarified

ZVS Loss Measurement Results (2)

- Analysis of a *Permanently-Off Half-Bridge* Excited with Switch Node Voltage
- Measurement of Energy Loss per Switch and Switching Period





- Heating Indicates Losses in the Permanently-Off Devices
- Losses Comparable to the Losses of the Switching Half Bridge for Same d*v*/d*t*

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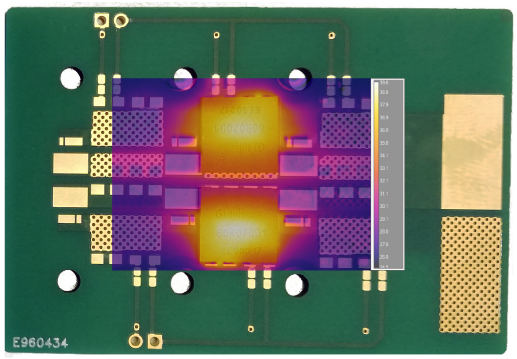

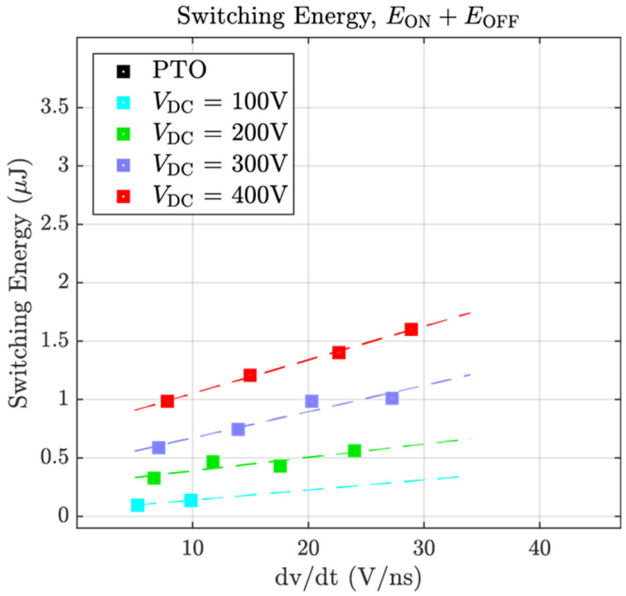

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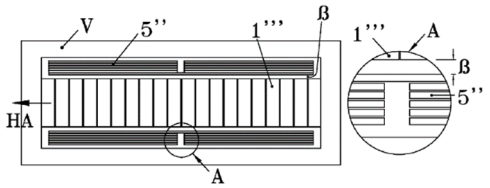
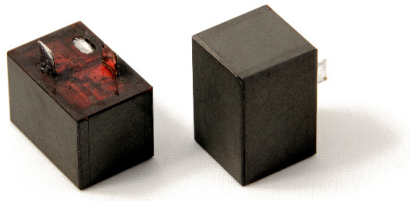
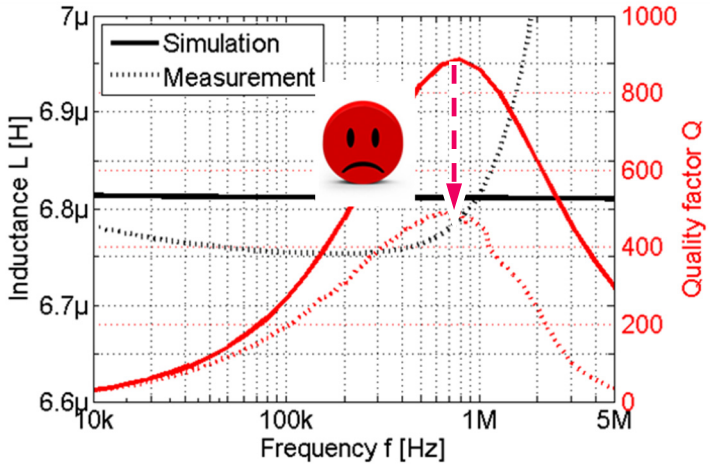
Measurement of Ferrite Multi-Airgap Core "Mystery" Losses

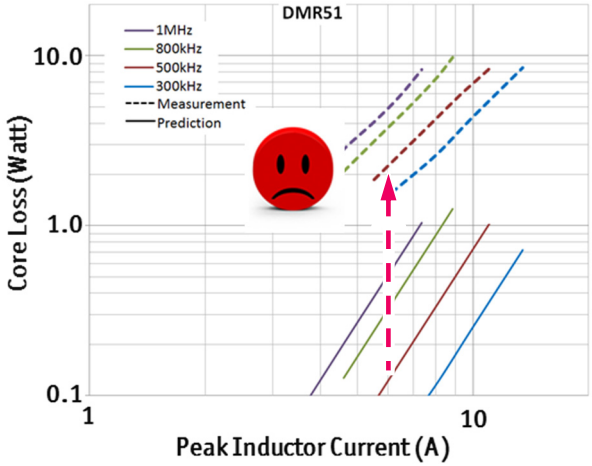


Multi-Airgap Inductor

- Ferrite E-Core with *50 x 0.3mm Thick Stacked Plates* as Center Post
- Power Loss of TCM Inductors Sign. Higher than Expected

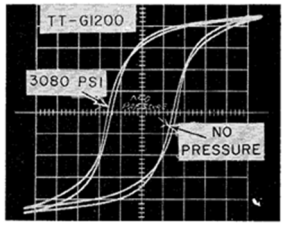




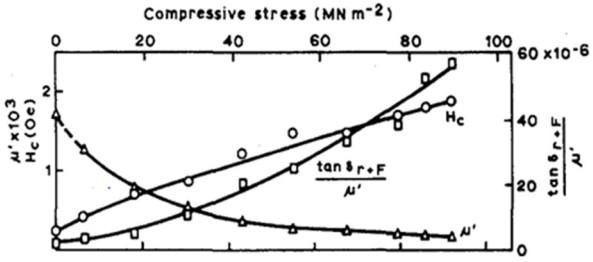


- Analysis by Fraunhofer IZM Shows *Up to Factor 10 High Core Losses (!)* → "Mystery" Losses

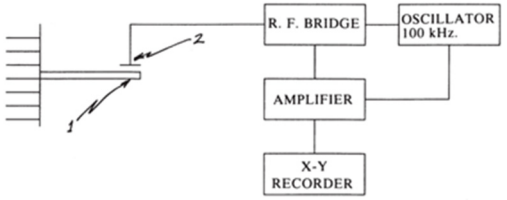
– Machining Increases Core Losses



- 1964 - E. Stern & D. Temme → Machining / Compressive Stress Changes BH-Loop of NiZn Ferrite



- 1974 - J. Knowles, E. Snelling → Compressive Stress Incr. Loss Fact., Reduces μ,



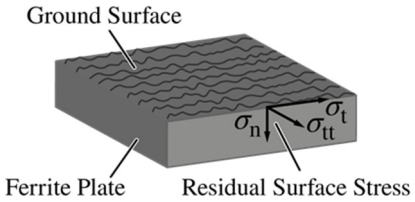
- 1984 - E. Klokholm & H. Wolfe → 40 μm Magn. Dead Surface Layer of MnZn Ferrite

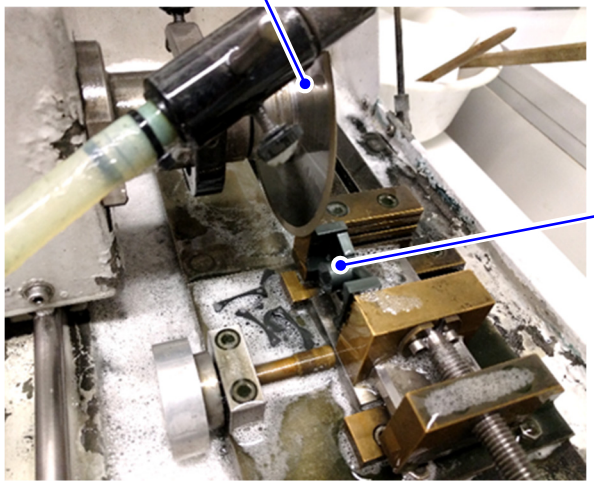
- 1987 - S. Chandrasekar et al. → Lapping Causes Greater Residual Stress than Grinding

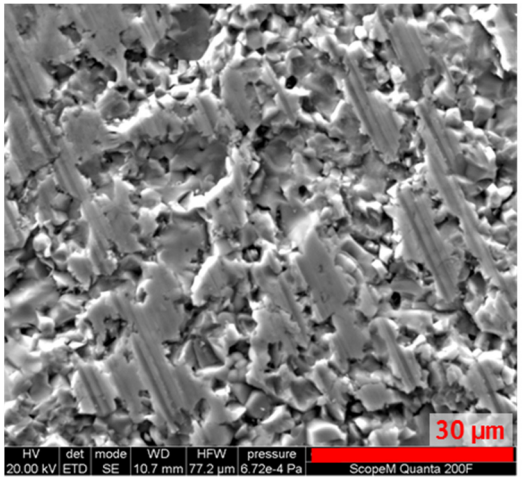
Ferrite Machining Process

laboratory for nanometallurgy

- Cutting of Thin Plates from Ferrite Rod with Diamond Saw
- Abrasive Machining Introduces Mech. Stress into Surface







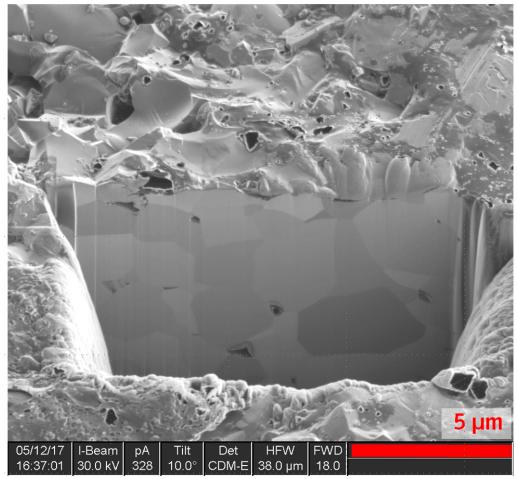
SEM Image of Machined MnZn Ferrite (3F4)

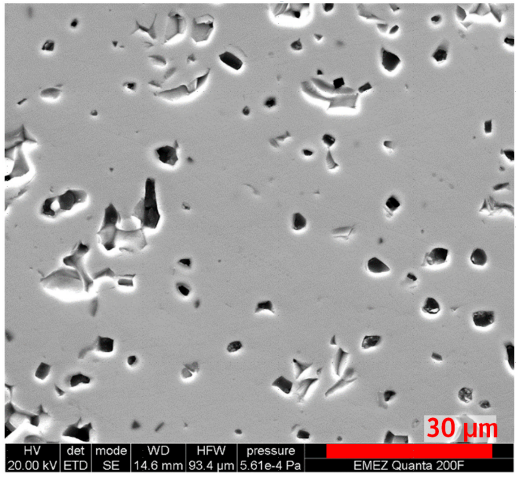
- Ferrite Properties in Surface Altered → Increase of Loss Factor

Subsurface Condition of Machined Ferrite

Empa
Materials Science and Technology

- Focused Ion Beam (FIB) Cut into Ferrite (3F4) Sample & Scanning Electron Microscopy (SEM)
- Polishing of Surface with Grain Sizes 2400 SiC → 4000 SiC → Colloidal Silica SiO_2

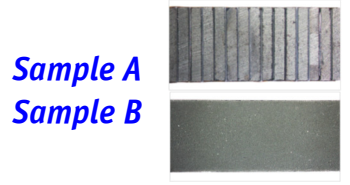


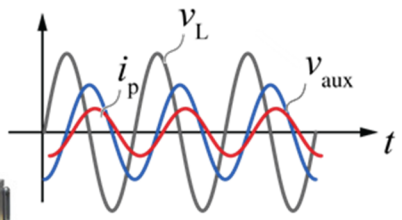


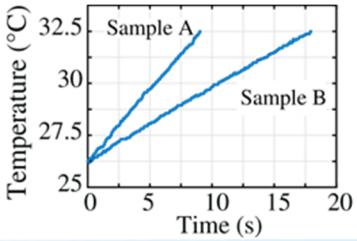
- Polishing Removes 500µm of Surface → Bulk Material Exposed
- Bulk Ferrite also Exhibits Cavities → Result of (Imperfect) Sintering Process

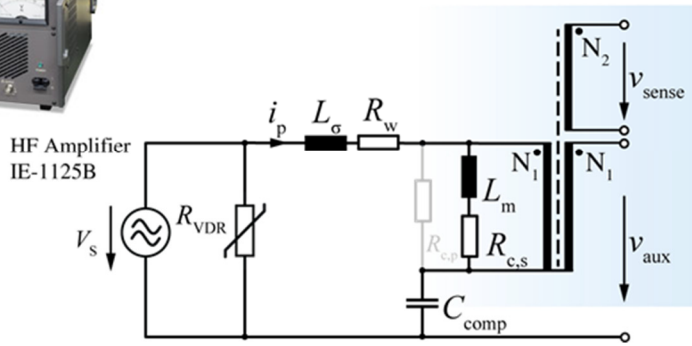
Thermometric Surface Loss Measurement

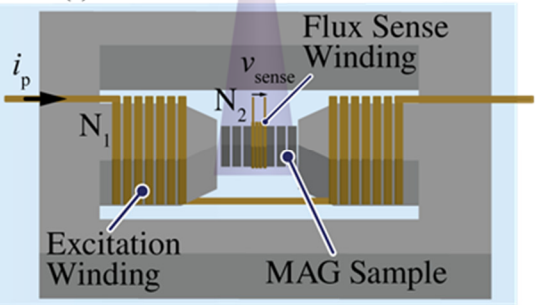
- Impression of Homogeneous Sin. Flux Density of Desired Ampl. / Frequ.
- Cap. Series Comp. for Lowering Impedance @ High Frequencies
- Measurement of *Transient* Temp. Change → Calcul. of Losses







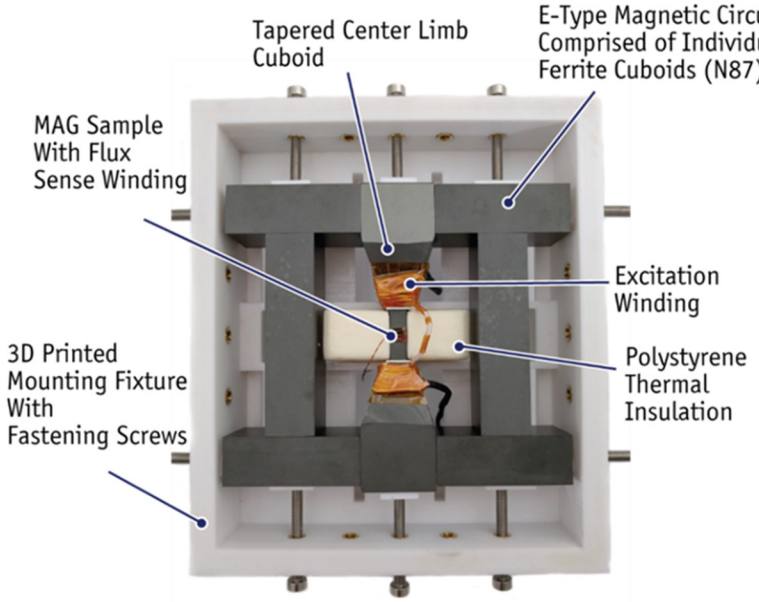


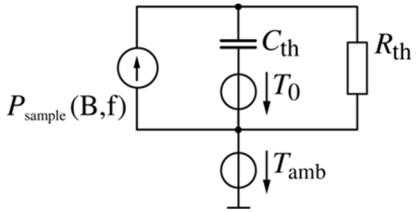


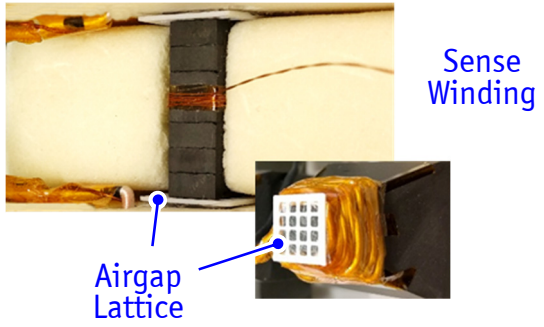
- Temperature Rise of ΔT= 1.5°...5°C Sufficient (Accuracy ±0.2°C), Fast Measurement (!)

Test Fixture / Magnetic Circuit

- E-Type Fixture for Swift Installation of Diff. Samples (7mm x 6.4mm x 21.6mm)
- FEM Optimiz. of Dimensions – Large Core Cross Section / Tapered Outer Limbs



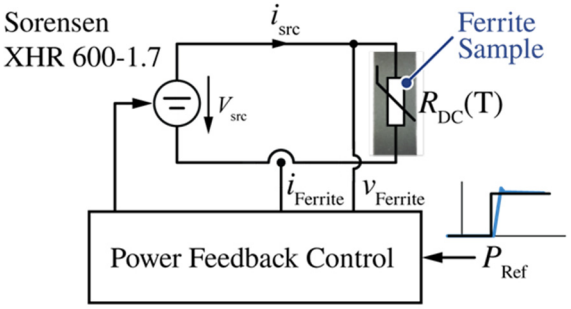


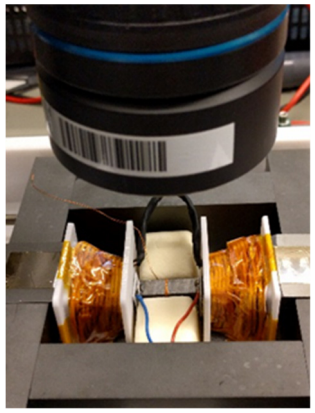


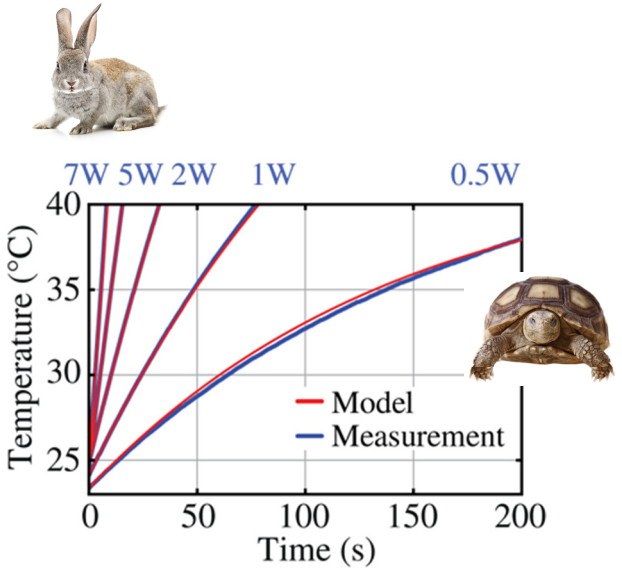
- Therm. Insul. & Airgap Lattice Ensure Low Heat Flux to Ambient
- Measurement of Temp. Increase Over Time Allows to Verify Homog. Flux Density in Sample

Identification of Therm. Parameters R_{th}, C_{th}

- DC Current Impressed in Ferrite, Voltage Control for Const. Power Dissipation as R_{DC}=R_{DC}(Temp.)
- Temperature Response of Sample Recorded (*FLIR A655sc W* with Close-Up Lens)
- Emissivity of Ferrite Determined Using Ferrite on Heating Plate (ε= 0.86)





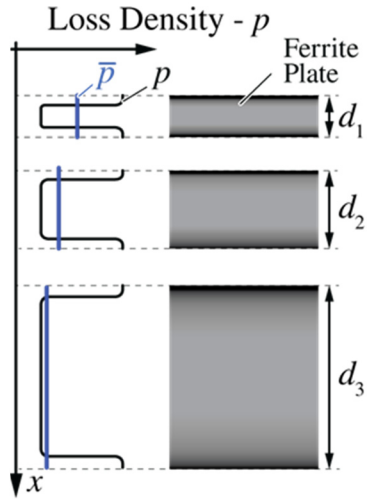


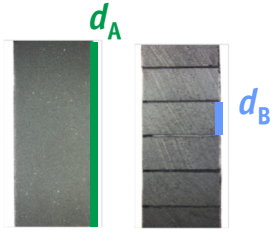
- R_{th} = 37.8 K/W Can be Neglected
- Obtained Parameter C_{th}=3.83J/K Close to C_{th} Calc. Based on Vendor Data (C_{th} = 3.6J/K)

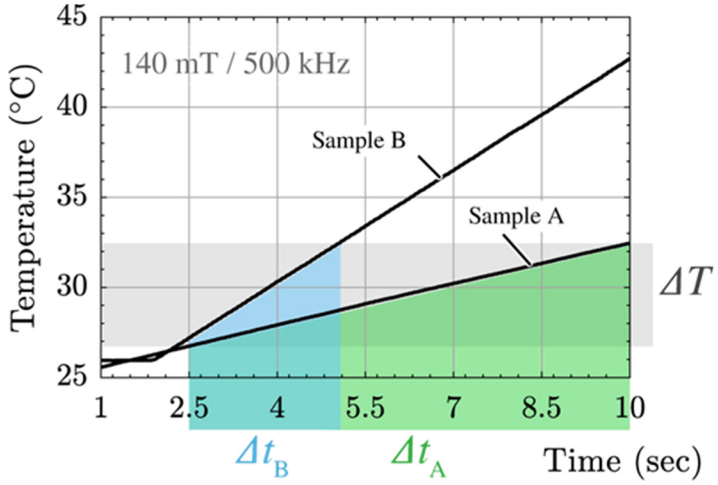
Surface Loss Measurement Principle

FERROXCUBE

- Hypothesis: Core Loss Density in Surface Layer Higher than in Bulk
- Thinner Plates → Higher Average Losses / Faster Temp. Rise
- Stacking of Plates Does NOT Affect Temperature Rise (!)



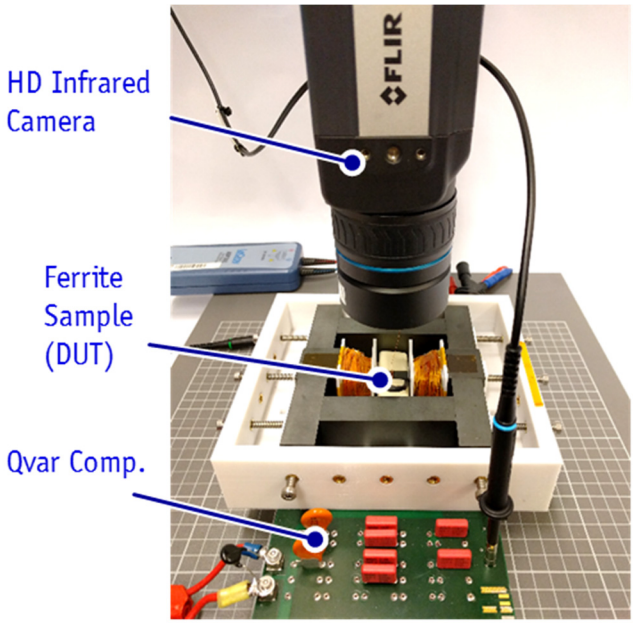




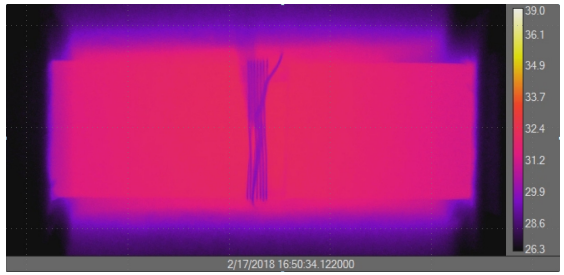
- Surface Loss Density Can be Directly Calc. from Mat. Parameters / Geometry & Δt_A and Δt_B

Temperature Rise Recording

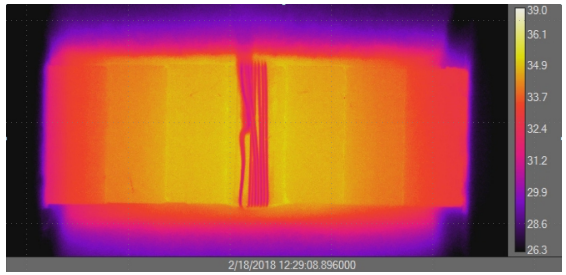
- Comparison of Solid 3F4 Sample (1 x 21.6mm) and Stacked Plates Sample (7 x 3mm)
- Sinusoidal Excitation *100mT / 400kHz*



3F4 Solid Sample / 21.6mm



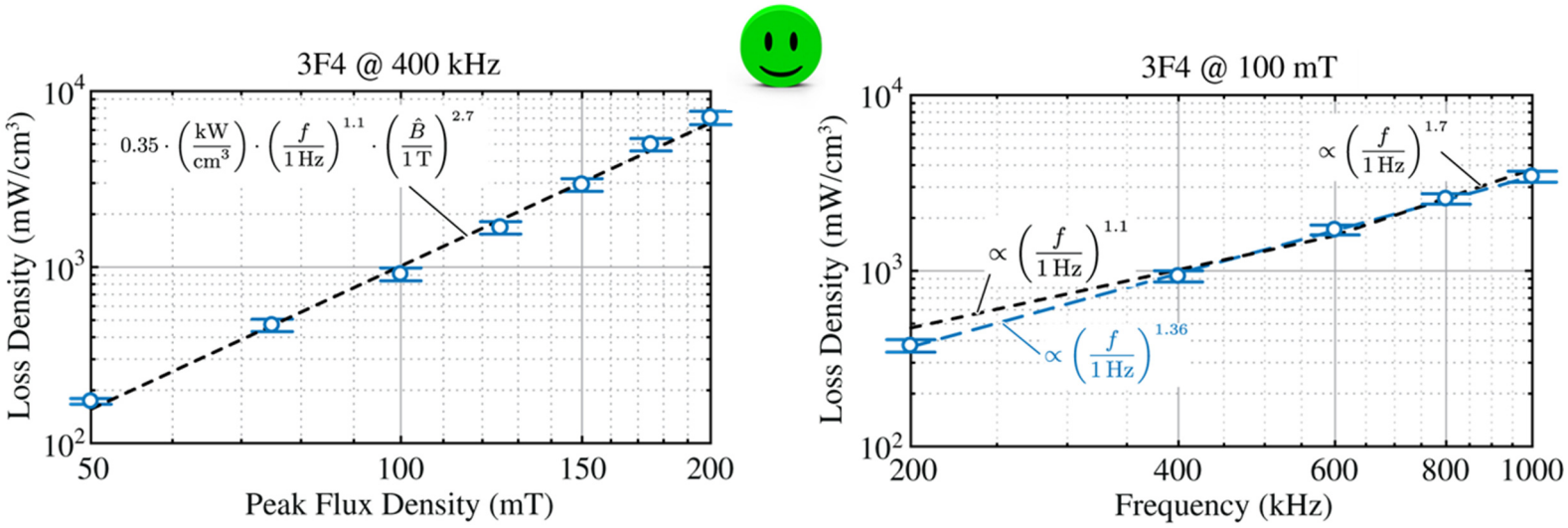
7 Plates 3F4 / 3mm



- Thermal Image shown *25 Seconds After Turn-On* of Magnetic Excitation

Measurement Results – *Bulk Losses*

- Comparison of Measurement Results and Datasheet Values, 3F4 @ 25°C
- Measurement Error Approx. ±10% (Worst Case)

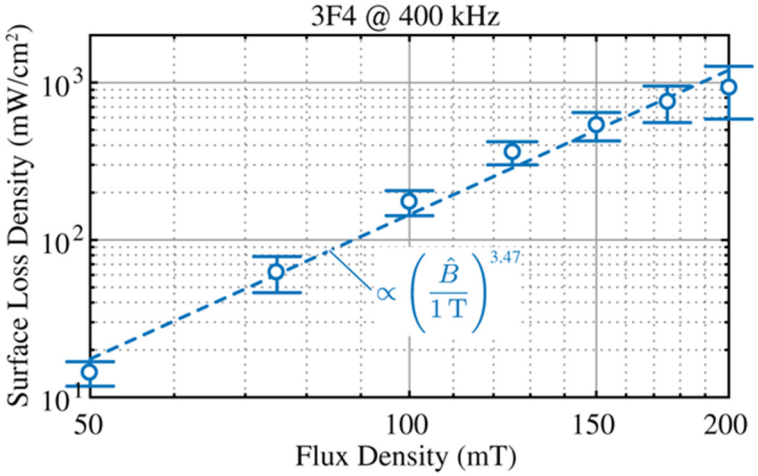


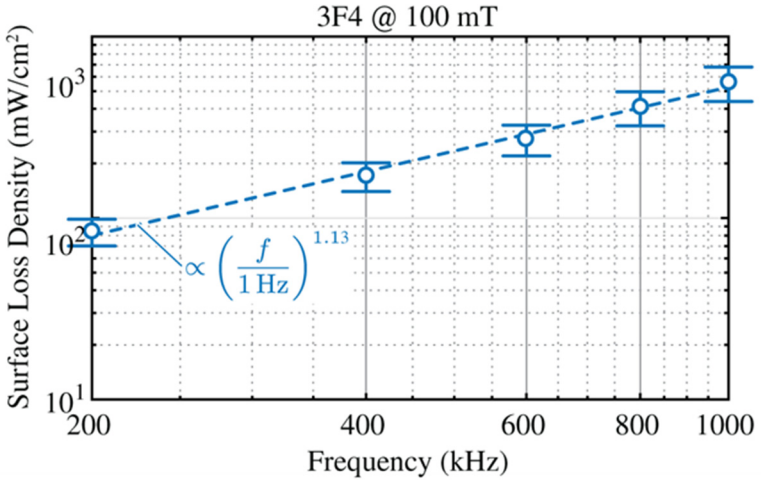
- Good Agreement with *Datasheet Values* / Vendor Steinmetz Parameters

Measurement Results – *Surface* Losses

- Measurement Error Approx. ±25% (Worst Case)
- Error Determined by Meas. Time & Temp. Reading Accuracy

$$p_{Surf} = 0.0615 \times \left(\frac{f}{1\text{Hz}}\right)^{1.13} \times \left(\frac{\hat{B}}{1\text{T}}\right)^{3.47} \left(\frac{\text{mW}}{\text{cm}^2}\right)$$

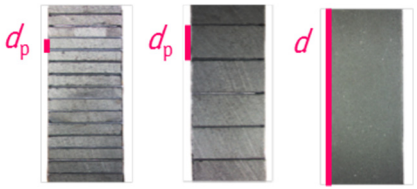




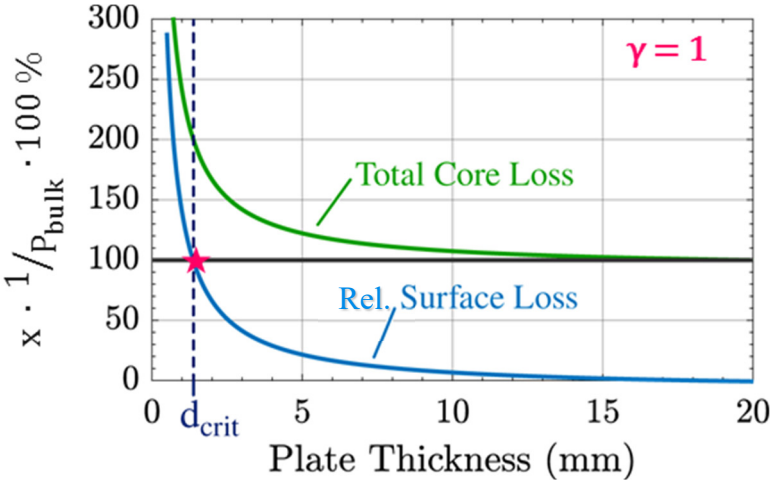
- Comp. of Steinmetz Parameters of Surface Losses & Bulk Losses $\beta_s > \beta$, $\alpha_s < \alpha$

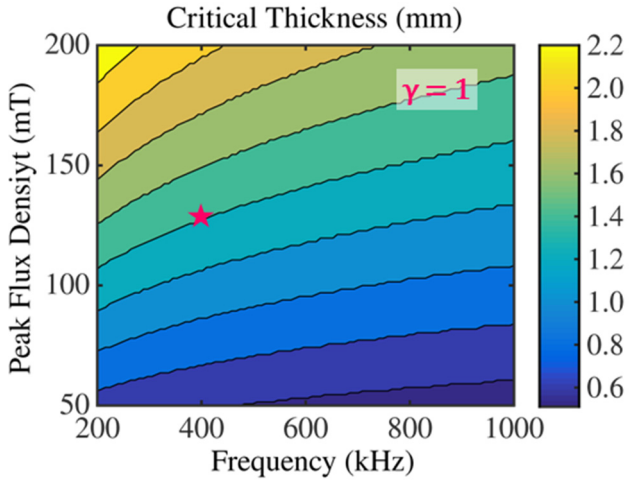
"Critical Thickness" of Ferrite Plates

- "Critical Thickness" Reached for Equal Losses in Bulk & Surface
- Critical Plate Thickness is INDEPENDENT of Cross Section (!)



3F4 Critical Thickness
for 125mT / 400kHz





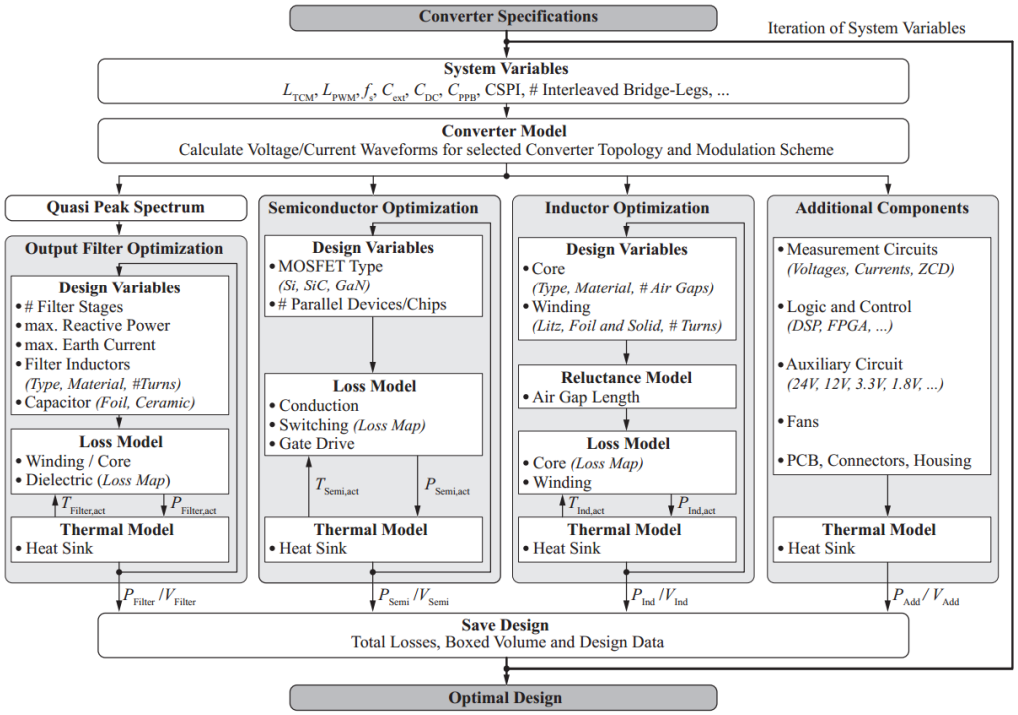
- Dependence on Flux Density Ampl. & Frequency !
- Dependence on Material / Machining Process / Power Processing Treatment

Optimization of Little-Box 1.0

ηρ-Pareto Front
TCM vs. Large Ripple PMW
The Ideal Switch is Not Enough (!)
Design Space Diversity

Multi-Objective Optimization

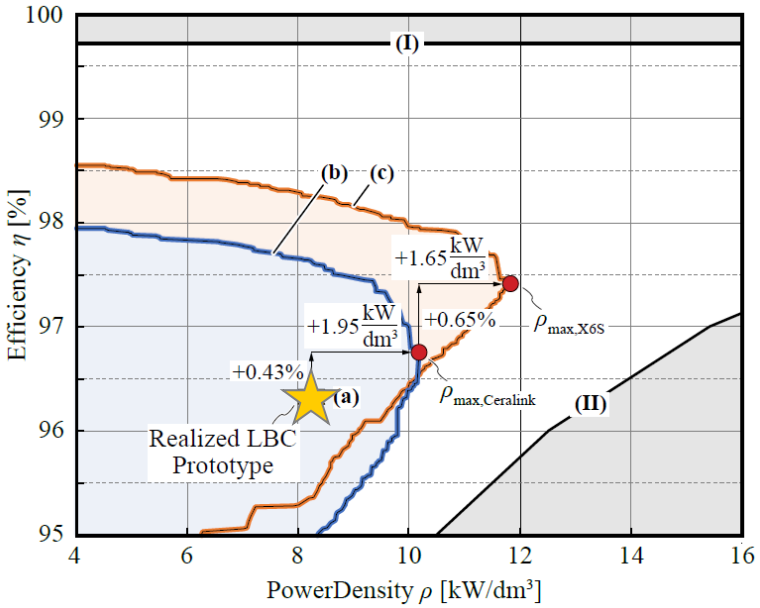
- Detailed *System* Models → Power Buffer/Output Stage/EMI Filter
- Multi-Domain *Component* Models → Passives & GaN & SiC Semicond.
- Consideration of Very Large # of Degrees of Freedom



- Pareto Optimization Shows Trade-Off Between Power Density and Efficiency

Little Box 1.0 ηρ-Performance Limits

- Multi-Objective Optimization of Little-Box 1.0 (incl. CeraLink™ → X6S)
- Absolute Performance Limits (I) - DSP/FPGA Power Consumption
  (II) - Heatsink Volume @ (1-η)



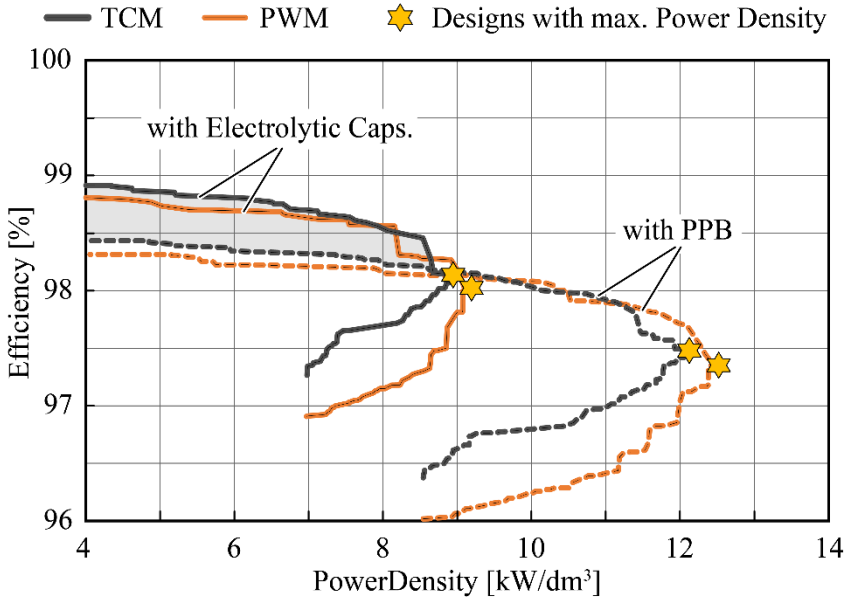
(a) ★ Realized Prototype

(b) CeraLink™ Power Pulsation Buffer
(c) X6S Power Pulsation Buffer

- Further Performance Improvement for Triangular Current Mode (TCM) → PWM

Little Box 1.0 -- Electrolytic Cap. / *Active* PPB

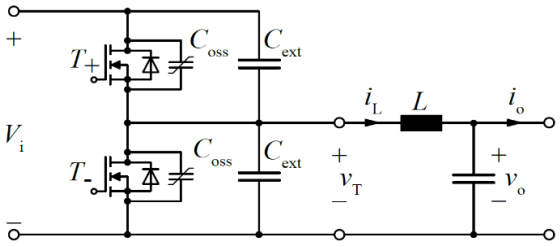
- Analysis for Google Little Box Challenge Specification $\Delta V/V < 3\%$
- Efficiency Benefit of PPB only for $\rho > 9\text{kW/dm}^3$



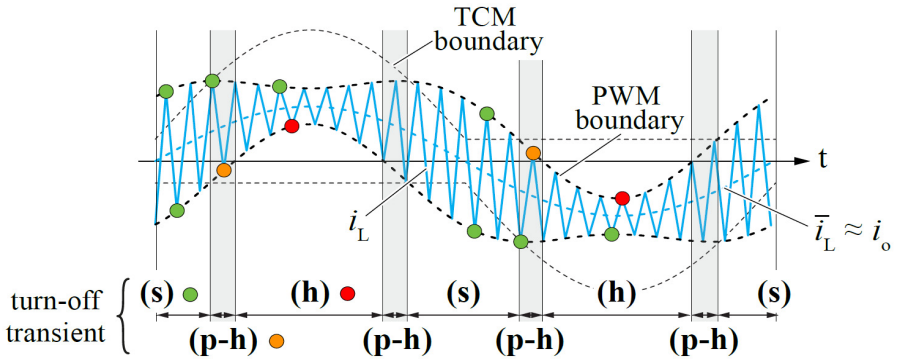
- Electrol. Cap. Favorable for High Efficiency @ Moderate Power Density ($\Delta\eta$= +0.5%)
- Electrol. Cap. Show Lower Vol. & Lower Losses if Large $\Delta V/V$ is Acceptable (e.g. for PFC Rectifiers)

Little Box 1.0 -- TCM → PWM

- Very High Sw. Frequency f_S of TCM Around Current Zero Crossings
- Efficiency Reduction due to Residual TCM Sw. Losses & Gate Drive Losses Reduction
- Wide f_S -Variation Represents Adv. & Disadvantage for EMI Filter Design



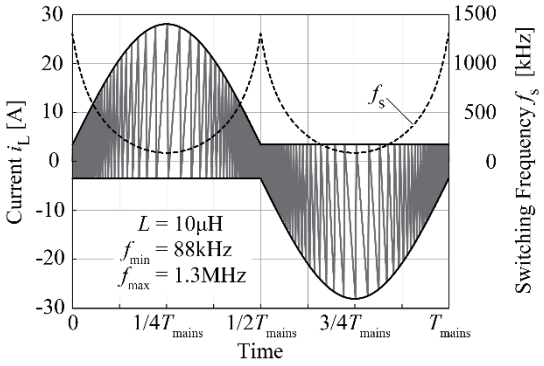
(s) Soft-Switching (ZVS)
(p-h) Partial Hard Switching
(h) Hard-Switching

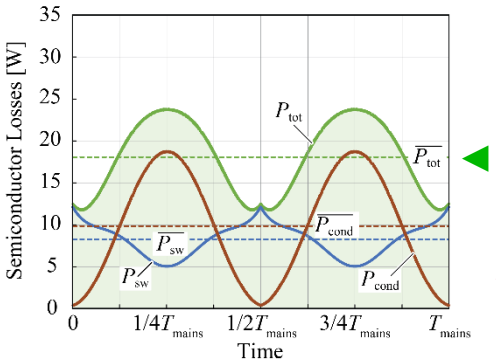


- PWM -- Const. Sw. Frequency & Lower Conduction Losses
- PWM @ Large Current Rippel -- ZVS in Wide Intervals

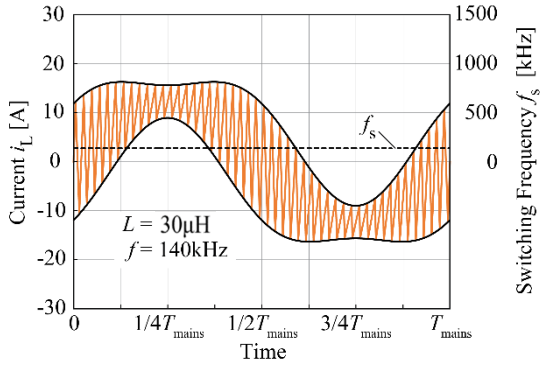
Little Box 1.0 -- TCM → PWM

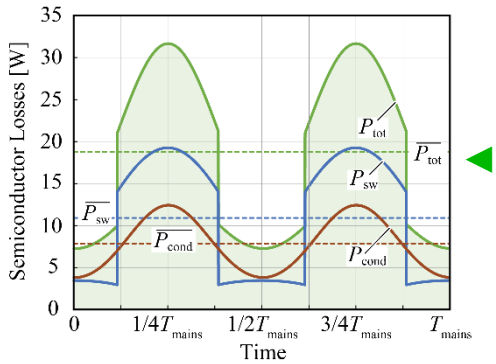
- Optimization for GaN GIT & No Interleaving
- Resulting Opt. Inductance of Output Inductor L=10µH (TCM), L=30µH (PWM@140 kHz)





ρ= 11.9kW/dm³
η= 97.4%





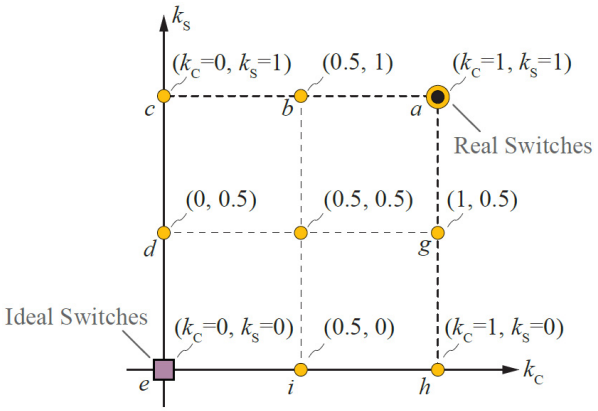
ρ= 12.5kW/dm³
η= 97.4%

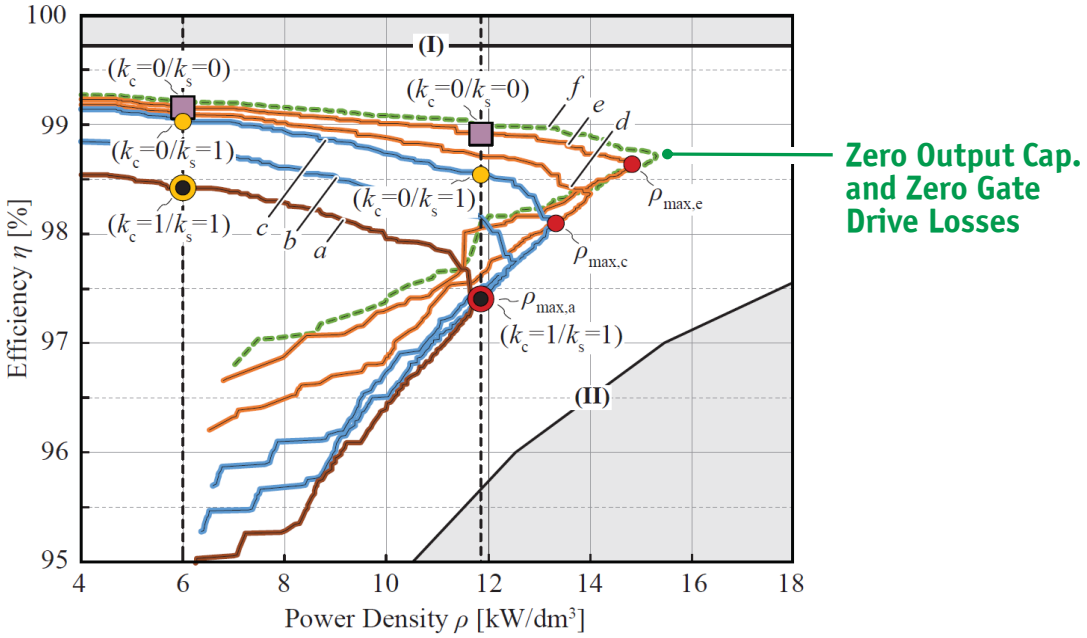
- PWM vs. TCM → Slightly Higher Max. Power Density @ Same Efficiency

The Ideal Switch is Not Enough (!) 

Little Box 1.0 @ Ideal Switches -- TCM

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_C = 0$ (Zero Cond. Losses); $k_S = 0$ (Zero Sw. Losses)

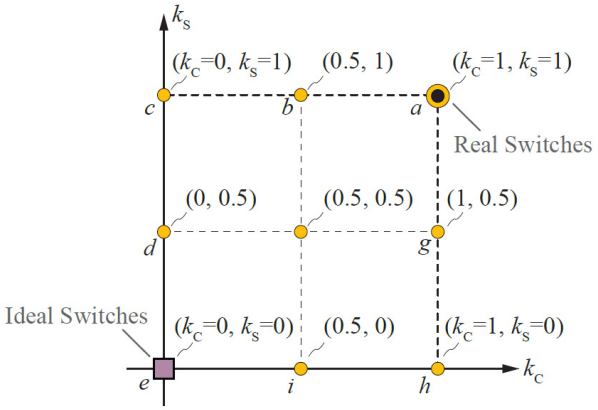


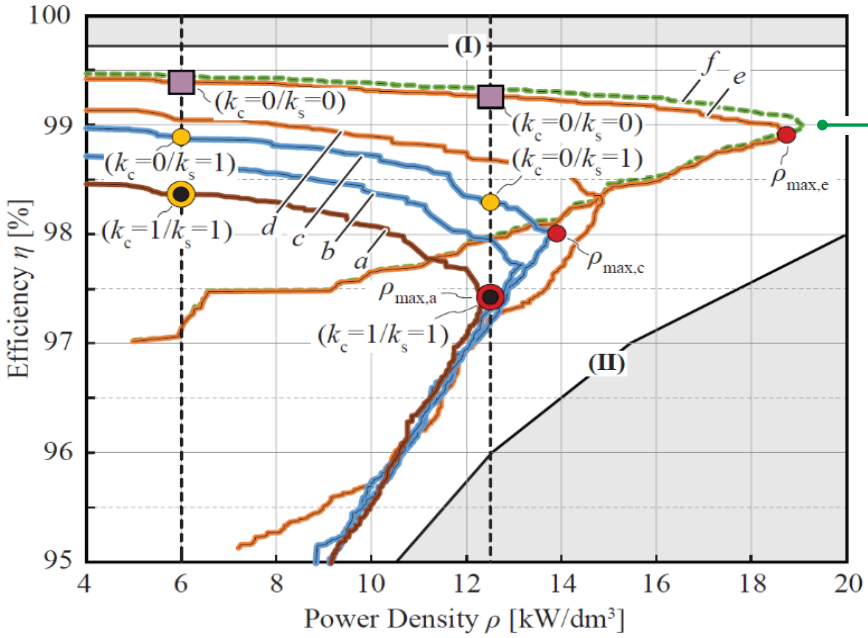


- Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density

Little Box 1.0 @ Ideal Switches -- PWM

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_C = 0$ (Zero Cond. Losses); $k_S = 0$ (Zero Sw. Losses)

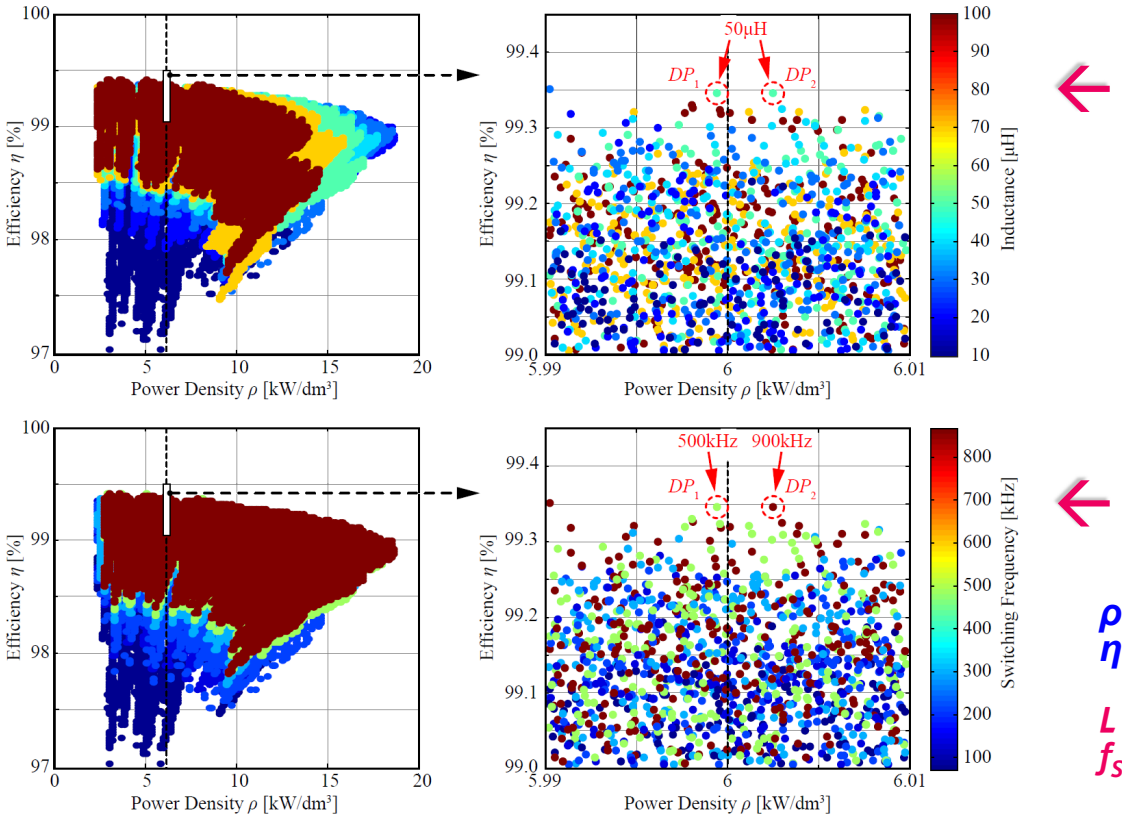




Zero Output Cap. and Zero Gate Drive Losses

- Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density

Little Box 1.0 @ Ideal Switches -- PWM

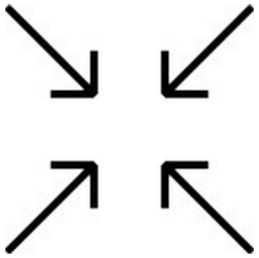


ρ = 6kW/dm³
$\eta \approx$ 99.35%

L = 50uH
f_S = 500kHz or 900kHz

- L & f_S are Independent Variables (Dependent for TCM)
- Large Design Space Diversity (Mutual Compensation of HF and LF Loss Contributions)

Little Box 2.0

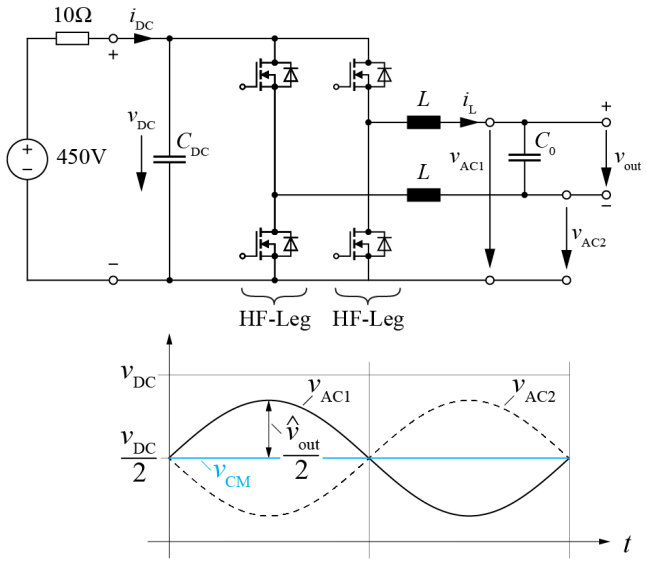


250 W/in^3

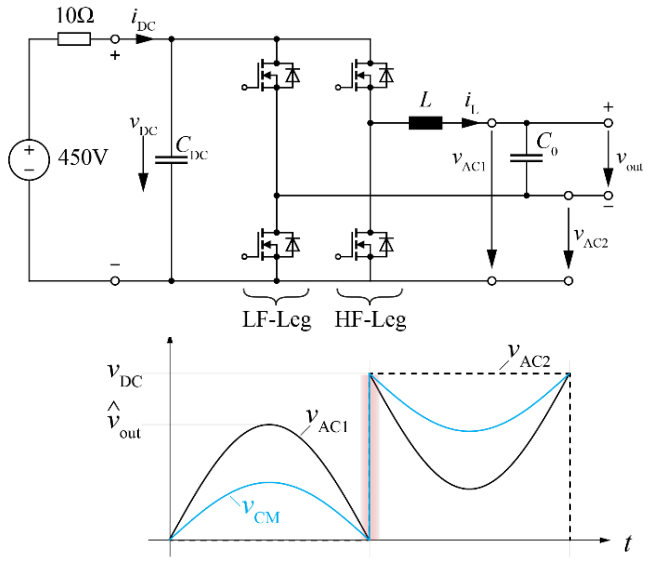
DC/ | AC | Converter + Unfolder
PWM vs. TCM incl. Interleaving
ηρ-Pareto Limits for Non-Ideal Switches
3D-CAD Construction
Exp. Results

Little Box 2.0 -- New Converter Topology (1)

- Alternative Converter Topology → Only Single High Frequ. Bridge Leg + 60Hz-Unfolder
- HF Half-Bridge & Half-Bridge Unfolder DC/|AC| OR Buck Converter + Full-Bridge Unfolder



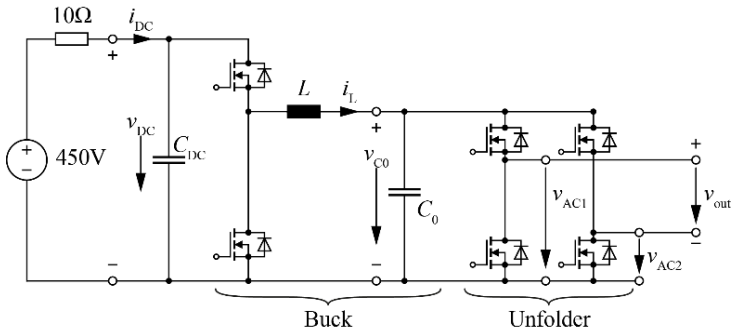
- v_{AC1}, v_{AC2} More Diff. to Gen. but Add. DOF
- Higher Sw. Losses & Gate Drive Losses
- Zero Low-Frequ. CM-Noise (DC Comp. Only)
- C_{CM} Not Limited by Allowed Gnd Current

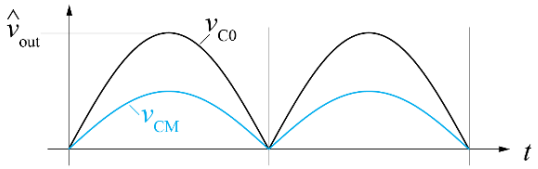


- v_{AC1} More Difficult to Generate/Control
- Lower Sw. Losses & Gate Drive Losses
- Higher CM-Noise (DC and n x 120Hz-Comp.)
- C_{CM}=150nF Allowed for 50mA Gnd Current

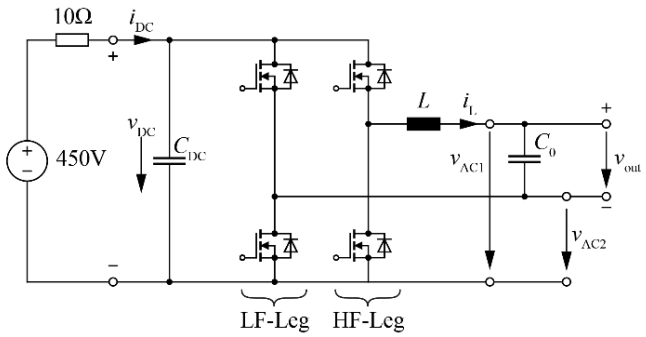
Little Box 2.0 -- New Converter Topology (2)

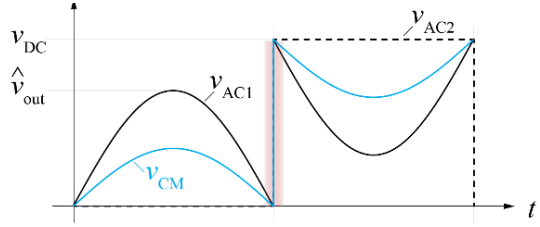
- Alternative Converter Topology → Only Single High Frequ. Bridge Leg + 60Hz-Unfolder
- HF Half-Bridge & Half-Bridge Unfolder DC/|AC| OR Buck Converter + Full-Bridge Unfolder





- v_{C0} Easy to Generate/Control
- Higher Cond. Losses Due to FB-Unfolder
- Lower CM-Noise (DC & n x 120Hz-Comp.)
- C_{CM}=700nF Allowed for 50mA Gnd Current

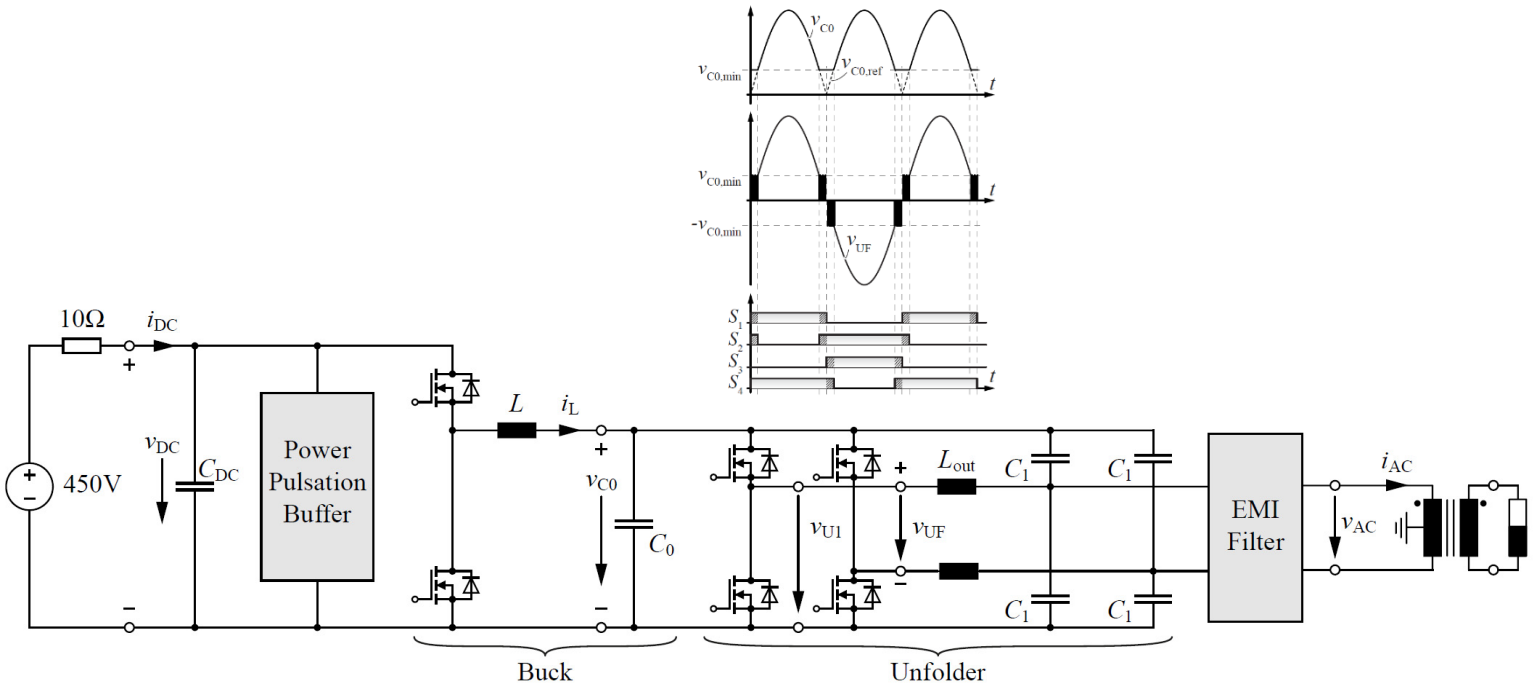




- v_{AC1} More Difficult to Generate/Control
- Lower Sw. Losses & Gate Drive Losses
- Higher CM-Noise (DC and n x 120Hz-Comp.)
- C_{CM}=150nF Allowed for 50mA Gnd Current

Little Box 2.0 -- New Converter Topology (3)

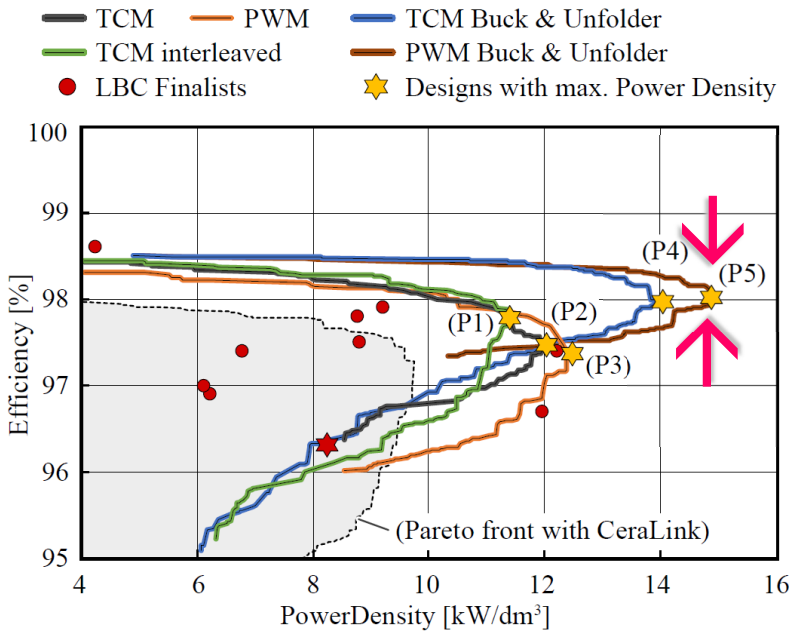
- Alternative Converter Topology - DC/ | AC | - Buck Converter + Unfolder
- 60Hz-Unfolder (Temporary PWM for Ensuring Cont. Current Control)
- TCM or PWM of DC/ | AC | - Buck-Converter



- Full Optimization of All Converter Options for Real Switches / X6S Power Pulsation Buffer

Little Box 2.0 -- Multi-Objective Optimization

- DC/ | AC | - Buck Converter (Single *PWM* Bridge Leg) + Unfolder Shows Best Performance
- Full-Bridge Would Employ 2 Switching Bridge Legs - Larger Volume & Losses
- Interleaving Not Advantageous – Lower Heatsink Vol. / Larger Vol. of Switches and Inductors

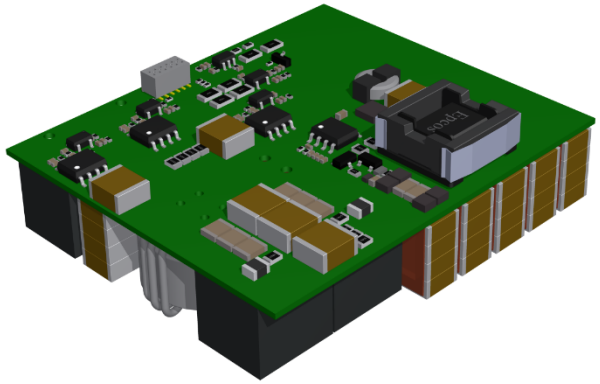


- ρ= 250W/in³ (15kW/dm³) @ η= 98% Efficiency Achievable for Full Optimization

3D-CAD Construction of the Final System →

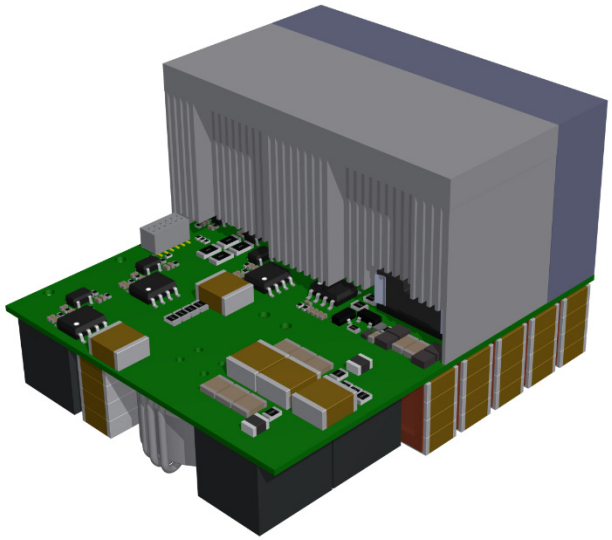
250 W/in³

Little Box 2.0 -- Mechanical Construction (1)



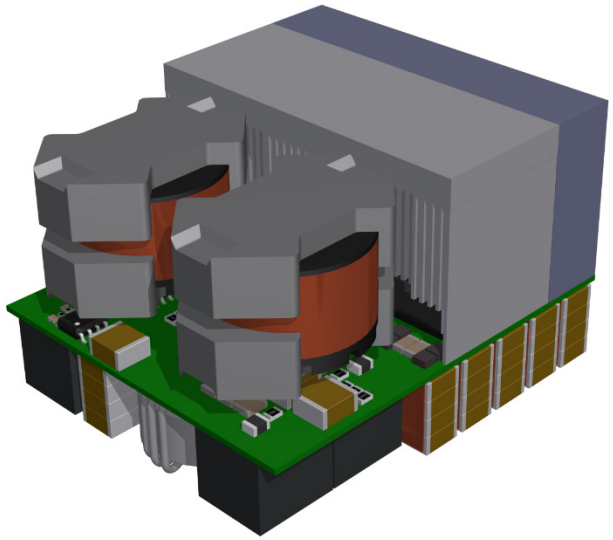
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 -- Mechanical Construction (2)



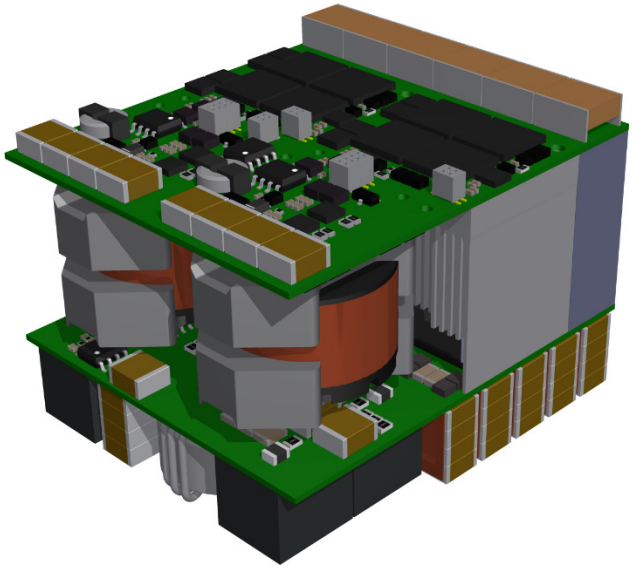
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 -- Mechanical Construction (3)



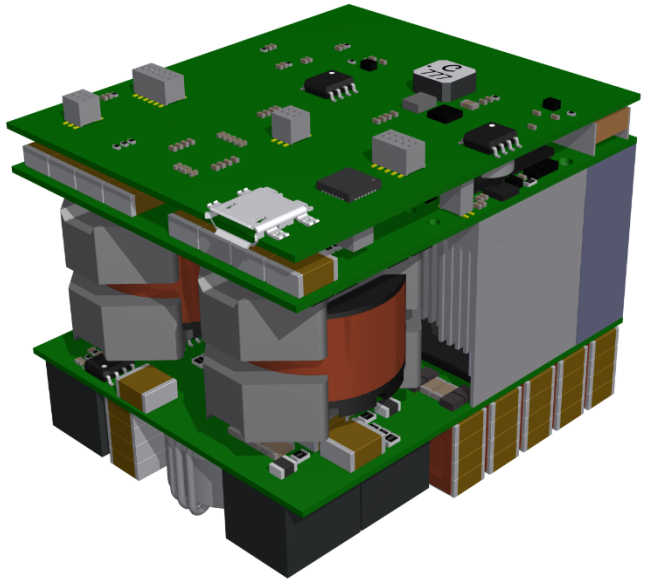
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 -- Mechanical Construction (4)



- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

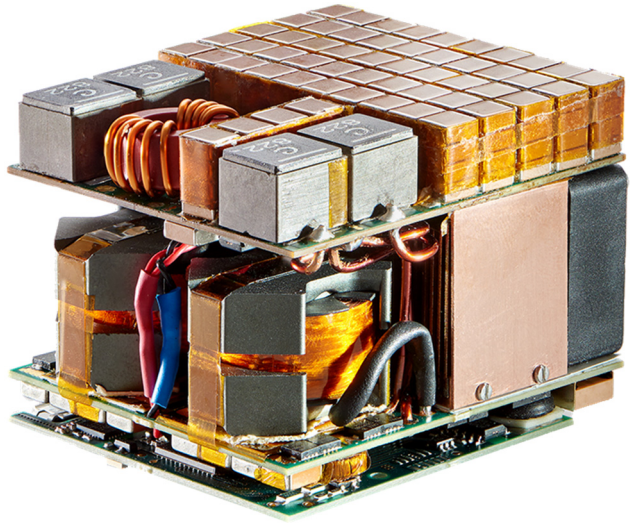
Little Box 2.0 -- Mechanical Construction (5)



- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 -- Demonstrator

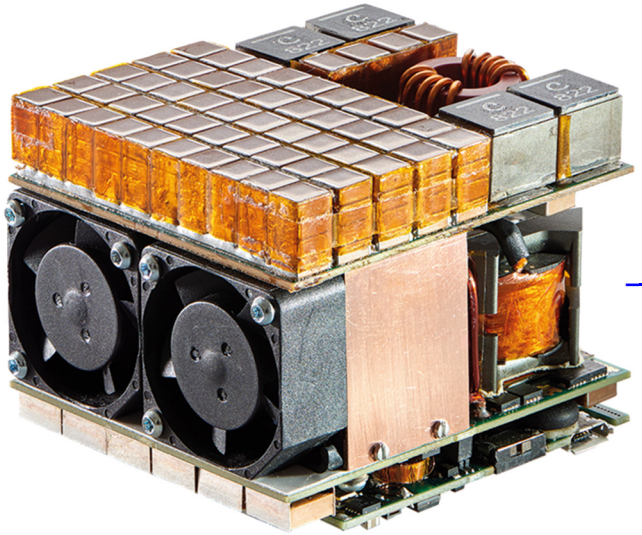
★ 240 W/in³



- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2in³) → 14.8 kW/dm³ (243 W/in³)

Little Box 2.0 -- Demonstrator

★ 240 W/in³

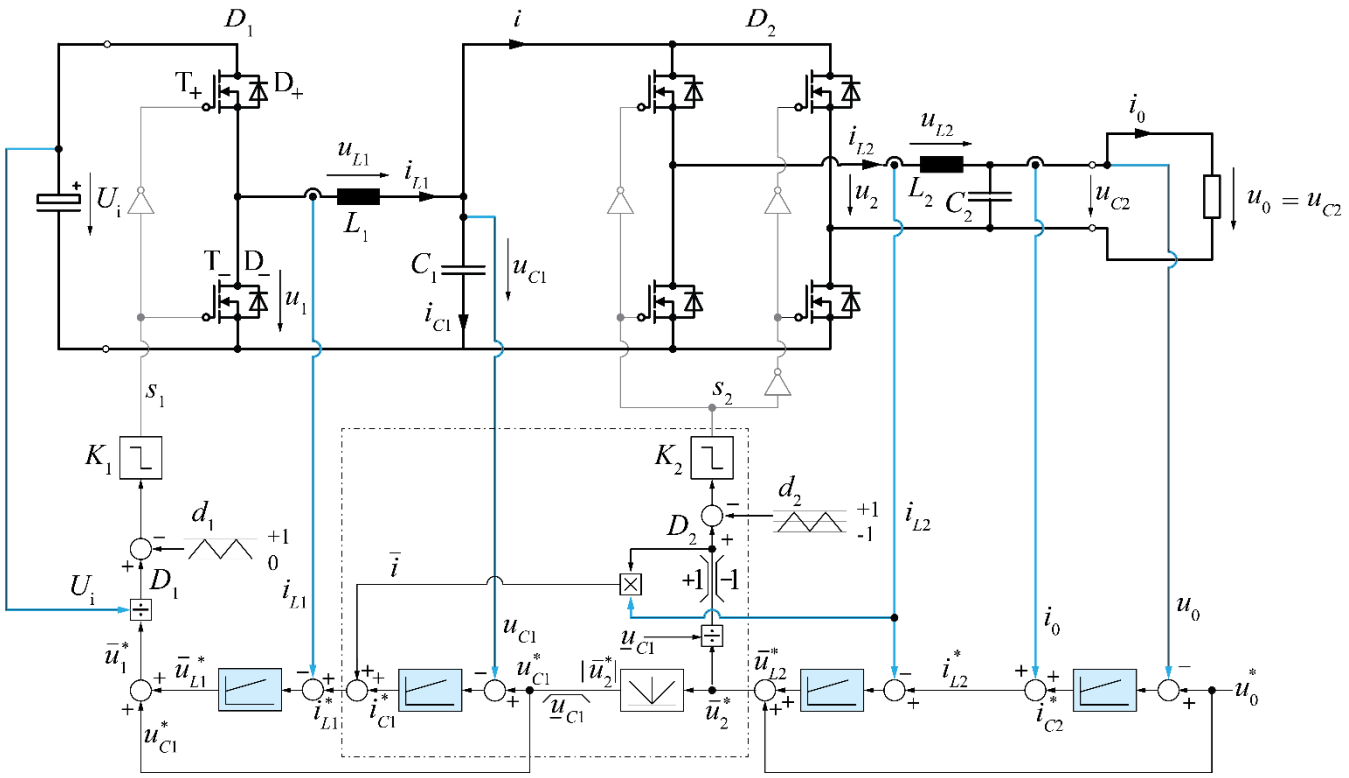


- 60 mm x 50 mm x 45 mm = 135 cm³ (8.2in³) → 14.8 kW/dm³ (243 W/in³)

Experimental Results

Control Block Diagram
Output Voltage / Input Current Quality
Efficiency

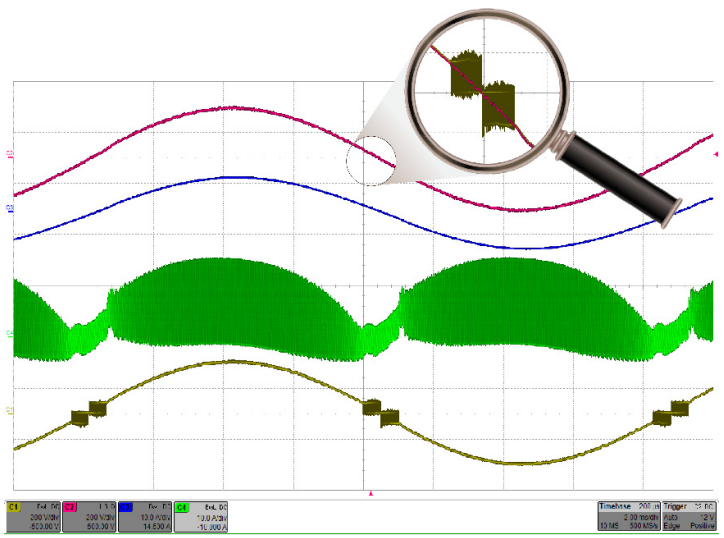
Little Box 2.0 – Control Structure

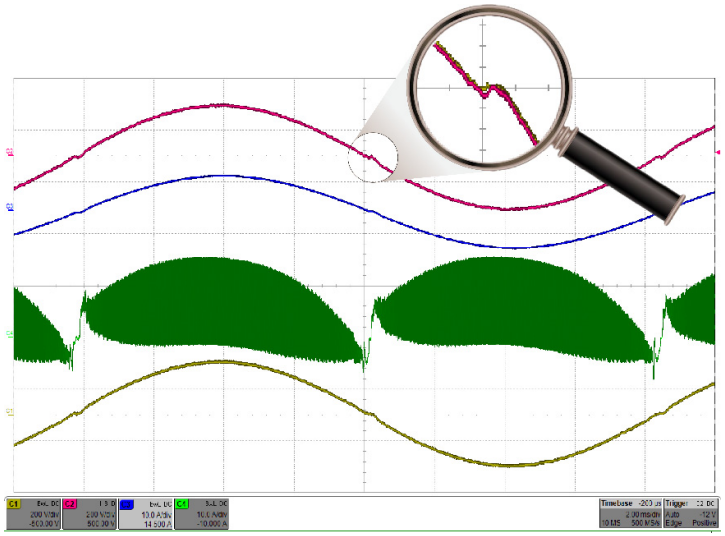


- Each Stage (Buck & Unfolder) Controlled with Cascaded Current and Voltage Loop
- Without Switching of Unfolder Control Like for Conventional Boost PFC Rectifier

Little Box 2.0 – Experimental Results (1)

- Voltage Zero Crossing Behavior - With (Right) & Without (Left) Switching of Unfolder



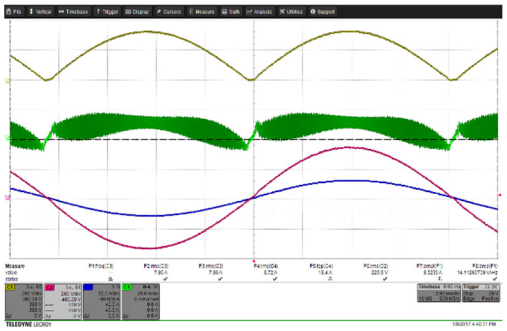


Output Voltage (200 V/div)
Output Current (10 A/div)
Buck Inductor Current (10 A/div)
Unfolder Output Voltage (200 V/div)

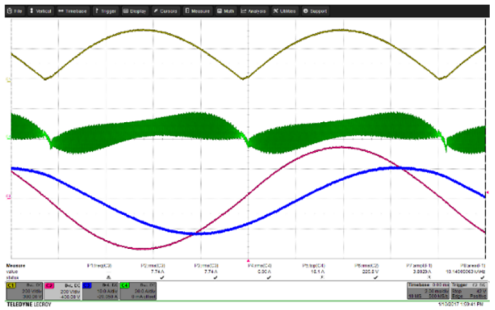
- Output Voltage & Current Fully Controlled Around Voltage Zero Crossings
- Slope of Buck Conv. Outp. Curr. can be Decreased – Adv. for React. Loads (No Step-Change of DC Curr.)

Little Box 2.0 – Experimental Results (2)

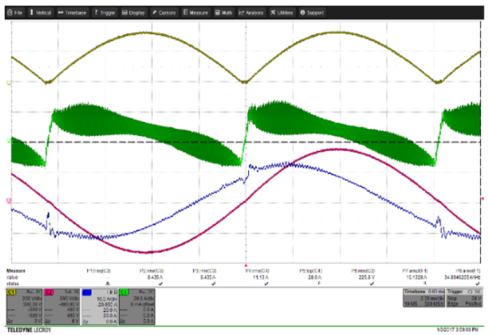
- DC/|AC| Buck-Stage Output Voltage & Inductor Current



■ Resistive Load



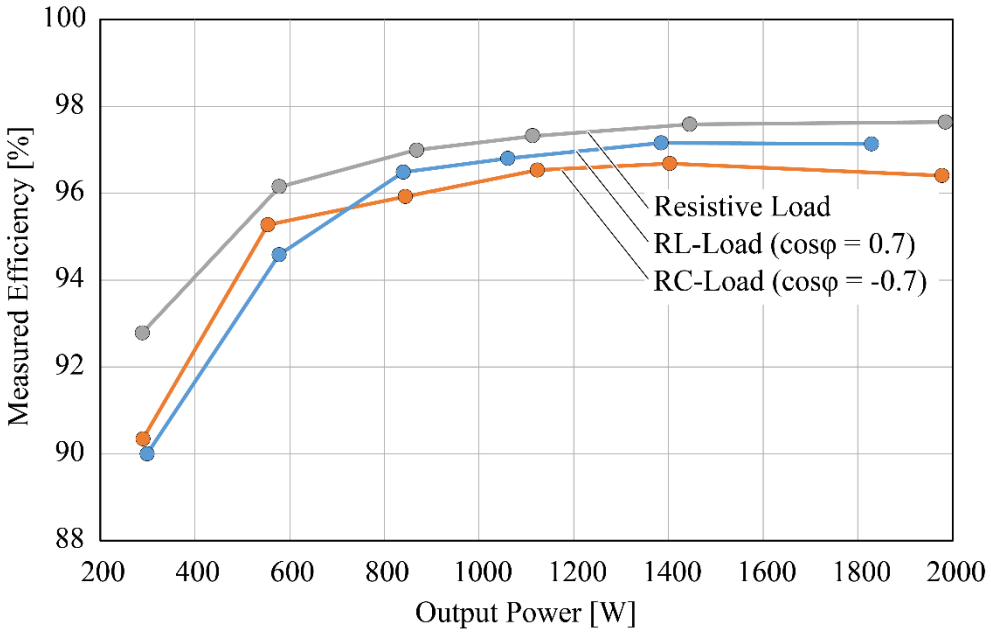
■ Inductive Load



■ Capacitive Load

Little Box 2.0 – Experimental Results (3)

- Performance of First DC/|AC|- Buck Converter + Unfolder Prototype
- PWM Operation
- Without Power Pulsation Buffer

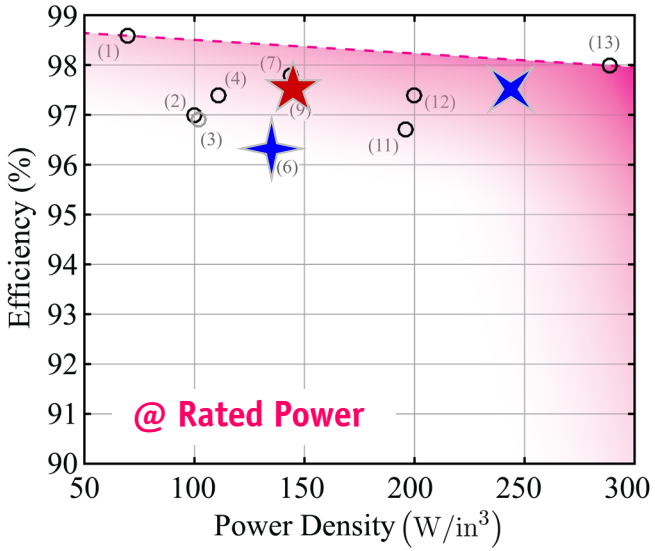


- 98% for Res. Load Achievable if Cond. Losses of PCB (Copper Cross Sect.) & Unfolder ($R_{ds,on}$) are Red.

Litte Box 2.0 – Performance Comparison

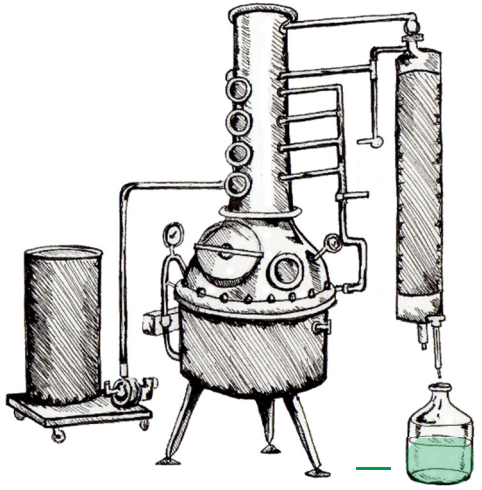
- 18 Finalists (3 No-Shows)
- 7 Groups of Consultants / 7 Companies / 4 Universities

Note: Numbering of Teams is Arbitrary



(1) Virginia Tech
(2) Schneider Electric
(3) EPRI (Univ. of Tennessee)
(4) Venderbosch
(5) Energy Layer
(6) ETH Zurich
(7) Rompower
(8) Tommasi-Bailly
(9) Red Electric Devils
(10) AHED
(11) FH IISB
(12) Univ. of Illinois
(13) AMR

- 70 ... 300 W/in³
- 35 kHz ... 500kHz ... 1 MHz (up to 1MHz: 3 Teams)
- Full-Bridge or DC/|AC|Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- GaN (11 Teams) / SiC (2 Teams) / Si (2 Teams)



Source: whiskeybehavior.info

Overall Summary

Performance Limits / Future Requirements

- 220...250W/in^3 for Two-Level Bridge Leg + Unfolder
- 250...300W/in^3 for Highly Integrated Multi-Level Approach
- Isol. Distance Requirements Difficult to Fulfill
- Fulfilling Industrial Inp. Overvoltage Requirem. would Signific. Reduce Power Density

- Low Frequency (20kHz...120kHz) SiC vs. HF (200kHz...1.2MHz) GaN
- Multi-Cell Concepts for LV Si (or GaN) vs. Two-Level SiC (or GaN)

- New Integr. Control Circuits and i=0 Detection for Sw. Frequency >1MHz
- Integrated Gate Drivers & Switching Cells
- High Frequency Low Loss Magnetic Materials
- High Bandwidth Low-Volume Current Sensors
- Low Loss Ceramic Capacitors Tolerating Large AC Ripple
- Passives w. Integr. Heat Management and Sensors
- 3D Packaging

- New U-I-Probes Required for Ultra-Compact Conv. R&D
- Specific Systems for Testing → Devices Equipped with Integr. Measurement Functions
- Convergence of Sim. & Measurem. Tools → Next Gen. Oscilloscope
- New Multi-Obj. Multi-Domain Simulation/Optim. Tools

Thank You!

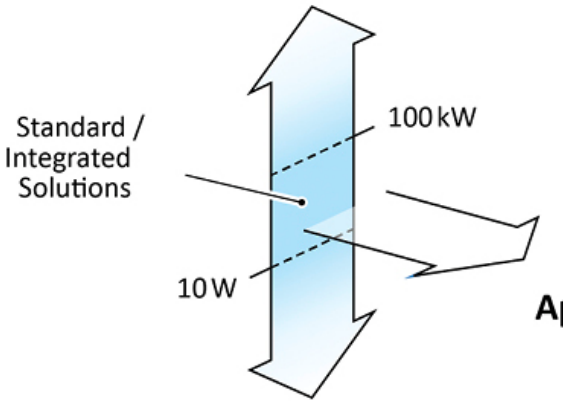
Questions


BACKUP

Future Development 1/2

- Commoditization / Standardization
- Extreme Cost Pressure (!)

"There is Plenty of Room at the Top" → Medium Voltage/Frequency Solid-State Transformers



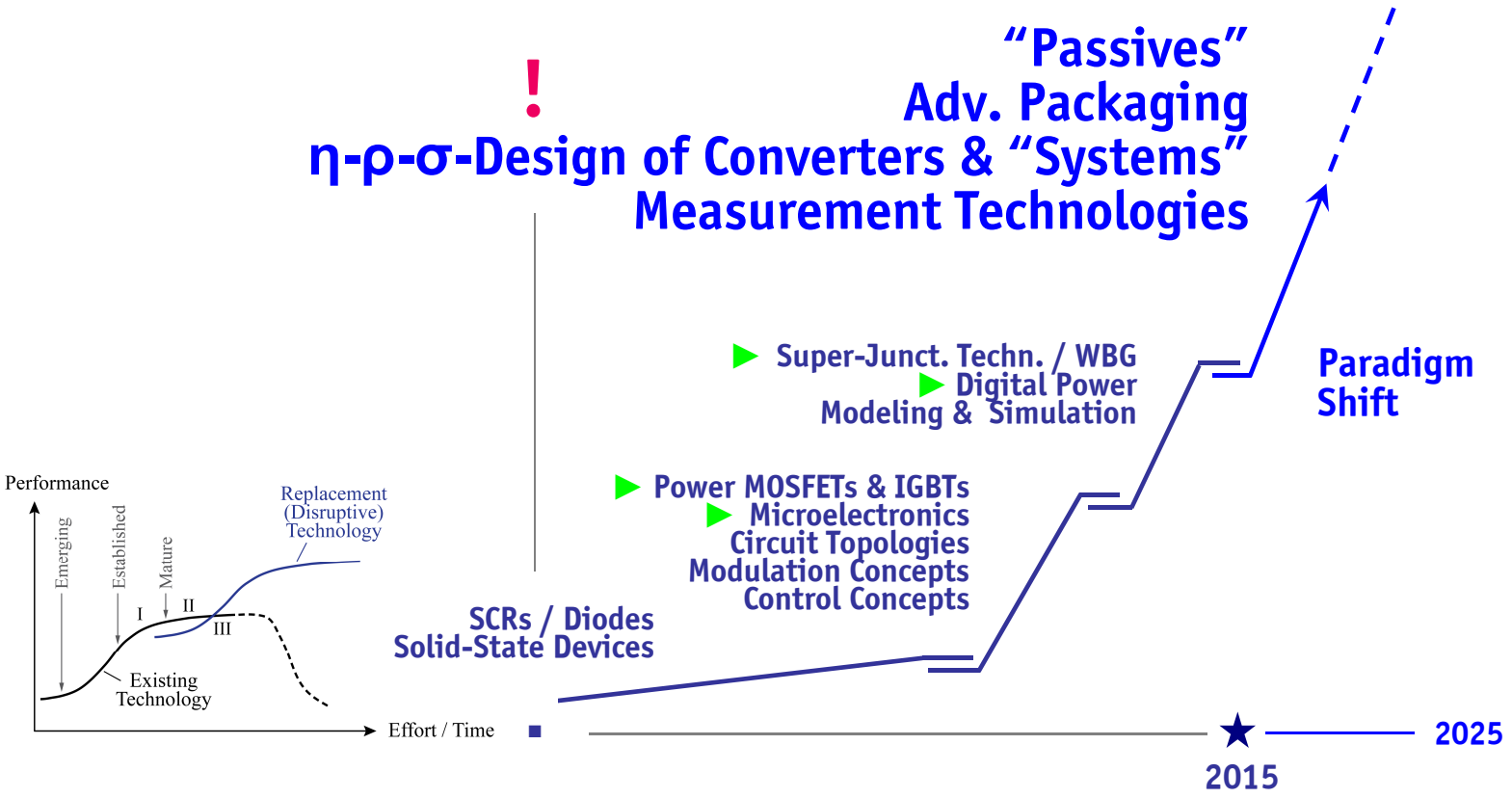
System Applications

Power-Supplies on Chip ← "There is Plenty of Room at the Bottom"

► Key Importance of Technology Partnerships of Academia & Industry

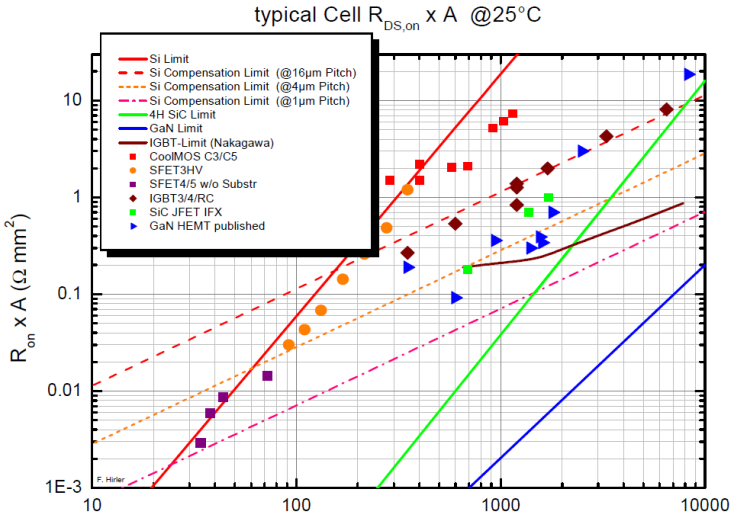
Future Development 2/2

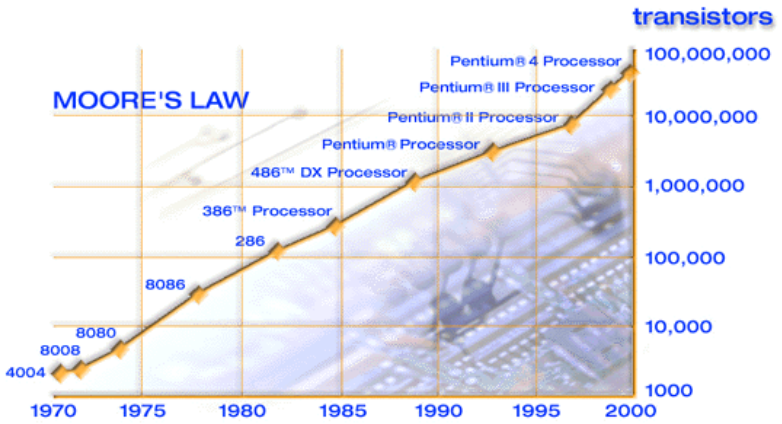
- Extrapolation of Technology S-Curve



Technology Progress – *Technology Push*

- **WBG Semiconductor Technology** → **Higher Efficiency, Lower Complexity**
- **Microelectronics** → **More Computing Power**



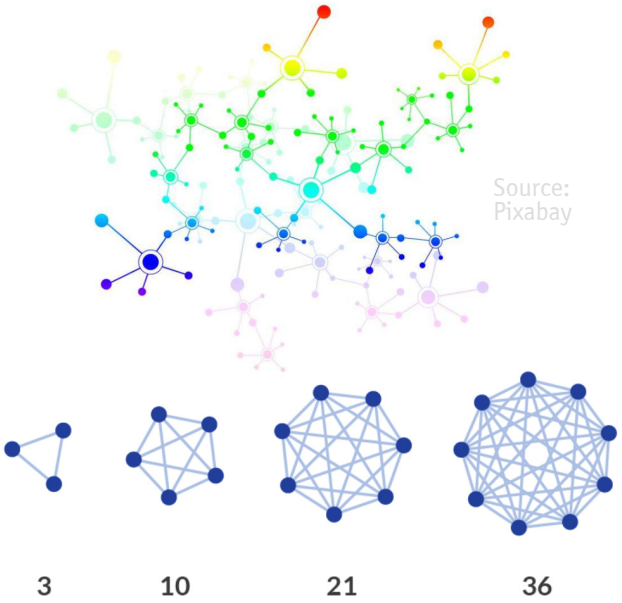


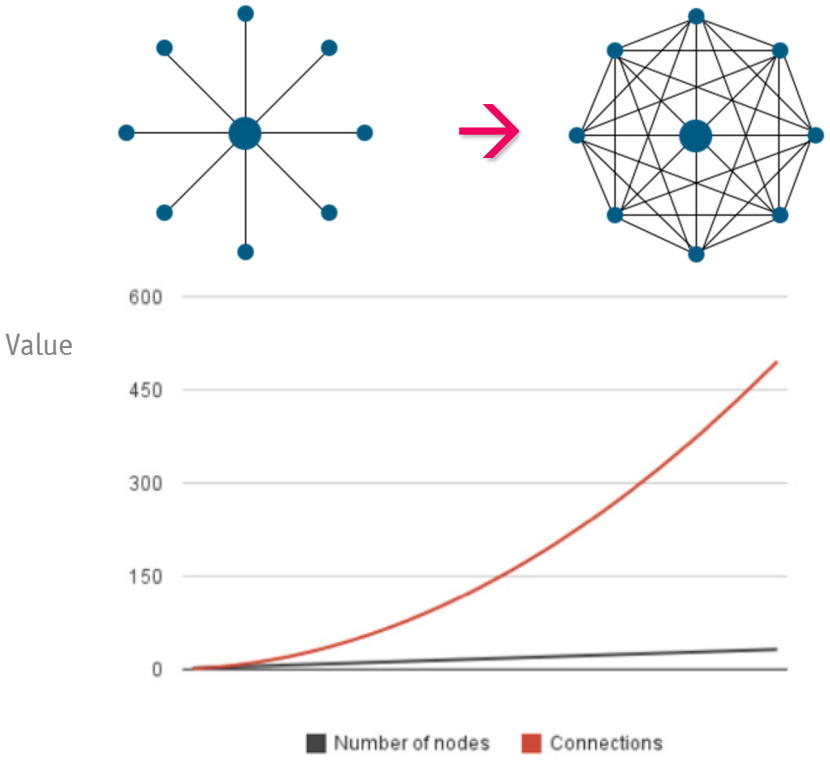
→ + Advanced Packaging (!)

→ Moore's Law

System / Smart Grid Drivers

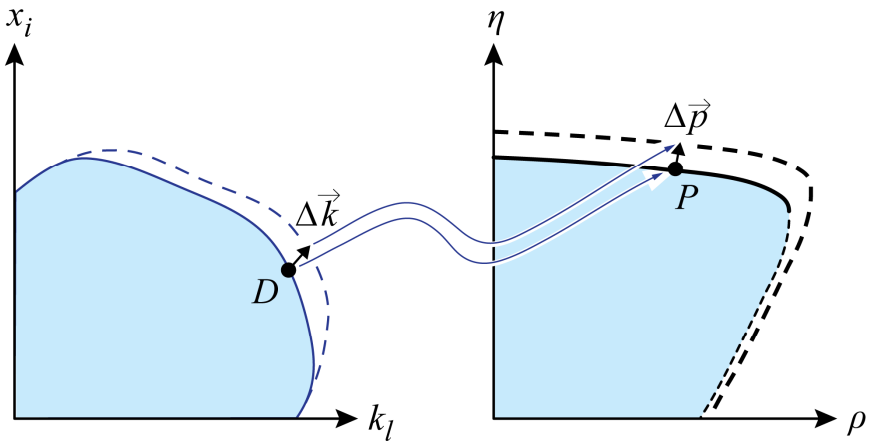
- **Metcalfe's Law**
  - **Moving form Hub-Based Concept to Community Concept Increases Potential Network Value Exponentially (~n(n-1) or ~n log(n))**



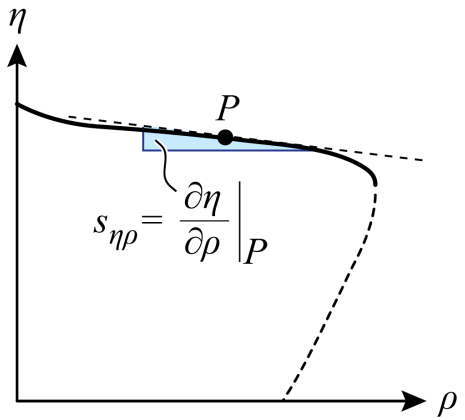


Technology Sensitivity Analysis Based on η-ρ-Pareto Front

- Sensitivity to Technology Advancements
- Trade-off Analysis

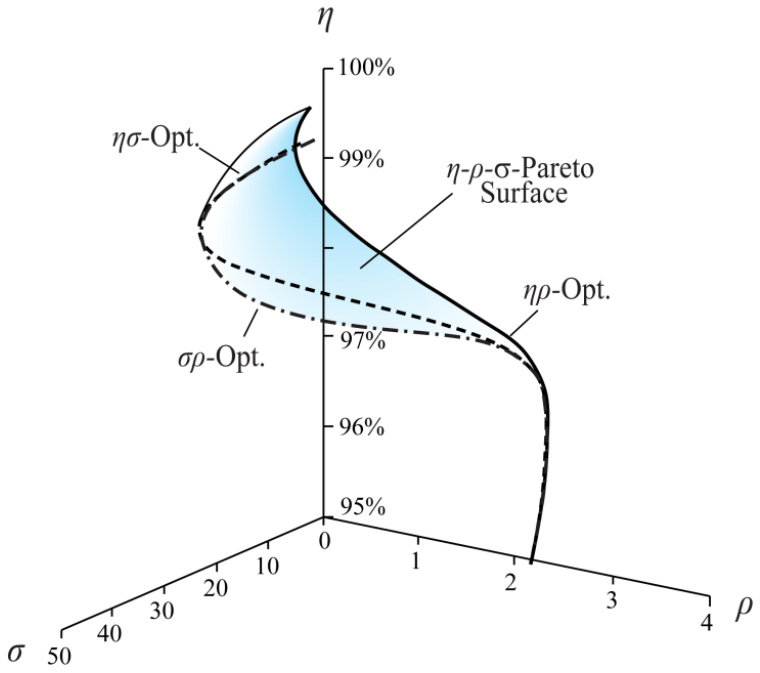


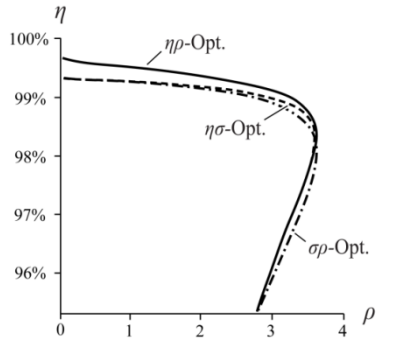
Design Space Performance Space

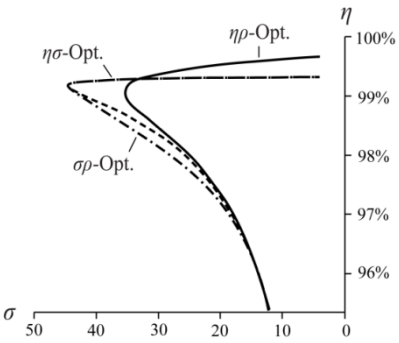


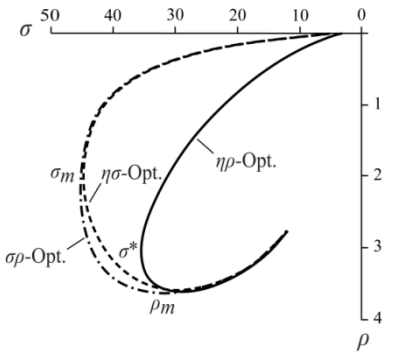
Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

► σ: kW/$



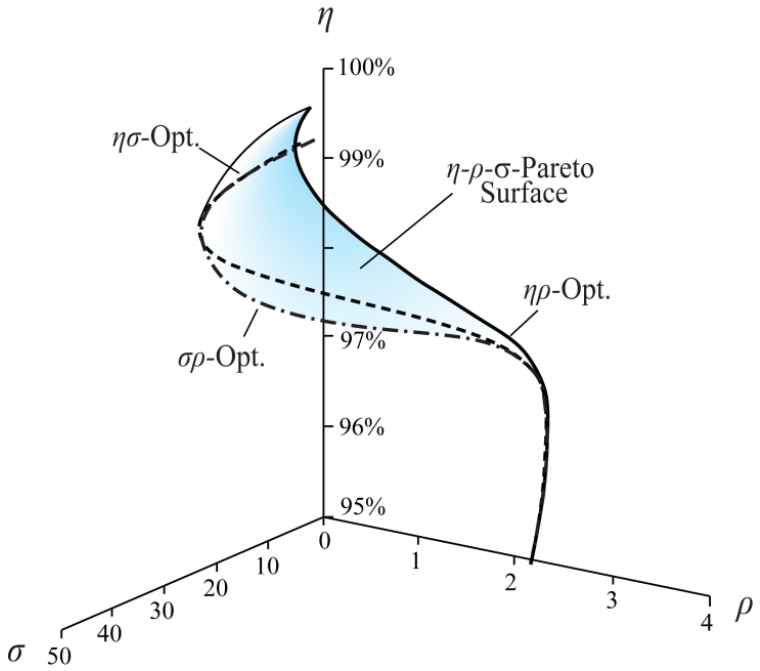


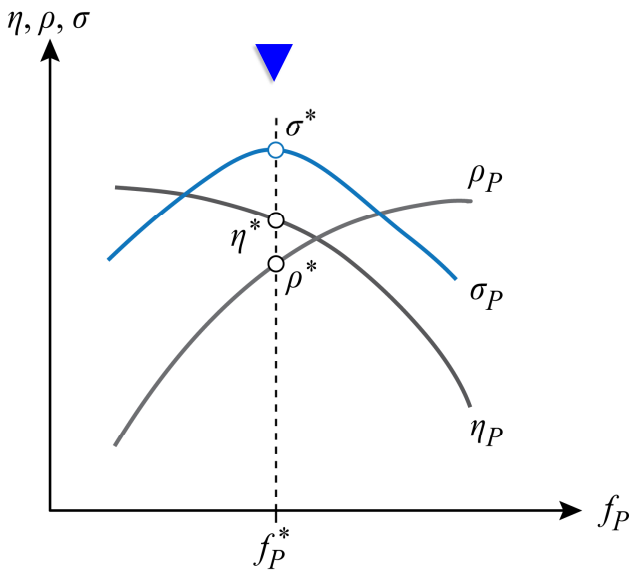




Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

- *´Technology Node´*





Technology Node: $(\sigma^*, \eta^*, \rho^*, f_P^*)$

Future Development

"Devices"
- Minimize / Avoid Packages → (PCB) Embedding
- Integrate Driver Stage
- Integrate Sensors / Monitoring
- Multiple Use of Isolated Gate Drive Communication Channel
- Offer Test Devices with Integrated Measurement Function
- Facilitate (Double Sided) Heat Extraction

Converters
- Standardized Very Low Cost Building Blocks
- "Application Specific" = Wide Operating Range Standardized Blocks
- Self-Parametrization
- Bidirectional Converters

Systems
- AC and DC Distribution
- Single Converter vs. Combination of Modules / Cells
- Initial Costs / Life Cylce Cost Trade-off
- Grid 4.0

Design
- Minimize Design Time / Fully Computerized
- Maximize Design Flexibility for Appl. Specific Solution (PCB)
- Maximize Design Insight for Trade-off Analysis
- Design for Manufacturing (Planar / PCB Based)

Literature
- More & More "White Noise"