Controllable dv/dt Behaviour of the SiC MOSFET/JFET Cascode An Alternative Hard Commutated Switch for Telecom Applications

Daniel Aggeler, Juergen Biela, Johann W. Kolar
Power Electronic Systems Laboratory (PES)
ETH Zurich,Switzerland
Email: aggeler@lem.ee.ethz.ch

***Abstract*— Switching devices based on SiC offer outstanding performance with respect to operating frequency, junction temperature and conduction losses and enable a significant improvement of the system performance. There, the cascode consisting of a MOSFET and a JFET additionally has the advantage of being a normally off device and offering a simple control via the gate of the MOSFET.**

Without dv/dt control, however, the transients with hard commutation reach values of up to 45 kV/μs, which could lead to EMC problems and especially in drive systems to problems related to earth currents (bearing currents) due to parasitic capacitances. Therefore, new dv/dt control methods for the SiC MOSFET/JFET cascode as well as measurement results are presented in this paper. Based on this new concepts the outstanding performance of the SiC devices can be fully utilised without impairing EMC.

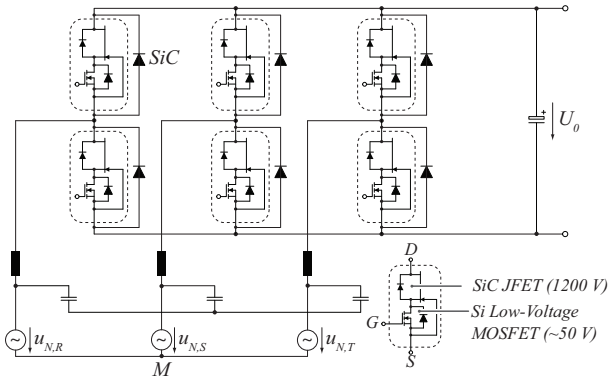

Fig. 1: Bidirectional three-phase boost topology with input and output filter and the SiC MOSFET/JFET cascode.

I. Introduction

The trend for the design of power electronic systems applied for example in telecom applications is towards higher power density and higher efficiency values. In order to reduce the system volume and achieve a higher power density, first the appropriate topology for the intended application must be chosen. Second, the design parameters must be chosen so that minimal volume and/or efficiency results. Due to large number of design parameters and coupling between these parameters this is advantageously done with an optimization procedure as presented in [1]. There, usually a high switching frequency is required for minimizing the volume of the passive components and the conduction as well as switching losses of the semiconductors must be low for achieving a high efficiency.

In the voltage range up to 600 V, high performance MOSFET switches capable of working at high switching frequency (e.g. COOLMOS) with low switching losses are applied in PFC converter systems (e.g. *VIENNA* rectifier [2],[3]). However, these devices offer a poor performance with respect to conduction losses in the 1200V range, so that usually IGBTs are used, which have significantly higher switching losses. This limits the reasonable operating frequency in this voltage range and therewith also the achievable power density. In order to overcome this limitation new devices based on SiC could be used.

The 1200 V SiC JFET [4] from SiCED offers very fast transients of up to 45 kV/μs (**Fig.** 2) with a blocking voltage of 1200V due to its vertical structure and the resulting low input/miller capacitance. However, the normally-on behaviour of the SiC JFET prevented that the switch is fully accepted for industry applications although improved gate drive circuits have been developed [5].

A normally off behavior could be achieved by using a cascode configuration with a low-voltage Si MOSFET in series with the 1200 V SiC JFET, without losing the excellent characteristics of the SiC device. In this configuration only the low-voltage MOSFET is actively controlled whereas the SiC JFET is inherently controlled by the drain-source voltage of the MOSFET. The gate drive circuit for the SiC cascode is a standard IGBT/MOSFET driver and therefore the currently used switches could directly replaced by the SiC MOSFET/JFET cascode as shown for a three-phase boost topology in **Fig.** 1.

As a result of extremely fast voltage edges, which are

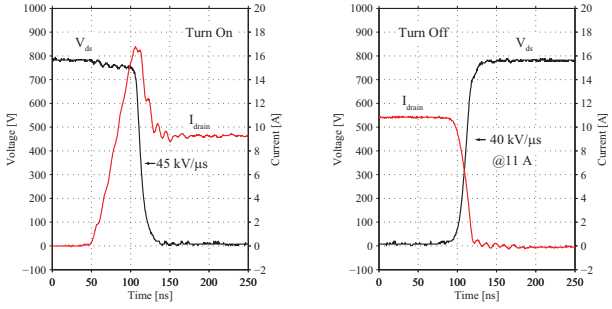

Fig. 2: Measurement result @ $V_{dc} = 800\,\mathrm{V}/I_{drain} = 9\,\mathrm{A}/11\,\mathrm{A}$ (hard switching) with the SiC MOSFET (IRF2804)/JFET cascode.

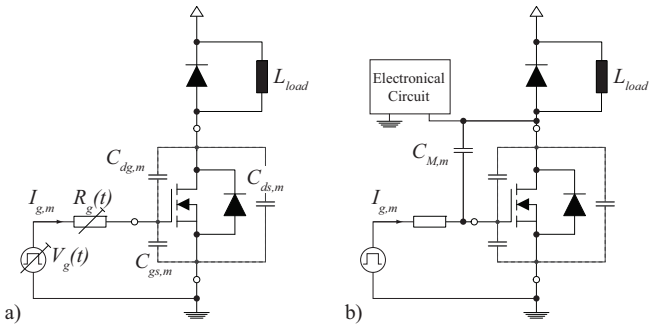

Fig. 3: Often used dv/dt limitation methods for MOSFET and IGBT switches; a) Varying gate resistors and 2- or 3-step controlled gate voltage. b) Additional drain source Capacitor $C_{M,m}$ causes an increased negative miller feedback.

achieved with the SiC cascode in hard commutated switching actions Fig. 2, the effort for the design of a low inductive layout avoiding switching related overvoltages is increasing. In [6] overvoltages are occurring due to parasitic and not avoidable module and layout inductances. Furthermore the desire for a controllable dv/dt of the cascode switching transients is high also due to EMI/EMC filtering [7].

In this Paper novel methods to control and adjust the dv/dt behaviour of the SiC MOSFET/JFET cascode are presented. Standard and well know techniques for MOSFET and IGBT semiconductors are shortly discussed in **Section** II. The application of the conventional techniques controlling dv/dt is evaluated related to the cascode configuration and the novel dv/dt controlling methods are detailed described in **Section** III. In **Section** IV experimental results of fast and controlled transients voltage edges of the cascode are shown. Finally, the switching energy of the SiC cascode is discussed and an exemplary calculation for a three-phase boost topology consisting of the SiC cascode is given.

II. Conventional dv/dt limitation techniques

For currently often used semiconductors as Si MOSFET and IGBT devices several techniques [8] to reduce and control the dv/dt at fast switching edges are well known as shown in **Fig.** 3. The most simple and applied one is the control with the external gate resistor. The optimal gate resistance has to be selected to the corresponding switching device. In [9] the evaluation between varying gate resistors and an active gate voltage control (2-or 3-step gate voltage) is presented. There are different and more complex active gate control methods published as in [10] where the additional external ('artifical') miller capacitance is electronically adjusted to the effective gate to drain capacitance. An advanced methode is introduced in [11] where the current of the external miller capacitance is electronically controlled and at the same time the optimal point for minimal switching losses is calculated.

Most of these dv/dt limitation methods are based on the miller effect of an increased input capacitance at the switching events. For each turn on and turn off switching the gate source and the drain source capacitance has to be charged and discharged.

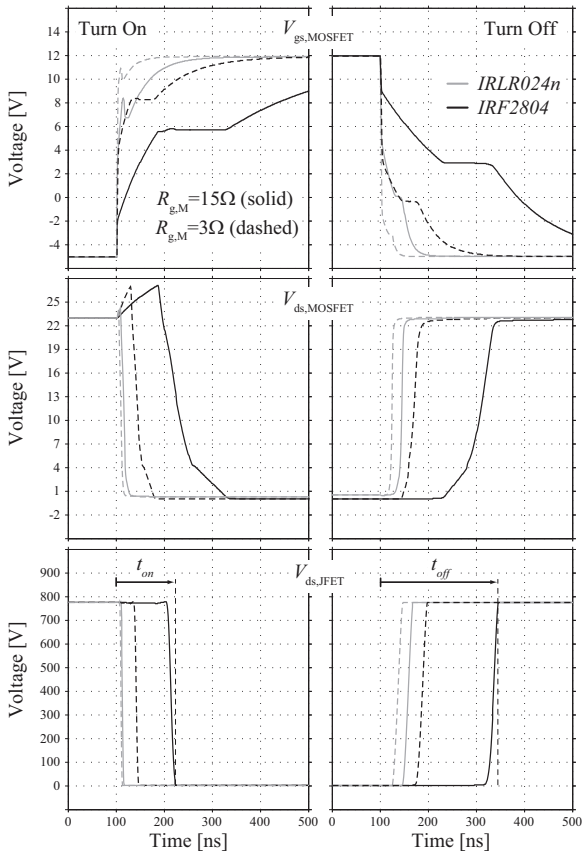

Fig. 4: Simulation results of applied conventional dv/dt limitation techniques with different gate resistors (3 Ω dashed line,15 Ω solid line) of the low-voltage MOSFET. Conventional techniques are not useful for the SiC cascode as illustrated by the equal dv/dt of the JFET drain source voltage.

Applying the conventional dv/dt limitation techniques to the SiC cascode results not in the desired behaviour of reducing the fast switching voltages edges. The reason is the serial connection of the low-voltage MOSFET and the SiC JFET. The conventional methods just influence the behaviour of the active controlled low-voltage MOSFET.

A. SiC Cascode

To investigate the influence of the conventional methods for the SiC cascode configuration a simulation setup (cf. schematic of experimental setup in **Fig.** 8) with $Simplorer^{TM}$ has been performed. There standard Spice models supplied by the manufacturers have been used for the low-voltage MOSFETs [12] and the freewheeling SiC Diode [13]. The applied SiC JFET model has been investigated and the Spice parameters have been extracted from experimental measurement in [14]. The simulation has been performed with different gate resistors ($R_{g,M} = 15\,\Omega$ and $R_{g,M} = 3\,\Omega$) of the various conventional techniques to control dv/dt behaviour. The same results could also be assumed with a 2 or 3-step

	IRLR024n	**IRF2804**
V_{DSS}	55 V	40 V
I_D@$T_c = 25\,\mathrm{C}$	17 A	75 A
$R_{DS(on)}$@$V_{GS} = 10\,\mathrm{V}$	65 mΩ@$I_D = 10\,\mathrm{A}$	2 mΩ@$I_D = 75\,\mathrm{A}$
$C_{iss,V_{ds}=0}$	680 pF	7800 pF
$C_{oss,V_{ds}=0}$	480 pF	5000 pF
$C_{rss,V_{ds}=0}$	230 pF	2100 pF

TABLE I: Main characteristics of the selected low-voltage MOSFETs from International Rectifier.

voltage or than an additional drain gate capacitor (artifical increasing of the miller capacitor) of the MOSFET.

The conventional techniques influence only the low-voltage MOSFET behaviour as shown in **Fig.** 4. Illustrated are the turn on switching behaviour of 4 A (hard switching) and the turn off switching at 7.5 A for two different low-voltage MOSFETs (cf. **Table** I; *IRLR024n* and *IRF2804*). Depending on the capacitance values, C_{iss},C_{oss} and C_{rss}, of the MOSFETs an increased value of gate resistance influence the charge and discharge behaviour of the gate source capacitance drastically. Therefore also the drain source voltage of the MOSFET is influenced. However there is almost no change in dv/dt behaviour.

The standard/conventional method to control the dv/dt value of the SiC cascode has no significant influence on the drain source voltage edge of the JFET as shown in the third simulation result. The influence by the different gate resistors is the time to start the switching action. In this case the delay time (t_{on},t_{off}) can be controlled by the conventional techniques. The slope of the drain source voltage keeps to be the same independent of the MOSFET type and also from the conventional techniques.

III. Novel dv/dt limitation methods - SiC Cascode

For the cascode topology novel methods to control the dv/dt has been investigated. Resulting are two concepts to slow down the very fast voltages edges at turn on as well as at turn off. In **Fig.** 5 the novel topologies for the cascode configuration to control the dv/dt behaviour are shown and in the following investigated.

A. Drain Gate Capacitor $C_{dg,M}$

The dv/dt controlling concept with the additional drain gate capacitor $C_{dg,M}$ is based on the conventional method of the MOSFET. The operating principle to control the dv/dt of the drain source voltage is explained in four time periods for the turn on characteristics as for the turn off characteristics as shown in **Fig.** 6. In the following the influence of the capacitor $C_{dg,M}$ in the cascode topology is investigated and detail discussed for the turn on behaviour.

1) Period T_1: During T_1 a positive voltage is applied to the gate source voltage of the MOSFET and the corresponding capacitance $C_{gs,M}$ is charged. This result in a marginal increase of the MOSFET drain source voltage. The cascode switch is still turned off and the behaviour is comparable with a single MOSFET device.

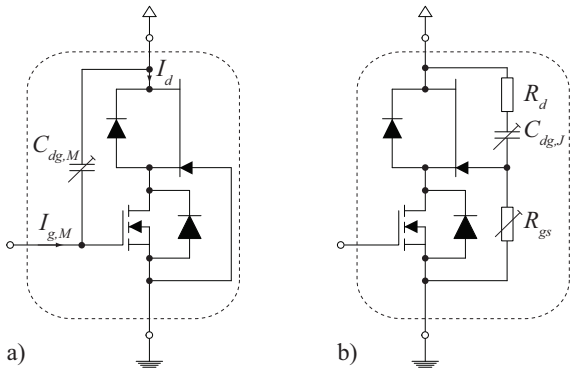

Fig. 5: The novel dv/dt controlling concepts for the SiC MOSFET/JFET cascode; a) Additional drain gate capacitance resulting in an increased negative feedback to the MOSFET gate. b) RC-circuit between drain and gate of the JFET and a gate resistance for the JFET.

2) Period T_2: At the beginning of T_2 the gate source voltage achieves the miller level, where the drain current is equal to the load current and the current stops to conduct through the freewheeling diode. The $V_{ds,MOSFET}$ decreases fast to a level, which could be called cascode JFET miller level $V_{cascode,JFET,miller}$, and keeps the level almost constant until the cascode drain source voltage is decreased to the on voltage. The MOSFET voltage level of 16 V is depending on the drain current I_d of the JFET. The drain current can be approximatively calculated to

$$I_d = I_{g,M} + I_{load} \tag{1}$$

assuming that $\frac{V_{gs,M}}{dt} = \frac{V_{dg,M}}{dt} = 0$. The gate current $I_{g,M}$ is defined by the gate resistor R_g to

$$I_{g,m} = \frac{V_g - V_{gs,M}}{R_g} = C_{dg,M} \cdot \frac{V_{ds,J}}{dt}. \tag{2}$$

The cascode miller level is decreasing with a higher load current. Responsible for this load current cascode miller level is the JFET characteristics which has to open the channel to conduct the load current and consequently the gate source voltage of the JFET ($V_{ds,M} = V_{gs,J}$) has to decrease. At the end of period T_2 there is a fast small drop of I_d (cf. Fig. 6) where the capacitor $C_{dg,M}$ is completely discharged ($I_{g,M} = 0$).

3) Period T_3: Across the SiC JFET there is just the voltage drop caused by the $R_{ds(on)}$ of the channel applied at the beginning of period T_3. The gate source voltage is still in a stable level, in this case it's the well known miller level of a single MOSFET.

4) Period T_4: The cascode switch is completely in conduction mode and therefore the gate source voltage is increasing to the nominal gate voltage V_g applied from the gate driver. Furthermore the inductive load current increases in dependence of the load voltage and the inductance value.

The main part to limit the dv/dt is the time period T_2. There, only a gate driver limited current is flowing through the

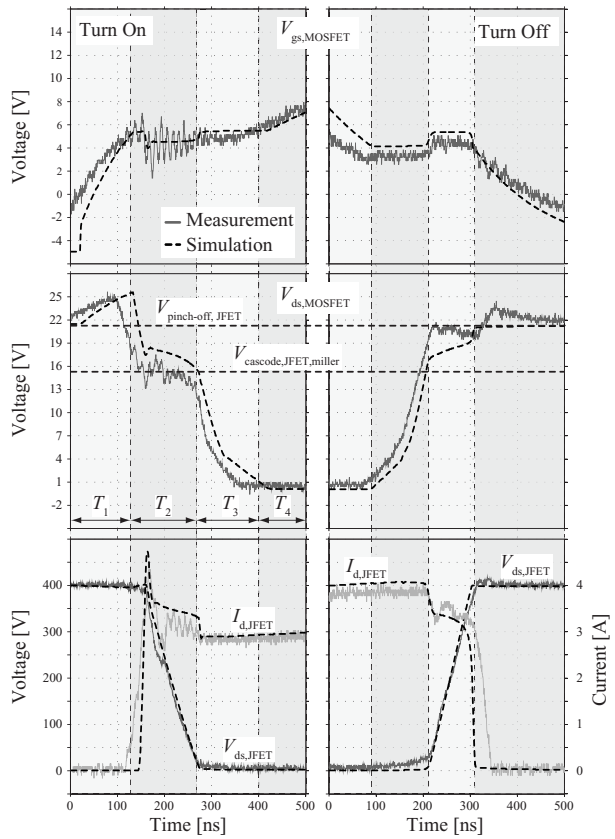

Fig. 6: Measurement and simulation results of the SiC cascode illustrate the influence of the $C_{dg,M}$ @400 V/3 A(turn on) and 4 A(turn off). Concept A. with $C_{dg,M} = 100\,\mathrm{pf}$ and $R_g = 20\,\Omega$.

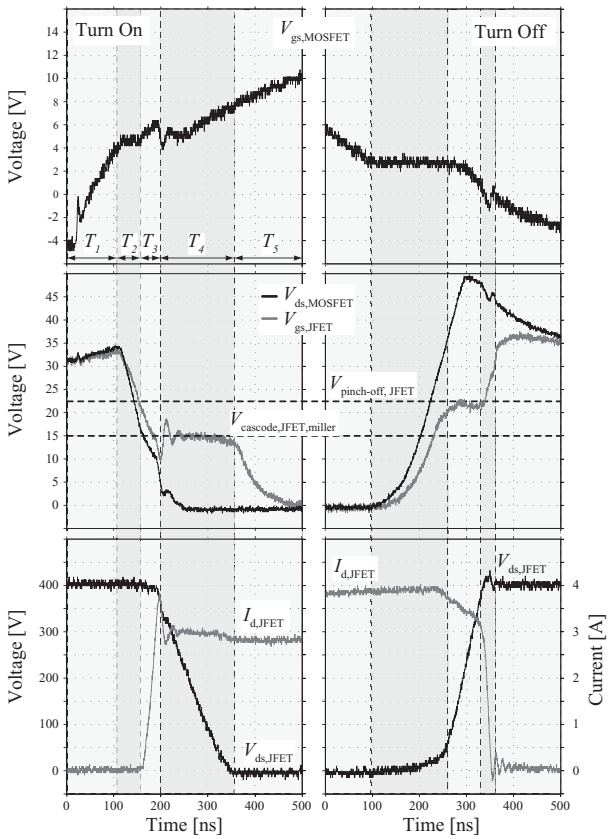

Fig. 7: Measurement results of the SiC cascode illustrate the influence of the RC-circuit and the JFET gate resistor @400 V/3 A(turn on) and 4 A(turn off). Concept B. with $R_d = 100\,\Omega$, $C_{dg,J} = 100\,\mathrm{pF}$, $R_{gs} = 47\,\Omega$ and $R_g = 20\,\Omega$.

capacitor $C_{dg,M}$ and therefore the length T_2 is controllable. At turn off the detail described turn on behaviour is analog and therefore the MOSFET blocks first to the called cascode miller level. Then, the main dv/dt rating event starts with charging the additional capacitor and finally the whole voltage is across the cascode switch.

B. RC-Circuit and JFET Gate Resistance

An alternative concept to control the dv/dt consists of a RC-circuit and an additional resistor R_{gs}. The detailed description of the dynamic behaviour is described based on **Fig.** 7.

1) Period T_1: Period T_1 is equal to the first control method described in (A.). The gate source voltage is applied and the MOSFET gate source capacitor is charged until the miller level is achieved. Remarkable is the level of the drain source voltage of the MOSFET because it's above the pinch-off voltage of the JFET and it's nearly the avalanche voltage of the MOSFET. This high level will be explained in detail in part four in particular at the turn off switching.

2) Period T_2: The gate source voltage of the MOSFET is equal to the miller level at the beginning of this time period. Hence, the drain source voltage of the MOSFET is decreasing rapidly and also the $V_{gs,JFET}$ is decreasing. At the same time the drain source voltage of the JFET keeps at the same level because the gate source junction is still pinched-off as shown with the measurements.

3) Period T_3: The MOSFET drain source voltage is still decreasing while the gate source voltage of the MOSFET keeps the miller level. With decreasing $V_{ds,m}$ the gate source voltage of the JFET is also decreasing. At the beginning of T_3, $V_{gs,JFET}$ achieves the $V_{pinch-off,JFET}$ and continues to decrease. Therefore the SiC JFET channel opens and the drain current of the JFET increases fast with a small capacitive peak current. Achieving the value of the load current the freewheeling diode is turn off and the whole load current is flowing through the cascode.

4) Period T_4: At the beginning of T_4 the cascode JFET miller level is achieved and controlled by the load current. The JFET drain source voltage starts to decrease. Additional to the load current the limited current which discharges the capacitance $C_{dg,J}$ is flowing through the switch. At the end of the time period T_4 the gate source voltage is already increasing to the nominal gate voltage because the MOSFET is turned on earlier than the JFET.

5) Period T_5: The JFET gate source voltage is decreasing to zero volt and the cascode switch is turned on completely.

The dv/dt limitation in this concept of the cascode topol-

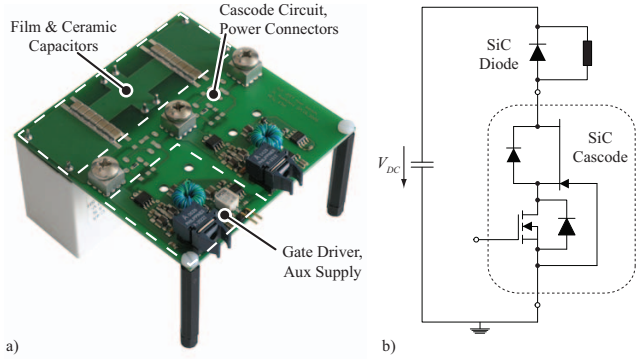

Fig. 8: a) Experimental setup to verify the concepts of the dv/dt controlling of the SiC MOSFET/JFET cascode. b) Schematic of the experimental topology (buck-topology).

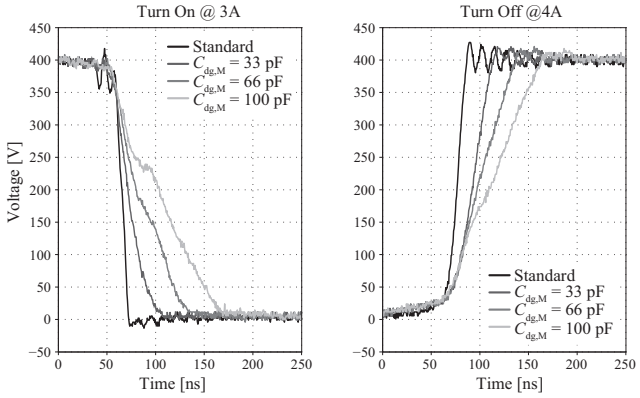

Fig. 9: Measurement results of the dv/dt concept A. @ 400 V with different values of the capacitance $C_{dg,M}$.

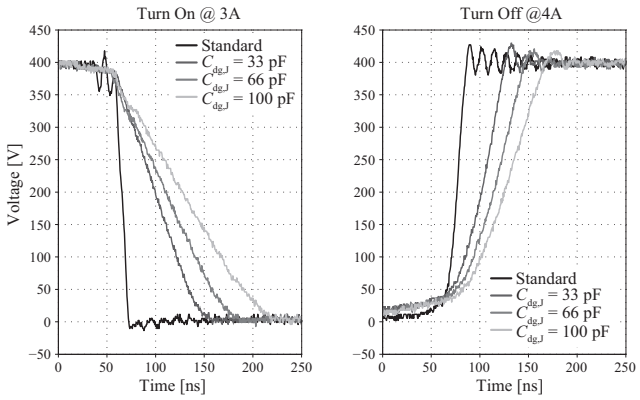

Fig. 10: Measurement results of the dv/dt concept B. @ 400 V with different values of the capacitance $C_{dg,J}$ and $R_{gs} = 47\,\Omega$.

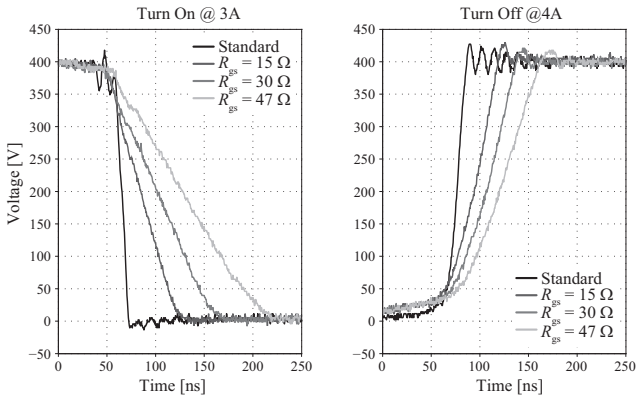

Fig. 11: Measurement results of the dv/dt concept B. @ 400 V with different values of the resistance R_{gs} and $C_{dg,J} = 100\,\text{pF}$.

ogy takes place in the fourth time period where the discharge/charge of the capacitor is occurring. Resistance R_d is necessary due to damping gate drive oscillation and helps in the same way to limit the discharging/charging current. Therefore, the dv/dt limitation can be controlled by two or three parameters respectively. There is also the gate resistance R_{gs} of the JFET which builds an RC-circuit together with the gate source capacitance of the JFET. Resulting is a challenging behaviour at turn off as shown in the measurement (cf. Fig. 7). The MOSFET drain source voltage is increasing until the pinch-off voltage of the JFET is achieved. At this point the drain source voltage of the JFET starts to increase while the drain source voltage of the MOSFET is further increasing until the whole voltage is blocked by the cascode. During this dynamic behaviour the gate source diode of the JFET is pushed into avalanche. Depending on the MOSFET blocking voltage also the MOSFET is in avalanche mode a short time. After turn off there is a static balancing avoiding the avalanche. In case of continuous operation at high frequency the static balancing time will be too short and both junctions of the JFET and the MOSFET operating continuously in avalanche mode. Due to no available accurate avalanche Spice model of the avalanche behaviour of the MOSFET and the JFET gate source diode no simulation results are presented in Fig. 7.

Both concepts are working and reduces the dv/dt rating of the cascode. Advantageously of the first concept is the proper operation in the nominal and specified ranges of the devices. In the second concept there are more parameters to control the dv/dt but also the avalanche mode operation. Furthermore, both concepts have additional losses due to the additional capacitors and the decreased dv/dt of the cascode voltage edges. The resulting energy losses are shortly discussed in Section IV. Depending on the application of the cascode a combination of both concepts additional with conventional techniques lead to an optimized switching behaviour. In the following Section IV the controllable dv/dt is verified with measurements.

IV. Experimental Results

An experimental setup shown in **Fig.** 8 has been built for the SiC MOSFET/JFET cascode to verify the concept of controlling the dv/dt behaviour at turn on as well as at turn off. The experimental testing has been performed with a buck topology.

Therefore, the setup consists of capacitors stabilizing the

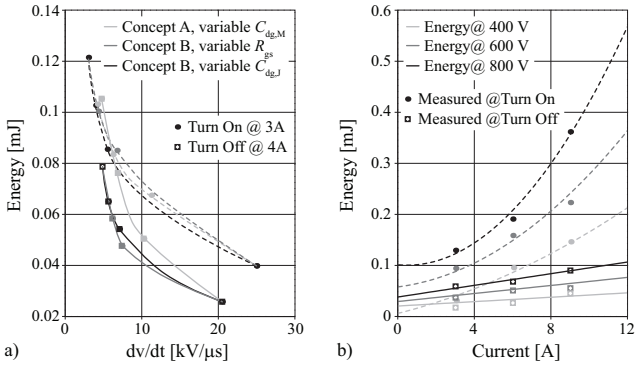

Fig. 12: Switching energy losses for a) the different dv/dt concepts @ 400 V and b) the SiC MOSFET/JFET cascode @ 400 V, 600 V and 800 V measured in a half-bridge configuration.

dc-link voltage, a halfbridge of SiC MOSFET/JFET cascodes and a standard gate drice circuits for MOSFET switches. Due to high dc-link voltage, the transfer of the gate signal is made with fiber optic transmitter/receiver. Furthermore, auxiliary power supplies are on the board feeding both gate drives and the fiber optic receivers.

In the following measurement results are presented to verify, with different values of the parameters ($C_{dg,M}, C_{dg,J}$ and R_{gs}), both concepts which are discussed in Section III . The measurement labeled as standard means the cascode topology with a low-voltage MOSFET and the SiC JFET without additional components. The gate resistance for this configuration has been selected to $4.7\,\Omega$. For all the other measurement verifying the both concepts a gate resistance of $20\,\Omega$ has been selected. **Fig.** 9 shows the measurement result of concept A. with three parameters $C_{dg,M} = 33\,\mathrm{pF}, 66\,\mathrm{pF}, 100\,\mathrm{pF}$. In **Fig.** 10 and **Fig.** 11 measurements with concept B. are shown. The experimental measurement verify the controllable dv/dt with different parameters.

Analysis of the measurement results show the switching energy dependency on the dv/dt of the SiC cascode as pictured in **Fig.** 12 a). With a controlled dv/dt the energy losses are increasing. Thereby, almost no difference of the energy losses is remarkable for turn on events. However, at turn off events concept A shows more energy losses than concept B. This additional amount of energy losses could be explained by the drain source voltage of the cascode (cf. Fig. 9). At turn off the drain source voltage is increasing fast up to $150\,\mathrm{V}$ compared to the turn off voltages edges achieved with concept B.

As an application for the SiC cascode is exemplary a three-phase boost topology (cf. Fig. 1) selected. Due to the high switching frequency possibility of the SiC material the input inductance of the three-phase boost converter is decreasing and the power density is increasing. Fig. 12 b) shows the energy characteristic of the standard SiC cascode for different voltages and currents. Therefore, the performance of the power stage (without input inductor, input and output filter) results in a maximal efficiency of $98\,\%$ with an output power of $1.5\,\mathrm{kW}$ as shown in **Fig.** 13 for $50\,\mathrm{kHz}$ and $100\,\mathrm{kHz}$.

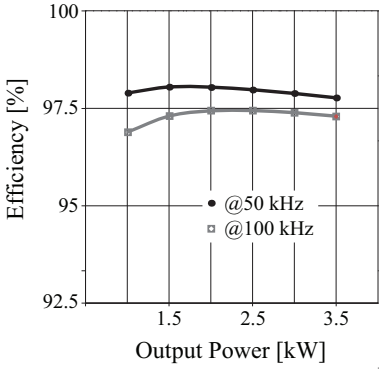

Fig. 13: Efficiency calculation of the three-phase boost converter (cf. Fig. 1) with a constant dc-link voltage of 800 V and a peak line voltage of 325 V.

V. Conclusion

In this paper novel concepts/methods to control and adjust the dv/dt of the SiC MOSFET/JFET cascode has been presented. It has been shown with experimental measurements that the cascode switch could decrease the fast voltages edges. Therefore EMC problems as layout caused overvoltages could be handled and the SiC cascode could be applied as an alternative hard commutated switch.

Acknowledgment

The authors are very much indebted to the ABB Corporate Research Center, Baden-Daettwil, Switzerland, for supporting research on future SiC power semiconductor applications at the Power Electronic Systems Laboratory, ETH Zurich.

References

[1] J. Biela, U. Badstuebner, and J. Kolar, "**Design of a 5kW, 1U, 10kW/ltr. resonant DC-DC converter for telecom applications**," in *Proc. 29th International Telecommunications Energy Conference INTELEC 2007*, Sept. 30 2007–Oct. 4 2007, pp. 824–831.

[2] J. Kolar and H. Ertl, "**Status of the techniques of three-phase rectifier systems with low effects on the mains**," in *Proc. 21st International Telecommunications Energy Conference INTELEC '99*, 6–9 June 1999, p. 16pp.

[3] S. Round, P. Karutz, M. Heldwein, and J. Kolar, "**Towards a 30 kW/liter, Three-Phase Unity Power Factor Rectifier**," in *Proc. Power Conversion Conference - Nagoya PCC '07*, 2–5 April 2007, pp. 1251–1259.

[4] P. Friedrichs, "**Silicon carbide power devices - status and upcoming challenges**," in *Proc. European Conference on Power Electronics and Applications*, 2–5 Sept. 2007, pp. 1–11.

[5] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "**A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter**," in *Fourtieth IAS Annual Meeting Industry Applications Conference Conference Record of the 2005*, vol. 1, 2–6 Oct. 2005, pp. 410–416.

[6] T. Nussbaumer, "**Netzrueckwirkungsarmes Dreiphasen-Pulsgleichrichtersystem mit weitem Eingangsspannungsbereich**," Ph.D. dissertation, ETH Zurich, 2004.

[7] M. Moreau, N. Idir, P. Le Moigne, and J. Franchaud, "**Utilization of a behavioural model of motor drive systems to predict the conducted emissions**," in *Proc. IEEE Power Electronics Specialists Conference PESC 2008*, 15–19 June 2008, pp. 4387–4391.

[8] P. Lefranc and D. Bergogne, "**State of the art of dv/dt and di/dt control of insulated gate power switches**," in *Proceedings of the Conference Captech IAP1*, 2007.

[9] N. Idir, R. Bausiere, and J. Franchaud, "**Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors**," vol. 21, no. 4, pp. 849–855, July 2006.

[10] S. Park and T. Jahns, "**Flexible dv/dt and di/dt control method for insulated gate power switches**," *IEEE J IA*, vol. 39, no. 3, pp. 657–664, May–June 2003.

[11] J. Kagerbauer and T. Jahns, "**Development of an Active dv/dt Control Algorithm for Reducing Inverter Conducted EMI with Minimal Impact on Switching Losses**," in *Proc. IEEE Power Electronics Specialists Conference PESC 2007*, 2007, pp. 894–900.

[12] "**International Rectifier**." [Online]. Available: http://www.irf.com

[13] "**CREE**." [Online]. Available: http://www.cree.com

[14] Y. Wang, C. J. Cass, T. Chow, F. Wang, and D. Boroyevich, "**SPICE Model of SiC JFETs for Circuit Simulations**," in *Proc. IEEE Workshops on Computers in Power Electronics COMPEL '06*, 16–19 July 2006, pp. 212–215.