# A compact, high voltage 25 kW, 50 kHz DC-DC converter based on SiC JFETs

D. Aggeler, J. Biela, J. W. Kolar
Power Electronic Systems Laboratory (PES), ETH Zurich, Switzerland
Email: aggeler@lem.ee.ethz.ch / Homepage: www.pes.ee.ethz.ch

***Abstract*— In the area of power electronics there is a general trend to higher power densities and efficiency. In order to continue this trend new devices, which enable high switching frequencies at higher power levels or show reduced losses at moderate switching frequencies are required.**

**High voltage switches based on a series connection of SiC JFETs and one MOSFET in cascode connection meet these demands. For investigating the performance of the SiC based switch and its influence on the power density/efficiency a dual active bridge, which could transfer 25 kW bidirectionally between a 5 kV and a 700 V dc bus at a switching frequency of 50 kHz, is presented in this paper.**

**There, especially the design of the high voltage/high frequency transformer and the switching as well as the static behaviour of the SiC switch is investigated in detail by simulations and experimental results in this paper.**

## I. Introduction

In the area of power electronic converter systems there is a general trend to higher power densities and higher efficiency which is driven by cost reduction, an increased functionality, saving resources and in some applications by the limited weight/space requirements (e.g. automotive, aircraft). In distributed energy systems, for example, efforts are made to replace the bulky line frequency transformers by high frequency (HF) transformers combined with power electronics [1]. Also in future autonomous drilling robots, which could replace traditional drilling methods by a high voltage (HV) cable and an electrically driven drilling head, costs and above all space/volume plays a decisive role. In this application, a high dc voltage feed via a flexible cable to the drilling head is converted by a dual active bridge (DAB - cf. **Fig.** 2) to a lower voltage, which supplies the inverter for the drilling motor.

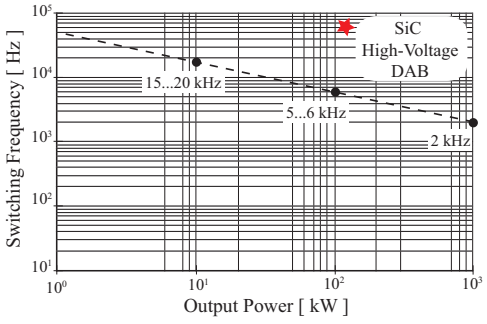



Figure 1: Common converter operating frequency versus output power with conventional semiconductors. The star marks the operating point of the DAB based on SiC-JFET devices presented in this paper.

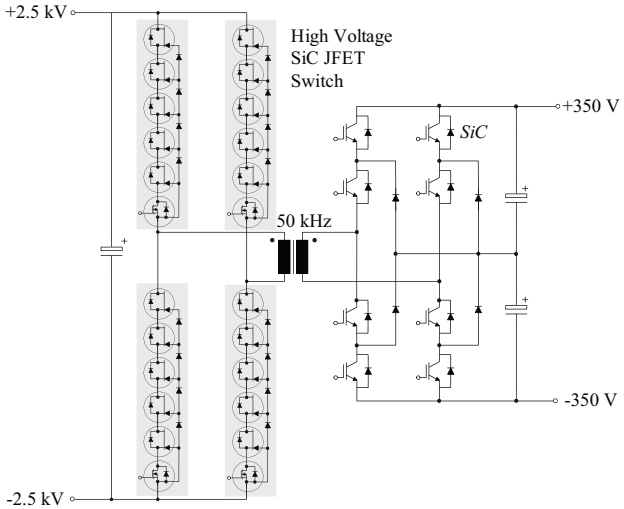



Figure 2: 25 kW (5 kV/700 V), 50 kHz DAB DC-DC converter based on high voltage SiC JFETs.

For reducing the volume of converter systems high operating frequencies are required in order to decrease the volume of the passive components. Due to the limitations of the available semiconductors the high operating frequency leads, especially at higher power levels, to high switching losses. Therefore, the operating frequency usually decreases with increasing power/voltage level (cf. **Fig.** 1).

In order to avoid the derating of the switching frequency at higher power levels and utilise the decreasing volume of the passive components, new devices, which combine high blocking voltage and fast switching operation, are required. High voltage JFETs based on SiC material offer these advantages [2] because of the material characteristic of SiC. Furthermore, the high blocking voltage allows a high dc voltage for power transfer which reduces ohmic losses in case of the autonomous drilling robot and increases efficiency of the distributed energy system.

For investigating the achievable performance of SiC based converters and the switching behaviour of the SiC JFETs,

| | |
|---|---|
| Input voltage $V_{in}$ | 5 kV |
| Output voltage $V_{out}$ | 700 V |
| Rated power $P_{out}$ | 25 kW |
| Switching frequency $f_s$ | 50 kHz |
| Transformer turns ratio | 50:7 |
| Input current $I_{in,rms}$ | 6.7 A |
| Output current $I_{out,rms}$ | 48.2 A |

Table I: Specification of the presented DAB dc-dc converter.

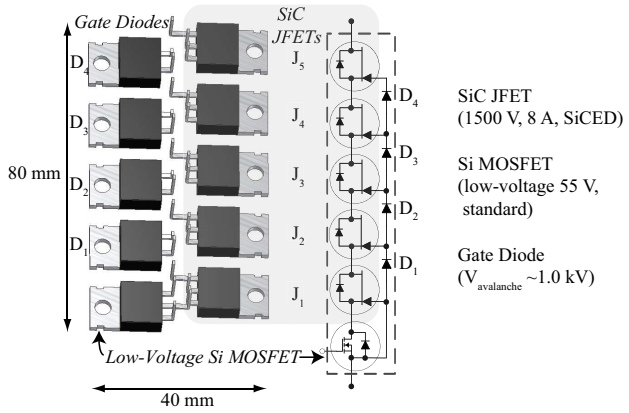



Figure 3: A SiC JFET cascode consists of five SiC JFETs, a low-voltage Si MOSFET and four gate diodes.

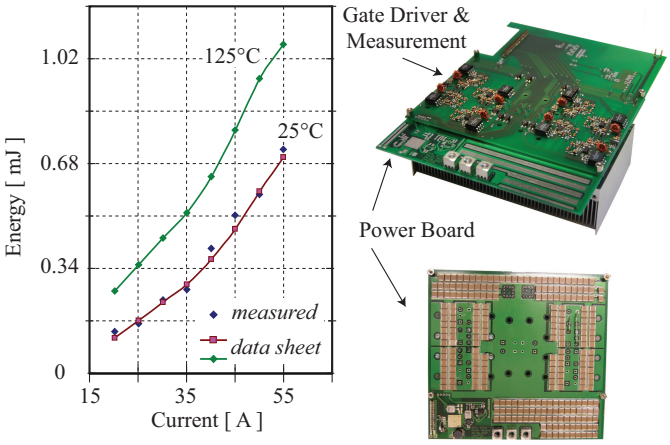



Figure 4: Measurement of the IGBT turn-off energy losses @350 V with the three level converter prototype.

which are connected in series/cascade for increasing the blocking voltage, a DAB converter (5 kV to 700 V, galvanically isolated) has been designed. There, cascaded SiC JFETs, which operate at a switching frequency of 50 kHz at a power level of 25 kW, are used on the primary side. On the secondary side a three level structure is applied, which allows the use of fast 600 V IGBT devices. In the following sections the switching behaviour of the SiC cascade and the design of the HF 5 kV transformer will be discussed in detail.

The operating principle of the three level topology, the specifications and the modulation method of the DAB are briefly presented in **Section** II. There, also the operating principle of the SiC JFET is explained. The design of the HF-HV transformer, which is an important component of the converter system, is discussed in **Section** III. Thereafter, the static and the dynamic behaviour as well as the stabilisation of the SiC JFET cascade is discussed based on experimental results in **Section** IV. The performance of the complete DAB bridge is presented in **Section** V.

## II. 5 kV - 700 V DUAL ACTIVE BRIDGE

The DAB converter, shown in Fig. 2 with the specification given in **Table** I, has a primary side voltage of 5 kV and a secondary side voltage of 700 V, which is used as dc link voltage for the inverter drive. For galvanic isolation a HF transformer consisting of E80 cores made of N87 material is used (cf. section III).

Due to the high primary voltage SiC JFETs in a cascode connection with a MOSFET, as shown in **Fig.** 3, are used. The switch consists of a low voltage (55 V) MOSFET for controlling the switch and five series connected/cascaded JFETs, with a blocking voltage of 1.5 kV each, for blocking the 5 kV dc voltage. The cascode connection of the MOSFET and the JFETs results in a normally off behaviour of the switch although the JFETs are normally on devices. The on/off state of the whole switch simply is controlled via the gate voltage of the low voltage MOSFET and no special gate drivers are required. Further details on the SiC cascade are discussed in Section IV. The fast turn on and off transients of the SiC based cascade and the associated low switching losses enable operation of the DAB at 50 kHz. The current rating of the SiC JFETs, which are available at the moment, is quite low (8 A). Therefore, the power which these devices could transfer is relatively limited and the output power of the prototype is 25 kW. In order to use the SiC devices as a replacement for IGBTs, SiCED/Infineon plans to commercialise devices with a reduced blocking voltage of 1200 V and a current rating of 5 A. These JFETs offer on resistances in the area of 0.36 Ω ...0.40 Ω. In case of 1.2kV devices the cascade must be extended by one more SiC-JFET in order to increase the blocking voltage capability of the switch.

On the secondary side a three level topology has been chosen so that fast 600 V IGBTs (or Superjunction MOSFETs), which are appropriate for operating at 50 kHz and higher power levels, can be used. With the chosen output voltage of 700 V, the operating voltage is 350 V, what allows the usage of 600V devices. At full load the RMS current on the secondary side is 48.2 A. Therefore, APT40GP60B IGBTs with a blocking voltage of 600 V and a current rating of 77 A@110 °C have been selected.

For the antiparallel IGBT diodes as well as for the three level diodes, 600 V/62 A@110 °C DSEI120 devices are used. There, separate diodes have been used since the losses in the antiparallel diodes are relatively high during power transfer from primary side to secondary side. The separate diodes offer a much lower thermal resistance from junction to case compared to diodes, which are combined in one housing with the IGBT, since the IGBTs are usually designed for normal inverter operation. There, the diodes are utilised lower.

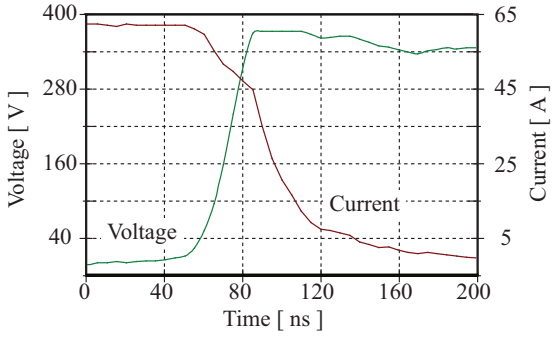



Figure 5: Turn-off waveforms of the APT40GP60B IGBTs utilised in three level converter at a voltage of 350 V and a current of 62 A.

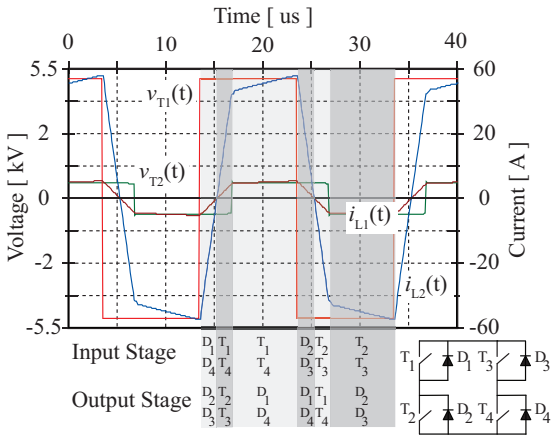



Figure 6: DAB waveforms for phase-shift modulation at $V_1$=5 kV, $V_2$=700 V and $P_{out}$=25 kW. At the bottom the semiconductors, which conduct in the respective interval, are shown.

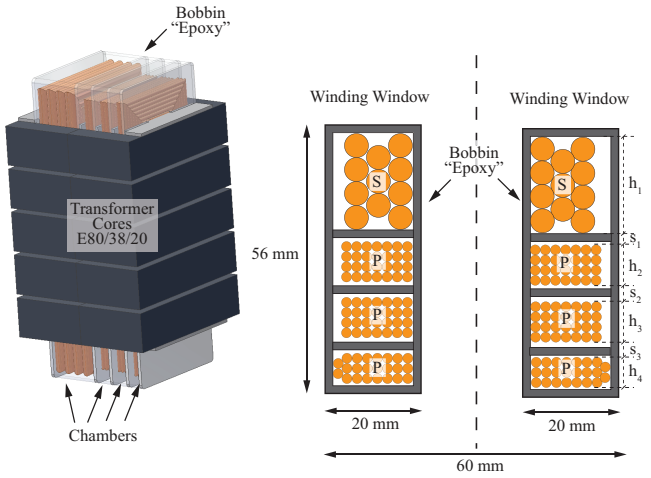



Figure 7: 3D-model of the 5 kV, 50 kHz transformer made of five parallel EE80/38/20 cores with a possible winding arrangement.

The three level prototype (cf. **Fig.** 4) is realised on two boards, a power board and a gate drive/measurement board. The overall design of the DAB and also the loss distribution are presented in Section V.

In **Fig.** 5 the turn off losses for the nominal voltage of 350 V are given. There, the losses at (25 °C) have been measured and as could be seen, these correspond very well to the losses given in the data sheet. Therefore, the loss data for a junction temperature of 125 °C has been taken from the data sheet. Measurements of these losses as well as the loss distribution for different modulations schemes, which utilise the three level structure, will be presented in future paper.

The conduction losses are 34 W for the switches and 164 W for the antiparallel diodes in case the power is transferred from primary to secondary side. The high losses in the antiparallel diodes are caused due to the operation mode (cf. **Fig.** 6), where the secondary side converter mainly operates as rectifier.

Due to phase shift modulation, all switches operate under ZVS conditions and do not cause turn on losses. The power flow is controlled by the phase shift angle $\Phi$, which is designed to be in the range of $[\pi/4 \ldots \pi/3]$. In Fig. 6 the simulated waveforms of the DAB, operating in phase shift mode, and the conducting semiconductors for the corresponding interval of the input and output stage are shown. There, it is assumed that the three level converter is operated like a two level converter, i.e. the two switches building one three level branch are always switched at the same time.

## III. 5 kV HIGH FREQUENCY TRANSFORMER

Besides the cascaded SiC JFETs, the 5 kV transformer operating at 50 kHz is an essential component of the DAB with respect to efficiency and power density. The voltage and current waveforms of the transformer, which determine the design, are fixed by the phase-shift operation of the converter. There, a phase-shift angle of $\pi/3$ is chosen for transferring the power of 25 kW. A higher phase shift value would increase significantly the reactive power and consequently the efficiency of the converter is reduced.

Based on the resulting waveforms different core materials (ferrite, iron powder, nanocrystalline) have been compared with the loss model presented in [3], which is based on data sheet values. There, the lowest overall losses and a compact design resulted with five parallel EE80/38/20 cores made of N87 material (cf. **Fig.** 7). With this design the flux density amplitude $\hat{B}$ at nominal power is 160 mT and the primary winding consists of 79 and the secondary of 11 turns. For the winding, litz wire is used in order to limit the losses due to skin- and proximity effect. The losses have been calculated by analytical equations for litz wire [4] in order to minimise the winding losses (cf. Table III). Based on these calculations a litz wire with a strand diameter of 0.1 mm (skin depth of 50 kHz is 0.3 mm) has been chosen. The resulting cross sections for the two windings are given in Table II.

| | Turns | Strands | External diameter | Cross section |
|---|---|---|---|---|
| Primary | 79 | 175 | 1.83 mm / 0.1 mm | 1.38 mm$^2$ |
| Secondary | 11 | 1260 | 5.12 mm / 0.1 mm | 9.90 mm$^2$ |

Table II: Specification of the transformer windings made of litz wire.

The arrangement of the windings is significantly influenced and the insulation requirements due to the high operating voltage – cf. Fig. 7. In order to avoid creepage distances in the bobbin it is advantageously manufactured as single piece. There, POM-material [5], which has a dielectric strength of 40 kV/mm could be used, but the mechanical properties of this material impede a bobbin design with thin walls ($\approx 1mm$).

Therefore, epoxy, which shows good mechanical and electric characteristics with several kV/mm dielectric strength, is utilised in the prototype. An alternative would be to use selective laser sintering (rapid prototyping), which also allows the manufacturing of a single piece bobbing.

Besides the bobbin also the litz wires have high breakdown voltage, since the isolation is made of 3 layers mylar. This allows to omit a separate layer insulation. In order to reduce the voltage between successive layers and also the parasitic capacitance of the transformer, the high voltage winding is divided in three chambers. The turns in the chambers are wound in conventional manner (forth-back-forth...). The reduced layer voltage is also important for operation at high switching frequency and high *dv/dt*-values. The fast edges

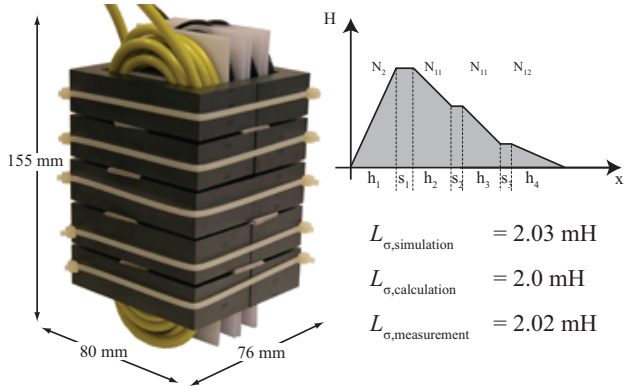



Figure 8: $5\,\text{kV}/50\,\text{kHz}$ transformer prototype with a leakage inductance of $L_\sigma = 2.02\,\text{mH}$ and distribution of the magnetic field between the primary and secondary winding.

of the voltage, presented in Section IV, could lead to a non uniform voltage distribution between the single turns/layers of one winding and to higher turn voltages at the ends of the winding during high *dv/dt*. This effect will be presented in detail in a future paper.

For proper operation of the DAB the series inductance between the primary H-bridge and the secondary one must be not too small. In the considered converter design a series inductance of 2.2 mH (referred to the primary) is required, which is integrated as the leakage inductance of the transformer. Therefore, the primary and secondary winding are separated.

For analytically estimating the leakage inductance of the transformer, it is assumed that the $H$-field in the core is zero and that the field lines are orthogonal to the core ($\mu \to \infty$). With these assumptions a field distribution as shown in **Fig.** 8 results for balanced magnetomotive forces ($N_1 I_1 = N_2 I_2$). The energy stored in this magnetic field is equal to the energy ($1/2LI^2$) stored in the leakage inductance.

The energy stored in the magnetic field could be calculated by

$$W_m = \int_V \frac{1}{2} BH dV = \frac{1}{2} L_\sigma I_1^2. \tag{1}$$

Evaluating the above equation for the magnetic field distribution of the prototype and equating this to the energy stored in the leakage inductance results in

$$L_\sigma = \mu_0 \frac{l_w}{l} \Big( \frac{2h_2 N_{11}^2 + h_4 N_{12}^2}{3} + \frac{h_1 I_2^2 N_2^2 + 3 I_2^2 N_2^2 s_1}{3 I_1^2} + \frac{(h_2 + s_2)}{I_1^2} ((-2 I_1 N_{11} + I_2 N_2)^2 + (-I_1 N_{11} + I_2 N_2)^2) \Big). \tag{2}$$

with

| | |
|---|---|
| $l_w$ | Average winding length |
| $l$ | Length of the winding window |
| $h_i$ | Width of the chambers |
| $s_i$ | Distance between the chambers/windings |
| $N_i$ | Number of windings in the corresponding chamber |
| $I_i$ | RMS current |

There, it is assumed that $h_2$=$h_3$ and $s_2$=$s_3$.

Besides the analytic calculations also 3D-FEM simulations with MAXWELL$^{TM}$ (cf **Fig.** 9) have been performed, in order to investigate the filed distribution in detail. The leakage inductance calculated with the FEM simulation is 2.03 mH and corresponds well with the analytically calculated (2.0 mH) and also the measured values (2.02 mH).

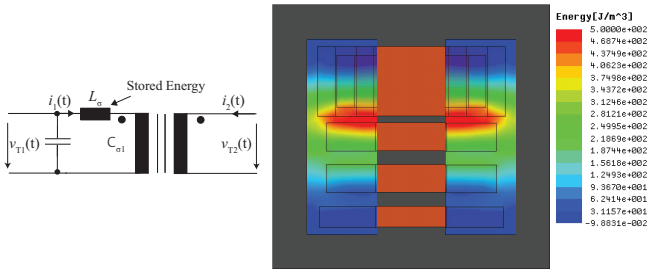



Figure 9: 3D FEM simulation of the the energy density in a cut plane through one of the cores. There, balanced magnetomotive forces $N_1 I_1 = N_2 I_2$ have been assumed, so that the magnetic field only represents the energy stored in the leakage inductance.

The dimensions and the remaining specifications of the HV transformer are summarised in Table III.

| | | |
|---|---|---|
| Material | | N87 |
| Core | | 5 × E80/38/20 |
| Dimensions | | 155mm x 80mm x 76mm |
| Turn number | | 79:11 |
| Power | | 25 kW |
| Core losses | $(100°C)$ | 26 W |
| HF losses | $(100°C)$ | 34 W |
| Leakage inductance | | 2.2 mH |
| Specified max. flux density | | 160 mT |
| Effective cross section | | 1950 mm$^2$ |
| Effective volume | | 359000 mm$^3$ |

Table III: Parameters of the 5 kV, 50 kHz transformer.

## IV. SiC JFET CASCADE

The basic concept of the SiC JFET cascode switch is described in [6]. There, also the static blocking characteristics and the dynamic switching behaviour are discussed based on experimental and simulation ($DESSIS - ISE^{TM}$) results. In the on-state of the SiC JFET cascade, the MOSFET is turned on by a positive gate voltage. Therefore, the gate of the bottom JFET $J_1$ (cf. Fig. 3) is connected to the source of the MOSFET and the JFET is conducting since it is a normally on device. Also the second JFET $J_2$ is conducting because its gate is shorted by JFET $J_1$. The same is true in analog manner for the other series connected JFETs. In the on state of the cascaded switch the JFETs work as a resistor connected in series to the on-resistance of the MOSFET.

For turning the cascaded switch off, first the MOSFET is turned off and the drain-source voltage of the MOSFET rises until the pinch-off voltage of JFET $J_1$ is reached. Then, JFET $J_1$ turns off and blocks the rising drain source voltage until the avalanche voltage of diode $D_1$ is reached. Due to the avalanche of diode $D_1$ the potential of the gate of JFET $J_2$ does not rise any more. Since the source of JFET $J_2$ continues to rise JFET $J_2$ also turns off as soon as the pinch-off voltage is reached. This sequential turn off continues with the next JFETs until the dc voltage is reached.

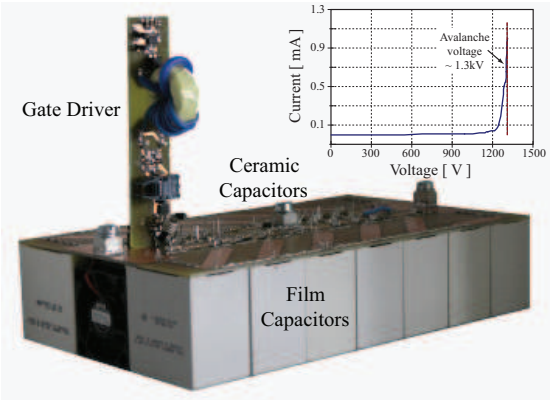



Figure 10: Test bench consisting of a half bridge with two switches consisting of a MOSFET and five cascaded JFETs for experimental investigation of the switching behaviour up to 5 kV. On the right hand side the avalanche behaviour of the voltage balancing diodes is shown.

In order to investigate the switching behaviour in detail, a half bridge with two switches consisting of a MOSFET and five cascaded JFETs connected to an inductor has been built (cf. **Fig.** 10). There, a standard gate driver is used to drive the MOSFET. The gate signal is transferred via fibre optics and the gate power via a small HV transformer. For minimising the stray inductance of the setup ceramic capacitors mounted closely to the JFETs are applied besides the film capacitors.

For a well defined static and dynamic behaviour of the SiC HV switch an avalanche rated gate diode, with stable avalanche voltage, is essential. In the prototype fast recovery rectifier diodes from STMicroelectronics are used, which show a stable avalanche behaviour at 1.3 kV (cf Fig. 10). In oder to reduce the voltage stress of the 1.5 kV JFETs to lower values, diodes with an avalanche voltage of $\approx$ 1.1 kV would be required. Unfortunately, such devices were not available at the moment.

### *A. Static behaviour*

As explained above the turn off and the voltage distribution (cf. **Fig.** 11) of the cascaded switch is mainly determined by the avalanche of diodes $D_1 \ldots D_4$. For a controlled and stable avalanche, i.e. for a controlled static behaviour/voltage distribution of the cascaded JFETs, a certain leakage current

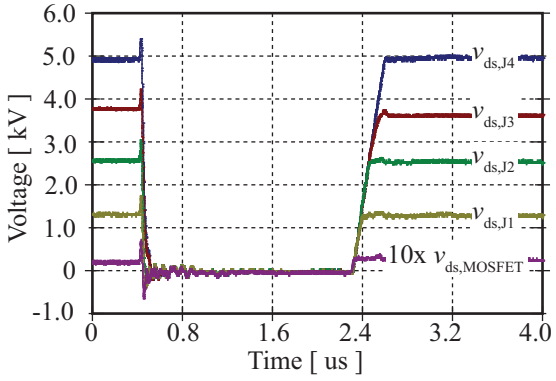



Figure 11: Voltage distribution across the SiC JFET cascade caused by the avalanche voltage of the gate diodes. The measurement are made with DA1855A amplifier from LeCroy.

through the diodes is required [6]. In order to guarantee this leakage current independently of the JFET gate parameters, resistors are connected between the gate and the source of the upper JFETs as shown in **Fig.** 13.

In order to investigate the influence of the gate-source resistors on the distribution of the leakage currents during off state, a PSpice model of the cascade (cf. **Fig.** 12) has been implemented. This is based on the PSpice SiC JFET model from SiCED [7] (preliminary beta-version). Due to numerical problems only two JFETs in series with a low-voltage MOSFET could be simulated, but the operating principle could be derived with this circuit.

Based on these simulations it could be concluded that the gate current $i_G(t)$ is negligible in static operation and the current from the source to the gate is mainly defined by the resistance value. This could be seen in Fig. 12 where the current $i_{SG}(t)$ for different gate resistors is depicted. The voltage across the resistor in the off-state is approximately defined by the pinch off voltage of the JFET, which varies significantly ($\approx$15 V... $\approx$30 V) with the available JFETs, what leads to largely varying leakage currents. In order to avoid this dependency on the pinch off voltage, only selected JFETs with similar pinch off voltages have been used during the measurements presented here.

By inserting the resistor a kind of control loop is initiated: In case the leakage current through the resistor decreases, since the JFET would like to turn off a bit more, the current through the resistor decreases. Consequently, also the voltage across the resistor decreases. This results in a lower gate-source voltage, what turns the JFET a little bit on, so that through the JFET a small current flows. Since the lower JFET/MOSFET is off this current only could flow via the resistor to the voltage balancing diode. Due to the increases current, also the gate-source voltage increases, so that the JFET turns a little bit off. This control mechanism leads to a stable leakage current through the resistor and the diode, so that the voltage sharing between the devices is stabilized by the avalanche voltage of the diode. This leakage current also flows through the upper JFET, what results in small off-state losses.

For a larger number of series connected devices the static behaviour as shown in **Fig.** 13 could be observed. There, the leakage current for the lower JFETs also flows via the upper JFETs, so that the current in the JFETs decreases from the upper to the lower one and the current in the voltage balancing diodes increases from the upper to the lower one. Again, the current distribution is self stabilizing, via the pinch off voltage and the resistors. The range of allowable pinch off voltage variations as well as the best value for the resistor, which guarantees a stable behaviour for all conditions and results in the lowest off-state losses, is part of the ongoing research and will be presented in a future paper.

With this leakage current distribution an operation could be achieved, where the lowest diode reaches its avalanche voltage first and therefore the blocking voltage is built up from the lower to the upper JFET.

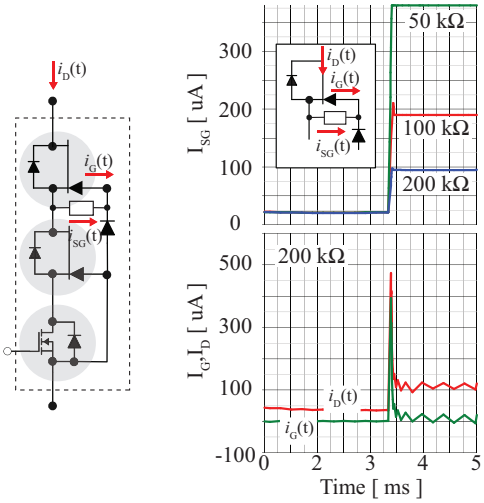
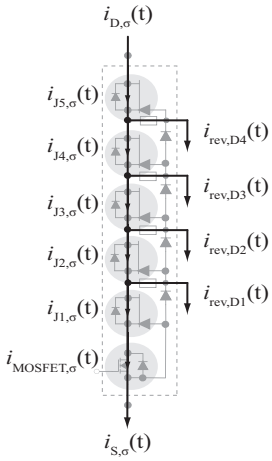



Figure 12: Depending on the gate-source resistor, the leakage current and therefore the operating point of the avalanche rated diode can be controlled. Simulations are made with SIMetrix and are based on the SiC JFET model from SiCED.




$$i_{D,\sigma}(t) = i_{J5,\sigma}(t) = i_{S,\sigma}(t)$$

$$i_{J5,\sigma}(t) > i_{J4,\sigma}(t) > i_{J3,\sigma}(t) > i_{J2,\sigma}(t) > i_{J1,\sigma}(t)$$

$$i_{rev,D4}(t) < i_{rev,D3}(t) < i_{rev,D2}(t) < i_{rev,D1}(t)$$

Figure 13: Leakage current distribution in the SiC HV Switch.

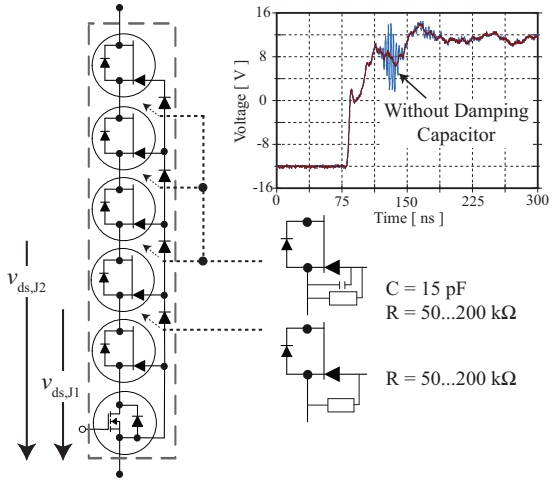



Figure 14: Additional resistors and capacitors guarantee a well defined leakage current and damp oscillations in the gate-source voltage (measured at a power supply voltage of 2 kV).

### *B. Dynamic behaviour*

As explained in the previous subsection the static behaviour is mainly determined by the leakage current distribution of the single devices in the stacked switches. During switching process the inner potentials of the switches are changing dynamically and are mainly defined by the capacitances of the JFETs and diodes.

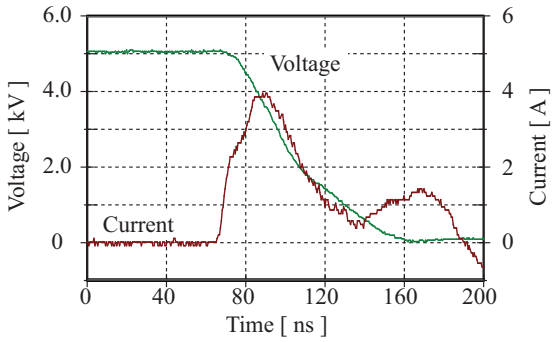



Figure 15: Turn on behaviour of the HV SiC JFET cascode at 5 kV.

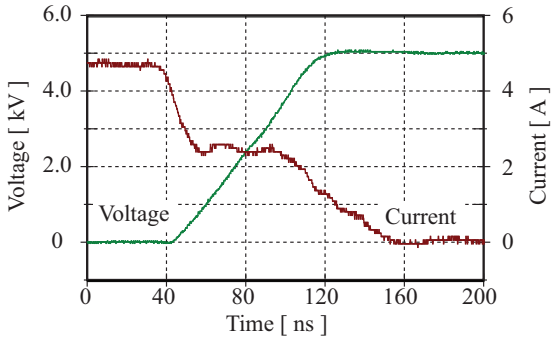



Figure 16: Turn off behaviour of the HV SiC JFET cascode at 5 kV.

In case no additional means except for the mentioned gate-source resistors are applied, oscillations in the gate-source voltage of the low-voltage MOSFET occur (cf. **Fig.** 14). The amplitude of the oscillations is increasing with increasing dc link voltage what finally leads to an unstable operation of the switch.

By inserting additional capacitors between the gate and the source connection of the upper JFETs ($J_3, J_4, J_5$) the oscillations could be significantly damped. Since the capacitances of the JFETs and diodes, which define the voltage distribution, are relatively small a measurement of the voltage distribution with probes is difficult, since the capacitance of the probe significantly influences the voltage distribution of the switches. Therefore, further investigations of the dynamic behaviour are made with a PSpice model and will be presented in a future paper.

In **Fig.** 15 and **Fig.** 16, the turn on and the turn off behaviour of the cascaded switch at a dc link voltage of 5 kV is shown. There, the gate-source resistors had a resistance of 200 kΩ and the capacitors were 15 pF. With the additional resistors/capacitors a stable and very fast switching could be achieved.

The current waveform at turn on shows a capacitive peak current at the beginning. At turn off a capacitive behaviour of the current could be seen, since the JFETs turn of very rapidly and therefore the current/voltage waveforms are mainly determined by the charging/discharging the drain-source ca-

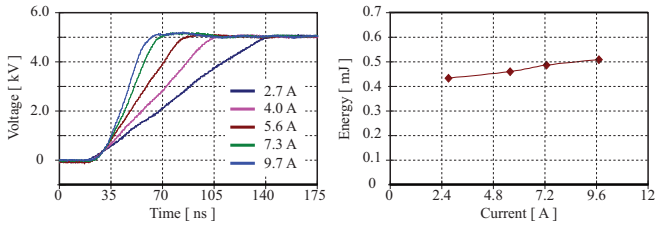



Figure 17: Voltage waveforms during turn off for different load currents and the "turn off" energy. This energy is stored in the parasitic capacitances, what results in negligible turn off losses.

pacitance of the two devices in the half-bridge.

In **Fig.** 17 the turn off losses, which are relevant for the phase shift operation of the DAB, are shown for different current levels. There, it could be seen that the turn off energy is approximately independent of the current. This is caused by the parasitic capacitances of the switch, which enable ZVS conditions during turn off. On the left hand side of Fig. 17 voltage waveforms for different currents are shown. There, it could be seen that the $dv/dt$ is only controlled by the current and the parasitic capacitances. Therefore, the energy shown in Fig. 17 is the energy stored in the parasitic capacitors and the turn off losses of the JFET are negligible.

## V. Design of the Converter System

Based on the experimental results of the half bridge presented in the previous section a DAB converter has been designed. A 3D CAD model is shown in **Fig.** 18, where a special focus was put on a compact design with high power density. The design of the input and the output side is similar. Both have a power board and a gate drive/measurement board. The DC-DC converter capacitor bank is realised with ceramic capacitors, 500 V/560 nF/X7R, from Holystone on the power board. There are two 80 ×80 mm fans for primary and secondary side, which cool actively the heat sink. Behind these and covered by the gate driver board, the HV HF transformer is located, so that the transformer is also actively cooled. The digital signal processor controlling the switches on the input side as well as on the output side is placed above the transformer. For protecting the control board from disturbances caused by the transformer an additional EMI shielding is used.

As already mentioned the nominal input voltage of the DAB is 5 kV and the rated power 25 kW. Applying the IGBTs and diodes as mentioned in section II results in the theoretical losses summarised in **Table** IV.

| | | Input stage | Output stage | Overall |
|---|---|---|---|---|
| Conduction losses | Switch | 84 W | 34 W | 118 W |
| | Diode | 84 W | 164 W | 248 W |
| Switching losses | calculated | ∼0 W | 224 W | 224 W |
| | measured | ∼0 W | 238 W | 238 W |
| | Transformer | | | |
| Core losses | 25 °C | 63 W | 100 °C | 24 W |
| HF losses | 25 °C | 28 W | 100 °C | 34 W |

Table IV: Loss distribution of the DAB converter operating at 50 kHz and with an output power of 25 kW.

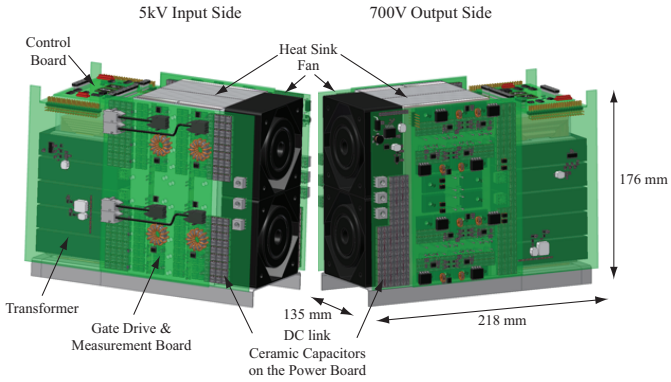



Figure 18: 3D-model of the DAB dc-dc converter.

Consequently, 700 W total losses and an efficiency of 97 % result.

## VI. Summary

In this paper a bidirectional 25 kW, 50 kHz dual active bridge DC-DC converter operating at a switching frequency of 50 kHz with a power density of 4.8 kW/l is presented. Due to the high input voltage on the primary side, which is 5 kV, high voltage series connected SiC JFETs are utilised in the converter. On the secondary side a three level structure based on 600 V IGBTs is used for the dc link voltage of 700 V. The resulting designed efficiency is 97 % (=700 W total losses).

Besides the construction of the converter system, especially the design of the 5 kV, 50 kHz transformer is examined in the paper. Furthermore, the switching behaviour and the static voltage distribution of the series connected devices is investigated in detail. With these devices the turn on and the turn off transient for an operation at 5kV is very fast (range of 40ns to 80ns). This results in very low switching losses of app. 250W for operating at full output power.

## References

[1] J. Biela, D. Aggeler, S. Inoue, H. Akagi, and J. W. Kolar, "Bidirectional isolated dc-dc converter for next-generation power distribution - comparison of converters using Si and SiC devices," vol. 127, 2007, PCC, Nagoya, Japan.

[2] P. Friedrichs, H. Mitlehner, K. Dohnke, D. Peters, R. Schorner, U. Weinert, E. Baudelot, and D. Stephani, "SiC power devices with low on-resistance for fast switching applications," in *Power Semiconductor Devices and ICs, 2000. Proceedings. The 12th International Symposium on*, 22-25 May 2000, pp. 213–216.

[3] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," pp. 36 – 41, 2002, Computers in Power Electronics.

[4] P. Wallmeier, "Automated optimization of inductive components in converter applications," Ph.D. dissertation, University of Paderborn, 2001.

[5] "Homepage of Kern GmbH." [Online]. Available: http://www.kern-gmbh.de/cgi-bin/riweta.cgi?nr=1201&lng=2.

[6] R. Elpelt, P. Friedrichs, R. Schorner, K.-O. Dohnke, H. Mitlehner, and D. Stephani, "Serial connection of SiC VJFETs - features of a fast high voltage switch," *REE. Revue de lElectricite et de lElectronique*, pp. 60 –68, 2004.

[7] "Homepage from SiCED (A Siemens Company)." [Online]. Available: www.siced.de.