Paper

Bi-Directional Isolated DC-DC Converter for Next-Generation Power Distribution - Comparison of Converters using Si and SiC Devices

J. Biela* Non-member
D. Aggeler* Non-member
S. Inoue** Member
H. Akagi** Member
J.W. Kolar* Member

In this paper two bi-directional DC-DC converters for a 1MW next-generation BTB system of a distribution system, as it is applied in Japan, are presented and compared with respect to design, efficiency and power density. One DC-DC converter applies commercially available Si-devices and the other one high voltage SiC switch, which consists of a SiC JFET cascode (MOSFET+1 JFET) in series with five SiC JFETs.

In the comparison also the high frequency, high voltage transformer, which ensures galvanic isolation and which is a core element of the DC-DC converter, is examined in detail by analytic calculations and FEM simulations.

For validating the analytical considerations a 20kW SiC DC-DC converter has been designed in detail. Measurement results for the switching and conduction losses have been acquired from the SiC and also for a Si system for calculating the losses of the scaled 1MW system.

Keywords: Next-generation BTB system, High voltage HF DC-DC converter, SiC JFET cascode, High voltage HF transformer

1. Introduction

Generally, the power generation with renewable energy sources is a discontinuous process and in most of the cases depending on the environment. Feeding in the produced energy into a distribution system influences the overall energy flow. Therefore, it is a challenge to control and keep the energy stabilised. **Figure** 1 shows a Japanese 6.6kV power distribution system having two feeders from a transformer.

Today, each distribution system in Japan has radial feeders, forming no loop. If the distributed power generators are installed concentrated on one of the feeders (feeder 2 in figure 1), regulating voltage on both feeders within an acceptable range becomes difficult.

Back-to-Back (BTB) systems, also known as loop controllers, have been investigated to solve the problem of power flow balancing. The dotted lines in figure 1 show where the BTB system would be installed and in **figure** 2 a circuit configuration is shown which is presented in [1]. The line-frequency (50Hz or 60Hz) transformers in figure 2 play an important role in stepping down/up the voltage and in ensuring galvanic isolation between the two feeders. Especially, galvanic isolation is desirable to prevent a zero-sequence current circulating between the two feeders. However, one 6.6kV, 1MW transformer weighs approximately 3,000kg to 4,000kg, and may be too heavy to be mounted on an electric pole. Actually, the solution with the transformers results in a large volume and occupy a big part of the conversion system. Furthermore, the costs are quite high due to rising prices for raw materials. As a consequence, a new topology is under investigation substituting the two line-frequency transformers. The present BTB system with two three-phase, line frequency transformers will be replaced by the next-generation BTB system given in **fig-**

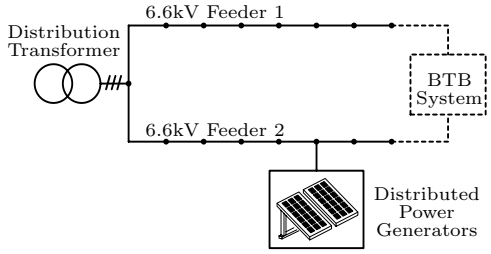

Fig. 1. A 6.6kV distribution system in Japan having two feeders.

* Based on "'Bi-Directional Isolated DC-DC Converter for Next-Generation Power Distribution - Comparison of Converters using Si and SiC Devices"', by D. Aggeler, J. Biela, S. Inoue, H. Akagi, J. W. Kolar which appeared in the proceedings of the 2007 Power Conversion Conference - Nagoya, (c) 2007 IEEE.

* ETH Zurich, Power Electronic Systems Laboratory
Physikstrasse 3, 8092 Zurich, Switzerland
** Tokyo Institute of Technology, Department of Electrical and Electronic Engineering
Tokyo, Japan

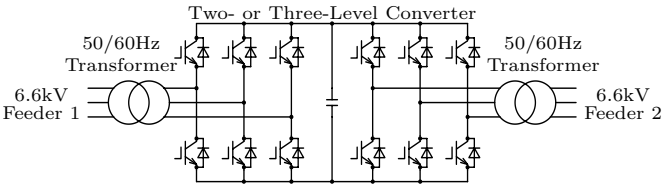

Fig. 2. The present BTB system for the 6.6kV power distribution system.

ure 3. There it is shown, that a BTB system in the next-generation consists of a number of converter cells which in each case consists of a rectifier/inverter stage and a DC-DC converter. The galvanic isolation of the proposed BTB system is guaranteed by a high frequency (HF) transformer. Due to the high operating frequency the volume and the weight of the passive components is reduced very much compared to the line-frequency transformers.

For the design of the full bridge converter different device technologies can be used: on the one hand a realisation with Si IGBT devices [2] and on the other hand with SiC JFET components provided by SiCED [3]. In the following a galvanic isolated BTB system with SiC will be designed, according the specification parameters given in **table** 1 and compared with the Si system of [2].

In **section** 2 the operation principle of the next-generation BTB system solution is summarised shortly. The following **section** 3 focuses on the DC-DC converter with SiC JFET cascodes. There, the converter specifications, the dual active bridge (DAB) as well as the high voltage (HV) SiC switch are explained. In **section** 4 experimental results of the SiC JFET cascode and the design of the HV-HF transformer based on analytic calculations and FEM simulations are presented. Furthermore, a 3D-model of the proposed DC-DC converter is shown. **Section** 5 summarises the performance of the Si IGBT system presented in [2]. Thereafter, the possible solutions for a next-generation BTB system – Si IGBT and SiC JFET cascode – are compared for a 1MW system in **section** 6 and finally conclusions are drawn in **section** 7.

2. Next-Generation Medium Voltage BTB System

The next-generation BTB system (figure 3) consists of a rectifier/inverter stage and as the core circuit a bi-directional, galvanic isolated DC-DC converter, as shown in **figure** 4 (Si IGBT) or **figure** 5 (SiC JFET cascode), is applied.

The cascaded converter cells form a single-phase part of the BTB system where each converter cell consists of a DC-DC converter. The DC-link voltage in each

Table 1. Design requirements of the BTB system.

Input Voltage	6.6kV
Output Voltage	6.6kV
Rated Power	1MW
Current THD	5%
Each Harmonic	<3%

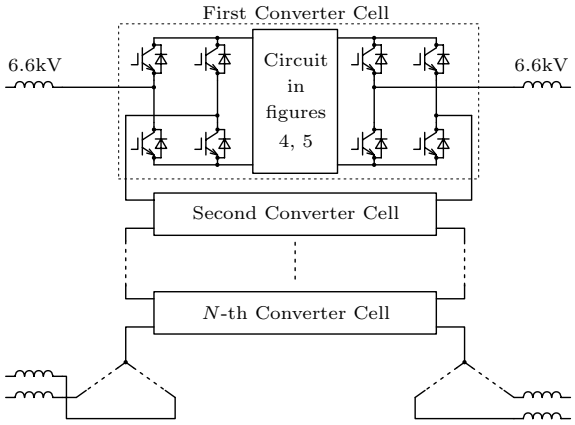

Fig. 3. A 6.6kV BTB system in the next generation.

converter cell depends on the number of cascade connections N. Hence, waveform levels, AC input voltages and DC-link voltages per converter cell are calculated, for a different number N of converter cells, and summarised in **table** 2.

The analysed Si IGBT system consists of six converter cells in each phase (N=6), what results in a DC-link voltage of 1.02kV in each cell, allowing to use 1.7kV IGBTs available at a lower cost than higher voltage Si devices. The application of several converter cells and phase shifted unipolar sinusoidal PWM of the rectifier/inverter stage, where the triangular carrier signal in one converter cell is phase shifted by π/N from each other, results in a multilevel waveform of the line-to-neutral voltage. Therefore, the equivalent switching frequency is $2Nf_c$, where f_c is the carrier frequency. As a result, the voltage waveform has ($2N$+1) levels with the switching frequency of $2Nf_c$. Thus, the carrier frequency of the PWM converters can be as low as 4kHz by six converter cells in each phase.

Table 2. Voltage and waveform levels depending on the number N of converter cells of a next-generation BTB system.

N	Waveform	AC Input	DC Link
1	3 Level	3,811V	6.10kV
2	5 Level	1,905V	3.48kV
3	7 Level	1,270V	2.03kV
4	9 Level	952V	1.52kV
5	11 Level	752V	1.22kV
6	13 Level	635V	1.02kV
7	15 Level	544V	870V
8	17 Level	476V	762V
9	19 Level	423V	677V

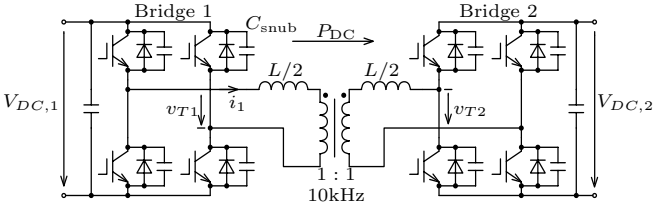

Fig. 4. A bi-directional isolated DC-DC converter.

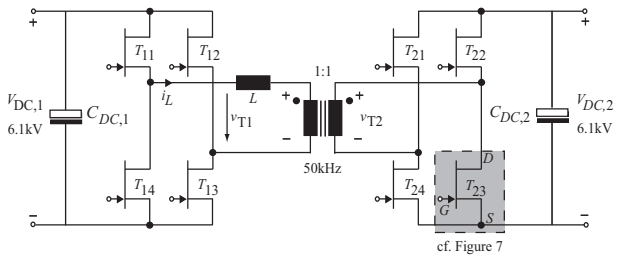

Fig. 5. SiC high voltage DC-DC converter.

The application of SiC JFET cascode devices for the DC-DC converter offer a HV blocking capability and thus only one converter cell (N=1) is required. Accordingly, a smaller number of power devices is utilised. While in the Si IGBT based design (N=6) the number of power devices is 288, for the SiC JFET cascode system 48 semiconductor devices are used. Due to the lower number of converter cells, in the SiC system a higher carrier frequency is needed.

3. Operation Principle of the SiC HV-HF-Converter

The proposed HV and HF DAB converter with SiC JFET cascode, replacing the conventional BTB system with the two line-frequency transformers, is shown in figure 5.

The specification of the SiC DAB converter is given in **table** 3. The design requirements for the distribution system given at a line-to-line voltage V_{AC} of 6.6kV (table 1), a DC-link voltage V_{DC} of 6.1kV (with 13% safety margin, table 2) is resulting. One goal of the next-generation BTB system is reduction in terms of size, especially of the passive components. A high switching frequency will result in smaller magnetic components/transformer but the HF losses increase considerable. For that reason the switching frequency of 50kHz is chosen to limit HF losses. Consideration of power controllability and a dynamical margin of continuous current flowing a rated power of 20kW is designed for the DAB. For transferring a bigger amount of power, devices must be connected in parallel to increase the continuous current capability. Furthermore, the transformer turns ratio is fixed because of the equal voltage level on both side of the distribution system.

3.1 Dual Active Bridge As modulation method the common phase shift operation is chosen for the DAB. The low computation complexity of the phase shift method, the simplicity of the circuit and the reduced power losses due to zero voltage switching (ZVS) are the main reasons for the wide application of this method. Characteristic of the DAB principle is the power transfer from the active bridge on the input side via the galvanic isolation (transformer) to the active bridge on the output side. There, the amount of transferred power is controlled by the phase shift angle ϕ [4],

$$P = \frac{V_{DC,1} V_{DC,2}/n \cdot \phi \cdot (\pi - \phi)}{2\pi^2 f_S L} \quad \cdots\cdots\cdots\cdots (1)$$

and the leakage inductance L is used as energy storing element. The variable n stands for the transformer turns ratio and f_S for the switching frequency.

Table 3. Specification of DC-DC converter.

DC-link Voltage	6.1kV
Switching Frequency	50kHz
Rated Power	20kW
Transformer Turns Ratio	1:1
Peak Inductance Current	7A
DC-link Voltage Ripple	$< 5\%$

The transferred power depends nonlinearly on the phase shift angle ϕ between the voltages v_{T1} and v_{T2} and is limited by the switching frequency and the leakage inductance. The minimal phase shift angle and with this the minimal controllable power step is given by the clock frequency of the control board. Depending on the nonlinear relation of power and phase shift angle, the biggest gradient is with a phase shift angle of zero degree. There, the maximal power step will appear respective the minimal controllable power at this point. With an increased phase shift angle, the power step will decrease and the controllable power will be smaller.

In [5] the active and reactive power are shown as a function of the phase shift angle. A high phase shift value will increase significantly the reactive part of the power and only a little bit the active power. Consequently, the efficiency of the converter is reduced. A small phase shift angle the control signal constrain the controllability of the power steps. Therefore, an operation in the phase shift interval of $[\frac{\pi}{4}, \frac{\pi}{3}]$ is favourable and chosen for the considered DAB.

In order to verify the operation of the DAB topology a simulation model was built for the specification given in table 3. There, only a simplified equivalent circuit of the HV SiC switch was used. An exact model, which describes static and dynamic behaviour of the HV switch in more detail is under investigation. **Figure** 6 shows the simulated transformer voltages v_{T1} and v_{T2} with the inductor current i_L, whereas the stray capacitance of the transformer is considered.

3.2 High voltage SiC switch As a result of the operation voltage, switches with a HV blocking capability are required. Thus, SiC JFET cascode are chosen because of the good material characteristics of SiC, as the low on-state losses and high frequency operation. Two different modules are applied: one contains four SiC JFETs, two connected in series and two in parallel. For controlling the switch additionally a low-voltage Si MOSFET is connected to the lower JFETs (A, figure 7). In the other module just two SiC JFETs are connected in series and two in parallel (B, figure 7).

The structure of the SiC JFET die is designed with a internal pn-junction from source to drain [6], which is working as the freewheeling diode of the SiC JFET. Thus, no external freewheeling diodes are required.

The gates of the JFETs are connected to additional diodes for passive controlling the turn-on and turn-off mechanism of each JFET. This diode is a low leakage fast recovery epitaxial diode (FRED) and is included in the SEMITOP package.

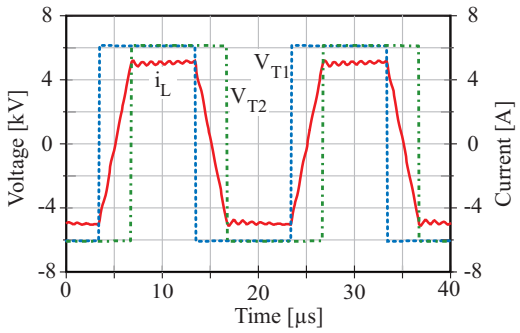

Fig. 6. Simulated waveforms for the phase shift mode at $V_1 = V_2 = 6.1$kV and $P_{Out} = 20$kW ($f_s = 50$kHz, $\phi = \pi/3$).

In order to achieve the required blocking voltage for the DC-link input voltage, multiple modules must be connected in series. Since the conventional JFET is a normally-on device a low-voltage Si MOSFET is connected in series to the JFETs. In the series connection the normally-off MOSFET allows a normally-off behaviour of the cascode and a control of the series switch by a standard gate drive circuit. Both modules are mounted in a SEMITOP package (**figure** 7) by Semikron International [7]. The ratings of the JFET are a blocking voltage V_{CES} of 1500V and a continuous drain current I_D of 8A.

The basic concept of the SiC JFET cascode switch is described in [8]. There, also the static blocking characteristics and the dynamic switching behaviour are discussed. In the on-state of the SiC JFET cascode, a positive gate voltage is applied to the MOSFET. Then, the gate of the lower JFET in the A module is connected to the source of the MOSFET and the JFET is conducting. Also the other in series connected JFETs are conducting due to its already mentioned normally-on characteristics. For this case the JFETs work as a resistor connected in series to the on-resistance of the MOSFET.

In the blocking state the MOSFET gate is shorted to the ground and the drain-source voltage of the MOSFET increases until the pinch-off voltage of the first JFET is reached. Further increasing of the MOSFET's drain-source voltage is now blocked by the first JFET, which is blocking the excess voltage, until the belonging Diode between the gate of the upper and the lower JFET reaches its avalanche blocking voltage. At this point the avalanche current is flowing and the gate of the second JFET drops down below its source potential. The gate-source voltage of the second JFET is negative and therefore in blocking state. For the next stages this process is iterative until the DC-link voltage is blocked.

4. Design of DC-DC converter

In the following the design of the SiC DC-DC converter for an output power of 20kW is presented. For calculating the switching and conduction losses measurement results for the SiC JFET are presented. Moreover, the design of the high voltage transformer will be discussed in detail and a 3D model of the converter is presented.

4.1 Experimental Results For an application in the distribution system with the specifications given in table 1 the HV switch consists of two modules B and one module A, resulting in a total blocking voltage of 9kV. There, a safety voltage margin is included for dynamic voltage balancing. In the following these three series connected modules are denoted as one HV switch.

For determining the switching and conducting losses an experimental setup as shown in **figure** 8 was built. There, also a simplified schematic is given. On the high voltage side the gate of the HV switch is connected to the source so that it works as freewheeling diode. The HV switch on the low voltage side is actively controlled by a gate driver.

In a first step single pulses for testing the turn-off behaviour with an inductive load at different current amplitudes have been acquired. With the measured current and voltage waveforms the ZVS turn-off losses of the DAB converter can be calculated. In a next step double pulse measurements will be performed in order to test also the turn-on behaviour of the SiC JFET devices.

The gate drive circuit is designed with a small transformer, which could withstand the 6.1kV DC-link voltage, for the gate drive power supply. Furthermore, the gate drive signal is transferred via fiber optic to the gate driver, where the standard MOSFET driver IXDI409SI

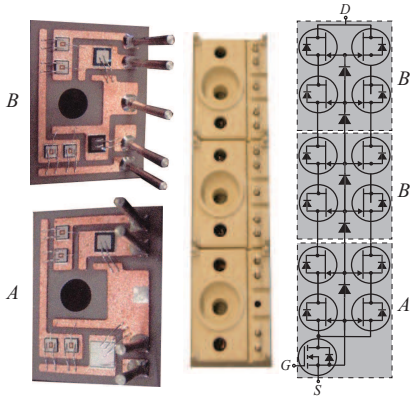

Fig. 7. SiC JFET cascode mounted in a SEMITOP package.

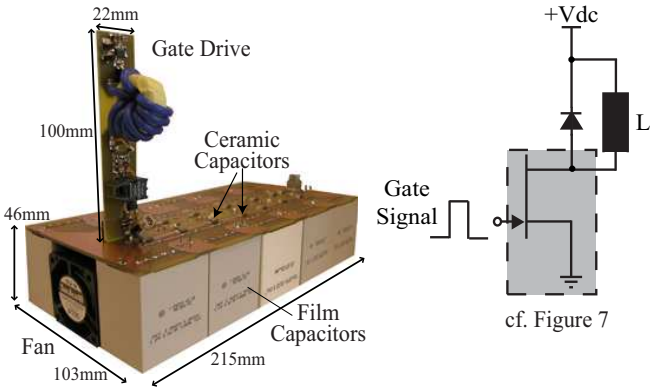

Fig. 8. Power loss measurement setup for the HV switch with the corresponding simplified schematic.

from IXYS is used. The gate-source voltage to turn the HV switch on is +12V. For turning the MOSFET off a negative gate-source voltage of -12V is used in order to reduced the influence of induced noise.

In the test circuit (**figure** 8) the HV switch is on the bottom side of the PCB between the film capacitors mounted on a heat sink behind the fan. Additionally, to the film capacitances ceramic capacitors are placed on the top side close to the switches in order to minimise the stray inductance and reduce voltage overshoot.

In **figure** 9 and **figure** 10 experimental results for the switching behaviour with a DC-link voltage of 5kV and a gate resistance of $R_{off} = 10\Omega$ for turning off and of $R_{on} = 0\Omega$ for turning on are presented. The measurements are made with high voltage probes from LeCroy and trimmed, isolated current transformers.

The turn-on current waveform in figure 9 of the HV switch shows a significant peak of capacitive current during the falling edge of the voltage. This usually would result in significant turn-on losses of the SiC JFET. In the DAB, however, the switch is operated under ZVS conditions what leads to negligible turn-on losses, since the parasitic capacitances are dis-/charged by the load current and the switches are turned on at zero voltage [9, 10].

In figure 10 the turn-off characteristic is shown. There, the current first decreases rapidly to half of the original drain current, stays constant and then falls down to zero. The total fall time of the current is approximately 80ns. The drain-source voltage V_{DS} rises within 70ns. This current shape reflects a capacitive turn-off behaviour (cf. figure 10).

The equivalent circuit during the ZVS turn-off is shown in **figure** 11. During the period (A) the load current flows through the low side HV switch. At turn-off, the current splits up into two capacitive currents (B). One is charging the lower capacitance which has a high value at low drain-source voltage. With increasing voltage the capacitance is decreasing due to the spreading space charge region. The second current is discharging the capacitance of the upper switch, which is increasing with increasing voltage. Finally, the load current flows through the freewheeling diode of the upper HV switch (C) and then in reverse direction through the n-channel as soon as the upper switch is turned-on. Due to this approximately capacitive turn-off behaviour (ZVS) the turn-off and also the turn-on switching losses are negligible.

There, the interlocking delay time must be larger than the rise time of the drain-source voltage in order to guarantee soft switching. In the considered case with a voltage of 5kV a interlocking time of at least 80ns results (depending on the load current and the ZVS range). For a constant load current this time will increase with higher DC-link voltages, since the parasitic capacitances must be dis-/charged by the load current.

In **figure** 12 the drain-source voltages for different load currents are shown at turn-off. There, the on time of the HV switch and the load was the same for all DC-link voltages. Since the parasitic capacitances of the JFETs and the load must be dis/-charged by the load current, the dv/dt increases with increasing load current. This results in a decreasing rise times of the HV switch voltage for increasing load current. At a DC-link voltage of 5kV the dv/dt is approximately $60\text{kV}/\mu s$ for turn on and $70\text{kV}/\mu s$ for turn off ($I_{Load} = 5\text{A}$, $R_{off} = 10\Omega / R_{on} = 0\Omega$).

During the switching tests several voltage balancing diodes (FRED) of the integrated modules have been destroyed. This was caused due to excessive avalanche energies during the turn-off of the JFETs at rising voltages. Therefore, a discrete setup with a Si-MOSFET, SiC JFETs and Si-balancing diodes has been designed as shown in **figure** 13. Due to limitations of the current voltage source, measurements could be just performed up to 5kV, but the switching behaviour will be investigated at higher voltages with a new power supply in a future paper.

Besides the switching losses also the conduction losses are required for calculating the overall system losses. Therefore, the on-resistance $R_{DS,on}$ of the HV switch has been measured. The value is approximately 1.35Ω at $25°C$, which results in 18.7W conduction losses in forward direction per HV switch at 50kHz and a continuous load current of 4A. For higher temperatures this value must be multiplied by $(T_j/298)^{1.6}$, where T_j is the absolute junction temperature.

In the reverse direction the current first flows through

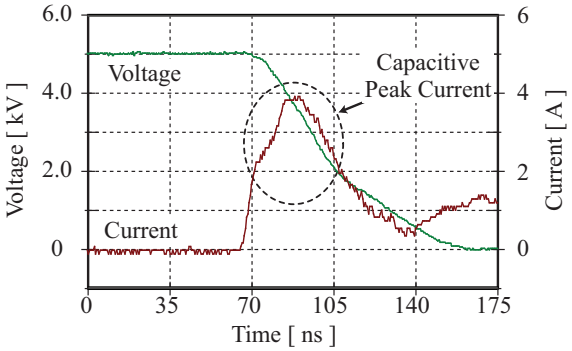

Fig. 9. Turn-on characteristic of the SiC HV switch: drain-source voltage and drain-source current.

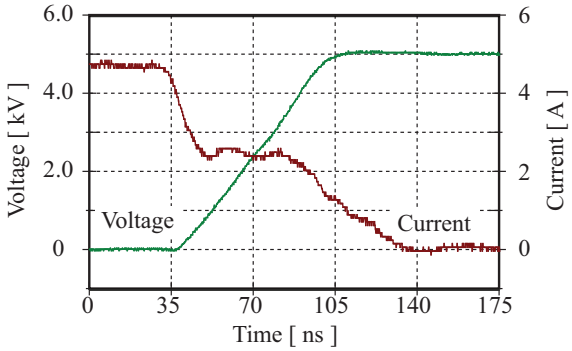

Fig. 10. Turn-off characteristic of the SiC HV switch: drain-source voltage and drain-source current.

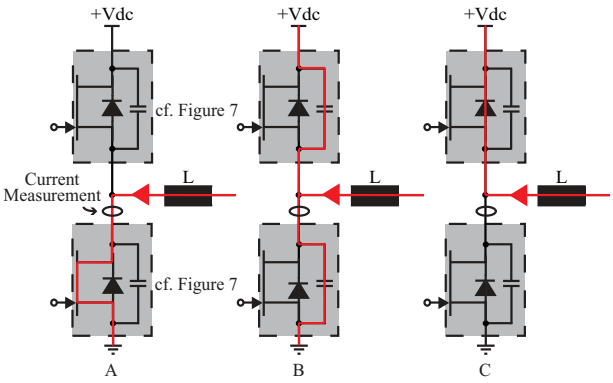

Fig. 11. Current flow during turn-off: A) HV switch is in on-state. B) Charge/discharge of capacitors. C) High side diode is conducting.

the antiparallel diodes of the MOSFET and of the JFETs. The forward voltage of the intrinsic antiparallel JFET diodes is in the range of 4V at a current of 4A. This would lead to relatively large conduction losses during the freewheeling period. However, as soon as the MOSFET and the JFETs are turned on the current could also flow in reverse direction through the n-channel of the MOSFET/JFETs which has a resistance in the range of 1.35Ω what results in much lower reverse conduction losses. These are 3.7W per HV switch for conducting MOSFET/JFETs and 0.39W for the short period where the freewheeling diodes are conducting.

4.2 High Voltage - High Frequency Transformer In the next-generation BTB system the line-frequency transformer should be replaced by a HV transformer operating at HF. Each DC-DC converter in the BTB system uses one transformer which also ensures the galvanic isolation between the input and output stage. The HV-HF transformer is one of the core elements in DAB operation considering power transfer and efficiency of the whole DC-DC converter. The phase shift operation mode of the DAB defines the requirements of the transformer, which will be designed in the following for an output power of 20kW and a phase shift angle between $\frac{\pi}{4}$ and $\frac{\pi}{3}$. Due to the HF operation ferrite material must be used for the core and the HF losses in the windings must be considered.

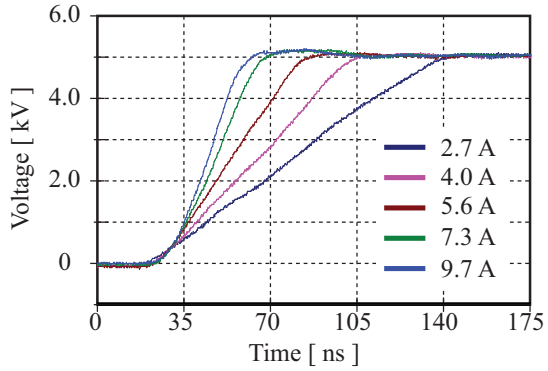

Fig. 12. HV SiC switch turn-off behaviour for different load currents.

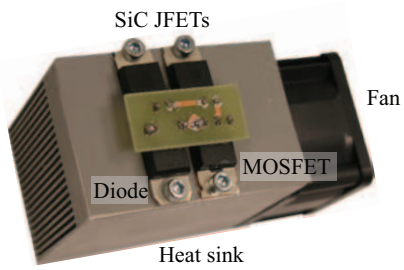

Fig. 13. High-voltage SiC switch built with discrete components.

For calculating the core losses Van den Bossche's [11] loss model of ferrites cores, considering non-sinusoidal waveforms, is used and compared to the losses resulting with the conventional Steinmetz equation and with also the modified Steinmetz equation [12]. The values of the loss models do not differ significantly and for the considered design the worst case value is used.

Based on these equations different ferrite materials have been examined. There, it turned out that the N87 material from Epcos has the lowest core losses at the specified switching frequency of 50kHz and a maximal flux density of 150mT. The core selection results in four UU93/152/30 cores, where the primary and secondary winding are wounded around the middle leg as shown in the 3D-Model (**figure** 16) of the 20kW DC-DC converter system. For choosing the number of turns and also the flux density in the core different designs have been compared. There, it turned out that with 120 turns on the primary and on the secondary winding the lowest overall losses occur. In this operating point also the core and the HF losses in the windings are approximately balanced.

For guaranteeing a high isolation voltage the distance between the windings and also between the winding and the core must be large enough and some high voltage isolating material must be used for the bobbin. Furthermore, the winding should be covered by an isolating material at the outer side between the winding and the core. The insulation of the wire itself must be capable of withstanding at least voltage between the different layers of the winding. These requirements significantly influence the winding arrangement of the transformer. In **figure** 14 a possible arrangement, which fulfils the above mentioned requirements, is shown.

There, each winding is distributed into three chambers in order to reduce the layer voltage and the para-

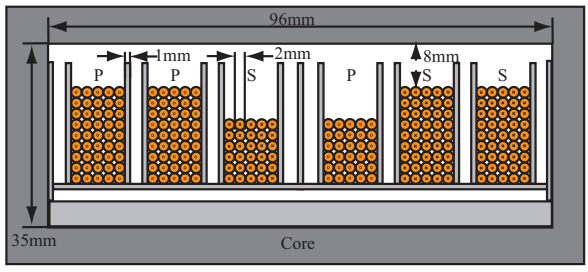

Fig. 14. Arrangement of the transformer windings.

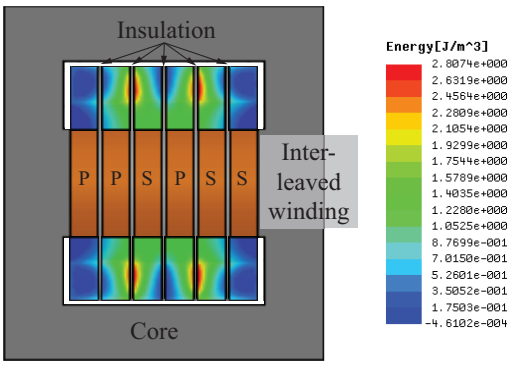

Fig. 15. Energy density in a cut plane through the core determined by a 3D FEM simulation with Maxwell^{TM} of the specified transformer as shown in figure 14.

sitic capacitance of the transformer [13]. This results in a relatively low layer voltage, what is important for the high frequency operation with high dv/dt-values. The fast edges of the voltage leads to a non uniform voltage distribution between the single turns of one winding and to higher turn voltages at the ends of the winding during high dv/dt. This is like charging a transmission line with a voltage pulse where a wave travels along the line until a uniform distribution is reached. This effect will be examined in detail in a future paper.

Another advantage of the higher number of chambers is an interleaving of the windings which could be used for reducing the HF losses in the windings or to control the leakage inductance of the transformer. In the considered case the two inner chambers are interleaved, i.e. primary and secondary chamber are exchanged and a sequence: primary - primary - secondary - primary - secondary - secondary chamber results (cf. figure 14). The two chambers in the middle of the winding window have less turns than the outer ones. Instead of 9 layers and 5 turns per layer, only 6 layers and 5 turns. With this arrangement a leakage inductance of approximately 4mH – calculated by 3D FEM simulations with MAXWELL^{TM} (cf. **figure** 15)– results. This inductance is required for transferring the rated power of 20kW at the optimal phase shift angle of $\pi/3$. Thus, no additional external inductor is needed and the power density of the system increases.

In conventional windings the layers are wound from the left to the right and then back in the next layer (S- or U-winding). There, the maximum voltage between two consecutive layers is twice the layer voltage – in the considered case maximal $500V$. This relatively high layer-to-layer voltage could be divided by two with a Z-winding, where each layer is wound in the same direction, i.e. for example all layers are wound from left to right. In this case the wire must be returned to the beginning of the layer outside the chamber in order to avoid a crossing of all wires of the considered layer. In order to guarantee a high isolating voltage also for the returning wire also the middle leg of the core is surrounded by an insulation. In **table** 4 the transformer design characteristics are summarised.

Table 4. Characterization of the HV-HF transformer.

Material	N87
Turn Number	120
Turn Ratio	1:1
Transferred Power	20kW
Core Losses ($25°C$)	35W
($100°C$)	15W
HF Losses ($25°C$)	24W
($100°C$)	30W
Leakage Inductance	3.4mH
Main Inductance	215mH
Magnetising Current	283mA
Specified max. Flux Density	150mT
Effective Cross Section	3360mm^2
Effective Volume	1188cm^3

For reducing the influence of skin- and proximity effects litz wire with 315 strands/strand diameter of 0.071mm, a total external diameter of 2.01mm and 1.27mm^2 cross section is used.

4.3 Rectifier/Inverter Besides the DC-DC converter also single phase PWM converters in the input (rectifier) and output (inverter) stage of the BTB system are required. There, also the HV SiC cascodes is applied as switching device in order to reduce the switching losses and the number of series connected stages. The selection of the switching frequency is a trade-off between switching/HF-/capacitor losses and the size of the input/output inductance. With the relatively low switching losses of the SiC cascode a switching frequency of 50kHz is achievable what results in small passive components.

The required capacitance for a voltage ripple $v_{DC,link,pp}$ of less than 5% of the DC-link voltage $V_{DC,link}$ can be calculated [14] by

$$C_{DC,min} = \frac{P}{V_{DC,link} \cdot \omega \cdot v_{DC,link,pp}}, \cdots\cdots\cdots (2)$$

where P is the nominal power and ω is the line-frequency. For dimensioning the input/output inductor a maximal admissible current ripple of 5% of the nominal current amplitude $I_{N,i}$ is assumed. Therefore, a minimal inductance L (cf. figure 5) of

$$L = \frac{V_{DC,link}}{f_S\, 8 \cdot 5\%\, I_{N,i}} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (3)$$

is required, where f_S again is the switching frequency.

With the specifications for the 20kW system in table 3 a capacitance value of 34.2μF and an input/output inductance value of $L = 41$mH (cf. figure 3) results.

4.4 3D-Model of DAB converter In order to achieve a small volume of the system a compact layout of the DAB converter is required. Accordingly, an optimal placement of the components is essential. A 3D-model of the DC-DC converter is shown in figure 16 with an approximated power density of 1.9kW/dm^3 and the power per kilogram is 1.39kW/kg.

The DC-link capacitor is realised with electrolytic capacitor banks which consist of Epcos 450V/33μF capacitors. Between the two capacitor banks on the input and

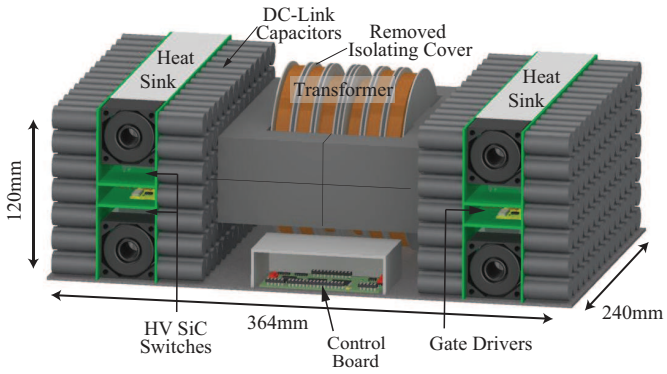

Fig. 16. 3D-model of the high voltage, high frequency DC-DC converter featuring SiC JFET cascode (removed isolating cover of transformer winding).

output side of the DC-DC converter the full bridge with four HV switches mounted on two heat sinks with fans is located. The gate drive circuits of the SiC JFET cascodes including auxiliary supply are mounted in between the upper and the lower heat sink. There, additionally high voltage ceramic capacitors are placed close to the modules for reducing the stray inductance. The control circuit for the DC-DC converter and its supply could be mounted below the transformer in a EMI protective housing.

5. Losses of Si System

The comparative system with latest trench-gate Si IGBTs, evaluated in [2], operates with a switching frequency of 20kHz, at a rated power of 10kW and with a DC-link voltage of 350V. An experimental setup was built and measurements results were presented. Based on this the overall loss have been determined and a loss analysis was performed.

The specified application is the same as for the SiC system and is also based on the specification parameters of table 1. A summary of the determined power component losses and magnetic losses of the Si System and also of the SiC system are given in **table** 5.

Table 5. Power losses based on measurements and simulations of the Si IGBT system and the SiC JFET system. (Inductor losses of the SiC-system are included in the transformer losses, since the inductance is realised by the leakage inductance of the transformer.)

	Si-IGBT (**10kW**)		SiC-JFET (**20kW**)	
	Core Loss	HF Loss	Core Loss	HF Loss
Transformer	20W	18W	35W	24W
Inductor	9W	10W	-	-
	Switching	Conduction	Switching	Conduction
Switch Losses	90W	189W	$\sim$ 0W	90W
Total Losses	336W		149W	

6. Comparison Si IGBT system - SiC JFET system

In the previous section, the losses for the Si and the SiC system have been evaluated based on measurement results. There, it could be seen that the SiC material shows a better performance in comparison to the conventional Si material. In general, the achievable current density, the operating temperature and the breakdown voltage are higher and the switching and conduction losses are lower. The drawback of the SiC material are the limited current carrying capability (limited die size) and the high price due to higher manufacturing costs for the SiC wafers/processing costs at the moment.

With the results for the 10kW/20kW system, a system with the specifications given in table 1 for a BTB system of the distribution system in Japan at a rated power of 1MW could be designed. Therefore, the Si IGBT system [2] and the SiC JFET cascode system are scaled up to this power level and are compared with respect to power losses, the performance and the efficiency in the following. The differences between the two converter systems are on the one hand the applied core materials and on the other hand the semiconductor devices. Due to the different semiconductor materials different switching frequencies and voltage levels result. In **table** 6 the parameters of the scaled systems, referred to a transferred power of 1MW, are summarised.

A significant advantage of the SiC JFET switch is the high blocking voltage what results in only one converter cell per phase for a distribution system operating with an AC line-to-line voltage of 6.6kV. In the Si system, applying commercial 1.7kV IGBTs, six in series connected converter cells in each phase are required to adapt the voltage to the blocking capability of the Si DC-DC converter. The benefit of the larger amount of series connected stages is, that the number of switching levels is higher and therefore a smaller input/output inductance of the inverter/rectifier stage is required.

To transfer a rated power of 1MW fifty 20kW SiC DC-DC converters, as presented in this paper, must be connected in parallel and none of them in series. Due to the lower power rating of the Si DC-DC converters this number must be doubled for a 1MW Si system and because of the lower DC-link voltage (1.02kV) six Si DC-DC converters are connected in series and also in parallel per phase. Resulting is a large number of power component devices in the Si system.

The conduction losses of the Si IGBT system are dominated by the current flowing through the switch at

Table 6. Performance of the Si and SiC DC-DC converters linear scaled for the 1MW systems. (L_σ is the leakage inductance of the transformer.)

	Si-IGBT	SiC-JFET
Number of Converters	100	50
Switching Frequency	20kHz	50kHz
Conducting Losses	18.9kW	4.5kW
Switching Losses	9kW	$\sim$ 0W
Transformer Core Losses	2kW	1.42kW ($50^\circ C$)
Transformer HF Losses	1.8kW	1.3kW ($50^\circ C$)
Inductor Core Losses	900W	Integrated in L_σ
Inductor HF Losses	1kW	Integrated in L_σ
Efficiency	97%	99%

the nominal operating point of 10kW. With a voltage drop of 5.9V and a RMS current of 32A, across two IGBTs and two diodes, conduction losses of 189W, respectively 18.9kW for the scaled 1MW system result. A single HV SiC switch is operating at a rated current of 4A (corresponding to 200A in the 1MW system) what leads to smaller conduction losses. With a measured on-resistance of 1.4 Ω per HV switch 4.5kW conduction losses results for the 1MW system.

Due to ZVS conditions in both systems the switching losses could be reduced. The measured switching losses in the Si system are 9kW, whereas the losses in the SiC system can be neglected due to the fast switching of the JFET and the relatively large output capacitance.

In the Si system Finemet FT-3M magnetic material is used for the transformer and the ferrite material PC44 for the inductor. Especially, Finemet allows a high saturation magnetic flux density of 1.2T at a temperature of $100°C$ and shows a small temperature dependence at a range from $25°C$ to $150°C$. In the SiC converter system the material N87 from Epcos was applied. There, an external inductor is not needed any more, because the transformer was designed with the necessary leakage inductance to transfer the rated power. This solution allows a further reduction of the system volume and weight and also the magnetic losses.

7. Conclusion

In this paper a bidirectional DC-DC converter based on high voltage SiC JFETs for a 1MW next-generation back-to-back system of a distribution system is presented and compared to a conventional Si system. For validating the considerations a 20kW system operating at a switching frequency of 50kHz with a DC-link voltage of 6.1kV has been examined in detail and scaled up to 1MW. Based on a 3D CAD construction a power density of 1.9kW/dm^3 - 1.39kW/kg for the DC-DC converter has been determined.

As integral part of the converter system also a 20kW/50kHz high voltage HF transformer with increased leakage inductance for the dual active bridge has been designed by analytical calculations and 3D FEM simulations. The power density of the transformer is 5.9kW/dm^3 and 2.7kW/kg.

For measuring the switching waveforms and the switching losses a high voltage test system has been constructed. Due to the fast switching of the JFETs, the relatively large output capacitance and the ZVS operation of the DAB the switching losses are approximately negligible. With an on-resistance of 1.4Ω 90W conduction losses per 20kW DC-DC converter result. Due to limitations of the current power supply the switching losses have been measured only up to 5kV. Measurements at higher voltages with a new supply will be presented in a future paper.

In the comparison of the scaled 1MW Si and SiC systems the good material characteristic of SiC and the resulting high operating frequency lead to a compact and low loss system with an efficiency of approximately 99% in contrast to 97% of the Si system.

References

(1) N. Okada, "'Control of loop distribution network and result,"' Technical Meeting on Power Systems Engineering, IEEJ, 2000.

(2) S. Inoue and H. Akagi, "'A bi-directional isolated dc/dc converter as a core circuit of the next-generation medium-voltage power conversion system,"' IEEE Power Electronics Specialists Conference (PESC), 2006.

(3) http://www.siced.de

(4) F. Krismer, S. Round, and J. W. Kolar, "'Perfomance optimization of a high current dual active bridge with a wide operating voltage range,"' Proc. 37th Power Electronis Specialists Conference, Jeju, Korea, June 18 - 22 2006.

(5) N. Schibli, "'Symmetrical multilevel converters with two quadrant DC-DC feeding,"' PhD. Thesis, ETH Lausanne, 2000.

(6) B. Weis, M. Braun, P. Friedrichs, "'Turn-off and short circuit behaviour of 4H SiC JFETs,"' Industry Application Conference, Vol. 1, pp. 365 - 369, 30 Sept. - 4 Oct. 2001.

(7) http://www.semikron.com

(8) R. Elpelt, P. Friedrichs, R. Schorner, K.-O. Dohnke, H. Mitlehner,and D. Stephani, "'Serial connection of SiC VJFETs - features of a fast high voltage switch,"' REE. Revue de l'Electricite et de l'Electronique, No. 2, pp. 60-68, Feb. 2004.

(9) G.G. Oggier, R. Ledhold, G.O. Garcia, A.R. Oliva, J.C. Balda, F. Barlow, "'Extending the ZVS Operating Range of Dual Active Bridge High-Power DC-DC Converters,"' 37th IEEE Power Electronics Specialists Conference (PESC'06), 2006.

(10) N. Mohan, T.M. Undeland, W.P. Robbins, "'Chapter 9.6 in Power Electronics - Cpnverters, Applications and Design,"' 3rd edition, John Wiley and Sons, 2003.

(11) A. Van den Bossche, V. C. Valchev, and G. B. Georgiev, "'Measurement and Loss Model of Ferrites with Non-sinusoidal Waveforms,"' 35th Annual IEEE Power Electronics Specialists Conference, Aachen, Germany, Vol. 6, pp. 4814-4818, June 2004.

(12) J. Reinert, A. Brockmeyer, and Rik W. A. A. De Doncker, "'Calculation of Losses in Ferro- and Ferrimagnetic Materials Based on the Modified Steinmetz Equation,"' IEEE Transactions on Industry Applications, Vol. 37, No. 4, July/Aug. 2001.

(13) J. Biela, J.W. Kolar, "'Using Transformer Parasitics for Resonant Converters - A Review of the Calculation of the Stray Capacitance of Transformers,"' Conference Record of the 2005 IEEE Industry Applications Conference 40th IAS Annual Meeting, Hong Kong, China, Oct. 2 - 6.

(14) R. D. Greul, "'Modulare Dreiphasen-Pulsgleichrichtersysteme,"' PhD. Thesis, ETH Zurich, 2006.

Juergen Biela (Non-member) was born in Nuremberg, Germany, on July 12, 1974. He studied electrical engineering at the Friedrich-Alexander-Universitt Erlangen. During his studies he dealt in particular with resonant DC-link inverters at the Strathclyde University, Scotland and the active control of series connected IGCTs at the Technical University of Munich, Germany. After he had received his diploma degree with honours from FAU Erlangen in 2000, he worked on inverters with very high switching frequencies, SiC components and EMC at the research department of A&D Siemens, Germany. From July 2002 to Dec. 2005 he has been a Ph.D. student at the PES, ETH Zurich. Since 2006 he is working as PostDoc there and his research is focused on compact DC-DC converter, magnetic components, pulsed power systems and system optimisation.

Daniel Aggeler (Non-member) was born on April 22, 1981.

He studied electrical engineering at the ETH Zurich. During his studies, he dealt with power electronics and control engineering. His master thesis research involved control strategies (harmonic elimination, direct power control) for 3-level grid connected inverters. Since 2006, he is Ph.D. student at the PES, ETH Zurich, and his current research is focused on high voltage, dual active bridge dc-dc converters featuring SiC components.

Shigenori Inoue (Member) was born in Fujimi, Saitama, Japan, on January 29, 1979. He received B.S. and M.S. degrees from the Tokyo Metropolitan University, in 2002 and 2004, respectively, and the Ph.D. degree from the Tokyo Institute of Technology in 2007. He is currently a Research Fellow with the Japan Society for Promotion of Science (JSPS). His research interests include medium-voltage power conversion systems, bidirectional isolated dc-dc converters, SiC/GaN-based power devices, and active power filters.

Hirofumi Akagi (Member) was born in Okayama, Japan, in 1951. He received the B.S. degree from the Nagoya Institute of Technology, Nagoya, Japan, in 1974, and the M.S. and Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1976 and 1979, respectively, all in electrical engineering. In 1979, he joined the Nagaoka University of Technology, Nagaoka, Japan, as an Assistant and then Associate Professor in the Department of Electrical Engineering. In 1987, he was a Visiting Scientist at the Massachusetts Institute of Technology (M.I.T.), Cambridge, for ten months. From 1991 to 1999, he was a Professor in the Department of Electrical Engineering, Okayama University, Okayama, Japan. From March to August 1996, he was a Visiting Professor at the University of Wisconsin-Madison and then M.I.T. Since January 2000, he has been a Professor in the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. He has published some 70 IEEE Transactions papers and two invited papers in the Proceedings of the IEEE. He has made presentations many times as a Keynote or Invited Speaker internationally. His research interests include power conversion systems, ac motor drives, high-frequency resonant inverters for induction heating and corona discharge treatment processes, and utility applications of power electronics such as active filters for power conditioning, self-commutated BTB systems, and FACTs devices.

Dr. Akagi received two IEEE IAS Transactions prize paper awards in 1991 and in 2004, two IEEE PELS Transactions prize paper awards in 1999 and in 2003, nine IEEE IAS Committee prize paper awards, the IEEE William E. Newell Power Electronics Award in 2001, and the IEEE IAS Outstanding Achievement Award in 2004. He was elected as a Distinguished Lecturer of the IEEE Industry Applications and Power Electronics Societies for 1998-1999. He currently is President of the IEEE Power Electronics Society.

Johann W. Kolar (Member) studied industrial electronics at the University of Technology Vienna, Austria, where he also received the Ph.D. degree (summa cum laude). From 1984 to 2001 he was with the University of Technology in Vienna, where he was teaching and working in research in close collaboration with the industry. He has proposed numerous novel converter topologies, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter concept. Dr. Kolar has published over 200 scientific papers in international journals and conference proceedings and has filed more than 50 patents. He was appointed Professor and Head of the Power Electronics Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001. The focus of his current research is on ultra-compact intelligent AC-AC and DC-DC converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and active EMI filtering, multi-disciplinary simulation, bearing-less motors, power MEMS, and wireless power transmission.