# Solid-State Transformer based on SiC JFETs for Future Energy Distribution Systems

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## I. Introduction

In order to reduce the emission of greenhouse gas and replace the limited energy sources like coal, oil or uranium, the number of renewable energy sources is constantly growing. This development results in a rising number of distributed power plants, which are principally subject to substantial energy fluctuations. In order to easily connect the new energy sources to the grid and improve the power quality by harmonic filtering, voltage sag correction and highly dynamic control of the power flow new power electronic systems - so called Intelligent Universal / Solid-State Transformers (SST) - are required. These interconnecting devices would enable full control of magnitude and direction of real and reactive power flow and could replace not controllable, voluminous and heavy line frequency transformers. Based on such devices a smart grid comparable to the internet, where a plug and playconnection of sources and loads, distributed energy uploads and downloads and energy routing for transferring energy from the producer to the consumer, is possible.

In the top of **Fig.**1 a conventional interconnecting system based on a back-to-back (BTB) converter and slow IGBT devices is shown. This system consists of ac-dc/dc-ac converters and two line-frequency transformers, which provide galvanic isolation as well as voltage level conversion and which have a large volume and weight. In order to decrease the volume/weight of the system and reduce the raw material consumption new topologies [1]–[3], which replace the line frequency transformers by high frequency and high voltage transformers, have been proposed. These proposals are also based on IGBT devices, which significantly limit the feasible switching frequencies and the voltage level of the converter systems. In order to overcome these limits, new converter systems (cf. A, B & C in Fig.1) based on high voltage SiC JFETs cascades, which enable a much higher power density and a significantly higher system dynamic are presented in **Section**II of this paper. Furthermore, these systems require a lower number of converter stages, what results in lower system costs and a higher reliability.

In **Section**III a 5kV/50kHz bi-directional, isolated dc-dc converter, which is a key element of the solid-state transformers, is discussed in detail. There the switching behaviour of the SiC switches, the design of the transformer and the achievable performance of the dc-dc converter are presented. Finally, the system parameters of a 1MW solid-state transformer based on the SiC dc-dc converter are calculated and the performance of the different topologies with respect to power density, efficiency and realisation effort is compared in **Section**IV.

## II. Topologies for Solid-State Transformers

In Fig.1 three different topologies for realising a solid state transformer by applying a high-frequency (HF) and high voltage (HV) single phase transformer are shown. All of the concepts consist of a rectifier/inverter stage and a HF/HV dc-dc converter. Due to the high operating frequency the volume and the weight of the isolating transformer becomes very small in comparison to line frequency based concepts. In order to limit the switching losses at the high frequencies switches based on SiC JFETs, which switch several kilovolts in less than 100ns, are applied. With these devices operating frequencies of several tens of kilohertz are possible. A blocking voltage in the range of several kilovolts is achieved by a series connection of JFETs (Super Cascode). There, the voltage balancing between the single devices is crucial and could be achieved by connecting small resistors/capacitors between the gate and the source of the single JFETs as will be explained in more detail in section III.

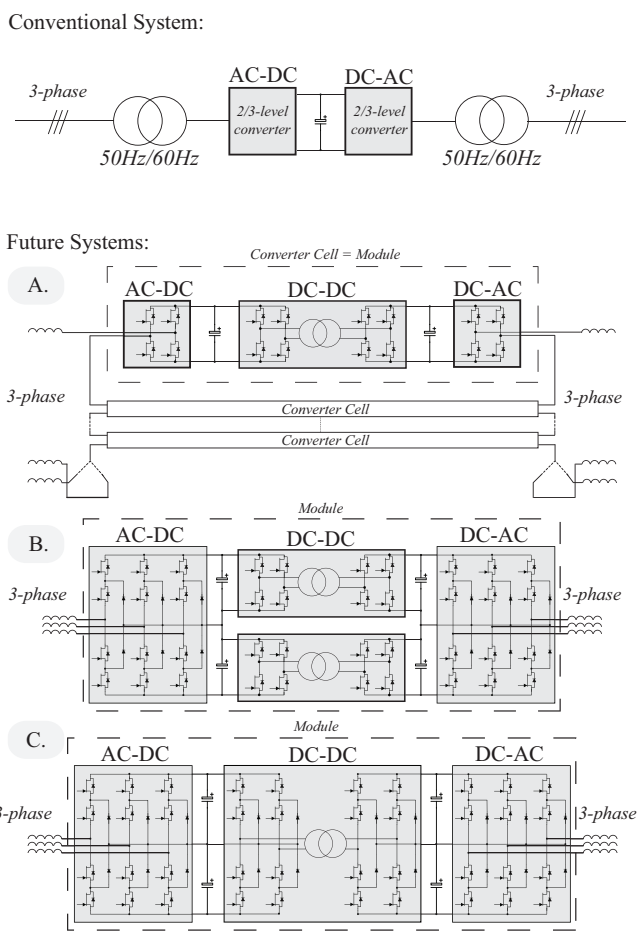


Fig. 1: Conventional system with the bulky line frequency transformer; Future solid-state transformers: A. single-phase modular converter cells, B. 3-level converter/inverter and 2-level dc-dc converter, C. 3-level topology system design.

Based on the Super Cascode in topology A a 2-level single phase inverter/rectifier stage and a 2-level dc-dc converter are combined in a converter cell. In order to reduce the required blocking voltage of the semiconductors several cells are connected in series. Furthermore, the three converter branches are star connected. With this concept SSTs for medium voltage level (11-35kV) applications can be realised.

Based on the available switches also a direct 3-phase topology as shown in Fig.1 B and C could be used for AC voltages up to 10kV. Due to the reduced number of required switches the system costs reduce and the reliability increase. There, a 3-level boost rectifier/inverter stage is applied, which allows higher operating voltages than a 2-level concept. In topology B the DC link is split up, so that a series connection of two 2-level dc-dc converter as in topology A is possible. There, the balancing of the two dc voltages is possible with the proper control of the AC-DC stage. In topology C 3-level branches are also utilised in the dc-dc converter so that a single dc-dc converter cell is sufficient.

In the final paper a detailed comparison of the topologies and

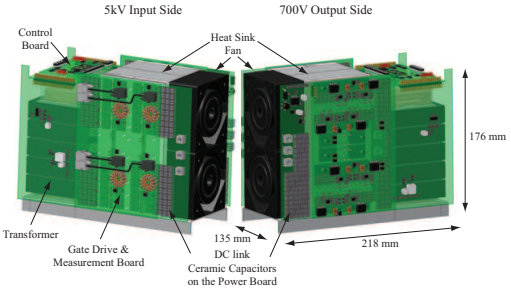


Fig. 2: 3D-Model of the proposed dc-dc converter.

concepts based on 3-phase transformers, which allow a further volume reduction, as well as the achievable system performance with a 30kV SiC switch are presented.

## III. 5 kV/50 kHz Bi-Directional DC-DC Converter

A key element of all topologies is the HF/HV dc-dc converter, which enables a significant volume reduction of SSTs compared to line frequency concepts. Therefore, the design and the performance of a 25kW converter operating at a DC link voltage of 5kV and an operating frequency of 50kHz is discussed in detail in the following. In Fig.2 a 3D model of the system is depicted, which has a power density of 4.8kW/ltr. and an efficiency of 97%. There, a SiC SuperCascode with a blocking voltage of 7.5kV and a transformer based on ferrite, which are explained in the following, are applied.

### *A. SiC Super Cascode*

The SiC Super Cascode consist of a low-voltage Si MOSFET, a SiC JFET cascade, whereas the number of series connected devices depends on the blocking voltage, and the gate diodes for voltage balancing and turning the upper JFETs on and off. The basic operating principle of the SiC Super Cascode is described in [4] and the concept for voltage balancing is derived in [5]. In Fig.4 the measured switching waveforms for an operating voltage of 5kV and 5 cascaded 1500V JFETs are depicted, which show that the rise and fall times are below 100ns. This fast switching transition in combination with the ZVS switching condition drastically reduces the switching losses. In the final paper simulation results for a 30kV switch based on 6.5kV JFETs will be presented, which significantly extends the useable power and voltage range of this concept.

### *B. 50 kHz-5 kV Transformer*

Besides stable and fast operation of the SiC SuperCascode, the design of the integrated HF/HV transformer (cf. Fig.4 is very important for the SST. Due to the high operating frequencies the HF losses in the windings must be limited by a careful design, so that the efficiency of the transformer is high and its volume low. Furthermore, the very step voltage transitions, which are required for the reduction of the switching losses, result in a non uniform voltage distribution within the winding during and shortly after the rising/falling edges. In the final paper the detailed design of the transformer and the calculated transient voltage distribution are presented.

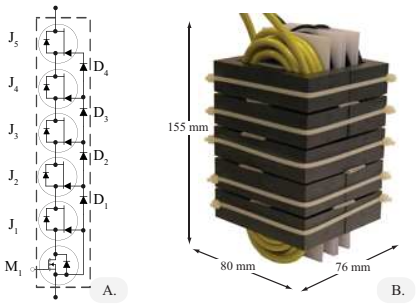


Fig. 3: A.: SiC JFET/Si MOSFET Cascade - Super Cascode. B.: 5 kV/50 kHz transformer.

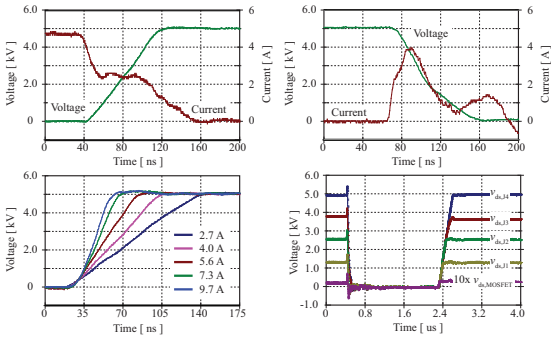


Fig. 4: SiC Super Cascode characteristics: Turn on and turn off behaviour (at different current), voltage distribution.

## IV. 1 MW Smart BTB System (modular built)

For comparing the different topologies and relating it to the existing line frequency concepts a detailed performance analysis of the proposed BTB conversion systems with SiC SuperCascodes and the performance of a 1 MW system will be presented in the final paper(**Table**I estimated).

| Topology | A. | B. | C. |
|---|---|---|---|
| Switching Frequency | | 50 kHz | |
| Number of Modules | 40 | 20 | 20 |
| Volume/Module [$dm^3$] | 6.3 | 13.5 | 13.6 |
| Number of SiC Super Cascodes/Module | 16 | 40 | 40 |
| Total Switch Losses [kW] | 27 | 34 | 34 |
| Transformer Losses [kW] | 2.4 | 2.4 | 2.4 |
| Efficiency [%] | 97 | 96 | 96 |

TABLE I: Performance of a 1 MW system based on the measurement and design results of the bi-directional dc-dc converter.

## V. Conclusion

In this paper three new topologies for solid-state transformers (SST) based on SiC Super Cascodes are presented and compared. Furthermore, a detailed analysis of the design and the performance of a 5kV/50kHz dc-dc converter with a power density of 4.8kW/ltr., which is a core element of the SSTs, is presented. There, also the operating principle of the Super Cascode and voltage balancing methods as well as the detailed design of the high voltage transformer are explained. Based on these results the parameters of a 1MW SST, which shows an efficiency of approximately 97% and a volume of $0.27m^3$, are derived and discussed.

## References

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