An Optimized 5 kW, 147 W/in^3 Telecom Phase-Shift DC-DC Converter with Magnetically Integrated Current Doubler

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***Abstract*— In the last decade there has been a tremendous growth in the number of data centers due to the increasing demand for internet services. At the same time, the cost for energy and materials have increased because of reducing resources and increased demand. That has caused a change in the driving forces for new power supply development, with more consideration on power density and efficiency.**

The commonly used DC-DC converter in the power supply unit (PSU) for data centers and telecom applications are full bridge phase-shift converters since they meet the demands of high power levels and concurrently efficient power conversion as well as a compact design. The constant operating frequency allows a simple control and EMI design.

To develop a new converter with higher power density and/or high efficiency the designer has a lot of degrees of freedom. An optimization procedure, based on comprehensive analytical models, has been developed and leads to the optimal parameters (e.g. switching frequency or transformer design) to achieve the most compact and/or efficient design.

In this paper an volume optimized 400 V/48 V phase-shift DC-DC converter with current doubler rectifier based on analytical models is constructed. The power density of the converter is increased by integrating the output inductors in the transformers core. The intrinsic voltage ringing of the rectifier diodes is damped by a lossless magnetic snubber, which feeds ringing energy to the output.

Experimental results prove the theoretical analytical models and the design procedure. The 5kW DC-DC converter prototype had a power density of 9 kW/liter (147W/in^3) and a maximum efficiency of 94.75 %.

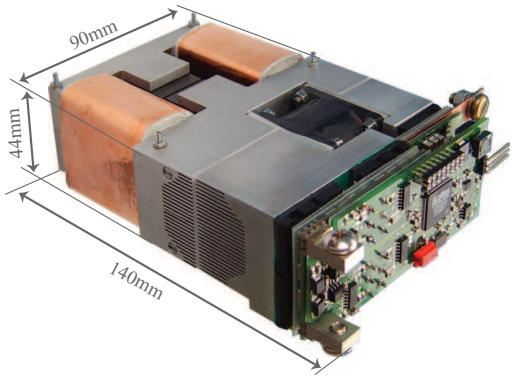
I. Introduction

In the area of power electronic converter systems there is a general trend to higher power densities that is driven by cost reduction, increased functionality and in some applications by the limited weight/space (e.g. automotive, aircraft) [1]. Moreover, when used in the continuously growing data centers, these converter focus more on high efficiencies in order to decrease the cooling effort and save energy.

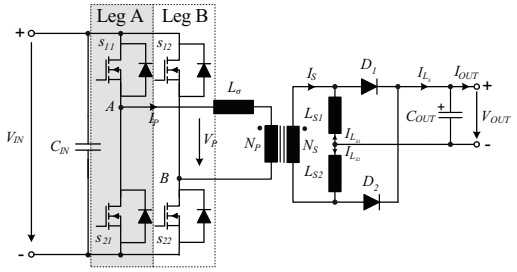
In power supply units (PSU) for telecommunication facilities or data centers, DC-DC converters are utilized for converting the rectified mains voltage to intermediate voltage levels for power distribution. In the literature many different topologies have been proposed for this application but for high power conversion usually full bridge topologies operating with soft switching, like a series-parallel resonant converter or phase shift converter with current doubler are applied, since these are relatively simple, robust and meet the demands of high power density and efficiency.

TABLE I: Specifications for the proposed IT DC-DC converter.

Input voltage	V_{IN}	400 V
Output voltage	V_{OUT}	48. . . 54 V
Output power	P_{OUT}	5 kW
Output ripple voltage	V_{ripple}	300 mV_{pp}
Max. ambient temperature	T_{amb}	45 °C
Max. height	h	1 U ($\approx$ 44 mm)



a) 5 kW prototype of the proposed 400 V/48..54 V DC-DC converter: Height: 1 U, volume: 0.56 liter, power density: 147 W/in^3 (9 kW/liter)



b) Schematic of the phase-shift full bridge converter with current doubler rectifier

Fig. 1: Phase-shift DC-DC converter with current doubler output

The design of the DC-DC converter has many degrees of freedom which complicates the selection of the best topology and the determination of the component values, which result in the best solution. In order to enable a direct design process for the solution with the highest power density/efficiency an optimization procedure, based on comprehensive analytical models and equations considering the losses in the semiconductors, in the magnetic devices and the other passive components, has been developed [2]. With this procedure the optimal design parameters in respect to power density and/or efficiency, such as switching frequency, component values for the capacitors and inductors, magnetic devices geometry or total heat sink volume, respectively, could determined.

In [2], this procedure has been utilized for optimizing and comparing a series-parallel resonant converter and phase-shift converters with capacitive and current doubler output with respect to power density and efficiency. A theoretical power density of 10 kW/liter and of 8.6 kW/liter have been achieved for the resonant converter and/or the phase-shift converter with current doubler. However, for the sake of brevity the design equations only could be shortly summarized. Therefore, the derivation of the

analytical models for the currents/voltages as well as for designing the magnetic components are presented in **Section II** of this paper. There, the design of the transformer with integrated output inductors and its integrated thermal management is also discussed. Furthermore, a new lossless snubber circuit for the rectifier diodes, which could experience high overvoltages in current doubler circuits in principle, is presented. The optimization procedure is discussed in **Section III**. The snubber circuit, the analytical models applied in the optimization procedure as well as the power density prediction are validated with measurement results on a 5 kW prototype with a power density of 9 kW/liter in **Section IV**.

II. Phase-Shift DC-DC Converter with Current Doubler Rectifier

The full bridge phase-shift DC-DC converter with current doubler rectifier in Fig. 1 fulfills the demands on a robust and simple design with a high power density and high efficiency. As shown in Fig. 1b), the converter consists of 4 switches as part of the full bridge, a transformer which provides galvanic isolation and transforms the voltage (400 V to 48..54 V), and the rectifier with the two output inductors and diodes. As shown later in this section, the two output inductors can be integrated in the transformer, in order to reduce the volume of the magnetic components and save the space required for interconnections and mounting. In order to derive the analytical models in subsection II-A, the relative simple control scheme and basic functionalities of the phase-shift converters are shortly explained in the following. Due to parasitic elements, overvoltages occur across the rectifier diodes, so that a snubber circuit is required. Therefore, three lossless snubber circuits are presented and compared on the basis of measurement results in subsection II-B.

In Fig. 2 the control scheme with the four basic switching states and the currents/voltage waveforms is depicted. Each full bridge switch is 50 percent of a switching period turned on. Regarding Fig. 2, the duty cycle D is adjusted by a phase-shift ϕ between the control signals of the two full bridge legs (A and B). This leads to the four main states: In the two powering states the diagonal switches of the legs are switched on (states 1 and 3, cf. Fig. 2) and in the two free-wheeling states the opposite MOSFETs of the legs are switched on (states 2 and 4). A detailed description of the switching states of this well known topology can be found in the literature, i.e. [3].

A significant reduction of the switching losses can be obtained by zero-voltage switching where the parasitic capacitances of the MOSFETs in one leg are recharged during an interlock delay between the switching states, driven by the leakage inductance L_σ of the transformer. As shown section in IV-A, L_σ is enlarged in order to have enough energy for the recharging process.

A. Analytical Models for the Phase-Shift DC-DC Converter

For the optimization of the DC-DC converter analytical models are required, which describe the currents/voltages in the circuit, and model the semiconductor, the dielectric and the transformer losses and which describe the temperature distribution in the system. With the thermal model the different components can be kept below their maximal values in the optimization, so that the components are not destroyed during operation.

These models are derived in the following based on the phase-shift DC-DC converter with current doubler as shown in Fig. 1b) but are in particular also valid for the „integrated“ current doubler, as presented in II-A.4.

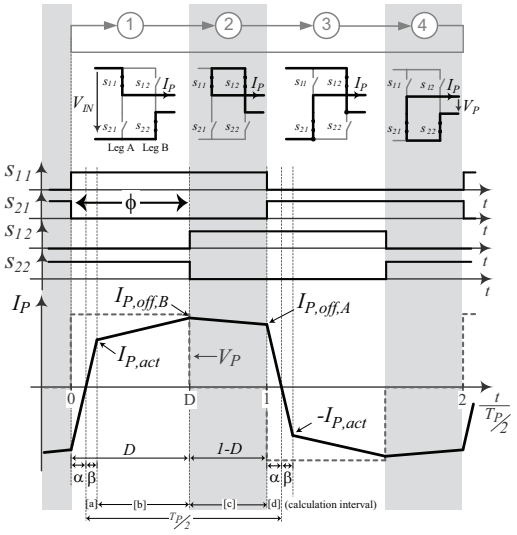


Fig. 2: Switching states and inverter waveforms for the phase shift converter with current doubler cf. Fig. 1 (ϕ indicates the phase-shift between the two legs of the full bridge, which determines the duty cycle and thus the output voltage)

1) Analytical Converter Model (cf. Fig. 1b)): In Fig. 2 the current waveform of the transformers primary current I_P is shown. The switched currents of the full bridge legs A and B ($I_{P,off,A}$ and $I_{P,off,B}$), as well as the point, where the active phase starts ($I_{P,act}$) are essential for further calculation. Concerning Fig. 2, during the time interval $t \in [\alpha \cdot {}^{T_P}/_2..(1+\alpha) \cdot {}^{T_P}/_2]$ with the duration of ${}^{T_P}/_2$, I_P is positive and can be described by four piecewise linear parts:

- $t \in [\alpha \cdot {}^{T_P}/_2..(\alpha+\beta) \cdot {}^{T_P}/_2]$: The positive input voltage $V_P = +V_{IN}$ is applied across the transformer and the primary current I_P increases from zero to $I_{P,act}$, determined by the transformers leakage inductance L_σ:

$$I_{P,a} = \frac{I_{P,act}}{\beta \cdot \frac{T_P}{2}} (t - \alpha \cdot \frac{T_P}{2}) \tag{1}$$

  During this interval, both rectifier diodes (D_1, D_2) are still conducting, thus the secondary side voltage V_S is clamped to zero and therefore, no power is transferred from the primary to the secondary side. At $t = (\alpha+\beta) \cdot {}^{T_P}/_2$ the primary current I_P equals the transformed output inductor current $I_{L_{S2}} \cdot {}^{N_S}/_{N_P}$.
- $t \in [(\alpha+\beta) \cdot {}^{T_P}/_2..D \cdot {}^{T_P}/_2]$: Delimited by the output inductance L_{S2} and L_σ the primary current I_P increases from $I_{P,act}$ to $I_{P,off,B}$. The linearized primary current in the powering state can be calculated with:

$$I_{P,b} = \frac{I_{P,off,B} - I_{P,act}}{(D-(\alpha+\beta)) \cdot \frac{T_P}{2}} \cdot (t - (\alpha+\beta) \cdot \frac{T_P}{2}) + I_{P,act} \tag{2}$$

  At the point $D \cdot {}^{T_P}/_2$, I_P reaches the max. value of $I_{P,max} = I_{P,off,B}$ (cf. Fig. 2), s_{22} is turned off and the opposite MOSFET s_{12} is switched on after a certain interlock delay in order to obtain ZVS condition.
- $t \in [D \cdot {}^{T_P}/_2..{}^{T_P}/_2]$: During this interval the primary current is free-wheeling as presented in Fig. 2. The transformer voltage V_P is clamped approximately to zero and the current I_P decreases from the turn off current of leg B $I_{P,off,B}$ down to the turn off current from leg A $I_{P,off,A}$, determined by

L_σ in series with $L_{S1,2} \cdot (N_P/N_S)^2$:

$$I_{P,c} = \frac{I_{P,off,A} - I_{P,off,B}}{(1-D) \cdot \frac{T_P}{2}} (t - D \cdot \frac{T_P}{2}) + I_{P,off,B} \quad (3)$$

At $t = T_P/2$, the high side switch of leg A (s_{11}) is turned off and diagonal switch s_{21} is turned on.

- $t \in [T_P/2..(1+\alpha) \cdot T_P/2]$: While changing from the freewheeling state to the active state, the negative input voltage $V_P = -V_{IN}$ is applied to the transformer and I_P decreases to 0 A determined by L_σ:

$$I_{P,d} = \frac{-I_{P,off,A}}{\alpha \cdot \frac{T_P}{2}} (t - \frac{T_P}{2}) + I_{P,off,A} \quad (4)$$

After that interval, the second half of the switching period starts with the first interval (a) again but with changed direction of primary current and voltage.

With the current waveform given in (1)-(4) the RMS value of I_P (important for the loss calculation) can be calculated:

$$I^2_{P,rms} = 2 \cdot \frac{1}{T_P} \left[\int_{\alpha \cdot \frac{T_P}{2}}^{(\alpha+\beta) \cdot \frac{T_P}{2}} I^2_{P,a}\, dt + \int_{(\alpha+\beta) \cdot \frac{T_P}{2}}^{D \cdot \frac{T_P}{2}} I^2_{P,b} dt + \right.$$
$$\left. + \int_{D \cdot \frac{T_P}{2}}^{\frac{T_P}{2}} I^2_{P,c} dt + \int_{\frac{T_P}{2}}^{(1+\alpha) \cdot \frac{T_P}{2}} I^2_{P,d}\, dt \right]$$

The duty cycle D, which defines the converter output voltage, is divided into the effective duty cycle D_e (power transfer), determined by twice of the output voltage V_{OUT} and secondary side voltage $V_{IN} \cdot N_P/N_S$, and a duty cycle loss $D_l = (\alpha + \beta)$ (cf. Fig. 2) caused by the transformers leakage inductance L_σ.

$$D = D_e + D_l \quad (5)$$

$$D = \frac{2 \cdot V_{OUT}}{V_{IN} \cdot N_P/N_S} + (\alpha + \beta) \quad (6)$$

The calculations presented so far, require the knowledge of α and β. Furthermore, besides the calculation of the RMS-value in order to calculated the conduction losses, the turn off currents $I_{P,off,A,B}$ have to be calculated for the switching losses and for solving the equations for α and β,which is presented in the following.

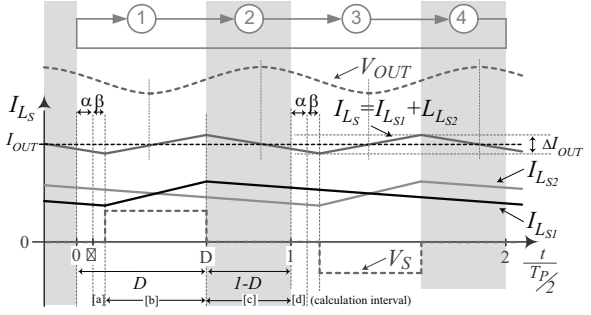


Fig. 3: Rectifier current waveforms for the phase shift converter with current doubler as presented in Fig. 1. (The ripple of the output voltage V_{OUT} is enlarged by way of illustration.)

The sum of the two inductor currents $I_{L_S} = I_{L_{S1}} + I_{L_{S2}}$ consists of the DC component I_{OUT} and the ripple current in the output capacitor $I_{C_{OUT}}$ as shown in Fig. 3. The minimum/maximum value of I_{L_S} are given by:

$$I_{L_S,min,max} = I_{OUT} \pm 1/2 \cdot \Delta I_{OUT} \quad (7)$$

where ΔI_{OUT} is the peak-to-peak value of the ripple current $I_{C_{OUT}}$ in the output capacitor. The DC component I_{OUT} can be simply calculated with the required output power P_{OUT} and the output voltage V_{OUT}:

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}} \quad (8)$$

The current ripple ΔI_{OUT} is defined by the factor k_I, a variable parameter for the optimization ($k_I \in [0..0.2]$), since the allowed current ripple defines the volume of the inductors and output capacitance:

$$\Delta I_{OUT} = k_I \cdot I_{OUT} \quad (9)$$

As presented in Fig. 3 the current ripple can be calculated within the interval $t \in [D \cdot T_P/2..(1+\alpha+\beta) \cdot T_P/2]$, where both inductor currents $I_{L_{S1}}$ and $I_{L_{S2}}$ and thus I_{L_S} are decreasing

$$\Delta I_{OUT} = 2 \cdot \Delta I_{L_{S1,2\downarrow}} \quad (10)$$

where $\Delta I_{L_{S1,2\downarrow}}$ is the current difference in the inductor L_{S1} and/or L_{S2} during that interval. The current ripple $\Delta I_{L_{S1,2}}$ in the output inductors $L_{S1,2}$ can be calculated with the total current decrease in this inductor (cf. Fig. 3):

$$\Delta I_{L_{S1,2}} = V_{OUT} \cdot \frac{T_P - (D - (\alpha + \beta)) \cdot \frac{T_P}{2}}{L_{S1,2}} \quad (11)$$

With equation (11) the current ripple $\Delta I_{L_{S2\downarrow}}$ can now easily be calculated with:

$$\Delta I_{L_{S1,2\downarrow}} = \Delta I_{L_{S1,2}} \cdot \frac{(1 - D + \alpha + \beta) \cdot \frac{T_P}{2}}{T_P - (D - (\alpha + \beta)) \cdot \frac{T_P}{2}} \quad (12)$$

The output current ripple ΔI_{OUT} is the sum of the two falling inductor current or the doubled ripple in one inductor (cf. equation (10)) , since both currents have the same slope during that interval.

Using Fig. 3, the required output inductances $L_{S1,2}$ can be calculated with the linearized voltage formula:

$$L_{S1,2} = V_L \cdot \frac{\Delta t}{\Delta I_L} = V_{OUT} \cdot \frac{(1 - D + \alpha + \beta) \cdot \frac{T_P}{2}}{1/2 \cdot k_I \cdot I_{OUT}} \quad (13)$$

By inserting $L_{S1,2}$ from equation (13) into (11) the current ripple $\Delta I_{L_{S1,2}}$ in the inductors can be calculated with the expression of α, β and the constraints k_I and I_{OUT}:

$$\Delta I_{L_{S1,2}} = \frac{1}{2} \cdot \frac{2 - D + \alpha + \beta}{1 - D + \alpha + \beta} \cdot k_I \cdot I_{OUT} \quad (14)$$

With the knowledge of the current ripple in the output inductors $\Delta I_{L_{S1,2}}$, the characteristic points of the primary current ($I_{P,off,B}$, $I_{P,act}$) can directly be obtained from Fig. 3:

$$I_{P,off,B} = \frac{1}{N_P/N_S} \cdot \left(\frac{I_{OUT}}{2} + \frac{\Delta I_{L_{S1,2}}}{2} \right) \quad (15)$$

$$I_{P,act} = \frac{1}{N_P/N_S} \cdot \left(\frac{I_{OUT}}{2} - \frac{\Delta I_{L_{S1,2}}}{2} \right) \quad (16)$$

In the freewheeling states 2 and 4 (cf. Fig. 2 and Fig. 3) the transformer is shortened by two opposite MOSFETs of the full bridge. The turn off current for the leg A $I_{P,off,A}$ is given by:

$$I_{P,off,A} = I_{P,off,B} - \frac{V_{OUT} \cdot (1 - D) \cdot T_P/2}{L_\sigma \cdot (N_S/N_P)^2 + L_{S1,2}} \cdot N_S/N_P \quad (17)$$

with the forward voltage drop V_{on} over the power switches.

As depicted in Fig. 2, the primary current slope during the duty loss time is constant and thus the quotient α/β can be expressed by $I_{P,act}$ and $I_{P,off,A}$:

$$\frac{\beta}{\alpha} = \frac{I_{P,act}}{I_{P,off,A}} \tag{18}$$

With the leakage inductance L_σ, the applied voltage V_{IN} and the current change during the duty loss time $(\alpha+\beta)\cdot T_P/2$, a further expression for $(\alpha+\beta)$ can be found:

$$\alpha+\beta = L_\sigma \cdot \frac{I_{P,off,A}+I_{P,act}}{V_{IN}\cdot\frac{T_P}{2}} \tag{19}$$

Solving (18) and (19) with respect to α and β, as well as the equations for the characteristic primary current points and the current ripple in the inductors (equations (17), (16), (15) and (14)), a solution for the values α, β and thus for $I_{P,off,A}$, $I_{P,off,B}$ and $I_{P,act}$ can be found. The obtained values, the current waveforms are defined and all component current/voltage waveforms can be determined in order to calculate e.g. the losses in the semiconductors, as presented in the next subsection.

2) Semiconductor Losses: With the obtained results from the analytical converter models the losses in the power devices (four MOSFETs, including the antiparallel diode, and the two rectifier diodes) can be calculated. There, the switching losses are calculated based on empirical equations, determined by measurements.

With the losses, the maximum allowed junction temperatures and the thermal resistance between junction and heat sink, the volumes of the heat sink is calculated based on the CSPI (Cooling System Performance Index) [4]. It is assumed that at each point of time one MOSFET is switched on and thus the current is carried by the MOSFET in the inverse direction (not by the antiparallel diodes) and therefore, the conduction losses of the MOSFETs are calculated with the RMS-value of the primary current $I_{P,rms}$ and the MOSFET's on resistance $R_{DS,on}$:

$$P_{cond,MOS} = R_{DS,on}\cdot I_{P,rms}^2 \tag{20}$$

Due to the ZVS condition the turn on losses are zero and the turn off losses in the leg A and B are estimated based on measurements for the applied MOSFETs [5]:

$$P_{zvs,off,A,B} =$$
$$2\cdot(1.9\cdot I_{P,off,A,B}^2 - 38\cdot I_{P,off,A,B} + 140)\cdot 10^{-7}\cdot f \tag{21}$$

if the turn off current in leg A and/or B $I_{P,off,A,B} \geq 15\,\text{A}$. In case of the currents $I_{P,off,A,B}$ are below 15 A, the switching losses under ZVS-condition are negligible.

For the rectifier diodes an approximately constant forward voltage drop $V_{F,rect}$ is assumed so that the conduction losses $P_{cond,rect}$ in one diode can be calculated with the average currents:

$$P_{cond,rect} = V_{F,rect}\cdot\frac{I_{OUT}}{2} \tag{22}$$

Since Schottky diodes are applied, the switching losses are relatively small and thus neglected.

For the specification of the efficiency the losses in the gate drivers and control unit P_{gate} are considered as well. These losses in the gate drives are dependent on the switching frequency and can be calculated with the gate charge and the gate capacitance.

With the present loss equations and the analytical model expressions of the currents described in before, the power loss in the semiconductors can be calculated as:

$$P_{semi} = 2\cdot(P_{zvs,off,A}+P_{zvs,off,B}) + 4\cdot P_{cond,MOS} + \\ + 2\cdot P_{cond,rect} + 4\cdot P_{gate}$$

3) Output filter capacitors: The output filter capacitors carrying high frequency ripple currents with relatively high amplitudes. In order to limit the losses and the temperature rise, dielectrics with a low loss factor $\tan\delta$ are required. In the prototype 2.2 µF / 100 V / X7R ceramic capacitors in a 1210 housing from muRata [6] are utilized, which have a very high allowed ripple current per volume ratio.

From Fig. 3, the voltage over the output capacitor increases during the charging process, i.e. when the sum of the inductor currents is bigger than the DC output current ($I_{L_S} > I_{OUT}$). This is true for half of the effective duty cycle D_e (current increase) and half of effective freewheeling time $(1-D_e)$ (current decrease). Thus, the capacitance value is calculated with the currents and the maximum allowed output ripple voltage $V_{ripple} = 300\,\text{mV}_{pp}$:

$$C_{OUT} = \frac{1}{V_{ripple}}\left[\int_0^{\frac{1}{2}\left(D_e\frac{T_P}{2}\right)} \frac{\Delta I_{OUT}}{D_e\cdot\frac{T_P}{2}}\cdot t\,dt + \right. \\ \left. + \int_0^{\frac{1}{2}\left((1-D_e)\frac{T_P}{2}\right)} \frac{\Delta I_{OUT}}{(1-D_e)\cdot\frac{T_P}{2}}\cdot t\,dt\right]$$

With the currents the losses can be determined with the loss factor and are compared with the maximum ratings from the data sheet. There, also the decrease of the capacitance with higher temperature and DC voltage is considered for the optimization.

4) Transformer Model: In the proposed optimization procedure the shape of the transformer is optimized for minimal volume while keeping the hot spot temperatures below the limits. For this calculation the losses and the transformers temperature distribution are needed as function of the geometry.

The core losses are calculated by the approach presented in [7], based on Steinmetz parameters [8] and the rate of magnetization (dB/dt). The winding losses are calculated by an 1D approach, which includes skin- and proximity effect loss [9]. There, foil windings are used which allow a better thermal management. In order to maximize the power density an advanced cooling method has been applied as described in [5]. The temperature distribution resulting from the losses can be calculated with the thermal model of the transformer. The model describes the heat flow from the windings/core via thermal interfaces and heat transfer components to the heat sinks and ambient, respectively. The transmission line based calculation is described in detail and validated in [10].

To decrease the volume and the losses, the two output inductors are integrated in the transformer based on a concept discussed in [11]. In the presented DC-DC converter the concept shown in Fig. 4 is applied, since the flux in the center leg of the transformer is almost constant and thus the core losses are small and standard E-cores could be applied. The value of the integrated inductors is adapted by the air gap in the center leg.

With the integration shown in Fig. 4 the operating behavior of the original current doubler changes as well. In case of the powering state 1, there the primary current is positive, a clockwise flux is induced in the outer legs. Only in the upper

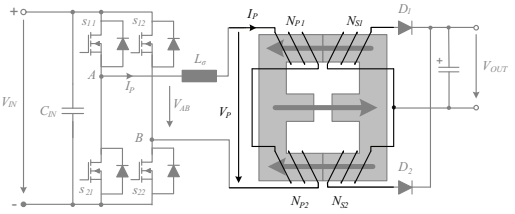


Fig. 4: Integration of the Output Inductors of the Current Doubler in a the transformers core ([11])

secondary winding N_{S1} (cf. Fig. 4) a current flow is possible, while the current flow in lower winding N_{S2} is blocked by the diode D_2. During the free-wheeling state 2 the primary current I_P remains positive and allows the current flow still only through the diode D_1. During states 3 and 4 (cf. Fig. 2) the negative primary current I_P causes the current flow through the secondary winding N_{S2}. That shows a significant change: Unlike in the original topology presented in Fig. 1b), there the inductor currents ($I_{L_{S1}}$ and $I_{L_{S2}}$) is almost constant over a switching period, the current in integrated topology flows only over one of the secondary winding/inductor. Thus, the original name „current doubler“is in principle not entirely correct any more. However, the current and voltage waveforms outside of the integrated transformer are remain the same like with the original current doubler as shown in Fig. 1b).

B. Comparison of Lossless Snubber Circuits

Due to a non ideal coupling coefficient between the primary and the secondary side of the transformer, a voltage ringing occurs across the rectifier diodes during the blocking phase. This ringing is caused by the resonant circuit resulting from the leakage inductance L_σ, the winding capacitances C_W and the diodes junction capacitances C_D (cf. Fig. 5d)). By decreasing the leakage inductance, the energy of this oscillation could be reduced, but a minimal value of the inductance is required for ZVS switching condition of the MOSFETs. This effect is even enhanced for the integrated topology because of the current shift from the first secondary winding (N_{S1}) to the other (N_{S2}). Furthermore, in order to reduce the volume of the magnetic components the switching frequency will be increased and the winding capacitance is relatively high since in the prototype system foil windings are utilized, because these allow a drastically reduced thermal resistance between the winding and the heat sink. In order to decrease the occurring ringing as depicted in Fig. 6d) without decreasing the efficiency, a lossless snubber circuit for the diodes is required. In Fig. 5, three possible snubber circuits are shown, which transfer a large share of the ringing energy to the output.

In Fig. 5a) a relative simple lossless snubber consisting of two additional diodes and one capacitor is given [12], which clamps the voltage over the winding. After a negative voltage is applied to primary transformer side and current in the rectifier diodes has commutated from D_1 to D_2, D_1 is able to absorb blocking voltage. During the positive oscillation, the capacitor C_{S1} is charged through the snubber diode D_{S1} over the transformer secondary voltage ($V_{C_{S1},max} \approx -(V_{IN}{}^{N_S}/_{N_P} + {}^1/_2 V_{OUT})$) and the diode D_1 reaches the maximum blocking voltage of $-(V_{C_{S1},max} + V_{OUT})$. Through the snubber diode D_{S2} the capacitor C_{S1} is discharged by feeding the leakage energy into the output, and therefore the oscillation is damped by the resonant charging-discharging behavior of the circuit. After the primary voltage changes its

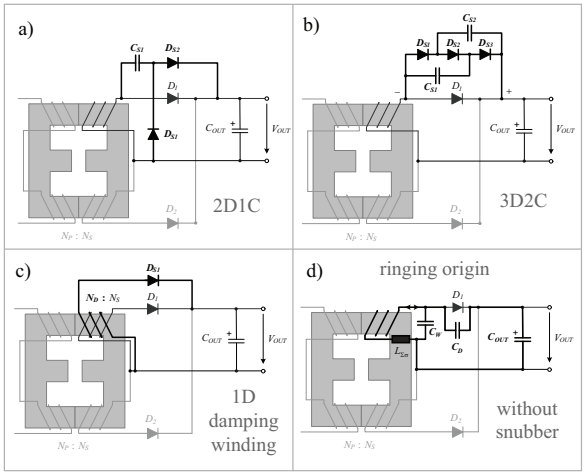


Fig. 5: Schematics of considered “lossless” snubber topologies for the integrated current doubler rectifier diode: a) snubber with 2 diodes and 1 capacitor (2D1C), b) snubber with 3 diodes and 2 capacitors (3D2C), c) snubber with 1 diode and damping winding. (Snubber circuit for only one diode is drawn for simplicity.) In d) the parasitic capacitors are delineated which causes the current ringing other the rectifier diodes.

polarity the snubber capacitance is discharged through D_{S2} to output.

An extended snubber circuit is presented in Fig. 5b), where three diodes and two additional capacitances are applied [12], which clamp the voltage over the rectifier diode. The operating principle of the different charge and discharge paths is related to the snubber presented above (cf. Fig. 5a)): The capacitors C_{S1} and C_{S2} are charged via D_{S2} for positives over voltages by the leakage energy in the transformer and discharged via D_{S1} and D_{S3}. The damping to the blocking voltage level of the rectifier diode ($V_{D_1} = -V_{IN}{}^{N_S}/_{N_P}$) is faster but with the penalty of a higher first voltage peak. Further information can be found in [12].

In Fig. 5c) the new circuit, which requires only a single snubber diode D_{S1} and an additional small winding N_D, is presented. The idea behind this topology is getting the leakage energy directly out with the damping winding and feed it to the output. In principle, the damping winding could also be installed on the center leg of the core. However, the coupling between the secondary windings $N_{S1,2}$ would be worse. The voltage over the secondary winding during the blocking phase is transformed with the turns ratio $N_D : N_{S1,2}$ to the snubber diode voltage $V_{D_{S1,2}}$ and clamped over the output voltage. The maximum diode voltages $V_{D_{1,2,max}}$ can be set with the damping winding's number of turns N_D:

$$N_D = N_S \cdot \frac{V_{OUT}}{V_{D_{1,2,max}} - V_{OUT}}. \tag{23}$$

With a proper choice of $V_{D_{1,2,max}}$ slightly over the steady state voltage of $V_{D_{1,2}}$ the snubber diodes D_{S_1} start conducting as soon as $V_{D_1} > V_{D_1,max}$ and the oscillation energy is directly fed to the output.

Fig. 6 presents the resulting experimental damped voltages over the rectifier diode V_{D_1}. Compared to the original curves in Fig. 6d), all three snubber circuits reduces the ringing significantly. However, the best result is obtained with the new snubber circuit presented in Fig. 5c) as shown in Fig. 6c). With this circuit the voltage amplitude is damped by a factor of four. Especially the first peak is significantly reduced in comparison to the other

tested lossless snubbers Fig. 5a) and b). Thus this circuit has been implemented in the prototype presented in section IV-A and IV-B.

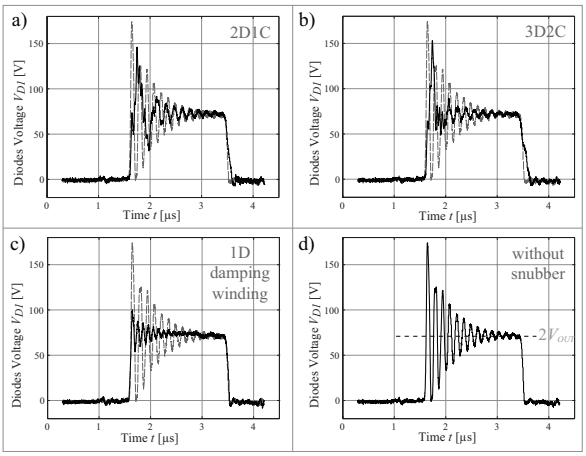


Fig. 6: Measurement results of the rectifier diode voltage V_{D1} with the presented snubbers a) (2D1C), b) (3D1C), c) snubber with 1 diode and damping winding and d) without snubber circuit. The obtained voltage without snubber are drawn gray in a), b), and c), as well. (In order not to destroy the rectifier diodes caused by over voltage, the measurement are taken at an input voltage $V_{IN} = 200\,V$, 1 kW, $V_{OUT} \approx 35\,V$.)

III. Power Density Optimization Procedure

Based on the analytical models presented in the previous section an automatic optimization procedure has been developed for finding the best set of converter parameters and component values, which result in a maximal power density and/or efficiency. In the proposed procedure shown in Fig. 7, all fixed electrical, thermal and magnetic components parameters and specifications are preset in the first step. These are, besides the system specifications (e.g. input/output voltage V_{IN}/V_{OUT}, output power P_{OUT}, ambient temperature T_{amb}), the characteristics of the employed components, like the thermal resistances of the semiconductors, isolation materials and thermal grease as well as characteristics of the core materials. In the next step, the free parameters like the switching frequency, number of windings and the allowed current ripple are set as initial values for the calculation. With the defined constraints, parameter settings and with the equations presented in section II-A the operating point is calculated, which is characterised by the duty cycle D, the duty cycle loss $\alpha + \beta$, the primary currents waveform characteristic $I_{P,off,A,B}/I_{P,1}$ and the output inductances $L_{S1,2}$, for instance. With the calculated operating point, the transformer and the inductor are optimized with respect to power density and/or efficiency within an inner optimization procedure, while keeping the temperatures for the core and windings below the maximum values. Furthermore, the volume of the filter capacitors can directly be calculated and the heat sinks determined by the losses in combination with the cooling system performance index CSPI [4]. The global optimization procedure changes systematically the free parameters for minimizing the overall system volume and/or efficiency. Further details are given in [5].

IV. Optimization, Construction and Measurement Results

With the presented optimization procedure in section III the phase-shift converter with current doubler has been optimized for

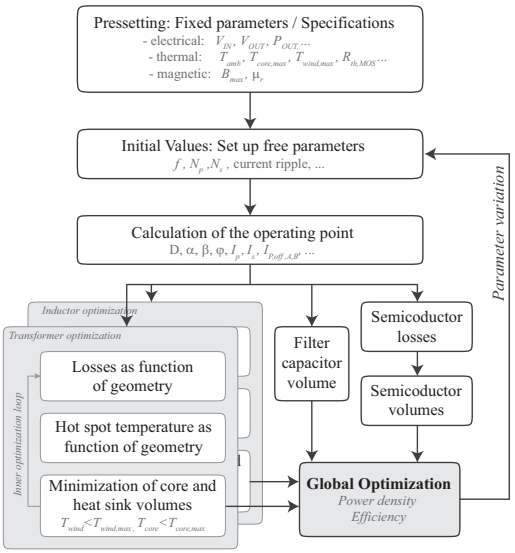


Fig. 7: Automatic procedure for optimizing the volume/efficiency of phase-shift converter with current doubler while keeping the device temperatures below given limits

the given specifications in table I. Amongst others, the following components/limitations have been used for calculation:

- Core material N87 from Epcos ($T_{max} \leq 115\,°C$)
- Foil windings ($T_{max} \leq 125\,°C$)
- Microsemi MOSFET APT50M75
- Microsemi diodes APT100S20
- Maximal junction temperature $T_{j,max} \leq 140\,°C$

The maximum calculated power density of $\approx$ 15 kW/liter. (246 W/in^3) is reached at a switching frequency of $\approx$ 200 kHz. There, only the net components volumes are considered since the final converter volumes depends strongly on the mechanical design. With the prototype shown in Fig. 1 a resulting power density of 9 kW/liter (147W/in^3) is obtained.

As presented in Fig. 8 the total volume of the converter at lower frequencies is determined by the magnetic components in the first place, since the magnetic flux density is increasing but is limited by the core materials on the one hand and the required inductance increases because of the increasing output current ripple on the other hand. For higher frequencies the core and winding losses and thus the cooling volume of the magnetic components is increasing. However, the significant rise in the volume at higher frequencies is caused by the increasing switching losses in the MOSFETs and the increased in the required cooling volume.

With a switching frequency of approximately 200 kHz a minimal volume and an efficiency 94.8 % results. Mainly caused by the lower switching losses at lower frequencies, the maximum efficiency of 95.1 % is reached around 100 kHz.

For the validation of the calculated values the resulting system design has been verified by an electrical simulation in a first step. The experimental verification is realized with the prototype shown in Fig. 1. The several parts of the converter are shown in the following.

A. Converter Assembly

In Fig. 9 the sliced CAD drawing of the assembled prototype (cf. Fig. 1) is presented. As explained in section II and depicted in Fig. 4, an integrated current doubler topology was applied. The primary and secondary winding are interleaved and mounted on

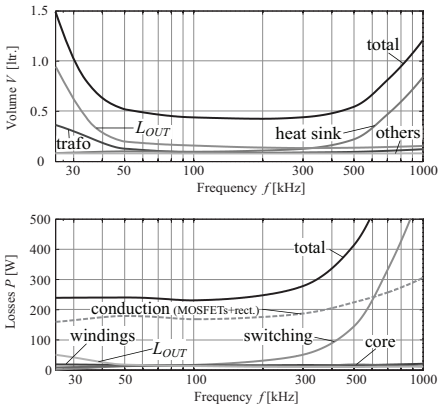


Fig. 8: Calculated Losses and Volumes (components housing only) for the Current Doubler

the outer legs of an standard E-core. The spacer between the primary and secondary/damping winding determines the necessary leakage inductance for the soft switching. The heat is extracted out of the core and the winding by the heat transfer components which are ending in the transformer heat sink. The airflow is forced by a high performance fan from the rectifier side (left) to the MOSFET's side. The energy is transferred by low inductive connectors to the output and input board. Due to the applied bootstrap topology, the digital control, gate driver and control supply could be implemented on one single PCB (90 mm x 40 mm) in front of the converter system. Further details are presented in Fig. 9 or the prototype in Fig. 1.

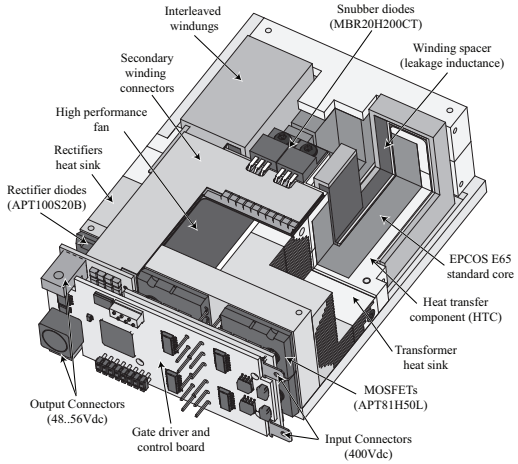


Fig. 9: Drawing of the prototype with a cut through the transformer heat sink and winding. (The upper cover have been omitted.)

B. Measurement Results

For the validation of the calculation and simulation results, thermal and electrical measurements have been performed with the presented prototype. The results are shown for the inter-leg voltage V_{AB} and the rectifier voltage V_{D1} in Fig. 10. Due to the zero voltage switching, V_{AB} shows no voltage ringing at full power and the rectifier diodes voltage ringing is drastically decreased to secured operation area. The measured efficiency at full power is 94.75 % and agrees very well with the theoretical calculations. Furthermore, the thermal design could be validated through IR temperature measurements.

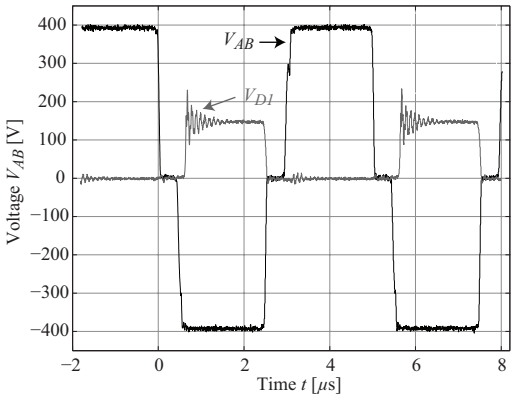


Fig. 10: Measured Curves: Primary Voltage V_{AB} and Rectifier Diode Voltage V_{D_1} at 5 kW Output Power

V. Conclusion

In this paper a power-density-optimized 400 V/48..56 V telecom phase-shift DC-DC converter with an integrated current doubler rectifier and 5 kW output power is presented. For the optimization a procedure, based on comprehensive analytical models of the converter including magnetic components and thermal management, is applied to determine the component values of the converter. After verifying the resulting parameters by an electrical simulation, a prototype has been constructed, which has a power density of 9 kW/liter (147W/in^3) and integrates the output inductors in the transformer. With this prototype measurements are performed for validating the analytical calculations.

Furthermore, a new snubber circuit for the rectifier diodes, which performs an almost lossless damping of the diode voltage is presented and validated by measurements.

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