Design of a Novel Multi-Chip Power Module for a Three-Phase Buck+Boost Unity Power Factor Utility Interface Supplying the Variable Voltage DC Link of a Square-Wave Inverter Drive

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Abstract – The power semiconductors of one bridge leg of the buck-type input stage of a three phase buck+boost PWM rectifier are integrated into a novel power module. The basic function of the rectifier system is described, and the current stresses on the power semiconductors are calculated analytically. By an experimental analysis of the module the switching losses of the power transistors are determined, and the system efficiency and the loss contributions of the different components are calculated. This gives a basis for the selection of advantageous operating parameters of the module in an industrial application.

I. INTRODUCTION

For variable-speed induction motor drives in heating, ventilation and air-conditioning (HVAC) applications there is in general a low demand on the dynamic performance and on the accuracy of the speed control [1], [2]. Therefore, variable-frequency square-wave voltage source inverters with variable DC link voltage (cf., e.g., p. 425 in [3]) can be applied instead of PWM controlled inverters with constant DC link voltage. In comparison to PWM control this concept shows advantages concerning the realization effort of the inverter control and the inverter losses (lower cooling effort). Furthermore, it is characterized by low electromagnetic emissions. However, if the input rectification and the variation of the DC link voltage is realized by a phase-angle controlled thyristor bridge there result low-frequency harmonics of the mains current having relatively high amplitudes and a very low power factor at partial load (i.e., at low speed). In contrast, in order to ensure an universal applicability of such systems in the European 400 V low-voltage mains with regard to the preliminary standard IEC61000-3-4 concerning electromagnetic compatibility of high-power systems the rectifier system should show ideally sinusoidal input currents lying in phase with the respective mains phase voltages besides allowing a wide variation of the output voltage.

In [4] a three-phase buck+boost PWM rectifier system has been proposed (cf. **Fig. 1**(a)) which permits an increase of the DC output voltage (DC link voltage) above the input voltage in the boost-operation mode as well as a decrease of the output voltage to zero and therefore could be employed in the case at hand [5]. There, the boost stage could be omitted by an appropriate choice of the rated voltage of the induction machine which is fed by the square-wave voltage-source inverter.

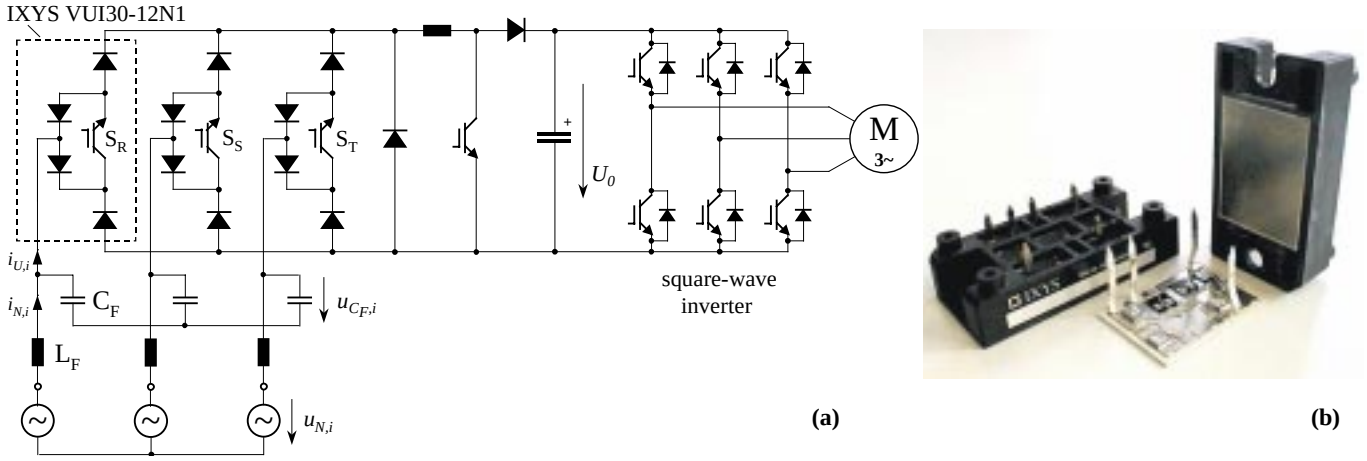


Fig. 1: *(a) Basic structure of the power circuit of a three-phase buck+boost PWM rectifier [4] varying the DC link voltage of a square-wave inverter supplying a set of induction machines (shown by a single representative) of an air-conditioning system. (b) Prototype (VUI30-12N1) of the power module integrating the power semiconductors of one bridge leg of the buck input stage of the system.*

As substantial advantages of this concept one has to point out

- the resistive fundamental mains behavior of the system,
- the possibility of limiting the input current for mains over-voltage (in contrast to rectifier systems with boost-type input stage), and
- the possibility of limiting the current in the buck+boost inductor.

However, a conventional realization of the power stage requires the insolated assembly of a large number of discrete components. Hence, the availability of a power module integrating the power semiconductors of one bridge leg of the buck input stage would considerably simplify the application of the proposed system and/or reduce the assembly and/or the realization costs.

In this paper the design, practical realization and experimental investigation of such power module is described for an output power of 15 kW at a maximum output voltage of 600 V of the buck+boost PWM rectifier system**.**

In **section 2** the basic principle of operation of the buck-type input stage of the system shown in Fig. 1(a) is described briefly. Based on this in **section 3** the current stresses on the power semiconductor devices are calculated in analytical closed form in dependency on the modulation depth and on the output power, and the internal layout of the power module is shown. Furthermore, the experimental switching evaluation of the power module VUI30-12N1 (cf. Fig. 1(b)) is described, and the results of the analysis are compiled. This data is used in **section 4** for calculating the maximum admissible output power and the efficiency of the buck input stage employing the power module. This provides a basis for an advantageous selection of the system operating parameters for an industrial application of the power module.

II. Basic Principle of Operation

II.1 Assumptions and Definitions

In order to achieve ohmic fundamental mains behavior we have to form fundamentals $i_{U,(1),i}$ (denoted by the index (1)) of the rectifier input currents $i_{U,i}$ lying in phase with the corresponding mains phase voltage $u_{N,i} \approx u_{C_F,i}$ which are assumed to be approximately equal to the filter capacitor voltage. For proper attenuation of switching frequency harmonics of $i_{U,i}$ by the low-pass filter $L_F C_F$ we then have

$$i_{N,i} \approx i_{U,(1),i} \quad . \tag{1}$$

Therefore, the relative on-times δ_{S_i} of the power transistors S_i have to be set proportional to the instantaneous value of the mains phase voltages. Considering the relation of the output current I of the buck stage and the mains current amplitude $\hat{I}_N$ which is characterized by the modulation index

$$M = \frac{\hat{I}_N}{I} = \frac{\sqrt{2}U}{\sqrt{3}U_{N,LL}} \tag{2}$$

($U_{N,LL}$ denotes the line-to-line voltage) one receives for the relative on-times of the power transistors S_i

$$\delta_{S_i} = M \frac{|u_{N_i}|}{\hat{U}_N} . \tag{3}$$

II.2 Switching State Sequence

A high system efficiency can be achieved by employing the switching state sequence proposed in [4] which does result in minimum switching losses. There, within a $\pi/3$-wide interval of the mains period the power transistor of the bridge leg of that phase i, $i=R,S,T$, which shows the lowest absolute value of the phase voltage $u_{N,i}$ is clamped ($\delta_{S_i} = 1$, cf. **Fig. 2**). Considering, e.g., the angle interval $\varphi_U \in (0;\pi/3)$ the mains phase voltage $u_{N,S}$ meets the criteria $|u_{N,S}| < \{|u_{N,R}|;|u_{N,T}|\}$, therefore, the power transistor S_S is clamped within this angle interval.

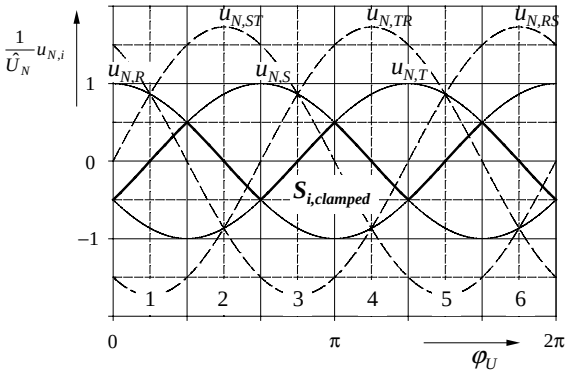


Fig. 2: *Mains phase voltages, line-to-line voltages and intervals being defined by different relations of the instantaneous mains phase voltage values. Always the power transistor S_i of one phase is clamped ($S_{i,clamped}$, $i=R,S,T$) within one $\pi/3$-wide interval as pointed out by bold segments of the corresponding phase voltage waveforms.*

Furthermore, a certain sequence of the switching states has to be implemented to achieve minimum switching losses. This sequence consists of three different switching states (two active switching states which are characterized by $i_{U,i} \neq 0$, and one free-wheeling state), which are arranged symmetrically to the center $t_\mu = T_P/2$ of one pulse period T_P, where t_μ denotes the local time running within T_P.

The sequence is starting at $t_\mu = 0$ with an active switching state $j = (111)$ [1] (cf. **Fig. 3**). For $j = (111)$ all power transistors S_i are in on-state, but only the power transistors of the bridge legs showing the largest absolute value of the line-to-line voltage are conducting, the third switch does not conduct any current. Considering interval 1 in Fig. 2, therefore, the switching state $j = (101)$ is equivalent with the switching state $j = (111)$. At the transition to the second switching state at $t_\mu = t_{\mu 1}$ the power transistor S_i of the bridge leg having the smaller absolute value of the mains phase voltages $u_{N,i}$ has to be switched off (for selecting this bridge leg the bridge leg with the clamped power transistor $S_{i,clamped}$ has to be ignored). In the angle interval $\varphi_U \in (0;\pi/6)$ (cf. Fig. 2) $|u_{N,T}|<|u_{N,R}|$ is valid, and therefore the power transistor S_T has to be switched off at $t_{\mu 1}$.

The last switching state within $T_P/2$ is the free-wheeling state, where only the clamped power transistor is in the on-state. If a free-wheeling diode is provided (as assumed here with respect to system reliability considering control malfunctions) the free-wheeling path always leads via the free-wheeling diode, because of the comparable higher forward voltage drops of the power semiconductor devices in one bridge leg.

[1] For the denomination of the switching states of the power transistors S_i, $i=R,S,T$, switching functions s_i are used in the following, where $s_i = 0$ denotes the off-state and $s_i = 1$ denotes the on-state. The characterization of the switching state of the buck input stage is defined by the combination $j = (s_R, s_S, s_T)$ of the phase switching functions.

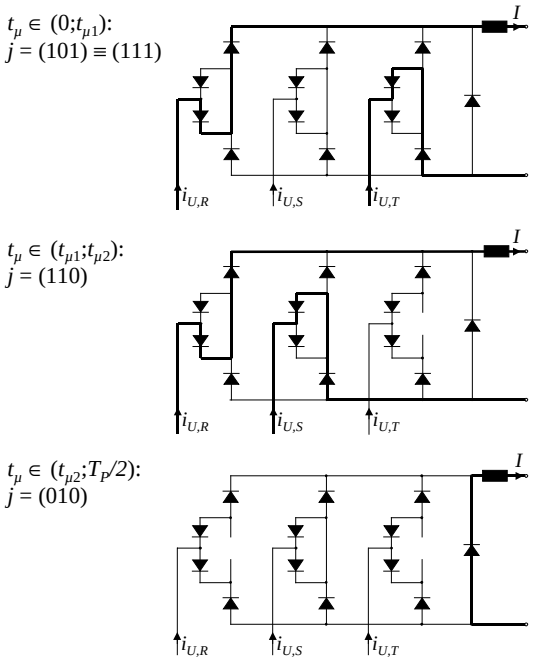


Fig. 3: *Conduction states of the buck input stage of the system shown in Fig.1(a) valid for* $u_{N,R} > 0 > u_{N,S} > u_{N,T}$.

Further switching state sequences being equivalent to the scheme described above concerning the switching losses are discussed in [4] but should not be treated here for the sake of brevity. Concerning a verification of the sinusoidal shape of the mains current (as determined by digital simulation) resulting for application of the given switching state sequence we also would like to refer to [4].

III. Stresses on the Power Semiconductors of the Power Module VUI30-12N1

III.1 Internal Power Module Structure

The power semiconductors (Diodes D_{N+}, D_{N-}, D_{+}, D_{-}, and transistor S, cf. **Fig. 4**(a)) of one bridge leg of the buck input stage are integrated in one power module. For the diodes power semiconductor dies of a fast recovery epitaxial diode IXYS DSEK 60 having a blocking voltage $U_{RRM} = 1200$ V (cf. [7]) are considered, the power transistor is realized by two 1200 V fast switching IGBTs (IXYS IXD 30N120, cf. [8]) in direct parallel connection. The internal layout of the module is depicted in Fig. 4(b). The power semiconductor dies are soldered on copper tracks on the upper side of a ceramic baseplate (dimensions: (35×26)mm = (1.4×1.0)in, identical with IXYS VUM25-05), whereby a low thermal resistance and a high insulation voltage to the mounting surface (heat sink) results for all elements. The power module package is shown in Fig. 1(b) (dimensions: (62×32×17)mm = (2.4×1.3×0.7)in).

III.2 Current Stresses on the Power Semiconductor Devices of a Bridge Leg

In the following, the current average and rms values are given as required for the calculation of the on-state losses and switching losses of the power semiconductors according to sections III.3 and III.4. In order to concentrate on the essentials, we again assume

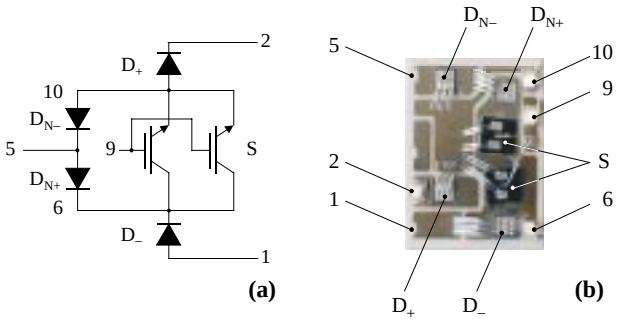


Fig. 4: *Structure of one bridge leg of the buck input stage* ***(a)****, and internal layout of the power module* ***(b)****.*

- a purely sinusoidal mains phase current lying in phase with the mains phase voltage
- a constant switching frequency f_P
- a constant inductor current I.

Furthermore, we neglect

- the mains frequency voltage drop across the AC side input inductors.

III.2.1 Power Diodes

For the positive half wave of the mains current ($i_{N,i} > 0$) the diodes $D_{i,N+}$ and D_{i+}, are conducting, for the negative half wave ($i_{N,i} < 0$) the diodes $D_{i,N-}$ and D_{i-} are conducting. The average and rms values are the same in both sets of diodes and can be calculated easily as

$$I_{D_{i,N,\mathrm{avg}}} = I_{D_{i,\mathrm{avg}}} = \frac{1}{\pi} \cdot \hat{I}_N \tag{4}$$

$$I_{D_{i,N,rms}} = I_{D_{i,rms}} = \frac{1}{\sqrt{M\pi}} \cdot \hat{I}_N \,. \tag{5}$$

III.2.2 Power Transistor

The power transistor is conducting during the positive *and* the negative half wave of the mains current fundamental. Therefore, one receives for the current average and rms values

$$I_{S_i,\mathrm{avg}} = \frac{2}{\pi} \hat{I}_N \tag{6}$$

$$I_{S_i,rms} = \frac{2}{\sqrt{M\pi}} \hat{I}_N \,. \tag{7}$$

III.2.3 Free-wheeling Diode

The current stress on the free-wheeling diode is defined by the difference of the average current in the diodes $D_{i,N}$ and/or D_i and the current in the buck+boost inductor,

$$I_{D_F,\mathrm{avg}} = \hat{I}_N \left(\frac{1}{M} - \frac{3}{\pi} \right) \tag{8}$$

$$I_{D_F,rms} = \hat{I}_N \sqrt{\left(\frac{1}{M^2} - \frac{3}{M\pi} \right)} \,. \tag{9}$$

III.3 Conduction Losses

III.3.1 Power Diodes

The forward characteristics of the power diodes as known from the data sheet (cf. Figs. 1 in [7], [9]) are approximated by a current independent forward voltage drop $U_{F,0}$ in addition to a differential resistance r_D

$$u_{D,F} = U_{F,0} + r_D i_D \,. \tag{10}$$

With Fig.1 in [7] one receives $U_{F,0}$ = 1.7 V, and r_D = 0.0186 Ω for the diodes of the power module VUI30-12N1, and with Fig. 1 in [9]: $U_{F,0(D_F)}$ = 0.9 V, and $r_{D(D_F)}$ = 0.01 Ω for the free-wheeling diode. The average conduction power losses then result as

$$P_D = U_{F,0} \cdot I_{D,\text{avg}} + r_D \cdot I^2_{D,\text{rms}} \,. \qquad (11)$$

III.3.2 Power Transistors

Considering Fig. 2 in [8] the forward characteristic of an IGBT can be approximated based on

$$u_{S,F} = U_{CE,0} + r_{CE} i_C \,. \qquad (12)$$

The power module VUI30-12N1 has an internal parallel connection of two IGBT-chips (cf. Fig. 4(b)), therefore, one receives $U_{CE,0}$ = 1.4 V, and r_{CE} = 0.023 Ω for U_{GE} = 15 V.

III.4 Switching Losses of the Power Semiconductors

If the power module is applied as bridge leg of a three-phase PWM rectifier system a sinusoidal variation of the switched voltage and, therefore, also of the switching power losses results over the mains period. Due to the thermal inertia of the power semiconductors one can limit the consideration in a first step to the average value of the switching power losses related to one mains period, however. For the sake of simplicity we assume

(i) the switching loss P_S to be proportional to the average value of the switched voltage $u_{sw}(t)$ (the proportional relationship is represented by a constant k), and

(ii) a constant switched current I (as impressed by the inductor L).

With this, one receives

$$P_S = k \cdot f_P \cdot I \cdot u_{sw,\text{avg}} \,. \qquad (13)$$

III.5 VUI30-12N1 Experimental Switching Evaluation

For measuring the switching losses of the power semiconductors of the power module VUI30-12N1 the experimental circuit shown in **Fig. 5**(a) was used. There, a PCB was employed for wiring of three modules resulting in the complete structure of the three-phase buck stage. With the auxiliary DC voltage sources instantaneous values of the AC mains line-to-line voltages can be simulated, R_L represents a resistive load. Due to the system propagation delay of a clip-on type current probe TCP202 (Tektronix) being too high for an exact determination of the switching power loss, the measurement of the transistor current is performed via a low-inductance shunt (cf. Fig. 4 in [6]). The shunt R_{Shunt} is realized using 10×1 Ω resistors in parallel connection, the voltage drop of the current to be measured is taken directly across the resistors by a coaxial cable. The transistors are protected by a RC- and RCD-snubber network in order to limit switching overvoltages (series connection: R = 47 Ω, C = 470 pF, parallel connection: R = 220 kΩ, C = 100 nF). To avoid a reverse current flow in the transistors (as occurring due to the reverse recovery currents of the diodes D_i and $D_{i,N}$ lying in series with the switched power transistors), an additional protecting diode is provided between transistor drain and source. To protect the free-wheeling diode from overvoltages in case of discontinuous DC link current, a RCD-snubber is provided: R = 220 kΩ, C = 100 nF is provided. A gate resistor of R_G = 14 Ω is chosen with respect to limiting the switching overvoltage occurring at turn-off (cf. Fig. 6(f)) and the peak value of the reverse recovery current of, e.g., the free-wheeling diode (cf. Fig. 6(c)) at turn on.

In order to cover all switching actions occurring within one pulse period the switching state sequence having low pulse widths and low repetition rate is provided (cf. Fig. 5(b)): T_{rise} is a variable time dependent on the current amplitude required in the buck+boost inductor, T_S = 5µs is a constant time between the switching actions. At t_1 the current I is commutated from the transistors S_R and S_T to the free-wheeling diode, at t_2 the transistor S_S is switched on, the current is commutated from the free-wheeling diode to the transistors S_R and S_S, at t_3 the transistor S_T is switched on, and due to $(u_{RS}+u_{ST})>(u_{ST})$ the current is commutated from S_S to S_T. At t_4 the current is commutated back to S_S.

Considering a π/3-wide interval of the mains period the DC voltages u_{RS} and u_{ST} were varied in the following range (cf. Fig. 2) providing additionally a margin of ± 10 %

$$\begin{aligned} u_{RS} &\in (\sqrt{3}/2;0.5)\cdot\hat{U}_{N,LL} \pm 10\% \\ u_{ST} &\in (0;0.5)\cdot\hat{U}_{N,LL} \pm 10\%. \end{aligned} \qquad (14)$$

The switching losses were evaluated for different currents $I \in (10;40)$ A, and for different junction temperatures of the semiconductor dies: T_J = 20° C (equal to ambient temperature) and T_J = 120 °C (due to the low repetition rate of the switching actions showing a low pulse width the junction temperature can be assumed to be equal to the heat sink, which can be adjusted by the voltage applied to a heating resistor R_H (Fig. 5) mounted on the bottom side. The measurements have been carried out by using a digital storage oscilloscope TDS3014 (100 MHz, 1.25 Gs, Tektronix). For the voltage acquisition probes TEK P5205 (Tektronix) have been used.

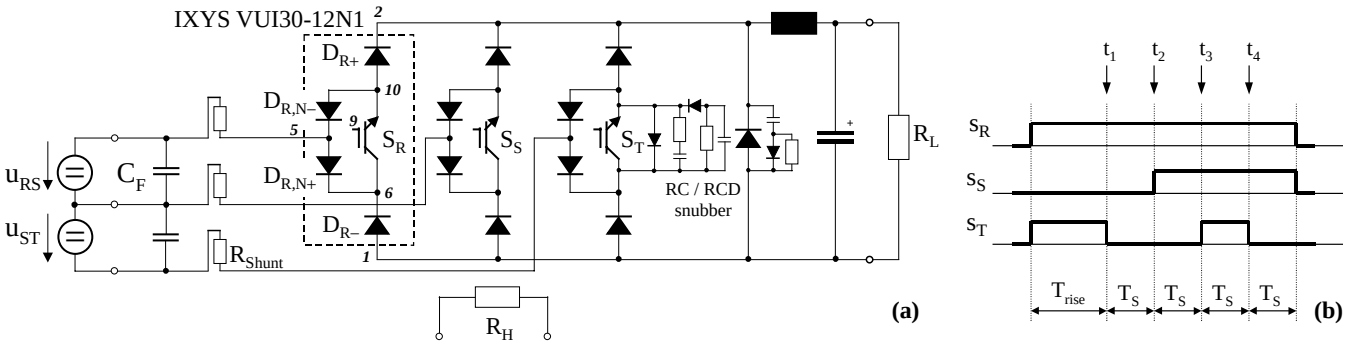


***Fig. 5**: **(a):** Experimental circuit for measuring the switching power losses (the snubber network shown for transistor S_T is provided in all bridge legs). **(b):** Applied switching pattern.*

III.6 Experimental Results

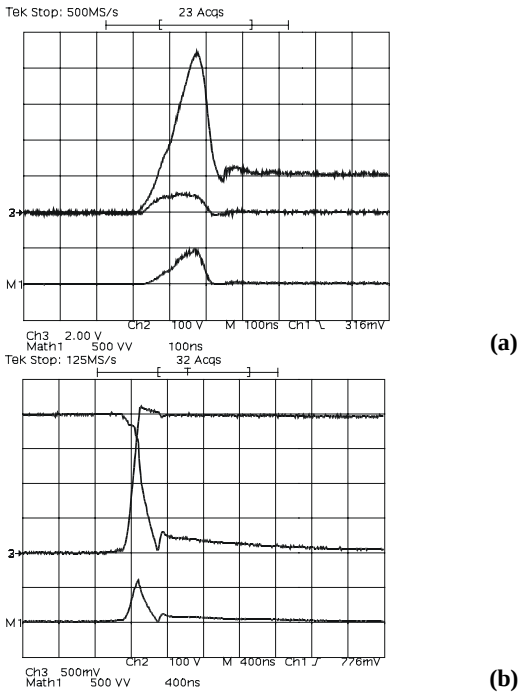
In the following, for all switching actions occurring within one pulse half period the time behavior of switched current and voltage is discussed, and the results of the experimental switching evaluation are summarized.

As **Fig. 6**(a) shows, the forward recovery losses of the power diodes $D_{i,(N)}$ are not negligible: The measured forward recovery voltage $U_{FR} \approx 60$ V matches the value given in the data sheet (cf. Fig. 6 in [7]: for di/d$t \approx 80$ A/130 ns one receives $U_{FR} \approx 55$ V). Due to the forward recovery voltages of the power diodes lying in series with the switched power transistors (cf. Fig. 6(c), and (e)) which are reducing the transistor turn-on voltage, the transistor turn-on losses are very low. But one has to mention that turn-on losses (forward recovery losses) occur in the power diodes (cf. Eq. (17)) and/or part of the transistor turn-on losses is transferred to the diodes.

A comparison of Fig. 6(c) and (e) clearly shows, that there is a dependence of the peak value of the reverse recovery current on the switched voltage. Furthermore, we would like to point out that for a junction temperature of 20 °C (oscillograms of the time behavior are not shown here for the sake of brevity) a decrease of the reverse recovery current peak value of only ≈10 % can be noticed.

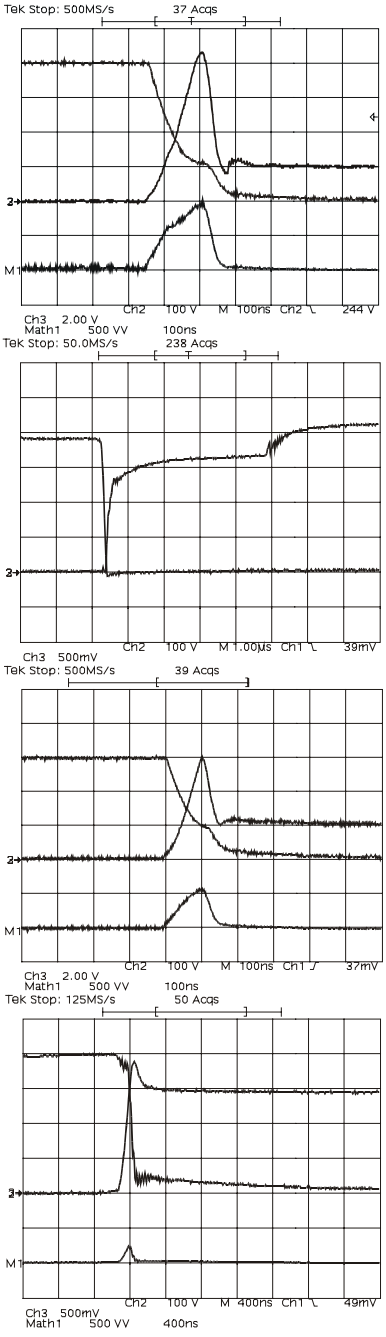
The overvoltage protection by the snubber network (cf. Fig. 5) is shown in Fig. 6(b): the overvoltage peak is limited to a few 10V. In Fig. 6(f) the overvoltage peak shows a value of ≈100 V (The snubber capacitor of the RCD snubber is charged by the previous switching action to a voltage being higher than the switching overvoltage occurring for the switching at hand, therefore, the overvoltage is limited only by the RC snubber, and not by the RCD snubber).

Regarding Fig. 6(d) one can see, that at the beginning of the free-wheeling state the current path does not only lead via the free-wheeling diode, but also via the bridge leg with the clamped switch (cf. section II.2), until the stored charge in the devices which have participated in the current conduction in advance to the free-wheeling state is removed, and the switch is blocking. For low junction temperature ($T_J = 20$ °C) the share of the free-wheeling current flowing across the clamped switch is reduced to a few percent. As an investigation of the turn-on behavior of the free-wheeling diode shows, the forward recovery losses of this diode can be neglected.



(a)

(b)



(c)

(d)

(e)

(f)

Fig. 6*: Different switching actions at T_J=120°C, I=20A (current scale: 1V=10A, power loss scale: 5 kW/div.). Transition between free-wheeling state and active switching state (and vice versa), $u_{RT} = u_{ST} = 400$V:* ***(a)*** *forward recovery losses (D→S (cf. Tab. I), t_2),* ***(b)*** *turn-off losses (S→D, t_1),* ***(c)*** *turn-on-losses (D→S, t_2), and* ***(d)*** *current in the free wheeling diode (S→D, t_1). Transition between two active switching states (S→S) (u_{RT}=570V, u_{ST}=285V):* ***(e)*** *turn-on losses (t_3), and* ***(f)*** *turn-off losses (t_4).*

As a closer investigation of the experimental results shows, the measured switching power losses of the power devices (power transistors, and power diodes) can be approximated with good accuracy by a linear dependency

$$w = k \cdot I \cdot u_{sw} \tag{15}$$

on the switched current, and on the switched voltage with good approximation. The results are compiled in **Tab. I**.

$k\,(\frac{\mu J}{VA})$	$k_{ON,S}$ $S\to S$	$k_{OFF,S}$ $S\to S$	$k_{ON,S}$ $D\to S$	$k_{OFF,S}$ $S\to D$	$k_{ON,D}$ $S\to S$	$k_{ON,D}$ $D\to S$
T_J=20°C	0.044	0.19	0.070	0.19	0.046	0.030
T_J=120°C	0.12	0.27	0.17	0.30	0.052	0.036

Tab. I: *Constants of proportionality k for turn-on and turn-off energy loss of the power transistors, and power diodes for different junction temperatures T_J and different switching actions ($S\to D$ denotes a transition between an active state and the free-wheeling state (and vice versa), $S\to S$ denotes the transition between to active switching states).*

IV. Assessment of the Practical Applicability of the Power Module VUI30-12N1

IV.1 Total Power Losses of the Individual Power Semiconductors

Considering the switching actions in one bridge leg of the buck input stage within one mains period the average value of the switching losses of the power transistors S_i and of the diodes $D_{i,(N)}$ can be calculated. If we look at, e.g., the bridge leg in phase $i=R$, the following switching actions (showing different switching losses) occur in interval 1 (cf. **Fig. 7** (dark gray shaded area), and section II.2 at $t_\mu=t_{\mu 2}$ (cf. Fig. 3):

- S_R is turned off
- current I commutates to free-wheeling diode D_F
- average value of switched voltage within interval 1: $U_{N,ST,\mathrm{avg}} = \frac{3}{\pi}(\sqrt{3}-1)\cdot\hat{U}_{N,LL} = 0.7\cdot\hat{U}_{N,LL}$
- average value of switching loss: $P_{S,S} \propto \underset{S\to D}{k_{OFF,S}}\cdot U_{N,ST,\mathrm{avg}}$.

In the subsequent pulse half period we have at $t_\mu=(T_P-t_{\mu 2})$:

- S_R is turned on
- current I commutates from D_F to S_R
- average value of switched voltage: $U_{N,ST,\mathrm{avg}} = 0.7\cdot\hat{U}_{N,LL}$
- average value of switching loss: $P_{S,S} \propto \underset{D\to S}{k_{ON,S}}\cdot U_{N,ST,\mathrm{avg}}$
- average value of forward recovery loss ($D_{R,N+}$, D_{R+}): $P_{S,D} \propto \underset{D\to S}{k_{ON,D}}\cdot U_{N,ST,\mathrm{avg}}$.

In the following interval 2 (light gray shaded area in Fig. 7) the switching state sequence changes due to the instantaneous mains phase voltage values being present at the input of the rectifier system: At $t_\mu=t_{\mu 1}$

- S_R is turned off
- current I commutates to S_S
- average value of switched voltage within interval 2: $U_{N,ST,\mathrm{avg}} = \frac{3}{\pi}(2-\sqrt{3})\cdot\hat{U}_{N,LL} = 0.26\cdot\hat{U}_{N,LL}$
- average value of switching loss: $P_{S,S} \propto \underset{S\to S}{k_{OFF,S}}\cdot U_{N,ST,\mathrm{avg}}$.

In the subsequent pulse half period at $t_\mu=(T_P-t_{\mu 1})$:

- S_R is turned on
- current I commutates from S_S to S_R
- average value of switched voltage: $U_{N,ST,\mathrm{avg}} = 0.26\cdot\hat{U}_{N,LL}$
- average value of switching loss: $P_{S,S} \propto \underset{S\to S}{k_{ON,S}}\cdot U_{N,ST,\mathrm{avg}}$
- average value of forward recovery loss ($D_{R,N+}$, D_{R+}): $P_{S,D} \propto \underset{S\to S}{k_{ON,D}}\cdot U_{N,ST,\mathrm{avg}}$.

In intervals 3 and 4 the power transistor S_R is clamped, therefore, no transistor switching losses do occur, but there are forward recovery losses of the diodes in dependency on the sign of the mains phase current $i_{N,R}$ and/or of the mains phase voltage $u_{N,R}$. In Fig. 7 the behavior of the switched voltage is given for the power semiconductors in bridge leg $i=R$. By multiplication with the appropriate constants of proportionality k, and under consideration of the switching state sequence presented in section II.2, and of Eqs. (2), and (4) – (12) the average value of the switching losses of the individual power semiconductors of one power module VUI30-12N1 can be derived.

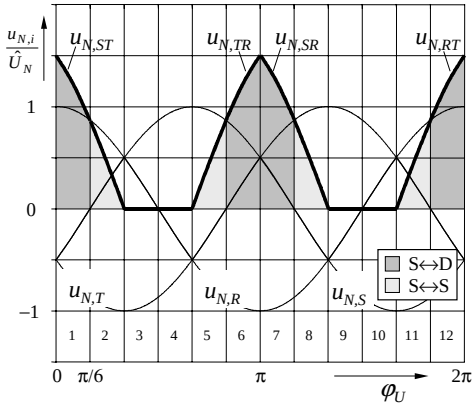


Fig. 7: *Switched voltage (denoted by a bold line) of the power transistor S_R as formed by segments of the line-to-line voltages for the switching state sequence given in section II.2, and mains phase voltages $u_{N,i}$ according to Fig. 2. The dark (light) gray shaded areas denote switching actions with high (low) value of the switched voltage.*

Based on Fig. 7 one receives for the average value of the losses of the power transistor S_i

$$P_{S_i} = \tfrac{1}{\pi} I\cdot f_P\cdot\hat{U}_{N_{LL}}\cdot\left[\left(\underset{S\to S}{k_{OFF,S}}+\underset{S\to S}{k_{ON,S}}\right)\cdot\left(2-\sqrt{3}\right)+\right.$$
$$\left.+\left(\underset{S\to D}{k_{OFF,S}}+\underset{D\to S}{k_{ON,S}}\right)\cdot\left(\sqrt{3}-1\right)\right]+\frac{2I\cdot M}{\pi}\left(U_{CE,0}+r_{CE}\cdot I\right) \tag{16}$$

and for one power diode $D_{i,(N)}$

$$P_{D_{i,(N)}} = \tfrac{1}{\pi} I\cdot f_P\cdot\hat{U}_{N_{LL}}\left[\underset{S\to S}{k_{ON,D}}\cdot\left(2-\sqrt{3}\right)+\right.$$
$$\left.+\underset{D\to S}{k_{ON,D}}\cdot\left(\sqrt{3}-1\right)\right]+\frac{I\cdot M}{\pi}\left(U_{F,0}+r_D\cdot I\right). \tag{17}$$

For the free-wheeling diode D_F one receives

$$P_{D_F} = I\left(1-\frac{3M}{\pi}\right)\cdot\left(U_{F,0(D_F)} + r_{D(D_F)}\cdot I\right) \qquad (18)$$

IV.2 Maximum Output Power Allowable With Regard to Junction Temperature Maximum Rating

In connection with a practical realization of a PWM rectifier system the obtainable maximum output power $P_{0,max}$ (for a given switching frequency f_P, and a given heat sink temperature T_S) is of special interest. According to Eqs. (16)–(18) for fixed mains line-to-line voltage amplitude $\hat{U}_{N,LL}$ the maximum rectifier power is defined by the allowable maximum value of the DC link current I, and, therefore, finally by the switching and the conduction losses in connection with the allowable thermal stress on the power semiconductors.

For a calculation of $P_{0,max}$ we have to define for each power semiconductor device of the module (transistor S_i, and diodes $D_{i,(N)}$) a maximum allowable value of the junction temperature $T_{J,max}$. With this, the maximum allowable semiconductor loss

$$P_{\max} = \frac{1}{R_{th,JS}}\cdot(T_{J,\max} - T_S) \qquad (19)$$

can be determined for a given heat sink temperature T_S. If one sets this power loss equal to the sum of conduction losses and switching losses (known from section IV.1 in dependency on the buck stage output current I)

$$P_{\max} = P_S\{I; f_P\} + P_C\{I\} \qquad (20)$$

one can directly calculate the DC link current I for the respective considered device. The allowable stress on the module is then defined by that semiconductor element which shows the lowest value of I.

As the comparison of the maximum allowable output power levels P_0 for the transistor and the diode shows, the obtainable output power of the rectifier system is limited by the thermal stress on the diodes for frequencies lower than $f_P \approx 13$ kHz. For higher switching frequencies the output power is limited by the losses of the power transistors. The results of an evaluation of Eqs. (16) and (17) are shown in **Fig. 8**, the calculations are based on the following operating parameters of the system, and characteristic values of the power module:

$T_{J,\max}$ = 125°C
T_S = 75 °C
$R_{th,JS,T}$ = 0.6 K/W (transistor)
$R_{th,JS,D}$ = 1.8 K/W (diode)
$U_{N,LL}$ = 400 V
M = 0.9.

The value $T_{J,\max}$ = 125 °C (lying below the maximum allowable junction temperature $T_{J,\max}$ = 150 °C given in the data sheets) is selected under consideration of a sufficient safety margin for the calculation which is based on a multitude of approximations, and with respect to a high reliability of the rectifier system. The value T_S = 75 °C corresponds to a value being commonly used for the dimensioning of a power supply for a maximum ambient temperature of T_a = 40 °C...50 °C. The modulation index of the buck input stage M is set to 0.9 in order to have a margin of 10 % for control and active damping of the low-pass input filter [10], [11]. For the constants of proportionality k between switching losses and switched voltage the values for T_J = 120 °C are used for the calculations (cf. Tab. I), whereby an additional safety margin is given (at higher pulse frequencies only the transistors reach a junction temperature of 120 °C, the power diodes remain at lower temperature, correspondingly the losses are decreasing, which results in an a higher efficiency.

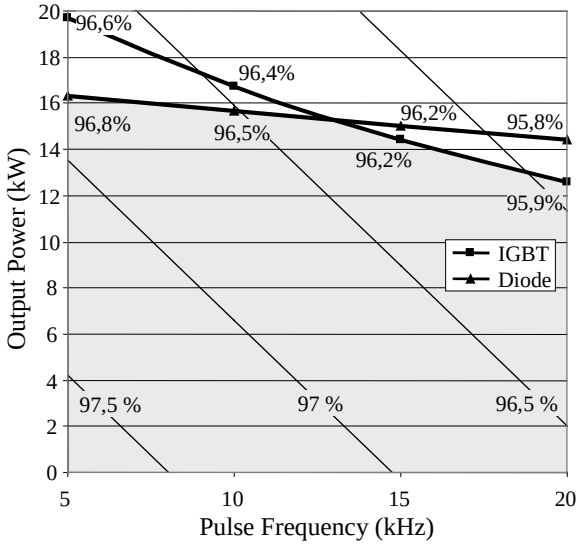


***Fig. 8**: Maximum allowable output power of the buck stage of the system shown in Fig.1 realized by combination of three modules VUI30-12N1 in dependency on the pulse frequency ("safe operating area" marked in gray), and lines of constant efficiency.*

IV.3 Efficiency and Loss Distribution

In the following, the efficiency of the buck input stage (considering only the losses in the power modules and in the free-wheeling diode) is estimated, and the contribution of the power transistor and of the power diodes to the switching losses and to the conduction losses of one module are shown graphically. It has to be pointed out that

- resistive losses of the input filter, of the buck+boost inductor, and of the output capacitor,
- the power consumption of the gate driver circuits, and of the control circuit, and
- the power consumption of the fans

are neglected. For the efficiency of the buck input stage there follows

$$\eta = 1 - \frac{P_{tot}}{P_{in}} \qquad (21)$$

with the total power semiconductor losses

$$P_{tot} = 3\cdot(P_{S_i} + 4P_{D_{(N)i}}) + P_{D_F}\,, \qquad (22)$$

the input power of the buck stage can be calculated via

$$P_{in} = \sqrt{3}U_{N,LL}\cdot\frac{I}{\sqrt{2}}\cdot M \qquad (23)$$

due to the impressed DC link current I.

In Fig. 8 lines for constant efficiency are shown. For constant output power P_0 the efficiency decreases with increasing pulse frequency f_P, for constant pulse frequency and increasing output power a decrease of the efficiency does occur.

The break-down of the total module switching losses, and total conduction losses to the power transistor, and to the power diodes are shown in **Fig. 9** for two pulse frequencies (f_P = 10 kHz and 20 kHz). The total losses of the power module at f_P = 10 kHz are set

equal to 100%, the losses at f_P = 20 kHz are given with reference to this value. One can see that in both cases the main share of the loss due to the conduction losses of the power diodes. For f_P = 20 kHz there is a slight decrease of the conduction losses as compared to f_P = 10 kHz due to the lower admissible power level ($P_{0,max}$ = 12.6 kW as compared to $P_{0,max}$ = 15.6 kW for 10 kHz), whereas the switching losses are doubled.

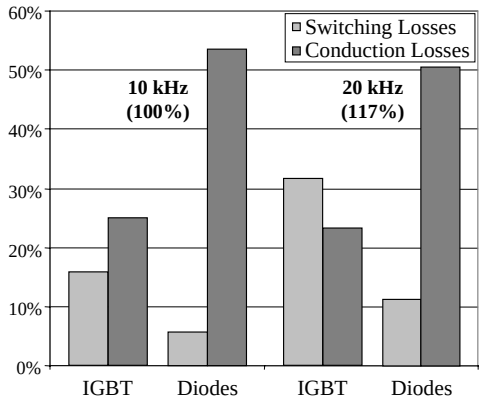


***Fig. 9**: Loss contribution of the components of a power module for maximum output power allowable at a pulse frequency of 10kHz and/or 20kHz.*

V. CONCLUSIONS

In this paper the switching losses and on state losses of a new power module for realization of one bridge leg of the buck input stage of a three-phase buck+boost PWM rectifier are analyzed. Based on this the maximum allowable output power of the buck stage is determined in dependency on the switching frequency. Furthermore, the efficiency of the buck input stage, and the loss contributions of power transistor and of the power diodes of a module are calculated at different pulse frequencies.

The considerations show, that a system output power of ≈15 kW with an efficiency of $\eta \approx 96.5$ % can be achieved for a mains voltage of 400 V_{rms} (line-to-line), a heat sink temperature of 70 °C, and a switching frequency of f_P = 10 kHz. For a pulse frequency of f_P = 20 kHz an output power of ≈ 12 kW can be reached for the same system parameters with an efficiency of $\eta \approx 96$ %.

For a switching frequency f_P = 10 kHz the main part of the losses (≈ 60 %) is due to the losses of the power diodes (forward recovery losses ≈ 10 %, conduction losses ≈ 90 %). Altogether, the power loss of the module is caused for f_P = 10 kHz by only ≈ 20 % by switching-frequency-dependent and by ≈ 80 % by switching-frequency-independent losses. For a switching frequency f_P = 20 kHz the power loss is caused by ≈ 37 % switching-frequency-dependent, and by ≈ 63 % switching-frequency-independent losses.

Regarding possible further developments of the power module we want to point out that (as Fig. 9 clearly shows) the main part of the losses is due to the conduction losses of the power diodes. For the development of a new power module one therefore should consider to employ diodes with a higher rated current, and a shorter reverse recovery time (there the dimensions of the module could stay the same but the internal layout would have to be adapted due to the larger footprint of the dies). As typical values there one could expect, e.g., a forward voltage drop U_{F0} = 1 V, and a differential on-resistance of r_D = 10 mΩ; also the reverse recovery time could be decreased by a factor 3 by using latest diode technology.

By this means, i.e., by reduction of the conduction losses of the power diodes an increase of efficiency of 0.8 % could be achieved, e.g., for a maximum admissible output power of $P_{0,max} \approx 13$ kW at a pulse frequency of f_P = 20 kHz one would reach η = 96.7 % instead of η = 95.9 % as in the case at hand. Considering furthermore the decrease of the switching losses due to a shorter diode reverse recovery time, a further improvement of efficiency up to η = 97 % seems to be possible. Under consideration of the losses due of control electronic, gate drive circuits, input filter and buck+boost inductor a total efficiency of the buck input stage of η = 96 % could be obtained, which is an acceptable value for the industrial application of the power module.

ACKNOWLEDGMENT

The authors are very much indebted to the *Hochschul-jubiläumsstiftung der Stadt Wien* which generously supports the work of the Power Electronics Group of the Department of Electrical Drives and Machines at the Technical University Vienna.

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