Experimental Evaluation of Space Vector Oriented Active DC-Side Current Balancing of Two Parallel Connected Three-Phase Three-Switch Buck-Type Unity Power Factor Rectifier Systems

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Abstract – In this paper the parallel connection of two three-phase buck-type unity power factor rectifier systems is investigated experimentally for a 10kW DSP-controlled prototype. There, a space vector modulation scheme is employed which shows all advantages of interleaved operation of the two systems. Three control schemes for active DC-side current balancing are described. The control schemes do differ concerning their control action and concerning additional switching losses. All control structures discussed in this paper are based on employing an additional free-wheeling states which do allow to influence the rate of change of the DC-side currents and can therefore be used for DC-side current balancing.

1 Introduction

In [1] the parallel connection of two three-phase/switch buck-type unity power factor PWM rectifier systems [2], [3] was theoretically investigated and a control concept for interleaved operation based on space vector modulation was proposed. At the Vienna University of Technology a prototype with a rated output power of 10 kW was realized by parallel connection of two single rectifier systems having a rated power of 5 kW [4], an input voltage range of (360...480)V_{rms} line-to-line and an output voltage of 400 V (cf. **Fig. 1**). The parallel systems are sharing a common LC input filter and are operating at $f_P \approx 24\,\text{kHz}$ switching frequency each. The parallel operation shows the following advantages over a single system with 10 kW rated power:

- input current harmonics of the partial systems with switching frequency do cancel each other, i.e. the first high frequency current harmonic occurring in the input current spectrum is at twice the pulse frequency, accordingly
- the input currents show a more continuous shape and therefore,
- the cut-off frequency of the input filter can be shifted to higher frequencies, resulting in a reduction of the input filter size; furthermore,
- the cross over frequency of the output current control can be shifted to higher frequencies, resulting in higher control dynamics; moreover,
- higher reliability is obtained; in case one rectifier system fails, reduced power still can be supplied.

To the knowledge of the authors, the parallel connection of two three-phase/switch PWM rectifier systems was treated in [5] and [6], but no control concepts for active DC-side current balancing were given in this publications.

In this paper, the control structure given in [1] is further improved and implemented, and the interleaved parallel connection of two rectifier systems is investigated experimentally with reference to the 10 kW DSP-controlled prototype. In **section 2** the basic principle of operation is described briefly and the implemented space vector modulation scheme is given. Furthermore, the possibility for DC-side current balancing by redundant switching states is treated. The principle of the proposed control structure is given in **section 3** and the influence of the additional switching state on the system operating behavior is investigated. The theoretical considerations are confirmed by digital simulations. In **section 4** the global and local system operating behavior is investigated experimentally and a modified control structure is proposed which allows to reduce additional switching losses.

2 Basics

In this section a brief outline of the basic principle of operation of the three-phase/switch PWM buck-type unity power factor rectifier is given based on single system operation. Furthermore, the modulation scheme employed for parallel operation of two rectifier systems as well as the time behavior of the resulting rectifier input currents and the corresponding rectifier input current space vectors are shown.

2.1 Principle of Operation

In order to obtain a resistive fundamental mains behavior, i.e. phase currents $i_{N,i}$ and/or fundamentals of the discontinuous rectifier input phase currents $i_{U,i}$, $i = R, S, T$, lying in

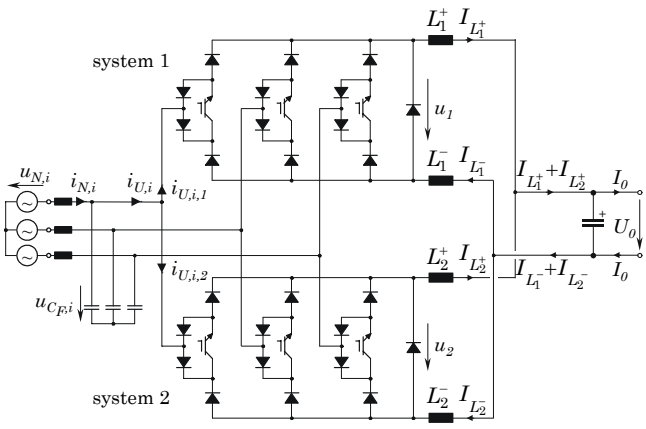

Fig. 1: Power circuit of the parallel connection of two three-phase/switch PWM rectifier systems.

phase with the corresponding mains phase voltages $u_{N,i}$ have to be formed (there, the voltage drop across the mains filter inductors L_F is neglected, i.e. $u_{N,i} \approx u_{C_F,i}$ is assumed). This is achieved by proper selection of the on-times of the power transistors S_i[1], whereby the output current is distributed sinusoidally to the mains phases. There, the output current is assumed to be impressed by the output inductors and does show a constant value. However, for deriving the modulation scheme the ripple components of the quantities on DC and AC side have to be considered, furthermore, switching losses of the power semiconductors have to be taken into account.

2.2 Modulation Scheme

The modulation scheme employed for the parallel connection of two three-phase buck-type rectifier systems was developed based on the modulation scheme of one system. The modulation scheme shows

(i) minimum switching losses [3],

(ii) a minimum ripple of the DC link inductor current [7] and of the input filter capacitor voltages [8] as well as

(iii) the possibility of active current balancing for two parallel connected rectifier systems (cf. section 3), furthermore,

(iv) during a $\pi/3$-wide mains interval one switch is clamped in the on-state.

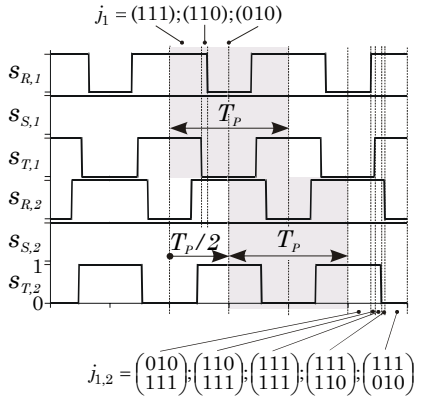

Fig. 2: Switching state sequences for the parallel connection of rectifier systems 1 and 2 within three pulse periods lying in mains interval 1. The modulation scheme for rectifier system 2 is obtained by phase-shifting of the modulation scheme of rectifier system 1 by one pulse half period. j_1 denotes the switching states for rectifier system 1, $j_{1,2}$ denotes the switching states for the parallel connection within one pulse half period.

In the proposed modulation scheme two active switching states (where current is drawn from the mains) and one free-wheeling state (the impressed output current free-wheels via the free-wheeling diode) are employed within one pulse half period, the free-wheeling state is placed subsequent to the active switching states at the end of each pulse half period. In the second pulse half period the switching states are arranged in reverse order, i.e. symmetrically to the middle of the pulse period. In **Fig.2** the switching functions $s_{R,1}, s_{S,1}, s_{T,1}$ of rectifier system 1 forming the active switching states $j_1 = (111)$ and $j_1 = (110)$ and the free-wheeling state $j_1 = (010)$ are shown for a mains voltage condition[2]

[1] For the characterization of a switching state of one system we use the combination $j = (s_R s_S s_T)$ of the phase switching functions s_i. There, the switching function does define the switching state of the corresponding power transistor, where $s_i = 0$ denotes the off-state, and $s_i = 1$ denotes the on-state.

[2] (1) is denoted as "interval 1" in this paper.

$$u_{N,R} > 0 > u_{N,S} > u_{N,T}, \tag{1}$$

with the mains phase voltages being defined as

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\varphi_U), \\ u_{N,S} &= \hat{U}_N \cos(\varphi_U - 2\pi/3), \\ u_{N,T} &= \hat{U}_N \cos(\varphi_U + 2\pi/3), \end{aligned} \tag{2}$$

where φ_U denotes the mains phase angle ($\varphi_U = \omega_N t$). The according rectifier input current space vectors $\underline{i}_{U,1}$ are given in **Fig.3**(a), Fig.3(b) shows the time behavior of the (discontinuous) rectifier input current $i_{U,R,1}$ in phase R in case of single system operation, i.e. rectifier system 2 is not connected in parallel.

The switching state sequence for rectifier system 2 is obtained by phase-shifting the modulation scheme of rectifier system 1 by half a pulse period $T_P/2$ whereby interleaved operation is achieved, cf. Fig. 2. The advantages of interleaved operation are

- cancellation of current harmonics occurring at pulse frequency f_P, i.e.
- the first high frequency current harmonic does occur at twice the pulse frequency, $2f_P$, and therefore
- the cut-off frequency of the input filter can be shifted to higher frequencies, resulting in a
- reduction of the input filter size as compared to one rectifier system for equal output power and in a
- higher admissible dynamic of the output voltage control; furthermore,
- the discontinuous rectifier input current does show a more continuous shape.

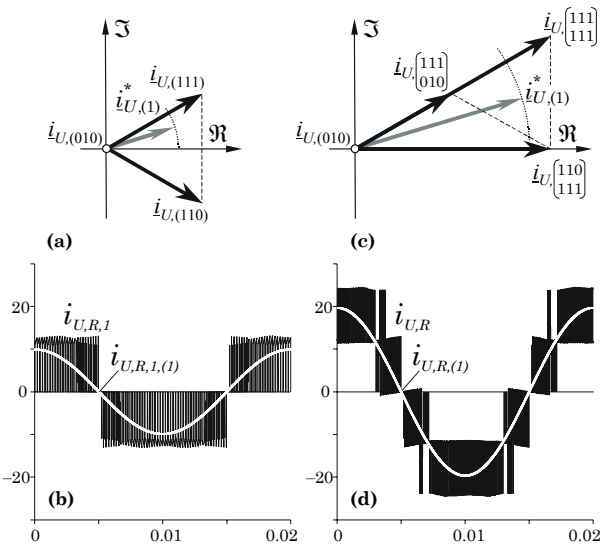

Fig. 3: Current space vectors and time behavior of the discontinuous rectifier input current in phase R for single system operation **(a),(b)** and parallel operation of two rectifier systems **(c),(d)**. Furthermore, the current fundamental $\underline{i}_{U,(1)}$ in the complex space vector plane and $i_{U,R,(1)}$ in the time domain, respectively, are given.

In Fig.2 all switching states of the parallel connection of the rectifier systems $j_{1,2}$ are given for one pulse half period, the total rectifier input current space vector $\underline{i}_U$ is calculated by adding the input current space vectors of systems 1 and 2,

$$\underline{i}_U = \underline{i}_{U,1} + \underline{i}_{U,2}, \tag{3}$$

the resulting input current space vectors for the considered interval 1 are depicted in Fig.3(c). The space vectors show three different magnitudes (apart from the zero vector), i.e., the total rectifier input current exhibits five different levels, which is also clearly shown in Fig.3(d) depicting the time behavior of the total rectifier input current in phase R. Moreover, the fundamental component for single system operation $i_{U,R,1,(1)}$ and for parallel connected rectifier systems $i_{U,R,(1)}$ is given.

2.3 Redundant Switching States

One set of total input currents $i_{U,i}$ of the parallel connection can be achieved by different switching states of the single rectifier systems. E.g., an input current condition

$$i_{U,R} = +I \quad i_{U,S} = 0 \quad i_{U,T} = -I \tag{4}$$

(I denotes the current in the DC-side inductors) is obtained if one system is in an active switching state,

$$i_{U,R,1} = +I \quad i_{U,S,1} = 0, \quad i_{U,T,1} = -I \tag{5}$$

while the other system is in the free-wheeling state,

$$i_{U,R,2} = i_{U,S,2} = i_{U,T,2} = 0. \tag{6}$$

The other possibility is switching both systems into an active switching state with

$$i_{U,R,1} = +I, \quad i_{U,S,1} = -I, \quad i_{U,T,1} = 0 \tag{7}$$

and

$$i_{U,R,2} = 0, \quad i_{U,S,2} = +I, \quad i_{U,T,2} = -I. \tag{8}$$

Both combinations (5) and (6) or (7) and (8) do result in input current condition (4), hence they are redundant switching states concerning input current formation. However, both possibilities do result in different rates of change $\mathrm{d}i/\mathrm{d}t$ of the currents in the DC-side inductors, whereby the DC-side current time behavior can be influenced.

However, the current change rates can not only be influenced by changing from an active to the free-wheeling state, but also by the free-wheeling state itself [9]. During the free-wheeling state one switch is clamped in the on-state (e.g., power transistor in phase S during interval 1, cf. Fig. 2). By default the power transistor of that phase showing the minimum absolute voltage (i.e. that phase lying in between the other two phases) is clamped in the on-state for a $\pi/3$-wide mains interval. Therefore, during the free-wheeling state the anode and (for neglecting the forward voltage drop) the cathode of the free-wheeling diode and hence the left-hand side terminals of the DC-side inductors of one rectifier system are connected to the mains phase having the power transistor in the on-state, i.e. phase S during mains interval 1.

The potentials of the terminals of the free-wheeling diodes and hence the DC current change rates during free-wheeling can be affected by turning on a different power transistor. E.g. if switch S_R is clamped in the on-state ($j_1 = (100)$) for a time interval $t_\pm$, cf. **Fig. 4**, the potential on the left-hand side inductor terminals is increased which results in an increase of the current in inductor L_1^+ of $\Delta i_{L_1^+}$ within one pulse half period as compared to the case where no additional free-wheeling state is incorporated into the switching state sequence, Fig. 4(b). On the other hand, employing $j_2 = (001)$ as additional free-wheeling state results in decreasing DC-side current. The value Δi_L can be increased (decreased) by increasing (decreasing) the on-time $t_\pm$ of the additional free-wheeling state. This can be used for an active DC-side current balancing as described in the following section.

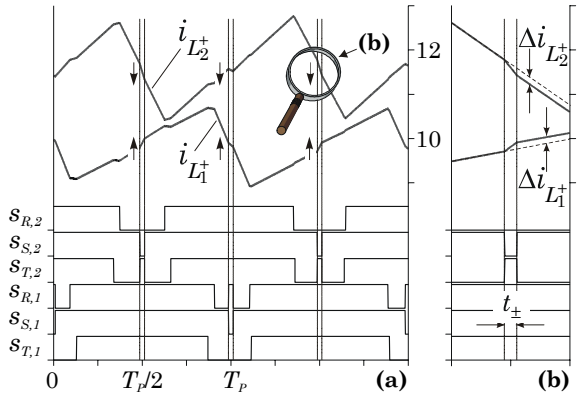

Fig. 4: Influence of the power transistor clamped in the on-state during free-wheeling on the rate of change $\mathrm{d}i/\mathrm{d}t$ of the DC link currents for different free-wheeling states within interval 1. The local time behavior of the DC-side inductor currents in L_1^+ and L_2^+ for unbalanced currents within two pulse periods and the switching functions of the rectifier systems are given in **(a)**; **(b)** shows the detailed time behavior within the additional free-wheeling state $t_\pm$. The arrows ↑ and ↓ indicate the desired direction for current changing.

3 Control Strategies

In order to ensure equal distribution of switching and conduction losses of the power semiconductors and in order to protect the rectifier systems from overloading and/or for limiting the current to its rated value, the DC output current has to be distributed equally to both rectifier systems. Ideally, there is no need for a current balancing control, because the modulation scheme developed in section 2.2 shows a natural stability of DC current sharing, i.e. if equal values of inductance are assumed, the DC-side currents show exactly the same value (neglecting the current ripple). However, due to non-ideal properties of an experimental setup, e.g. component tolerances like different values of inductance and resistance of the DC link inductors, forward voltage drops and/or different impedances of current conduction paths, the natural balance between the DC currents is disturbed. Therefore, a control structure has to be provided in case an unbalance of the DC-side currents does occur, which is described in the following [10].

3.1 Equivalent Circuit and Control Structure

In **Fig. 5** a DC/DC equivalent circuit of two parallel connected buck-type rectifier systems is given, where the buck-stage output voltage reference values u_1^*, u_2^* of rectifier systems 1 and 2 are splitted into two parts,

$$u_m^* = \underbrace{\Delta u_{pm}^* + u_0^*/2}_{u_{pos,m}^*} + \underbrace{\Delta u_{nm}^* + u_0^*/2}_{u_{neg,m}^*}, \quad m = 1, 2, \tag{9}$$

where $u_{pos,m}^*$ denotes the positive part and $u_{neg,m}^*$ denotes the negative part with reference to a common point C. The voltage sources $u_0^*/2$ represent a pre-control of the buck-stage output voltage which is defined by the output voltage reference value; the additional voltage sources Δu_{pm}^* and Δu_{nm}^* give the possibility for controlling the DC-side currents in the four inductors $L_{12}^\pm$. Furthermore, the actual output voltage u_0 across the output capacitor is considered in the equivalent circuit by a voltage source. The potential φ_C of common point C does equal the potential of that phase which is clamped in the on-state by default during free-wheeling within a $\pi/3$-wide mains interval, i.e. there is a voltage difference u_{CN} between the common point C and the neutral

N of the mains phase voltage system. The voltage difference u_{CN} shows three times the mains frequency, cf. **Fig. 6**. Via point C the paths of the two independent circulating currents i_{C1} and i_{C2} are closing, what is a significant difference as compared to paralleled boost-type rectifier systems where only one circulating current does exist due to the single DC-side energy storage (DC link capacitor), [11], [12].

If all DC-side inductor currents are balanced and equal to half the output current reference value $i_0^*/2$, voltage sources Δu_{pm}^* and Δu_{nm}^* are set to zero. In case an unbalance of the currents in, e.g., the DC-side inductors in the positive DC link rail is present, e.g. $i_{L_1^+} > i_{L_2^+}$, the potential φ_{p1} has to be decreased while φ_{p2} has to be increased in order to equilibrate the DC-side currents, i.e. $\Delta u_{p1}^* < 0$ and $\Delta u_{p2}^* > 0$. If the currents in the negative DC link rails do not show an unbalance, potentials φ_{n1} and φ_{n2} are not affected, i.e. $\Delta u_{n1} = 0$ and $\Delta u_{n2} = 0$. In summary, this results in decreasing the buck-stage output voltage reference value u_1^* for rectifier system 1 and in increasing the reference value u_2^* for rectifier system 2, whereby the buck-stage output current of rectifier system 1 is decreased and the buck-stage output current is increased. However, the total rectifier output current I_0 is not affected.

Increasing and decreasing the potentials φ_{p1} and φ_{p2} is realized by employing the additional free-wheeling states as described in section 2.3. Considering interval 1, switching state $j = (010)$ is used as free-wheeling state by default; therefore switching state $j = (100)$ is used to increase the positive potentials φ_{pm} due to $u_{N,R} > u_{N,S}$, while $j = (001)$ does decrease the positive potentials due to $u_{N,T} < u_{N,S}$.

The relative on-time $\delta_\pm$ of the additional free-wheeling state can be calculated via

$$\delta_+ = \frac{u_{pm}^*}{u_{ph,+} - u_{ph,cl.}} \quad \text{for } u_{pm}^* > 0, \tag{10}$$

$$\delta_- = \frac{u_{pm}^*}{u_{ph,-} - u_{ph,cl.}} \quad \text{for } u_{pm}^* < 0, \tag{11}$$

where $u_{ph,cl.}$ denotes the voltage of that phase where the power transistor is clamped in the on-state by default (shown in bold face in Fig. 6); $u_{ph,\pm}$ is the voltage of that phase where the power transistor is in on-state during the additional free-wheeling state, cf. Fig. 6. There $u_{ph,+}$ is used to increase

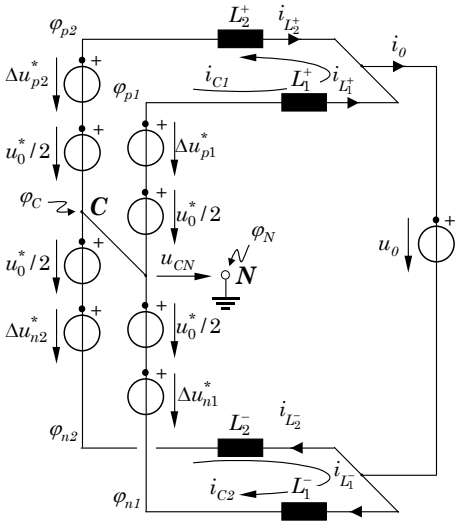

Fig. 5: DC/DC equivalent circuit of two parallel connected buck-type rectifier systems showing the circulating currents i_{C1}, i_{C2} representing DC side current unbalance and the potentials φ_{pm}, φ_{nm}, $m = 1, 2$ on the left-hand side of the DC-link inductors $L_{12}^\pm$.

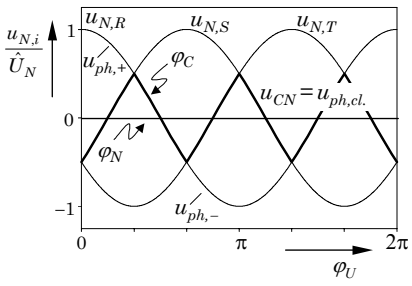

Fig. 6: Normalized mains phase voltages $u_{N,i}$, potential φ_C of the center point C of the equivalent circuit depicted in Fig. 5 and potential φ_N of the mains neutral point N; the voltage u_{CN} between center point and neutral point is depicted in bold face.

the positive potential and $u_{ph,-}$ is to decrease the positive potential, i.e for increasing the negative potential.

A corresponding control structure is given in **Fig. 7**, there the output current reference value i_0^* provided from an outer output voltage control loop (which is not shown) is divided by the number n of parallel connected rectifier systems and compared to the actual (filtered) DC-side currents. P-type controllers (gain k_{PV}) do set the reference value of the positive and negative voltages Δu_{pm}^*, Δu_{nm}^*, these reference values are transformed into buck-stage output voltage reference values u_m^*, where a pre-control with the total output voltage reference value u_0^* is provided. The relative on-times of active switching states δ_{im} for both rectifier systems are calculated according to (29)–(32) in [3], the durations of the additional free-wheeling states $\delta_{\pm m}$ are calculated using (10) and (11).

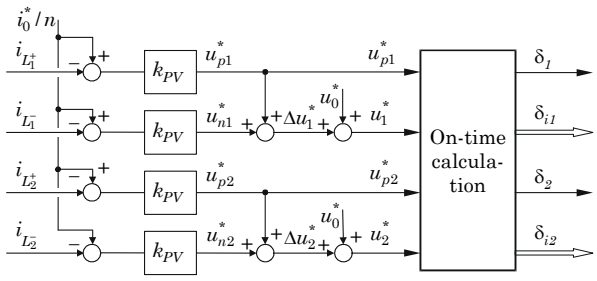

Fig. 7: Control structure for balancing the DC-side inductor currents based on the DC/DC equivalent circuit depicted in Fig. 5.

3.2 Simulation Results

In this section, the principle of operation of the proposed control structure is treated based on digital simulations using CASPOC. There the global time behavior as well as the influence of the additional free-wheeling state on the AC and DC-side currents is investigated.

The system parameters are set to

$$\begin{array}{llll} L_{12}^\pm & = 1\,\text{mH}, & U_{N,ph} & = 235\,\text{V} \\ U_0 & = 400\,\text{V} & I_0 & = 25\,\text{A} \\ f_N & = 50\,\text{Hz} & f_P & = 25\,\text{kHz}, \end{array}$$

(f_N denotes the line frequency, f_P the pulse frequency). In **Fig. 8** the time behavior of mains phase currents $i_{N,i}$ and of the DC-link currents is shown. For $t < t_1$ the balancing control loop is deactivated. As no source of unbalance (which could be present for a real system) is inserted in the parallel connection of the rectifier systems an ideally symmetric partition of the total DC current to the individual systems is given in this case. At $t = t_1$ a DC voltage source of 20 V is placed in series to DC link inductor L_1^+ in order to simulate a large unbalance. An unbalance of the DC link currents does occur immediately, which also results in a mains phase current distortion. At $t = t_2$ the control loop for DC-side current

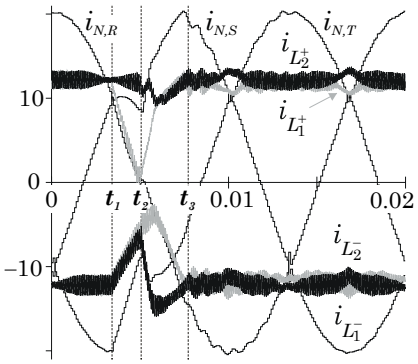

Fig. 8: Simulation results for unbalanced rectifier systems. Time behavior of mains phase currents and DC-side inductor currents in case a source of unbalance is added.

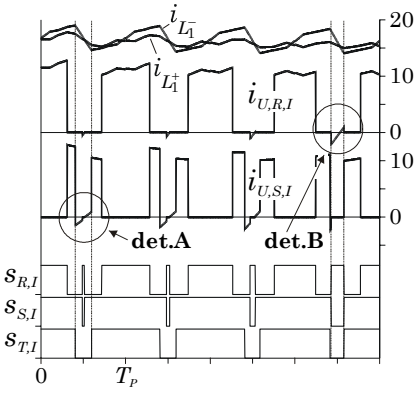

Fig. 9: Local time behavior of the currents in the parallel connection; currents of rectifier system 1 in L_1^+ and L_1^-, rectifier input current $i_{U,R,1}$ in phase R and $i_{U,S,1}$ in phase S and corresponding switching signals. For details **det.A** and **det.B** refer to the text.

balancing is activated by adding the additional free-wheeling states, whereby the symmetry of the currents is regained at $t = t_3$.

3.3 Circulating Current

Due to the different behavior of the current ripple in the DC-side inductors in the positive rail L_1^+, L_2^+ and in the negative rail L_1^-, L_2^- (e.g. time instant t_1 in Fig. 8) the instantaneous values of the currents of one rectifier system (e.g. current in L_1^+ and L_1^-) do differ from each other[3], whereby a differential current i_d results,

$$i_d = i_{L_1^+} - i_{L_1^-}, \tag{12}$$

which flows as a circulating current via the rectifier input into the second rectifier system. In **Fig. 9** the differential current is clearly shown during the free-wheeling state; for switching state $j = (010)$ (cf. **det.A**) the power transistor in phase S is clamped in the on-state, the differential current i_d resulting is flowing via phase S, and since the on-time of the additional free-wheeling state $j = (100)$ is approximately equal to zero, the differential current via phase R is negligible. For increasing on-time of the additional free-wheeling state (cf. **det.B**) phase R takes over the differential current i_d. However, a current path for the additional current has to be ensured, therefore one *must not* switch all power transistors into the off-state during free-wheeling.

4 Experimental Investigation

4.1 Experimental Setup

The experimental investigation was carried out on the parallel connection of two prototypes each having the following operating parameters

P_0	$= 5\,\mathrm{kW}$	f_N	$= 50\,\mathrm{Hz}$
$U_{N,l-l}$	$= 208\,\mathrm{V} \ldots 480\,\mathrm{V}$	f_P	$= 23.4\,\mathrm{kHz}$
U_0	$= 400\,\mathrm{V}$	$C_{F,i}$	$= 4\,\mu\mathrm{F}$
$L_{F,i}$	$= 0.17\,\mathrm{mH}$	C_0	$= 750\,\mu\mathrm{F}$
$L^{\pm}$	$= 0.9\,\mathrm{mH}$,		

which results in a total output power of $P_0 = 10\,\mathrm{kW}$ and/or a total output current of $I_0 = 25\,\mathrm{A}$ @ $400\,\mathrm{V}$ output voltage. The control is realized by a 32-bit floating point digital signal processor ADSP-21061 SHARC (Analog Devices).

[3] A difference in L_1^+ and L_1^- would not be present for a single rectifier system.

4.2 Influence of the Additional Free-Wheeling State

Ideally, if the DC-side current ripple is neglected and ideal switching behavior and/or no switching delay is assumed, the transition between the default free-wheeling state and the additional free-wheeling state (and vice versa) does occur without additional losses since the output current is guided via the free-wheeling diode and the power transistor which is in the on-state during free-wheeling does not carry any current. However, as a closer experimental investigation shows, the transition between two free-wheeling states does not happen directly but via an additional active switching state, e.g. at the transition from free-wheeling state $j = (010)$ to $j = (100)$ the active switching state $j = (110)$ does occur (cf. **Fig. 10**) which results in additional switching losses. This is due to the fact that the power transistor which is clamped in the on-state during free-wheeling does carry the differential current i_d (cf. (12)) and the power transistor which is clamped during the additional free-wheeling state has to take over this differential current.

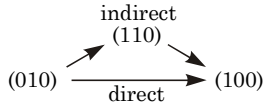

Fig. 10: Transition from one free-wheeling state to the subsequent free-wheeling state: direct, i.e in the ideal case, and indirect, i.e. via an additional active switching state.

In **Fig. 11** the time behavior of the discontinuous rectifier input currents $i_{U,R}$, $i_{U,S}$ is given for different on-times $t_{\pm}$ of the additional free-wheeling states. First, an additional free-wheeling state $t_{\pm} \approx 1\mu\mathrm{s}$ is applied to the rectifier system by turning on power transistor S_R and turning off S_S simultaneously at t_1 (cf. switching signal s_R in Fig. 11(a), s_S is not shown). After a time delay t_d (resulting from gate drive units and from turn-on and turn-off delay times of the power transistors) the switching action takes place at t_2, and for a time t_{add} both power transistor S_R and S_S are in the on-state (cf. gate drive signals V_{GE_R} and V_{GE_S} in Fig. 11(b)) and the differential current is commutated from switch S_S to S_R. Therefore an additional active switching state $j = (110)$ occurs where current is drawn from the mains and the free-wheeling diode D_F takes over blocking voltage (cf. Fig. 11(a), $V_{D_F} \neq 0$ at t_2). At the subsequent transition from (100) to (010) at t_3 the additional active switching state (110) is inserted again. Secondly, the additional free-wheeling state is decreased in on-time, e.g. to $t_{\pm} \approx 0.3\mu\mathrm{s}$, whereby the duration of the inserted active state exceeds $t_{\pm}$, hence no additional free-wheeling state does occur, cf. Fig. 11(c).

The ocurrence of the undesired additional active switching state has the following consequences,

- the duration of the additional free-wheeling state is decreased to $(t_{\pm} - 2\,t_{add})$,

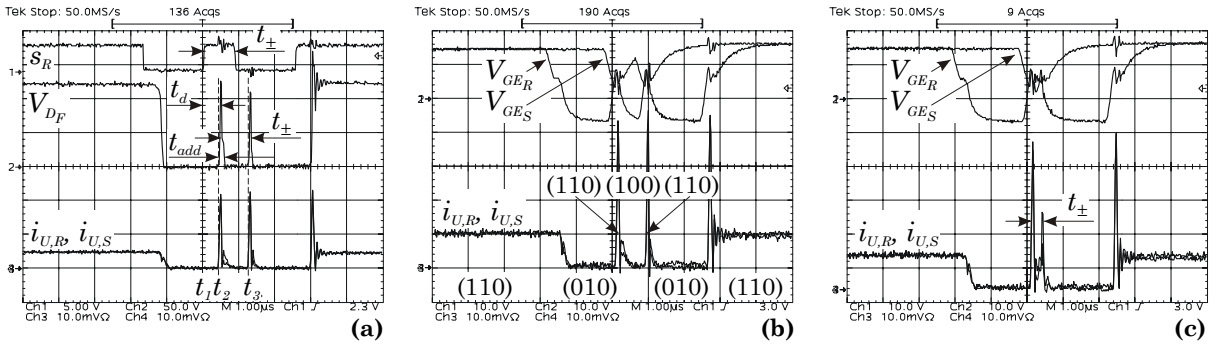

Fig. 11: Influence on the additional free-wheeling state on the rectifier input current behavior for a transition from free-wheeling state $j = (010)$ to (100) (and vice versa) in interval 1 for rectifier system 1. Additional free-wheeling state $t_\pm \approx 1\mu$s **(a)**, **(b)** and $t_\pm \approx 0.3\mu$s **(c)**. Switching signal s_R and voltage V_{D_F} across the free-wheeling diode (a), gate-drive signals V_{GE_R} and V_{GE_S} for the power transistors in phases R and S (b), (c), and rectifier input currents $i_{U,R}$ and $i_{U,S}$ (a)-(c). Current scales: (a): 4 A/div, (b), (c): 2 A/div. Voltage scales: (a): V_{D_F}: 50 V/div; s_R: 5 V/div; (b), (c): V_{GE}: 10 V/div.

- for a short duration $t_\pm$ the additional free-wheeling state is completely replaced by an active switching state, and
- at the (ideally lossless) transition from one free-wheeling state to the subsequent free-wheeling state switching losses do occur which can not be neglected.

In an experimental setup the control deviation between reference value and actual value of the current will always differ from zero due to errors in measurement, e.g. caused by offsets of current transducers and/or errors at the A/D-conversion, etc. This results in a permanent correction and/or a permanent presence of an additional free-wheeling state and/or a permanent increase in switching losses also in case the currents in positive and/or negative DC-link rail are (approximately) equal and no controlling action would be necessary. Therefore a modified control structure based on the control proposed in section 3 is chosen which is based on a bang-bang control and described in the next subsection for the parallel connection of two rectifier systems.

B.1 Modified Control Structure

In **Fig. 12** the modified control structure is depicted, there the currents in the DC-link inductors L_1^+, L_2^+ of rectifier systems 1 and 2 are controlled to equal values, where the current reference value $i_0^*/2$ again is provided by an outer output voltage control loop. u_1^* and u_2^* do represent the reference values for the buck-stage output voltage and are incorporated into the calculation of the relative on-times of the active switching states δ_{im} of both rectifier systems. It is assumed that the output current partitioning to both negative DC-link rails is approximately equal by default (cf. section 4.3). In case a deviation from half the output current $i_0/2$ does occur which exceeds a given value $\pm h$ an additional free-wheeling state $\delta_{\pm,1}$ is provided in rectifier system 1 which forces current $i_{L_1^-}$ (and hence current $i_{L_2^-}$) back to its reference value. There $\pm h$ represents the width of the tolerance band which is set to, e.g. ± 0.5 A, i.e. a control action only does take place if the difference of the average value of the negative DC-link currents is higher than 1 A.

For further reducing the switching losses which are occurring due to the additional free-wheeling state the duration of the additional free-wheeling state $\delta_\pm$, is set to the maximum possible value, i.e. the duration of the default switching state δ_{FW}. Thereby, the additional switching losses are avoided for additional free-wheeling state $j = (100)$ in interval 1 due to the fact that the power transistor in phase R is clamped in the on-state instead of the transistor in phase S, cf. **Fig. 13**(b).

For the additional free-wheeling state $j = (001)$ additional switching losses do occur at time instants t_1 and t_2 because the switching actions take place in all three bridge legs, cf. Fig. 13(c). But the additional switching losses are limited as compared to the case where an additional free-wheeling state with $t_\pm < t_{FW}$ is placed in the middle of the pulse period.

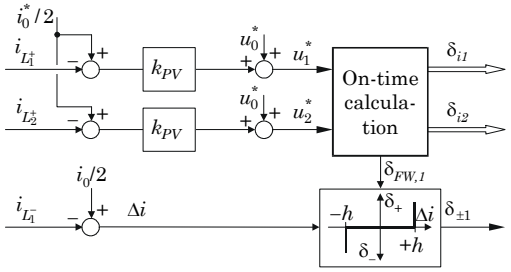

Fig. 12: Modified control structure for balancing the DC-side inductor currents based on a bang-bang control, $\pm h$ represents the width of the hysteresis.

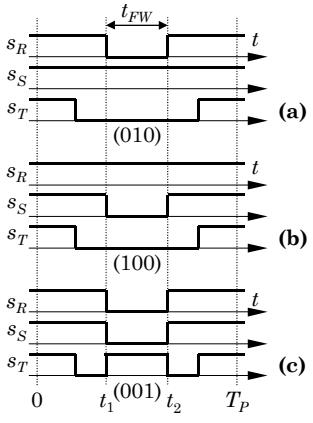

Fig. 13: Substitution of the default free-wheeling state by the additional free-wheeling state given for interval 1; **(a)** default free-wheeling state $j = (010)$ with on-time t_{FW}; **(b)** default free-wheeling state replaced by free-wheeling state $j = (100)$ (no additional switching losses do occur); **(c)** default free-wheeling state replaced by free-wheeling state $j = (001)$ (limited additional switching losses).

However, one has to mention that for decreasing modulation index M, $M = \hat{I}_N/I$, and for a constant source of unbalance the time behavior of the DC-side currents which are controlled to be equal by the additional free-wheeling state does get more and more disturbed. This is due to the fact that for decreasing modulation index the relative on-time δ_{FW} of the free-wheeling state does increase, whereby the influence on balancing the DC-side currents does increase, too. Therefore, an improvement of the control scheme could be

achieved by combining the basic control structure and the modified control structure, cf. **Fig. 14**. There, the additional free-wheeling state is used in case the average values of the negative DC-link rail currents exceed a given hysteresis value, but as compared to control structure given in Fig. 12 the relative on-time of the additional free-wheeling state is calculated according to (10) or (11), and the additional free-wheeling state is placed in the middle of one pulse half period according to Fig. 4.

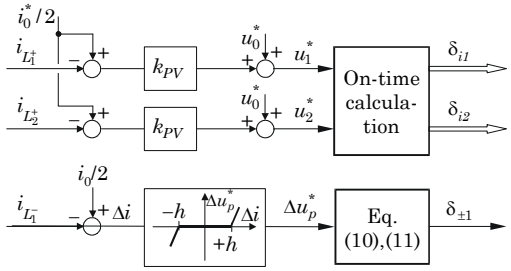

Fig. 14: Control structure for balancing the DC-side inductor currents based on a bang-bang control scheme with variable on-time of the additional free-wheeling state.

In a first step the control structure depicted in Fig. 12 was implemented in the experimental system by proper programming of the DSP, measurement results are given in the following subsection.

4.3 Evaluation of the Control Structure

The experimental investigation identifies a very good self-balancing behavior of the DC-side inductor currents, cf. **Fig. 15**(a). Since no source of unbalance is added in the experimental setup the currents in the positive and negative DC-link rails are approximately equal (only a negligibly small difference of a few 0.1 A does occur) independent on the mains phase voltage, on the output voltage and current and/or on the modulation index M.

In order to evaluate the operating behavior of the control scheme proposed in section B.1 a power resistor is added in series to the DC-side inductor L_1^+ in order to simulate a source of unbalance. For the given operating point, i.e. for an output current of 10 A, 100 V output voltage and 210 V line-line voltage, the resistance is set to $R \approx 1\Omega$ resulting in a voltage drop of 5 V (5 % of the output voltage) and/or heavy unbalance of the currents in the negative DC-link rails. The currents in the positive DC-link rails remain in balance due to their direct control, cf. Fig. 15(b). At t_1 the balancing control was activated, whereby the currents are immediately controlled to equal values within a hysteresis of ± 0.6 A.

Figure 15(c) does show the limits of the proposed control concept: one can see that in the neighborhood of a boundary B between two mains intervals as defined by a combination of signs of the mains phase voltages the effect of the additional free-wheeling state (and/or the balancing capability) is limited and/or close to zero; the current in inductor L_2^- has to be decreased, and although additional free-wheeling states are added the current is further increasing. This is due to the decreasing difference between the mains phase voltages – which is responsible for guiding back the currents to equal values – when approaching a mains phase voltage interval boundary. E.g. at the left boundary of interval 1 ($\varphi_U = 0$ in Fig. 6) the difference between mains phase voltages $u_{N,S}$ and $u_{N,T}$ is equal to zero, hence additional free-wheeling state $j = (001)$ will have no influence on the rates of change of the currents in the DC-side inductors at $\varphi_U = 0$. The influence increases with increasing mains phase angle φ_U, therefore current $i_{L_2^-}$ is guided back to the reference value with increasing distance from the interval boundary. The switching signals $s_{i,1}$ do show the occurrence of additional free-wheeling states.

4.4 Interleaved Operation Behavior

The advantage of an interleaved operation resulting in five levels of the total retifier input current is clearly shown in **Fig. 16** (cf. section 2.2 and Fig. 3). Rectifier systems 1 and 2 do show discontinuous rectifier input currents (cf. currents in phase R, $i_{U,R,1}$ and $i_{U,R,2}$). By phase-shifting corresponding switching signals of the parallel systems by half a pulse period the discontinuous input currents are added in such a manner that the total rectifier input current does show five levels, cf. Fig. 16(a), i.e. a more continuous shape with reduced ripple amplitude as compared to non-interleaved operation. There are sections where the discontinuous currents of the single rectifier systems do overlap in time, cf. Fig. 16(b), the total rectifier input current therefore alternates between levels I and $2I$, where I is the average value of the DC-link currents. Where the corresponding mains phase current $i_{N,R} \approx i_{U,R,(1)}$ is passing through zero, the discontinuous rectifier input currents do not overlap any more which results in a total rectifier input current alternating between 0 and I, cf. Fig. 16(c). Furthermore, the circulating differential current described in section 3.3 resulting from the difference in current ripple values is clearly shown in detail **det.A** in Fig. 16(b).

5 Conclusions

In this paper three different control strategies for active DC-side current balancing for two parallel connected three-phase/switch buck-type PWM rectifier systems were presented based on a space vector modulation scheme which provides

- all advantages of an interleaved operation,
- minimum ripple of the DC link inductor currents and
- minimum ripple of the AC side filter capacitor voltage.

The control scheme does use an additional free-wheeling state for current balancing whereby the rate of change of the DC-side currents is influenced. The basic control scheme, where an additional free-wheeling state does occur in each pulse period, was improved in order to minimize additional switching losses which are present in a practical system at the transition to a subsequent free-wheeling state. There, a hysteresis control was added whereby control action only takes place when the average values of the DC-side currents do differ by a given value. Two possibilities for adding the additional free-wheeling state are proposed,

1. the total default free-wheeling state is replaced by the additional free-wheeling state whereby the additional switching losses are minimized and/or set to zero, or
2. the duration of the additional free-wheeling state is calculated in dependency on the DC current unbalance, whereby the control action varies (which results in increasing additional switching losses as compared to 1.).

The experimental investigation shows that there is a very good self-balancing of the DC-side inductor currents, due to parasitic effects which stabilize the current partitioning. The detailed investigation of these effects will be considered in a future paper.

If a heavy unbalance is added in series to the DC-side inductors a current unbalance does occur which depends on size and position (positive or negative DC-link rail) of the source

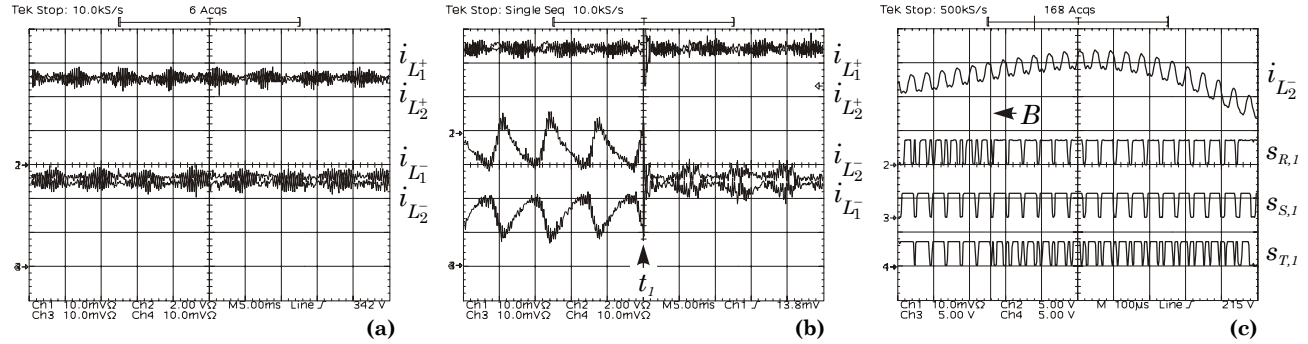

Fig. 15: Time behavior of the DC-side currents in inductors $L_{12}^{\pm}$ for 10 A output current, 100 V output voltage and 210 V line-line voltage. **(a)** Self-balancing of the DC-side currents (no control for current partitioning provided), **(b)** source of unbalance ($R \approx 1\ \Omega$) added in series to the inductor lying in the positive DC-link rail of rectifier system 1, time behavior before and after activating the balancing control loop, **(c)** detailed time behavior of the current in inductor L_1^- at an interval boundary B and corresponding switching signals $s_{i,1}$. Current scales: (a), (b): 2 A/div, (c): 1 A/div, 5 V/div.

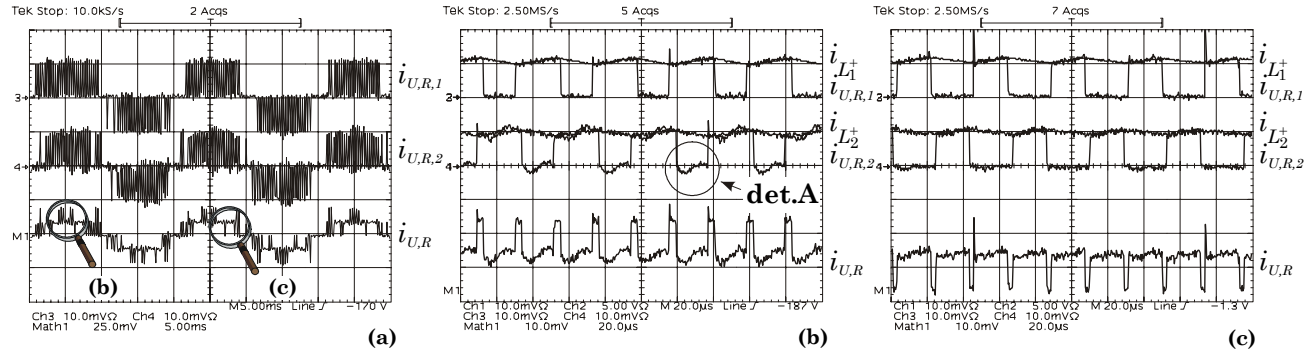

Fig. 16: Time behavior of the currents in inductors L_1^+, L_1^-, and L_2^+ and time behavior of discontinuous rectifier input currents of rectifier system 1 and 2 in phase R, $i_{U,R,1}$ and $i_{U,R,2}$, and total rectifier input current $i_{U,R}$ (obtained by adding $i_{U,R,1}$ and $i_{U,R,2}$) within one mains period **(a)** and detailed time behavior **(b)**, **(c)**. Detail **det.A** shows the circulating differential current during the free-wheeling state. Current scales: $i_{U,R,1}$, $i_{U,R,2}$, i_L: 5 A/div; $i_{U,R}$: (a): 12.5 A/div; (b), (c): 5 A/div.

of unbalance. The current unbalance is controlled within the given hysteresis, however, there is a limited controllability at the boundaries of the mains phase intervals. Furthermore, the correcting variable depends on the modulation index, i.e. for small modulation indices a bang-bang control structure with variable additional free-wheeling state is advantageous. A comparative evaluation of both bang-bang control structures in dependency on modulation index and/or position and size of an added unbalance will be investigated in a future paper.

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