Experimental Evaluation of a Three-Phase Three-Switch Buck-Type Unity Power Factor Corrector

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Abstract – In this paper the experimental evaluation of a 5 kW prototype of a three-phase three-switch buck PFC rectifier system is discussed. The basic principle of operation is treated briefly. The switching behavior of the power semiconductors is analyzed experimentally and based on the switching loss data gained thereby the maximum allowable output power of the system is calculated in dependency on the pulse frequency. Furthermore, the system efficiency is estimated. A breakdown of the losses to switching and on-state losses of the power semiconductors gives a basis for the further development of the rectifier system.

1 Introduction

In [1] a three-phase PWM rectifier formed by integration of a three-switch buck-derived front-end [2] and a DC/DC boost converter output stage has been proposed which gives the possibility of controlling the output voltage to 400V within a wide input range of $(90 \ldots 280)$ V mains phase voltage [3]. As substantial advantages of this concept one has to point out

- the resistive fundamental mains behavior, and
- the possibility of limiting the input current and the current in the DC link inductor for mains over-voltage, in contrast to rectifier systems with boost-type input stage.

Furthermore, the system shows

- high efficiency and high power density, and
- the advantageous possibility of omitting an auxiliary start-up circuit.

A prototype for a rated output power of 5 kW was realized using standard power semiconductors (e.g., TO 247 type packages). There, the system control is realized by a digital signal processor of type ADSP-21061 SHARC (cf. **Fig. 1**).

In this paper the maximum output power of the buck input stage (cf. **Fig. 2**) which can be achieved at different pulse frequencies is calculated. In **section 2** the basic principle of operation of the buck input stage is treated briefly, in **section 3** the results of the experimental switching evaluation are given, which are used in **section 4** to calculate the average switching energy losses. In **section 5** the practical applicability of the selected power semiconductor devices is evaluated.

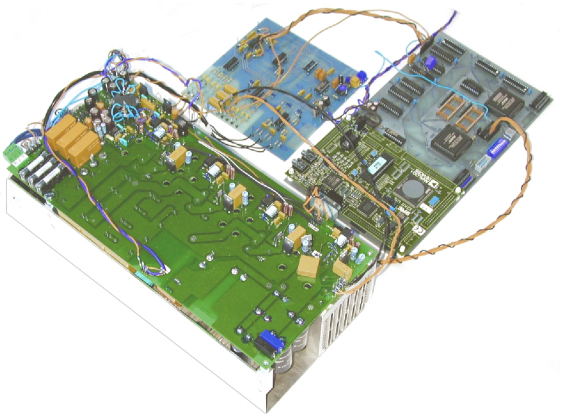

Fig. 1: Prototype of the buck+boost PWM rectifier system designed for a rated output power of 5kW and rated output voltage of 400V. Overall dimensions: $(34 \times 16 \times 12)\text{cm}^3 \doteq (13.4 \times 6.3 \times 4.7)\text{in}^3$. Shown are the power circuit, the digital signal processor board and an auxiliary PCB for signal acquisition and level adaption.

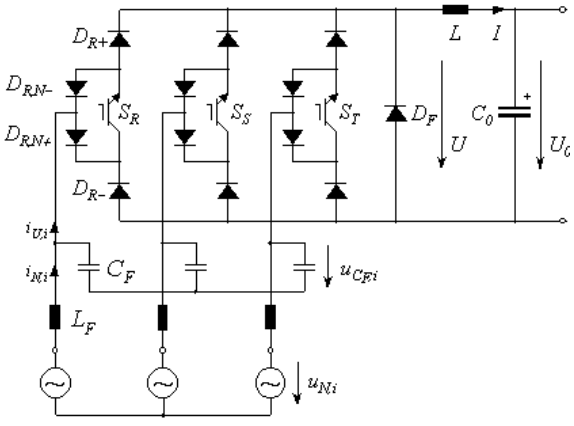

Fig. 2: Structure of the three-phase/switch buck input stage of the buck+boost PWM rectifier.

2 Basic Principle of Operation

For an ideally sinusoidal shape of the mains phase currents $i_{N,i}$, $i = R, S, T$, we would like to form fundamentals (denoted by the index (1)) of the rectifier input currents $i_{U,i}$ lying in phase with the mains phase voltages $u_{N,i}$ (which are approximately equal to the input filter capacitor voltages $u_{C_F,i}$),

$$i_{N,i} \approx i_{U,(1),i}. \tag{1}$$

Therefore, the relative on-times δ_{S_i} of the power transistors S_i have to be set proportional to the instantaneous value of the mains phase voltages and dependent on the required output current I of the buck input stage, which is assumed to be constant and impressed by the buck+boost output inductor L. With the modulation index M of the buck input stage

$$M = \frac{\hat{I}_N}{I} = \frac{\sqrt{2}\,U_0}{3\,U_{N,ph}} \tag{2}$$

(where U_0 denotes the average value of the output voltage of the buck stage, and $U_{N,ph}$ the rms value of the mains phase voltage) one receives for the relative on-times of the power transistors S_i

$$\delta_{S_i} = M\,\frac{|u_{N,i}|}{\hat{U}_{N,ph}}. \tag{3}$$

In order to achieve a high system efficiency, and a current ripple as small as possible a method for controlling the switching actions (switching state sequence) resulting in minimum switching losses has been identified in [1].

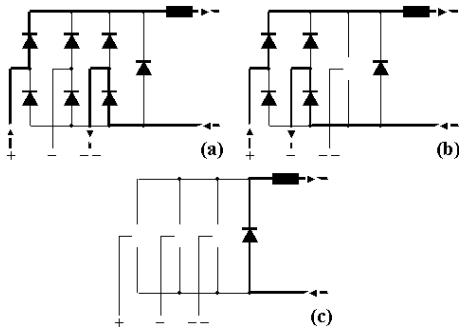

Fig. 3: Conduction states of the buck input stage valid for $u_{N,R} > 0 > u_{N,S} > u_{N,T}$, the current flow is indicated by a bold line. **(a)**, and **(b)**: Active switching states; **(c)**:Freewheeling state.

The proposed switching state sequence consists of two active switching states ($i_{U,i} = \pm I$) and of one freewheeling state ($i_{U,i} = 0$). In **Fig. 3** the switching states are depicted assuming mains phase voltages $u_{N,R} > 0 > u_{N,S} > u_{N,T}$. If a power transistor S_i is in on-state, the bridge leg of the buck input stage corresponds to a bridge leg of a diode bridge. Therefore, in Fig. 3 the diodes $D_{i,N\pm}$ and the power transistors S_i which are in on-state are omitted for the sake of clearness. If a power transistor is in off-state, all power semiconductors of the assigned bridge leg are omitted, too.

A prototype of the system (including a DC/DC boost output stage) was designed and realized for the following operating parameters:

$$\begin{aligned} P_0 &= 5\,\text{kW} \\ U_{N,ph} &= 90\,\text{V} \ldots 280\,\text{V} \\ U_0 &= 400\,\text{V} \\ f_N &= 50\,\text{Hz} \\ f_P &= 31.25\,\text{kHz} \end{aligned}$$

In **Fig. 4** the behavior of the mains phase current, the input filter capacitor voltage and the DC link current of the three-phase/switch buck rectifier system is given. Furthermore, the voltage across one power transistor (as required for calculating the switching losses, cf. section 4) is shown.

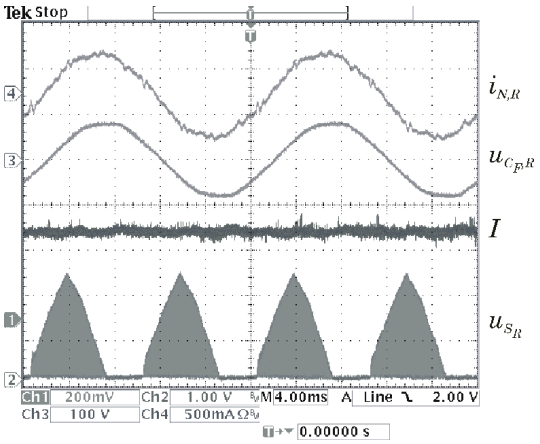

Fig. 4: Experimental analysis of the time behavior of the input current, input filter capacitor voltage, DC link current, and voltage across the power transistor in phase R.

3 Stresses on the Power Semiconductors

3.1 Experimental Switching Evaluation

For measuring the switching losses of the power semiconductors the mains AC voltages are replaced by auxiliary DC voltage sources, whereby a set of instantaneous values of the mains phase voltages can be simulated. Considering mains phase voltages

$$\begin{aligned} u_{N,R} &= \hat{U}_{N,ph}\,\cos(\omega_N t), \\ u_{N,S} &= \hat{U}_{N,ph}\,\cos(\omega_N t - 2\pi/3), \\ u_{N,T} &= \hat{U}_{N,ph}\,\cos(\omega_N t + 2\pi/3), \end{aligned} \tag{4}$$

(ω_N denotes the mains angular frequency), and the middle of the interval $u_{N,R} > 0 > u_{N,S} > u_{N,T}$ (i.e., $\omega_N t = \pi/12$), the auxiliary DC link voltages result in

$$\begin{aligned} U_{N,RS} &= 1.73\,U_{N,ph}, \\ U_{N,ST} &= 0.634\,U_{N,ph}, \\ U_{N,TR} &= -2.37\,U_{N,ph}. \end{aligned} \tag{5}$$

For a determination of the switching losses with good accuracy, and in order to cover the total input voltage range and/or different values of the output power P_0 mains phase voltages $U_{N,ph} \in (100; 250)\,\text{V}$ represented by auxiliary DC voltages (cf. (5)), and different currents in the range $I \in (5; 35)\,\text{A}$ are considered [4].

In order to cover all switching actions occurring within one pulse period the switching pattern shown in **Fig. 5** is provided. There, a variable time T_{rise} is used to adjust the DC link current I, the widths of the subsequent pulses are selected as $T = 4\mu$s. According to the low repetition rate of 1Hz the temperature rise due to switching losses is negligible, i.e., the heat sink temperature T_S can be assumed to be equal to the junction temperature T_J of the power semiconductor dies. The heat sink is heated up to $T_S = 120°\mathrm{C}$ in order to achieve a conventional operating temperature of the semiconductor dies.

The measurement of the transistor current is performed via a low-inductance shunt (cf. [5]) in order to avoid inaccuracies due to propagation delay like occurring for clip-on type current probes. The shunt is realized by $10 \times 1\,\Omega$ SMD-resistors in parallel connection, the voltage drop of the current to be measured is taken directly across the resistors by a coaxial cable.

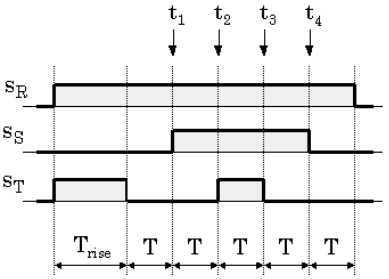

Fig. 5: Applied switching pattern.

3.2 Analysis of the Experimental Results

The turn-on and turn-off losses of the power transistors as well as the forward recovery losses of the power diodes are measured at the transitions of the phase switching functions t_i, $i = 1 \ldots 4$ (Fig. 5). For every switching action at least one factor of proportionality between the switching energy loss $W^n_{l,m}$ and the switched voltage and/or the switched current can be given, where l denotes either the turn-on ($l = \text{ON}$) or the turn-off ($l = \text{OFF}$) transition. The factor of proportionality refers to a switch, $m = S$, or a diode, $m = D$; n denotes the type of the switching action (commutation of the current I from one power transistor S_i to another ($n = S \to S$), or commutation from one power transistor to the free-wheeling diode D_F ($n = S \to D_F$), or vice versa ($n = D_F \to S$). E.g., at t_1 in Fig. 5 the current is commutated from the free-wheeling diode D_F to the power transistors S_R and S_S, hence turn-on losses $W^{D_F \to S}_{\text{ON},S}$ do occur in power transistor S_S (transistor S_R remains clamped in the on-state, therefore no switching losses occur in S_R, cf. section 4.2). The symbols in **Fig. 6** represent the measurement results of the turn-on losses $W^{D_F \to S}_{\text{ON},S}$. In order to be able to calculate the switching energy loss in an analytically closed form, the measurement results have to be expressed by a linear and/or quadratic approximation. In the case at hand, the turn-on losses can be approximated by

$$W^{D_F \to S}_{\text{ON},S} = 1\frac{\text{nJ}}{\text{AV}^2}\, I\, U^2_{N,ph} + 7.18\frac{\text{nJ}}{\text{V}^2}\, U^2_{N,ph}, \qquad (6)$$

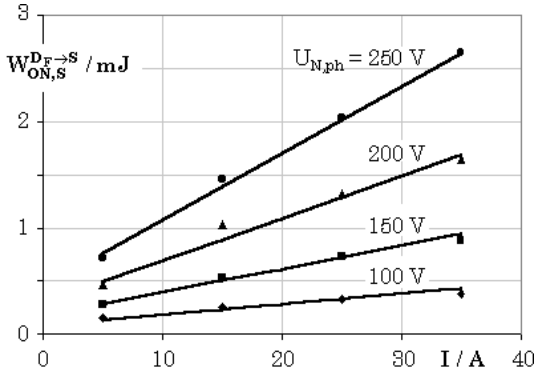

Fig. 6: Turn-on losses $W^{D_F \to S}_{\text{ON},S}$ in dependency on the DC link current I. Parameter of the family of curves: mains phase voltage $U_{N,ph}$ (measured for a set of auxiliary DC link voltages (5) corresponding to $U_{N,ph}$). The symbols show the measurement results, the approximation (6) is represented by continuous lines.

the current independent offset term denotes losses due to parasitic capacitances of the power circuit. As the continuous lines in Fig. 6 show, (6) gives a very good approximation of the measurement results.
Approximations for the losses occurring at the other switching transistions t_i are given in **Tab. 1** which gives the basis for an analytically closed calculation of the total switching power losses of the power transistors and power diodes in section 4.

t_i	$W^n_{l,m}$
t_1	$W^{D_F \to S}_{\text{ON},S} = 1\frac{\text{nJ}}{\text{AV}^2}\, I\, U^2_{N,ph} + 7.18\frac{\text{nJ}}{\text{V}^2}\, U^2_{N,ph}$
t_1	$W^{D_F \to S}_{\text{ON},D} = 5\frac{\mu\text{J}}{\text{A}}\, I$
t_2	$W^{S \to S}_{\text{ON},S} = 0.106\frac{\mu\text{J}}{\text{AV}}\, I\, U_{N,ph} + 1.11\frac{\text{nJ}}{\text{V}^2}\, U^2_{N,ph}$
t_3	$W^{S \to S}_{\text{OFF},S} = 0.1\frac{\mu\text{J}}{\text{AV}}\, I\, U_{N,ph}$
t_3	$W^{S \to S}_{\text{ON},D} = 2.67\frac{\mu\text{J}}{\text{A}}\, I$
t_4	$W^{S \to D_F}_{\text{OFF},S} = 0.731\frac{\text{nJ}}{\text{AV}^2}\, I\, U^2_{N,ph}$

Tab. 1: Approximation of the measurement results of the switching energy losses, where the mains phase voltage $U_{N,ph}$ is represented by auxiliary DC link voltages, cf. (5).

In the following, for different switching actions occurring within one pulse period the time behavior of the switched current and voltage is discussed. Regarding the transition from the free-wheeling state to an active switching state (t_1 in Fig. 5) the reduction of the transistor turn-on voltage U_{S_S} due to the forward recovery voltage of the power diodes $D_{R,N+}$, D_{R+}, $D_{S,N-}$, D_{S-} lying in series with the switched power transistor S_S (cf. item 1. in section 4.2) can be noticed. In **Fig. 7**(a) the forward recovery voltage of the power diode $D_{S,N-}$ is shown for a switched voltage of 400V and a switched current $I = 20$A. The peak value of the forward recovery voltage U_{FR} is ≈ 25V. In Fig. 7(b) the turn-on voltage of power transistor S_S is shown, which is reduced by four times a forward recovery voltage, $4\,U_{FR} \approx 100$V, whereby the turn-on loss of the

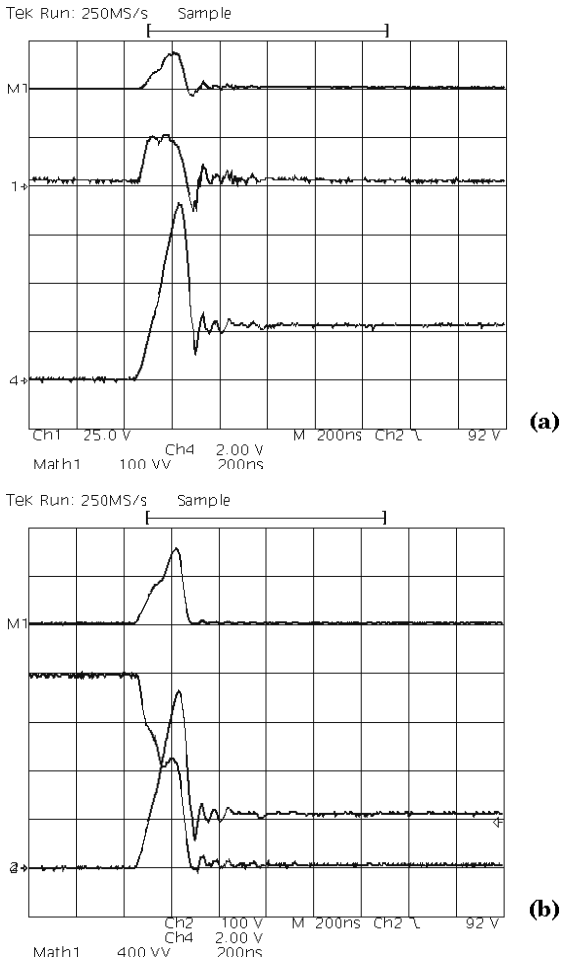

Fig. 7: Transition between free-wheeling state and active switching state (t_1 in Fig. 5) for $I = 20$A (current scale: 1V = 10A, power loss scale: 100VV = 1kW. **(a)**: forward recovery loss of power diode $D_{S,N-}$ (ultrafast diode RURG30100), and **(b)** turn-on loss of power transistor S_S (warp speed IGBT IRG4PF50W) at 120°C.

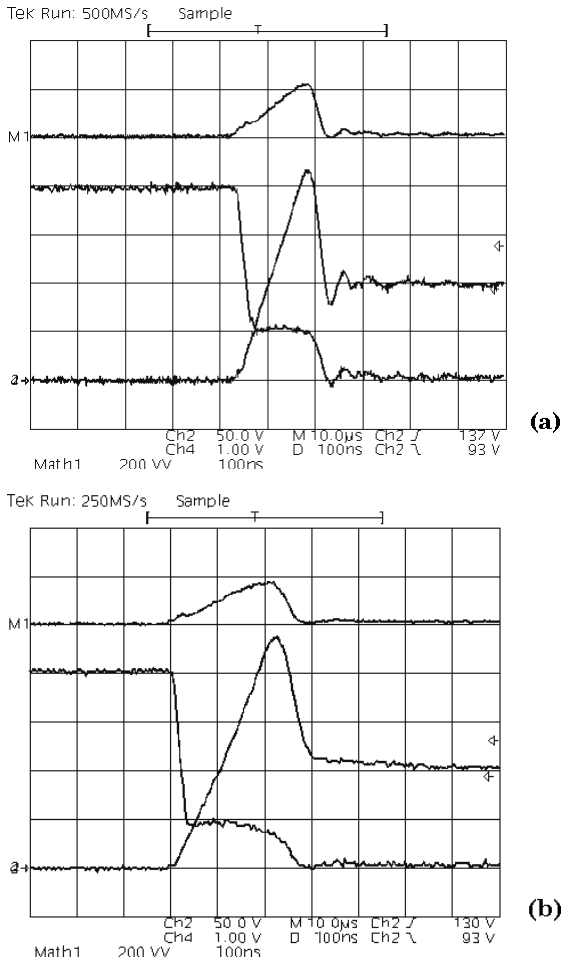

Fig. 8: Transition between two active switching states (t_2 in Fig. 5) for $I = 20$A (current scale: 1V = 10A, power loss scale: 100VV = 1kW. Turn-on behavior of power transistor S_R at 25°C **(a)**, and at 120°C **(b)**.

power transistor $W_{\mathrm{ON},S}^{D_F \to S}$ is reduced. But one has to point out, that turn-on losses (forward recovery losses) $W_{\mathrm{ON},D}^{D_F \to S}$ occur in the power diodes and/or part of the turn-on losses of the power transistor is transferred to the power diodes.

The switching behavior between two active switching states is shown in **Figs. 8**. In Figs. 8(a) and (b) the turn-on behavior of power transistor S_T is compared for two junction temperatures $T_J = 25°\mathrm{C}$ and $T_J = 120°\mathrm{C}$: An increase of the peak value of the reverse recovery current of only $\approx 10\%$ can be noticed, the reverse recovery time is increased by a factor of 1.5, however. Again, the decrease of the turn-on voltage due to the forward recovery of the power diodes involved in the switching action can be noticed.

4 Calculation of the Average Losses

4.1 Conduction Losses

4.1.1 Power Diodes

The forward characteristic of the power diodes as known from the data sheet (cf. Fig. 1 in [6]) can be approximated as

$$u_{D,F} = U_{F,0} + r_D\, i_D. \tag{7}$$

Accordingly, the average conduction loss of one power diode can be calculated using

$$P_D = I_{D,avg}\, U_{F,0} + r_D\, I_{D,rms}^2, \tag{8}$$

with

$$I_{D_{i,(N)\pm},avg} = \frac{1}{\pi}\,\hat{I}_N, \qquad I_{D_{i,(N)\pm},rms}^2 = \frac{1}{M\pi}\,\hat{I}_N^2 \tag{9}$$

for the diodes of the buck input stage, and with

$$I_{D_F,avg} = \frac{\pi - 3M}{M\pi}\,\hat{I}_N, \quad I_{D_F,rms}^2 = \frac{\pi - 3M}{M^2\pi}\,\hat{I}_N^2 \tag{10}$$

for the free-wheeling diode. The forward characteristic of both the diodes $D_{i,(N)\pm}$ and D_F is defined by $U_{F,0} = 0.92$V and $r_D = 10\mathrm{m}\Omega$ according to [6].

4.1.2 Power Transistors

Considering Fig. 2 in [7] the forward characteristic of the IGBTs can be approximated as

$$u_{S,F} = U_{CE,0} + r_{CE}\, i_S. \tag{11}$$

Accordingly, one receives for the average condction loss

$$P_S = I_{S,avg}\, U_{CE,0} + r_{CE}\, I^2_{S,rms} \tag{12}$$

with

$$I_{S,avg} = \frac{2}{\pi}\,\hat{I}_N, \qquad I^2_{S,rms} = \frac{2}{M\pi}\,\hat{I}^2_N. \tag{13}$$

According to [7] the forward characteristic of the power transistor is defined by $U_{CE,0} = 1.25\text{V}$ and $r_{CE} = 31\text{m}\Omega$.

4.2 Switching Losses

In order to explain the analytical calculation of the switching losses in detail, the different switching actions[1] (showing different switching losses) occurring within one pulse period are given in the following assuming a mains phase voltage condition $u_{N,R} > 0 > u_{N,S} > u_{N,T}$.

1. $t = t_1$, $(100) \rightarrow (110)$

- S_S is turned on
- current I commutates from the free-wheeling diode D_F to S_R, S_S
- **no** switching loss in S_R (clamped in the on-state, cf. [1])
- turn-on loss $W^{D_F\rightarrow S}_{\text{ON},S}$ in S_S
- switched voltage $U_{N,ST}$
- turn-on losses $W^{D_F\rightarrow S}_{\text{ON},D}$ in $D_{R,N+}$, D_{R+}, $D_{S,N-}$, D_{S-}

2. $t = t_2$, $(110) \rightarrow (111)$

- S_T is turned on
- current I commutates from S_S to S_T
- **no** switching loss in S_S (S_S remains in on-state)
- turn-on loss $W^{S\rightarrow S}_{\text{ON},S}$ in S_T
- switched voltage $U_{N,RS}$
- turn-on losses $W^{S\rightarrow S}_{\text{ON},D}$ in $D_{T,N-}$, D_{T-}

3. $t = t_3$, $(111) \rightarrow (110)$

- S_T is turned off
- current I commutates from S_T to S_S
- **no** switching loss in S_S (S_S was in on-state during the previous switching state)
- turn-off loss $W^{S\rightarrow S}_{\text{OFF},S}$ in S_T
- switched voltage $U_{N,RS}$
- turn-on losses $W^{D_F\rightarrow S}_{\text{ON},D}$ in $D_{S,N-}$, D_{S-}

4. $t = t_4$, $(110) \rightarrow (100)$

- S_S is turned off
- current I commutates from S_R, S_S to D_F
- **no** switching loss in S_R (S_R remains clamped in turn-on state)
- turn-off loss $W^{S\rightarrow D_F}_{\text{OFF},S}$ in S_S
- switched voltage $U_{N,ST}$
- turn-on losses in D_F are negligible

The average switching power loss P_m ($m = S, D$) of one power semiconductor device occurring within one mains period now can be calculated via

$$P_m = \frac{1}{3}\frac{f_P}{2\pi}\int_0^{2\pi} \Sigma W^n_{l,m}(\varphi)\,\mathrm{d}\varphi. \tag{14}$$

The factor $\frac{1}{3}$ is due to the cyclic permutation of the participance of transistors and diodes in the different switching actions. Depending on the switching action, the switching energy loss is proportional to the mains phase voltage $U_{N,ph}$ and/or to its square value $U^2_{N,ph}$ (cf. Tab. 1). Therefore, the average switching power loss has to be weighted for transitions between two active switching states[2] with

$$\begin{aligned} U^{S\rightarrow S}_{N,ph,avg} &= 0.443\,\hat{U}_{N,ph} \\ \left(U^{S\rightarrow S}_{N,ph,avg}\right)^2 &= 0.26\,\hat{U}^2_{N,ph}, \end{aligned} \tag{15}$$

and for switching actions between an active state and the free-wheeling state (and vice versa) by

$$\begin{aligned} U^{D_F\rightleftharpoons S}_{N,ph,avg} &= 1.21\,\hat{U}_{N,ph} \\ \left(U^{D_F\rightleftharpoons S}_{N,ph,avg}\right)^2 &= 1.5\,\hat{U}^2_{N,ph}. \end{aligned} \tag{16}$$

4.3 Total Average Losses

The total average semiconductor loss is the sum of the switching losses and conduction losses, and can be calculated using Tab. 1, (8)-(10), (12)-(13), and (14)-(16). With this, one receives for the average power loss of a power transistor

$$\begin{aligned} P_{S_i} = & \\ & \frac{f_P}{3}\left(1\frac{\text{nJ}}{\text{AV}^2}\, I\, 1.5\hat{U}^2_{N,ph} + 7.18\frac{\text{nJ}}{\text{V}^2}\, 1.5\hat{U}^2_{N,ph}\right. \\ & + 0.106\frac{\mu\text{J}}{\text{AV}}\, I\, 0.443\hat{U}_{N,ph} + 1.11\frac{\text{nJ}}{\text{V}^2}\, 0.26\hat{U}^2_{N,ph} \\ & \left. + 0.1\frac{\mu\text{J}}{\text{AV}}\, I\, 0.443\hat{U}_{N,ph} + 0.731\frac{\text{nJ}}{\text{AV}^2}\, I\, 0.26\hat{U}^2_{N,ph}\right) \\ & + \frac{2I\,M}{\pi}(U_{CE,0} + r_{CE}\, I). \end{aligned} \tag{17}$$

The mains voltage independent average power loss of one power diode can be calculated using

$$\begin{aligned} P_{D_{i,(N)\pm}} = & \\ & \frac{f_P}{3}\, I\, \left(5\frac{\mu\text{J}}{\text{A}} + 2.67\frac{\mu\text{J}}{\text{A}}\right) + \frac{I\,M}{\pi}(U_{F,0} + r_D\, I). \end{aligned} \tag{18}$$

[1] The system switching state is described by the combination $(s_R s_S s_T)$ of the switching functions of the power transistors, where $s_i = 1$ denotes the on-state, and $s_i = 0$ denotes the off-state.

[2] E.g., $U^{S\rightarrow S}_{N,ph,avg} = \frac{1}{\pi/6}\int_0^{\pi/6} U_{N,ST}(\varphi)\,\mathrm{d}\varphi =$
$= \frac{3\sqrt{3}}{\pi}\left(2-\sqrt{3}\right)\hat{U}_{N,ph} = 0.443\hat{U}_{N,ph}$.

4.4 Maximum Allowable Semiconductor Loss

For calculating the maximum admissible output power of the buck rectifier a maximum allowable value of the junction temperature $T_{J,max}$ for each semiconductor device has to be defined. With this, the maximum allowable semiconductor loss

$$P_{max} = \frac{1}{R_{th,JS}} \left(T_{J,max} - T_S\right) \tag{19}$$

can be calculated for a given heat sink temperature T_S ($R_{th,JS}$ denotes the thermal resistance between semiconductor junction and heat sink). If this power loss is set equal to the sum of the switching losses P_S and conduction losses P_C,

$$P_{max} = P_S\{f_P; I; U_{N,ph}\} + P_C\{I\}, \tag{20}$$

one can directly calculate the DC link current I for the respective device at a given mains phase voltage $U_{N,ph}$. The allowable stress on the semiconductors of the buck input stage is defined by that semiconductor element $(S, D_{i,(N)\pm})$ which shows the lowest value of I.

5 Selection of System Operating Parameters

Based on the results of section 4, the maximum admissible output power of the rectifier and the corresponding efficiency[3] in dependency on the pulse frequency is given in **Fig. 9** for the following operating parameters, and characteristic values of the power semiconductors,

$U_{N,ph} = 230\text{V}$	$U_0 = 400\text{V}$
$T_{J,max} = 120°\text{C}$	$T_S = 70°\text{C}$
$R_{th,JS,S} = 0.88\text{K/W}$	$R_{th,JS,D} = 1.74\text{K/W}$

The value of $T_{J,max} = 120°\text{C}$ (lying below the maximum allowable junction temperature which is specified in the data sheets [6] and [7] as $T_{J,max,S} = 150°\text{C}$ and/or $T_{J,max,D} = 175°\text{C}$) is selected under consideration of a sufficient safety margin for the calculation, and with respect to a high reliability of the rectifier system. The Safe Operating Area (SOA) is limited by the maximum allowable loss of the power transistor. The power diodes are overdimensioned[4] and are therefore remaining at lower junction temperature. As Fig. 9 shows one has to limit the pulse frequency to $\approx 26\text{kHz}$ for achieving the desired output power of $P_0 = 5\text{kW}$ without exceeding the junction temperature limits. The efficiency of the buck input stage then shows a value of $\eta \approx 95.7\%$.

The breakdown on switching and conduction losses of the power transistors and diodes is given in **Fig. 10** for different input voltages and the according maximum allowable output power $P_{0,max}$ for a pulse frequency of 31.25kHz. The losses are given with reference to the sum of the switching and conduction losses occurring at $U_{N,ph} = 230\text{V}$. One can see that the main share of the losses is due to the transistor losses, for low input voltages and/or high input currents the conduction losses increase, whereas the switching losses of the power transistors decrease due to the decreased voltage being switched.

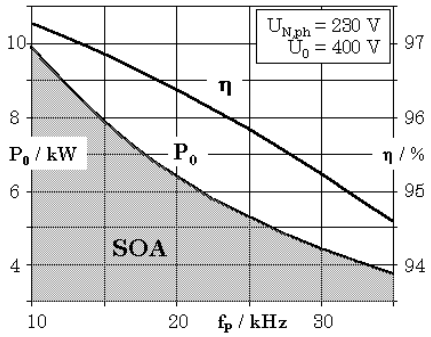

Fig. 9: Maximum admissible output power P_0 and efficiency η in dependency on the pulse frequency f_P for a phase voltage of 230V and 400V output voltage. The Safe Operating Area (SOA) is shaded in grey.

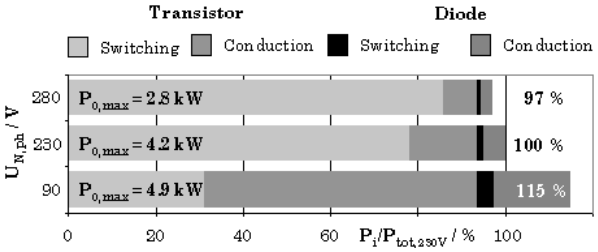

Fig. 10: Loss contribution of the power semiconductors for maximum admissible output power at different mains voltages for a pulse frequency of 31.25kHz.

In **Fig. 11**(a) the junction temperature T_J resulting for a given output power P_0 is shown for the wide input voltage range. The pulse frequency is assumed to be 31.25kHz, the modulation index M is set to the maximum modulation index $M_{max} = 0.9$ for mains phase voltages lower than 210V, for higher input voltages the modulation index is set in such a manner that the output voltage is held constant at 400V (cf. (2), and Fig. 8 in [1]), **Fig. 11**(b) shows the corresponding efficiency. For high input voltages and/or low modulation indices the junction temperature of the power transistors reaches values being unacceptably high (the maximum allowable transistor junction temperature given in the data sheet [7] is $T_j = 150°\text{C}$).

6 Conclusions

In this paper the switching losses and on-state losses of the power transistors and power diodes of the buck input stage of a three-phase/switch buck PWM rectifier are analyzed. Based on this, the maximum allowable output power is calculated in analytical closed form in dependency on the switching frequency. Furthermore, the efficiency and the loss contributions of power tran-

[3] One has to point out, that resistive losses of the input filter and of the output inductor and output capacitor, and additional losses (gate drive stage, fans, etc.) are not considered.

[4] Due to an advantageous mounting semiconductors in TO247 type package are preferred, there were no ultrafast diodes with lower current rating available in TO247 type package.

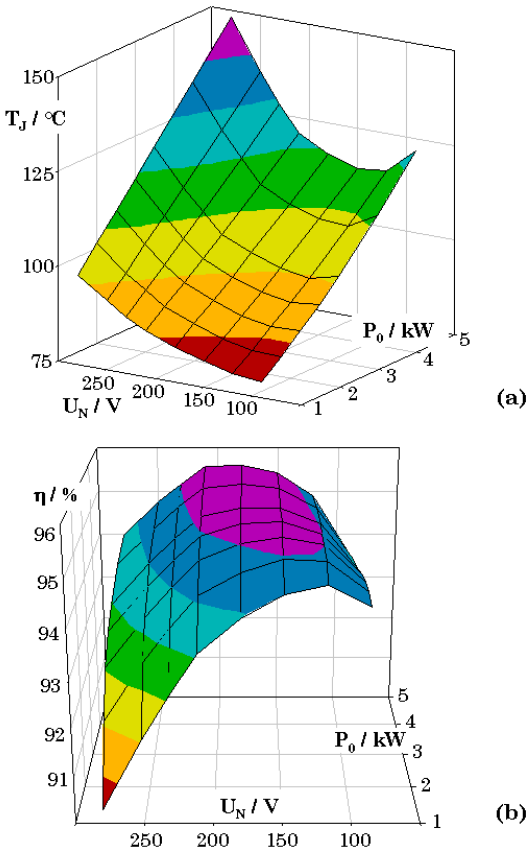

Fig. 11: Transistor junction temperature T_J **(a)** and rectifier efficiency η **(b)** for a given output power P_0 in a wide input voltage range. For the system operating parameters see section2.

sistors and power diodes are determined at different input voltages. Besides that, the junction temperature of the power transistors occurring for a constant output power in a wide input voltage range is given.

The considerations show, that a system output power of 5kW can be achieved at an efficiency of $\eta \approx 95.7\%$ for a pulse frequency of $\approx$ 26kHz and for 230V mains phase voltage. The limitation of the output power is due to the thermal stress on the IGBTs, the junction temperature of the power diodes shows a large margin to the maximum allowable temperature.

As the investigation of the loss breakdown to the power transistors and power diodes shows, the main part of the losses ($\approx$ 86%) is due to switching losses of the power transistor for high input voltage (conduction losses $\approx$ 8%). For low mains phase voltages the on-state losses are dominant (switching losses: $\approx$ 31%, conduction losses: $\approx$ 63%). In both cases the switching frequency is 31.25kHz as defined by the digital signal processor.

Regarding a further development of the buck-type rectifier we want to point out that the main part of the losses is due to the losses of the power transistor, and (for high input voltages) due to the switching losses of the power transistors, respectively. Accordingly, the switching frequency should be decreased to $f_P = 20$kHz in order to achieve the expected output power of 5kW within the wide input voltage range. For a further increase of the efficiency of the buck PWM rectifier and/or in order to decrease the conduction losses, employing an IGBT with higher rated current should be considered. Therefore, the application of a power module integrating the power semiconductors of one bridge leg [8], [9] is recommendable, whereby the output power can be increased, and the assembly of the power stage is simplified considerably.

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