DC Side Current Balancing of Two Parallel Connected Interleaved Three-Phase Three-Switch Buck-Type Unity Power Factor PWM Rectifier Systems

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Abstract – In this paper the active DC side current balancing of parallel connected three-phase buck-type rectifier systems is investigated using space vector calculus. Modulation schemes for the parallel connection are derived from the switching state sequences known for a single system and are comparatively evaluated by digital simulation. The independent current AC and DC side current paths are shown and two control schemes are presented which allow to balance the DC side currents of the individual systems. All theoretical considerations are verified by digital simulations.

1 Introduction

In [1] a novel three-phase three-switch buck-type unity power factor rectifier with integrated DC/DC boost converter output stage was presented, which allows to control the output voltage to $U_0 = 400\,\mathrm{V}$ within an universal input voltage range of $U_{N,l-l} = (208 \ldots 480)\,\mathrm{V_{rms}}$ line-to-line [2]. A prototype with a rated output power of 5 kW and a pulse frequency of $f_P = 23.4\,\mathrm{kHz}$ was realized at the Vienna University of Technology. In order to achieve a higher output power of 10 kW two systems are connected in parallel and controlled in interleaved manner. This shows the following advantages over a single system of higher power:

- the input currents show a more continuous shape,
- cancellation of current harmonics with pulse frequency, i.e the first current harmonic does occur at twice the pulse frequency, $2f_P$, and therefore
- the cut-off frequency of the input filter can be shifted to higher frequencies, resulting in a reduction of the input filter size and in a higher admissible dynamics of the output voltage control.

There are two possibilities for realizing the parallel connection of two three-phase buck+boost PWM rectifier systems: the two individual systems can be connected at the output terminals (cf. Fig. 12(a) in [1]) or one can connect the systems at the collector- and emitter-pins of the boost power transistor, i.e., both systems do share a single boost output stage.

In this paper all considerations are limited to the buck input stage in order to keep the investigation generally applicable. There, one has to provide a solution for active current balancing in case the boost transistor is deactivated, i.e. at high input voltages $U_{N,l-l} \geq 360\,\mathrm{V}$ for an output voltage $U_0 = 400\,\mathrm{V}$. By providing a boost output stage for each system another degree of freedom for balancing the DC current is given, which will be analyzed in a future paper. The parallel connection of two buck input stages is shown in **Fig. 1**.

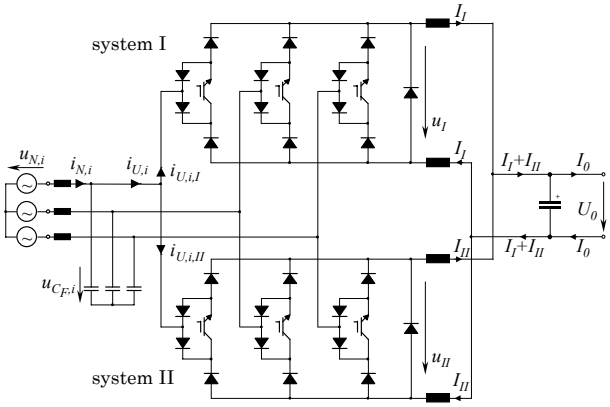

Fig. 1: Parallel connection of two three-phase/switch buck-type PWM rectifier systems.

Different strategies for paralleling three-phase buck-type PWM rectifier systems have been investigated in the literature where the power modules were interleaved in order to reduce current harmonics and/or the input filter size. The parallel connection of two three-phase/switch buck-type PWM rectifier systems was treated in [3], and [4], but no control concepts for active DC side current balancing were given in this publications.

To the knowledge of the authors, active balancing of the DC currents of paralleled buck-type rectifier systems so far was investigated only in [5]. There, modeling and control were derived from a control concept for three-phase boost-type rectifiers by measuring the zero-sequence current on the AC side of the rectifier system (cf. [6]). However, as a closer analysis shows, no direct relation is given between the AC side zero-sequence current and DC side current unbalance, i.e. for different unbalance conditions which would require different balancing control actions an identical zero-sequence current does occur.

Therefore, in this paper a novel and comprehensive analysis of the paralleling of n buck-type rectifier systems is given based on the space vector calculus consid-

ering the occurrence of $(2n-1)$ independent currents on the DC side. In **section 2** the space vectors which are available for input current formation are given and analyzed concerning their switching state redundancy. Furthermore, the derivation of space vector modulation schemes for parallel operation of two rectifier systems is treated and comparatively evaluated by digital simulations. **Section 3** describes the independent currents existing for the parallel connection of n buck type rectifier systems, and two control structures are presented which do allow to control the balancing of the DC side inductor currents. Furthermore, simulation results confirming the proposed control concept are given in **section 4**.

2 Space Vector Modulation

In this section, the input current space vectors which are available at the AC side of two parallel connected rectifier systems are determined, and different modulation schemes employing redundant current space vectors are developed.

2.1 Rectifier Input Current Space Vectors

For the characterization of a switching state of one system we use the combination $j = (s_R s_S s_T)$ of the phase switching functions s_i, $i = R, S, T$. There, the switching function does define the switching state of the corresponding power transistor, where $s_i = 0$ denotes the off-state, and $s_i = 1$ denotes the on-state.

For achieving a resistive fundamental mains behavior, $i_{N,i} \sim u_{N,i}$, and for neglecting the fundamental of the input filter capacitor currents ($i_{N,i} \approx i_{U,(1),i}$), fundamentals $i_{U,(1),i}$ of the discontinuous rectifier input phase currents $i_{U,i}$ lying in phase with the corresponding mains phase voltage $u_{N,i}$ ($\approx u_{C_F,i}$) have to be formed. There, only the space vectors lying in immediate neighborhood of a given reference value $\underline{i}_U^*$ of the input current and/or of a related mains current $\underline{i}_N \approx \underline{i}_U^*$ are incorporated into the switching state sequence in order to achieve a deviation as small as possible between the reference and the actual current space vectors.

If we, e.g., consider a combination of the mains phase voltages

$$u_{N,R} > 0 > u_{N,S} > u_{N,T} \tag{1}$$

being valid within the mains angle interval $\varphi_U \in (0; \frac{\pi}{6})$ (denoted as "interval 1" in this paper), in case the mains voltage $u_{N,i}$ is defined as

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\omega_N t), \\ u_{N,S} &= \hat{U}_N \cos(\omega_N t - 2\pi/3), \\ u_{N,T} &= \hat{U}_N \cos(\omega_N t + 2\pi/3), \end{aligned} \tag{2}$$

the current space vectors available for current formation at the input side of the parallel connection of two single systems I and II (cf. Fig. 1) within interval 1 and the subsequent mains interval are compiled in **Tab. 1** and are depicted in **Fig. 2** (cf. Fig. 2 in [7]). The given space vectors show three different magnitudes (apart from the zero vector), i.e., the total rectifier systems equals a three-level topology. Current space vectors showing a redundancy of switching states concerning current formation (i.e. by different input currents $i_{U,i,I}$ and $i_{U,i,II}$ of the individual systems the same total current space vector $\underline{i}_U$ is formed at the input side) are marked with an asterisk (*).

*	$\underline{i}_{U,A} = \frac{2}{\sqrt{3}} I \mathrm{e}^{-\jmath\pi/6}$			$\underline{i}_{U,E} = \frac{4}{\sqrt{3}} I \mathrm{e}^{+\jmath\pi/6}$
	$\underline{i}_{U,B} = \frac{4}{\sqrt{3}} I \mathrm{e}^{-\jmath\pi/6}$		*	$\underline{i}_{U,F} = 2\, I \mathrm{e}^{+\jmath\pi/3}$
*	$\underline{i}_{U,C} = 2\, I$		*	$\underline{i}_{U,G} = \frac{2}{\sqrt{3}} I \mathrm{e}^{+\jmath\pi/2}$
*	$\underline{i}_{U,D} = \frac{2}{\sqrt{3}} I \mathrm{e}^{+\jmath\pi/6}$			$\underline{i}_{U,H} = \frac{4}{\sqrt{3}} I \mathrm{e}^{+\jmath\pi/2}$

Tab. 1: Current space vectors for parallel operation of two systems for $\varphi_U \in (0; \pi/3)$. Redundant space vectors are marked with an asterisk (*).

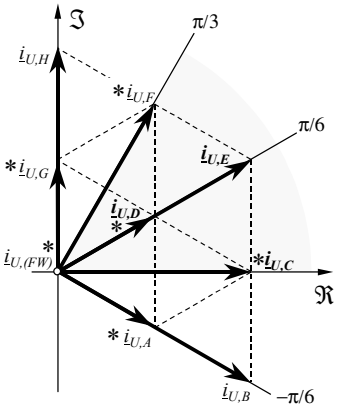

Fig. 2: Input current space vectors available for current formation in an angle interval $\varphi_U \in (0; \frac{\pi}{3})$. Redundant space vectors are marked with an asterisk (*).

E.g., current space vector $\underline{i}_{U,D}$ (cf. Tab. 1) can be formed by two different strategies;
Strategy I: one system is in active state (a current space vector $\underline{i}_U \neq 0$ is formed at the input of the system) and the other system is operating in free-wheeling state, e.g.,

$$\begin{aligned} j_I = (101) \qquad & \underline{i}_{U,(101),I} = \frac{2}{\sqrt{3}}\, I_I\, \mathrm{e}^{+\jmath\pi/6} \\ j_{II} = (100) \qquad & \underline{i}_{U,(100),II} = 0, \end{aligned} \tag{3}$$

or **Strategy II:** both systems are in active state,

$$\begin{aligned} j_I = (110) \qquad & \underline{i}_{U,(110),I} = \frac{2}{\sqrt{3}}\, I_I\, \mathrm{e}^{-\jmath\pi/6} \\ j_{II} = (011) \qquad & \underline{i}_{U,(011),II} = \frac{2}{\sqrt{3}}\, \jmath\, I_{II}. \end{aligned} \tag{4}$$

If $I_I = I_{II} = I$ (as assumed for current symmetrization) in both cases the total current space vector (cf. Fig. 2)

$$\underline{i}_{U,\binom{j_I}{j_{II}}} = \underline{i}_{U,j_I} + \underline{i}_{U,j_{II}} = \frac{2}{\sqrt{3}}\, I\, \mathrm{e}^{+\jmath\pi/6} = \underline{i}_{U,D} \tag{5}$$

is formed at the input side of the parallel systems. Therefore, input current space vector $\underline{i}_{U,D}$ (cf. Tab. 1) can be

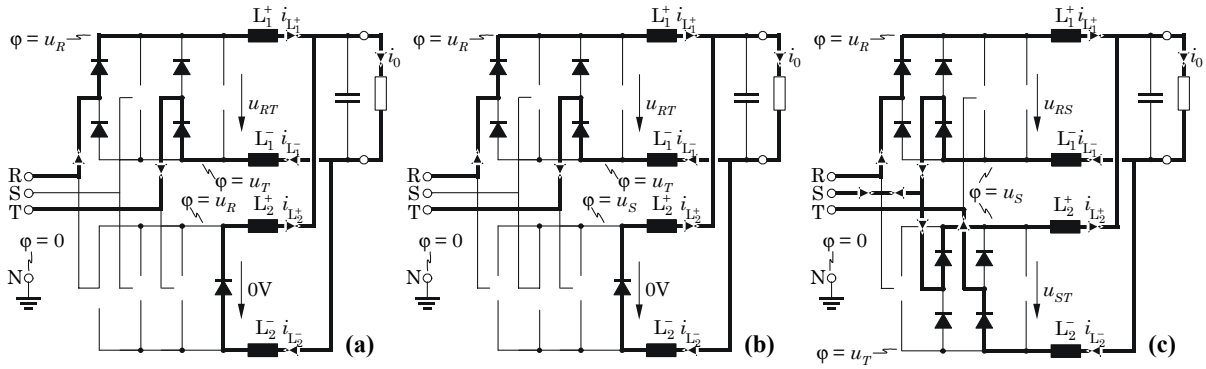

Fig. 3: Redundant switching states concerning input current formation (cf. (8) – (10)) for switching states **(a):** $j = \binom{111}{100}$, **(b):** $j = \binom{111}{010}$, and **(c):** $j = \binom{110}{011}$. The current paths are indicated by bold lines, for the sake of clearness, power semiconductors which are not involved in current conduction are omitted. The potentials effecting the current change rates in the DC side inductors related to a fictitious neutral point N, and the buck-stage output voltages u_I, u_{II} are given.

obtained via switching states

$$\begin{pmatrix} j_I \\ j_{II} \end{pmatrix} = \begin{pmatrix} 111 \\ 100 \end{pmatrix} \text{ or } \begin{pmatrix} 111 \\ 010 \end{pmatrix} \text{ or } \begin{pmatrix} 110 \\ 011 \end{pmatrix}, \qquad (6)$$

or by exchanging switching states j_I and j_{II}.

Remark: Switching state $j = (000)$ *must not* be used in order to avoid overvoltage peaks across the DC side inductors. Due to the DC side current ripple the instantaneous current values in the positive and negative DC link rail are not equal. At the transition from switching state $j = (110)$ to $j = (000)$ the Kirchhoff's current law is not fulfilled at the connection point of cathode and/or at the anode of the free-wheeling diode to the DC link bus which results in an overvoltage spike across the inductors forcing the currents to an equal value. Therefore, one power transistor has to be kept in the on-state during the free-wheeling state; one can clamp the power transistor in the on-state in that phase where the mains phase voltage either

- shows the highest absolute value (e.g., phase R in interval 1 [3]), or
- lies between the two other phases (e.g., phase S in interval 1 [1]).

However, different rates of change $\mathrm{d}i_L/\mathrm{d}t$ of the current are obtained for the DC side inductors $L_{12}^{\pm}$ dependent on the switching states of the rectifier systems resulting in different voltages applied to the input side of the DC side inductors. In **Fig. 3** the switching states given in (6) are shown and the potentials φ of positive and negative DC link rails related to a fictitious neutral point N are given. With this, the current change rates $\mathrm{d}i_L/\mathrm{d}t$ can be calculated for the considered switching states in dependency on the mains line-to-line voltages u_{RT}, u_{RS}, u_{ST} which are applied to the buck input stages u_I, u_{II} and on the output voltage U_0 within the considered mains interval 1;

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{pmatrix} i_{L_1^+} \\ i_{L_2^+} \\ i_{L_1^-} \\ i_{L_2^-} \end{pmatrix} = \frac{1}{4L} \mathbf{D}_{\binom{j_I}{j_{II}}} \cdot \begin{pmatrix} u_{RT} \\ u_{RS} \\ u_{ST} \\ U_0 \end{pmatrix} \qquad (7)$$

$$\mathbf{D}_{\binom{111}{100}} = \begin{pmatrix} 1 & 0 & 0 & -2 \\ 3 & 0 & 0 & -2 \\ 1 & 0 & 0 & -2 \\ -1 & 0 & 0 & -2 \end{pmatrix} \begin{matrix} \leftarrow \\ \\ \leftarrow \\ \end{matrix} \qquad (8)$$

$$\mathbf{D}_{\binom{111}{010}} = \begin{pmatrix} 1 & -2 & 0 & -2 \\ -1 & 2 & 0 & -2 \\ 1 & 2 & 0 & -2 \\ 3 & -2 & 0 & -2 \end{pmatrix} \begin{matrix} \leftarrow \\ \\ \leftarrow \\ \end{matrix} \qquad (9)$$

$$\mathbf{D}_{\binom{110}{011}} = \begin{pmatrix} 0 & 2 & 0 & -2 \\ 0 & 2 & 0 & -2 \\ 0 & -2 & 0 & 2 \\ 0 & 2 & 4 & -2 \end{pmatrix}. \qquad (10)$$

One can see that for different switching states (resulting in the same input current space vector $\underline{i}_{U,D}$) the rates of change of the current differ from each other, i.e., the balancing of the DC currents can be performed by the different switching states. Equal current change rates (marked by an arrow in (8) and (9)) are due to the direct parallel connection of DC link inductors, e.g., for switching state $j = \binom{111}{100}$ current change rates $\mathrm{d}i_{L_1^+}/\mathrm{d}t$ and $\mathrm{d}i_{L_2^+}/\mathrm{d}t$ are equal due to the parallel connection of L_1^+ and L_2^+. However, in an experimental setup, the proportion of the absolute currents in the inductors will be determined by impedances of the current paths.

2.2 Derivation of Space Vector Modulation Schemes

There are two possibilities for developing space vector modulation schemes which

- provide a possibility for DC current balancing,
- operate in an interleaved mode in order to
- show minimum input current and/or input filter capacitor voltage ripple (i.e., only current space vectors lying in the immediate neighborhood of the reference current space vector are incorporated into the switching state sequence).

First, switching states fulfilling the above-mentioned requirements are freely arranged within one pulse (half) period. There, numerous possibilities are given, in [7]

this strategy was used for DC side current balancing in a low switching frequency high power application. Alternatively, a switching state sequence for a single three-phase PWM rectifier system is taken as a basis for the space vector modulation scheme of the parallel connection, where the modulation of the second rectifier system is shifted by half or a quarter of a pulse period with reference to the first rectifier system.

In the case at hand, space vector modulation schemes were developed employing the second method based on two different modulation schemes for a single rectifier system [1]; in modulation scheme 1, the free-wheeling state is lying at the end (at the beginning) of one pulse half period, while for modulation scheme 2 the free-wheeling state is placed in between two active switching states in the middle of one pulse half period. Considering interval 1 of the mains period, one receives for modulation scheme 1,

$$\Big|_{t_\mu=0}\ (111)\ (110)\ (100)\ \Big|_{t_\mu=T_P/2}, \tag{11}$$

where the power transistor of the phase which shows the maximum absolute phase voltage value is clamped in the on-state (phase R). If the power transistor of the phase showing the minimum absolute voltage (i.e., lying in between the other two phases) is clamped in the on-state within a $\pi/3$-wide interval of the mains period (phase S), one receives

$$\Big|_{t_\mu=0}\ (111)\ (110)\ (010)\ \Big|_{t_\mu=T_P/2}, \tag{12}$$

and for modulation scheme 2,

$$\Big|_{t_\mu=0}\ (111)\ (100)\ (110)\ \Big|_{t_\mu=T_P/2}, \tag{13}$$

or

$$\Big|_{t_\mu=0}\ (111)\ (010)\ (110)\ \Big|_{t_\mu=T_P/2}. \tag{14}$$

In **Fig. 4** modulation schemes for a single rectifier system are given which are symmetric (cf. (b)), or asymmetric (cf. (c)) with reference to the middle of one pulse period. The modulation scheme for the paralleled rectifier systems can now be achieved by shifting the switching state sequences by half a pulse period for the symmetric modulation scheme (cf. Fig. 4(d)), and by a quarter of a pulse period for the asymmetric modulation scheme (cf. Fig. 4(e)).

The different modulation schemes were implemented in a simulation program CASPOC® [8] and compared in order to determine the scheme fulfilling the above defined requirements. There, no control algorithm for balancing the DC link currents was provided in order to evaluate the self-stability of current sharing properties of the different schemes. Furthermore, the mains filter was omitted in order to concentrate on the essentials and to avoid undesired effects. **Figure 5** shows the simulation results of DC link currents $i_{L_{12}^{\pm}}$, mains phase currents $i_{N,i}$, $i = R, S, T$, and the current space vectors of the total rectifier input currents $i_{U,i}$ as well as the current space vector of the mains phase currents $i_{N,i}$ (cf. Fig. 1) for the following system parameters:

$$\begin{array}{llll} L_{12}^{\pm} & = 1\,\text{mH}, & U_{N,ph} & = 235\,\text{V} \\ U_0 & = 400\,\text{V} & I_0 & = 25\,\text{A} \\ f_N & = 50\,\text{Hz} & f_P & = 25\,\text{kHz}, \end{array}$$

(f_N denotes the line frequency, f_P the pulse frequency).

The comparison shows that there is a distinct difference between the results of the employed modulation schemes. By arranging the free-wheeling state at the end (at the beginning) of one pulse half period and by clamping the power transistor of the phase showing

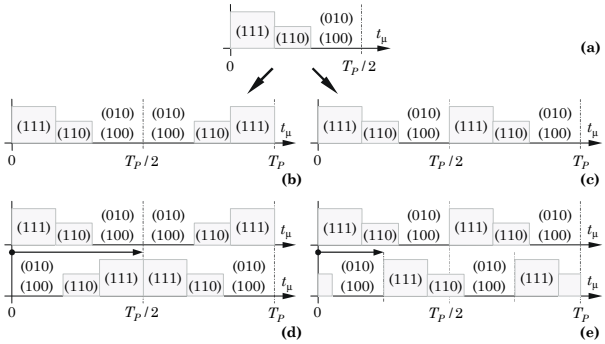

Fig. 4: Development of modulation schemes within one pulse half period for parallel connected rectifier systems based on the modulation scheme for a single rectifier system in interval 1 of the mains period **(a)**. Modulation schemes within one pulse period, arranged symmetrically **(b)** and asymmetrically **(c)** around the center of one pulse period. Schemes for paralleled rectifier systems **(d), (e)**, interleaving is achieved by proper phase-shifting (indicated by an arrow). t_μ is a time being running locally within a pulse period.

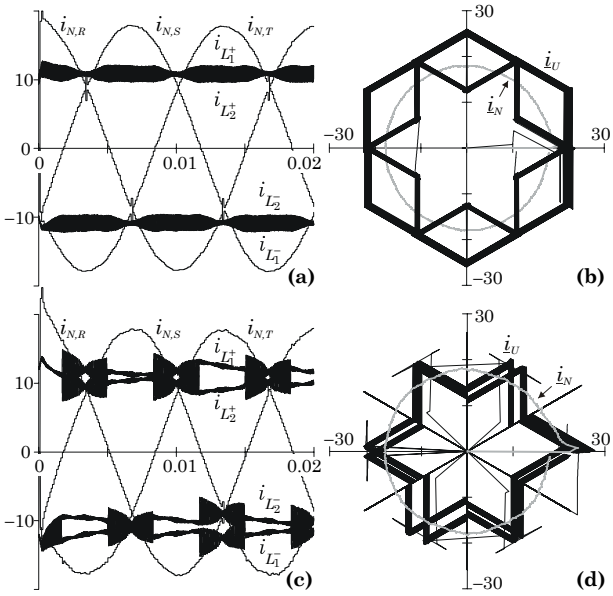

Fig. 5: Simulation results for different modulation methods; time behavior of mains phase currents $i_{N,i}$ and DC link currents $i_{L_{12}^{\pm}}$ **(a),(c)**, and trajectories of the total rectifier input current space vector $\underline{i}_U$ and of the mains phase current space vector $\underline{i}_N$ **(b),(d)** for modulation scheme 1 (cf. Fig. 4(d) and (12)) and for modulation scheme 2 (cf. (11)), both arranged symmetrically.

the minimum absolute voltage value (cf. (12)) one receives a constant average value of the currents in the DC link inductors, the envelopes of the current ripple are modulated with three times the mains frequency (cf. Fig. 5(a)), the trajectory of the total rectifier input current space vector $\underline{i}_U$ shows an ideal shape, only current space vectors lying in immediate neighborhood of the mains phase current (reference) space vector $\underline{i}_N$ are incorporated, the free-wheeling state of the total rectifier input current is not employed in this case (no connections of the trajectory to the origin of the coordinate system), i.e., the current ripple is held on a minimum level (cf. Fig. 5(b)).

If the free-wheeling state is arranged in the middle of one pulse half period, and if the power transistor of that phase showing the maximum absolute voltage value (cf.(11)) is clamped in the on-state, the DC link currents show different behavior. The average value is not constant any more (which does not take any effect on the mains phase currents !), there is a reduction in current ripple in the inductors connected to a phase being held in the on-state for $\pi/3$, but the current ripple does increase within the subsequent $\pi/3$ interval (cf. Fig. 5(c)). As Fig. 5(d) shows, the free-wheeling state is incorporated in the switching state sequence (existing connections to the origin of the coordinate system), i.e., the current ripple does not show the lowest value possible.

Therefore, the modulation scheme given in (12) and in Fig. 4(b) is further investigated in this paper.

3 Symmetrization

In order to ensure current balancing and power loss balancing to the single rectifier systems, a proper control algorithm has to be implemented. The need for current balancing is due to non-ideal properties, e.g., mains phase voltage unbalance, forward voltage drops, component tolerances, and/or different impedances of current conduction paths. In this section, different control methods for current balancing, and DC side circulating currents and their translation into a zero-sequence component of the AC side currents is investigated.

3.1 Circulating Currents and Zero-Sequence Current

Depending on the structure of the paralleled rectifier systems, there could exist a different number of circulating currents, i.e. currents which flow via both converters and do not pass the load. For paralleled boost converters, there is only one circulating current due to the single DC side energy storage (DC link capacitor) [9], [10]. Therefore, it is possible to measure the zero-sequence current on the AC side of the rectifier system which is characteristic for the circulating current on the DC side [6].

However, for the parallel connection of current source converters there is more than one circulating current on the DC side of the rectifier systems due to the higher number of DC side energy storages (DC link inductors), which results in a zero-sequence component at the AC side. This has to be considered for designing the control balancing the output currents of the individual systems.

In **Fig. 6** a DC/DC equivalent circuit of two three-phase buck-type rectifier systems is given, the input voltages are each splitted into two voltages u_{pm}, u_{nm}, $m = 1, 2$, connected to a common artificial point N (mains star point). Via point N the paths of the circulating currents i_{K1} and i_{K2} are closing. If, e.g., the circulating current i_{K1} in the positive DC link inductors L_1^+ and L_2^+ is assumed to be $+1\,\mathrm{A}$, and the circulating current i_{K2} is set to zero, i.e., $i_{K1} = +1\,\mathrm{A}$, and $i_{K2} = 0$, one receives for the average value of the zero-sequence current at the input of rectifier system I,

$$i_{U,I,0}^{avg} = \frac{1}{3}\left[i_{U,I,R}^{avg} + i_{U,I,S}^{avg} + i_{U,I,T}^{avg}\right] = +0.33\,\mathrm{A}, \quad (15)$$

and for the zero-sequence current at the input of rectifier system II,

$$i_{U,II,0}^{avg} = -i_{U,I,0}^{avg} = -0.33\,\mathrm{A}, \quad (16)$$

the zero-sequence current of the total rectifier input current is $i_{U,0} = 0\,\mathrm{A}$. The same results are obtained for $i_{K1} = 0\,\mathrm{A}$, and $i_{K2} = +1\,\mathrm{A}$,

$$i_{U,I,0}^{avg} = +0.33\,\mathrm{A},\ i_{U,II,0}^{avg} = -0.33\,\mathrm{A},\ i_{U,0} = 0\,\mathrm{A}. \quad (17)$$

Therefore, no unique conclusion on the behavior of the circulating currents can be drawn from the AC side zero-sequence currents $i_{U,I,0}$, and $i_{U,II,0}$. Therefore, the novel control concept proposed in the following for the balancing of the DC side currents does not refer to the zero-sequence current.

3.2 Control Structures

Control Structure I

If an unbalance in the currents in the DC link inductors connected to the positive output terminal is considered, e.g. $i_{L_1^+} > i_{L_2^+}$, the potential φ_{p1} at the input side of rectifier system I has to be decreased (cf. Fig. 6), while the potential φ_{p2} at the input side of rectifier system II has to be increased in order to equilibrate the DC link currents. The potentials on the negative inputs φ_{n1}, and φ_{n2} do not have to be changed in this case.

A corresponding control structure is given in **Fig. 7**, there the current reference value i_0^* provided from an outer output voltage control loop (which is not shown) is divided by the number of parallel connected rectifier systems n and compared to the actual (averaged) DC link currents. P-type controllers (gain k_{PV}) do set the reference value of the voltage u_{p1}^*, and u_{n1}^* for rectifier system I, the reference values are transformed into a buck-stage output voltage reference value $u_{0,1}^*$, where a pre-control of the output voltage reference value u_0^* is provided,

$$u_{0,1}^* = \underbrace{u_{p1}^* + u_{n1}^*}_{\Delta u_1} + u_0^*. \quad (18)$$

The same is true for rectifier system II; all reference values are incorporated in the calculation of the on-times of the switching states (cf. (32) in [1]). In order to achieve the desired modification of the potentials $\varphi_{p1} \dots \varphi_{n2}$, an additional free-wheeling state is provided in the switching state sequence which allows to increase or decrease the potentials as proposed in [5], [10]. Considering interval 1, switching state $j = (010)$ is used as free-wheeling state by default; therefore, if switching state $j = (100)$ is applied, the positive potentials φ_p are increased due to $u_{N,R} > u_{N,S}$, while switching state $j = (001)$ increases the absolute value of the negative potentials φ_n due to $u_{N,S} > u_{N,T}$. The relative on-time δ_+ of the additional free-wheeling state, which is placed in the middle of the pulse period, can be calculated via

$$\delta_+ = \frac{u_p^*}{u_{ph,cl.} - u_{ph,\pm}}, \tag{19}$$

where $u_{ph,cl.}$ is the voltage of that phase, where the power transistor is in on-state during the free-wheeling state by default, and $u_{ph,\pm}$ is the voltage of the phase, where the power transistor is in on-state during the additional free-wheeling state. There, $u_{ph,+}$ is used to increase the positive potential ($u_p^* > 0$), and $u_{ph,-}$ to increase the negative potential ($u_p^* < 0$).

The performance of the proposed control concept is confirmed by simulation results in section 4.

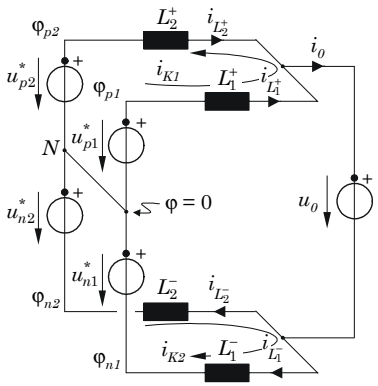

Fig. 6: DC/DC equivalent circuit of two paralleled rectifier systems showing the circulating currents i_{Km}, and the potentials φ_{pm}, and φ_{nm}, $m = 1, 2$, on the input side of the DC link inductors.

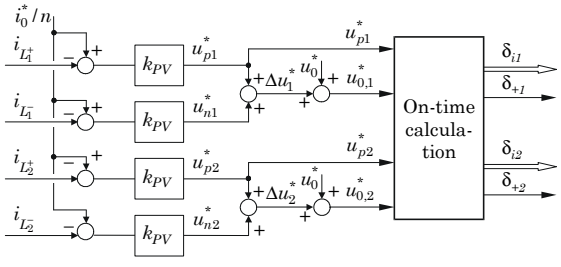

Fig. 7: Control structure I for balancing the DC link inductor currents based on the DC/DC equivalent circuit given in Fig. 6.

Control Structure II

The aforementioned control structure shows the drawback that by controlling the current in one DC link inductor the other currents are also influenced. In the following, a control structure based on a modified DC/DC equivalent circuit of the paralleled rectifier systems is presented briefly which allows to control the DC currents independently.

For the parallel connection of $n = 2$ buck-type rectifier systems there are $(2n-1) = 3$ independent currents, which have to be considered for control: i_0, i_{K1}, and i_{K2}. Therefore, the voltage sources given in Fig. 6 are combined in such a manner that one input voltage u^* and two voltages Δu_p^* and Δu_n^* shifting each potential individually on the input side of the DC link inductors $\varphi_{p1} \dots \varphi_{n2}$ are obtained. Under symmetric conditions, all three voltages are balanced and are therefore splitted into symmetrical parts $u^*/2$, $\Delta u_p^*/2$, and $\Delta u_n^*/2$ (cf. **Fig. 8**).

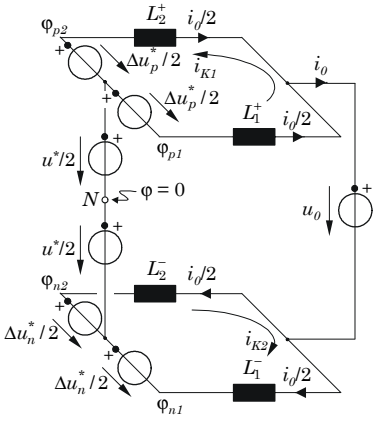

Fig. 8: Modified DC/DC equivalent circuit of two paralleled rectifier systems which allows to control the output current i_0 and the circulating currents i_{K1}, i_{K2} independently.

In the real system, four currents have to be balanced ($i_{L_1^+} \dots i_{L_2^-}$), which are dependent on four voltages (cf. Fig. 6) $u_{p1}^* \dots u_{n2}^*$; the dependency can be given by a 4×4-matrix,

$$4L \frac{\mathrm{d}}{\mathrm{d}t} \cdot \underbrace{\begin{pmatrix} i_{L_1^+} \\ i_{L_2^+} \\ i_{L_1^-} \\ i_{L_2^-} \end{pmatrix}}_{\mathbf{I}_L} = \tag{20}$$

$$= \underbrace{\begin{pmatrix} \mathbf{3} & -1 & 1 & 1 \\ -1 & \mathbf{3} & 1 & 1 \\ 1 & 1 & \mathbf{3} & -1 \\ 1 & 1 & -1 & \mathbf{3} \end{pmatrix}}_{\mathbf{A}} \underbrace{\begin{pmatrix} u_{p1}^* \\ u_{p2}^* \\ u_{n1}^* \\ u_{n2}^* \end{pmatrix}}_{\mathbf{U}} - 2 \underbrace{\begin{pmatrix} U_0 \\ U_0 \\ U_0 \\ U_0 \end{pmatrix}}_{\mathbf{U}_0}.$$

One can see that there is a strong dependency of a DC side inductor current on the related voltage (factor 3 in $\mathbf{A}$), and a weak dependence on the other voltages (factor ± 1 in $\mathbf{A}$). For the mathematical model which gives the basis for the control (cf. **Fig. 9**), one has to reduce the mathematical model of the real system to the system employing the $(2n-1)$ independent currents, i.e. to 3 variables for two ($n = 2$) paralleled rectifier systems, in

order to provide an independent control loop for each current,

$$\underbrace{\begin{pmatrix} i_0 \\ i_{K1} \\ i_{K2} \end{pmatrix}}_{\mathbf{I}} = \underbrace{\frac{1}{2}\begin{pmatrix} 2 & 2 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{pmatrix}}_{\mathbf{B}} \cdot \mathbf{I_L}. \tag{21}$$

The current reference value i_0^* is provided by an outer output voltage control loop, the reference values of the circulating currents are set to zero. A P-type controller (k_{Pu}, k_{Pn}, k_{Pp}) sets the reference values of the buck stage output voltage u^*, and of the differential potentials Δu_p^* and Δu_n^*. These values are transformed into the real system model in order to derive the voltages occurring in the actual circuit,

$$\mathbf{U} = \underbrace{\frac{1}{2}\begin{pmatrix} 1 & -1 & 0 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \\ 1 & 0 & -1 \end{pmatrix}}_{\mathbf{C}} \cdot \underbrace{\begin{pmatrix} u^* \\ \Delta u_p^* \\ \Delta u_n^* \end{pmatrix}}_{\mathbf{U}^*}. \tag{22}$$

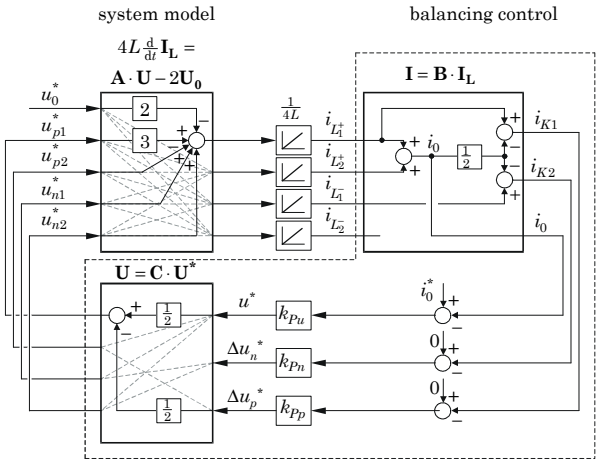

Fig. 9: Multivariable control of the DC link currents. The block diagram is comprised by system to be controlled having four input and output variables $u_{p1} \dots u_{n2}$ and $i_{L_1^+} \dots i_{L_2^-}$ which are transformed into three input and/or output variables i_{K1}, i_{K2}, i_0, and $u^*, \Delta u_n^*, \Delta u_p^*$ for control and the back-transformation into actual quantities to be applied to the system by proper modulation.

3.3 Control Design

The P-type controllers in Fig. 7 can be designed in a first step by considering only the respective DC link inductor, the related input voltage and the output voltage u_0 which can be assumed to be constant and impressed (cf. **Fig. 10**). We then have for the transfer function of the control loop controlling the current in the positive DC link rail of rectifier system I,

$$\frac{\tilde{i}_{L_1^+}}{\frac{i_0^*}{n}} = \frac{1}{\frac{L_1^+}{k_{PV}} \cdot s + 1}, \quad \tau = \frac{L_1^+}{k_{PV}}. \tag{23}$$

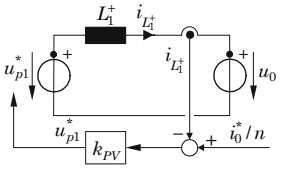

Fig. 10: Equivalent circuit to be considered for the design of the control of the current in a DC link bus of one rectifier system (shown for $i_{L_1^+}$).

The transfer function constitutes a first order delay (proportional negative-feedback of the integrator representing L_1^+), the time constant τ is set according to

$$\tau \ll \frac{1}{3f_N}, \tag{24}$$

in order to provide sufficient dynamics for attenuating the effect of disturbances with three times the mains frequency.

4 Simulation Results

In this section, simulation results for the control structure described in section 3.2.I are given. The system parameters are set according to section 2.2. In **Fig. 11(a)** the behavior of mains phase currents $i_{N,i}$, $i = R, S, T$, and of DC link currents $i_{L_{12}^\pm}$ is shown. For $t < t_1$ the control loop balancing the currents is deactivated. As no source of unbalance (which would be present for a real system) is inserted in the parallel connection of the rectifier systems an ideally symmetric partition of the total DC current to the individual systems is given in

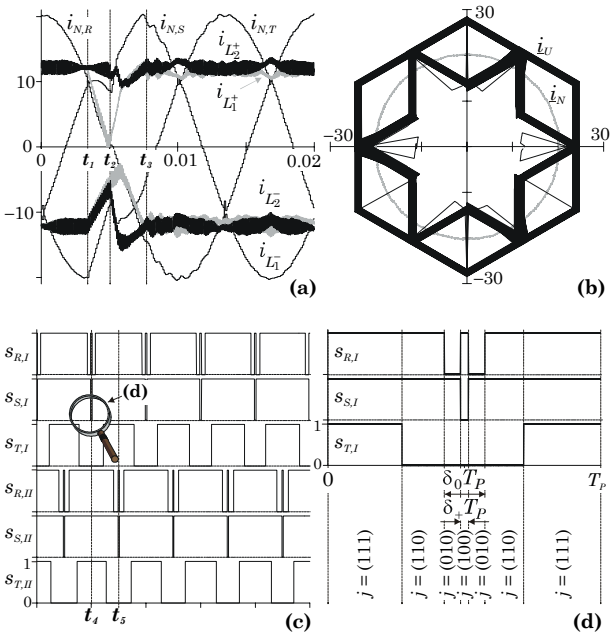

Fig. 11: Simulation results for unbalanced rectifier systems; **(a)** Time behavior of mains phase currents $i_{N,i}$, $i = R, S, T$ and DC link currents $i_{L_{12}^\pm}$, **(b)** trajectories of total rectifier input current $\underline{i}_U$ and mains phase current $\underline{i}_N$, **(c)** switching signals $s_{i,I}$ and $s_{i,II}$, $i = R, S, T$, and **(d)** switching signals $s_{i,I}$ within one pulse period.

this case. At $t = t_1$ a DC voltage source of 20 V is placed in series to DC link inductor L_1^+ in order to simulate a large unbalance. An unbalance of the DC link currents does occur immediately, which also results in a mains phase current distortion. At $t = t_2$ the control loop for DC link current balancing is activated, whereby a current symmetrization is achieved at $t = t_3$ by adding the additional free-wheeling states. In Fig. 11(b) the trajectory of the total rectifier input current space vector $\underline{i}_U$, and of the mains phase current space vector $\underline{i}_N$ are given for activated balancing control in a subsequent mains period; one can see that the additional free-wheeling state does not have any influence on the trajectories (cf. Fig. 5(b)), again only current space vectors lying in immediate neighborhood of the mains phase current (reference) space vector are used, i.e., the DC current ripple is held on a minimum value. The switching signals $s_{i,I}$ and $s_{i,II}$, $i = R, S, T$, applied to the power transistors of both rectifier stages I and II for activated balancing control are given in Fig. 11(c) for interval 1; at $t = t_4$ the additional free-wheeling state is inserted in the modulation scheme for power stage I, and at $t = t_5$ for power stage II (180° phase-shifted). Figure 11(d) shows the switching signals of power stage I within a pulse period T_P in detail; there, $(\delta_0\, T_P)$ denotes the duration of the total free-wheeling state (switching states $j = (010)$ and $j = (100)$), $(\delta_+\, T_P)$ denotes the duration of the additional switching state $j = (100)$ (cf. (19)).

5 Conclusions

In this paper, the DC side current balancing of three-phase buck-type rectifier systems was investigated. Based on the current space vectors, which are available for current formation at the input side of the paralleled rectifier systems, a modulation scheme was derived which

- provides all advantages of an interleaved operation,
- provides minimum ripple of the DC link inductor currents and minimum ripple of the AC side filter capacitor voltage, and
- allows to influence the buck-stage output voltages in such a manner that a balancing of the currents in the DC side inductors is ensured.

Two different control structures were treated; a scheme of low complexity where the four DC inductor currents are controlled independently, i.e., where the mutual influence of the current controls is not considered. There, a P-type controller was employed. Due to the controller type and the low balancing control dynamics required (unbalances are caused by only small differences of transistor or diode forward voltage drops, wiring resistances, or DC link inductor values) stabilizing the control loop does not pose problems. Additionally, a more complex multivariable control scheme was proposed which is based on a control-oriented model of the power circuit considering mutual influences. There, the four DC side inductor currents are transformed into three fictitious independent currents, which provides a basis for decoupled current control.

The more simple control strategy shows the advantages of lower realization effort, also the strategy could be extended to n paralleled systems easily. Both control strategies will be investigated experimentally and comparatively evaluated on a 10 kW prototype of the rectifier system in the course of future research.

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