A 5kW Three-Phase Buck+Boost Telecommunications Power Supply Module Input Stage Maintaining Unity Power Factor Under Failure of a Mains Phase

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Abstract - In this paper the reliable operation of a three-phase three-switch buck-type PWM unity power factor rectifier with integrated boost output stage is investigated experimentally under heavily unbalanced mains, i.e. mains voltage unbalance, loss of one phase, short circuit of two phases or earth fault of one phase. The control scheme which allows to control the system for any mains condition without change-over of the control structure is described in detail. Furthermore, experimental results which confirm the proposed control concept for different mains failure conditions and for the transition from balanced mains to a failure condition and vice versa are shown and the behavior of the output voltage in case of a mains failure is investigated. Moreover, efficiency, power factor and total harmonic distortion of the rectifier system under a mains failure are analyzed. The experimental results are derived from a 5 kW prototype of the rectifier system (input voltage range (208 ... 480) V_{rms} line-to-line, output voltage 400 V), where the control is realized by a 32-bit digital signal processor.

1 Introduction

High power telecommunications power supply modules usually show a two-stage topology, i.e. a front-end three-phase PWM rectifier and a DC/DC converter output stage. In [1] a three-phase unity power factor PWM rectifier formed by integration of a three-switch buck-derived input stage and a DC/DC boost converter output stage was proposed (cf. **Fig. 1**), which allows to control the output voltage to 400 V within a wide input voltage range of (280...480) V_{rms} line-to-line [2]. This results in an advantageous design of the power semiconductors of the rectifier stage and allows the application of output stage DC/DC converter technologies being well-known from systems with single-phase AC supply. According to the required high reliability of the power supply the PWM rectifier system should continue to operate also in case of a mains failure, i.e. for a transition from a symmetric to a heavily unbalanced mains voltage condition.

In [3], [4] and [5] control concepts for reliable operation under heavily unbalanced mains voltage conditions of a three-phase/three-level PWM *boost*-type (VIENNA) rectifier were presented. In [3] the operation of this system in a wide input voltage range and for a failure of a single mains phase is discussed. There, a detection of the phase-open failure is required and a change-over of the control structure has to be performed, which could cause problems for some mains failure conditions. In [4] and [5] a control concept is presented and analyzed experimentally which operates for a general unbalance of the mains phase voltages without any change-over of the control structure.

In this paper the theoretical analysis and the implementation of a control concept which allows to obtain sinusoidal mains phase currents which are proportional to the mains phase voltages also in case of any mains voltage unbalance or failure (e.g. mains phase-open failure, short circuit between two mains phases, or earth fault) are described in detail for the three-phase buck-derived PWM rectifier system with integrated boost output stage [6].

Section 2 gives a brief introduction into the theoretical background of the three-phase rectifier system. The control structure which ensures a reliable operation in case of a mains failure is explained in detail in **section 3**, **section 4** shows experimental results which are carried out on a 5 kW prototype of the rectifier system. There, the transition from balanced mains to a mains failure and vice versa is investigated, furthermore, the behavior of the output voltage during a mains failure and the effect of DC side current limitation are shown. **Section 5** treats power factor, efficiency and total harmonic distortion for the investigated mains failure conditions in comparison to an operation under symmetric mains.

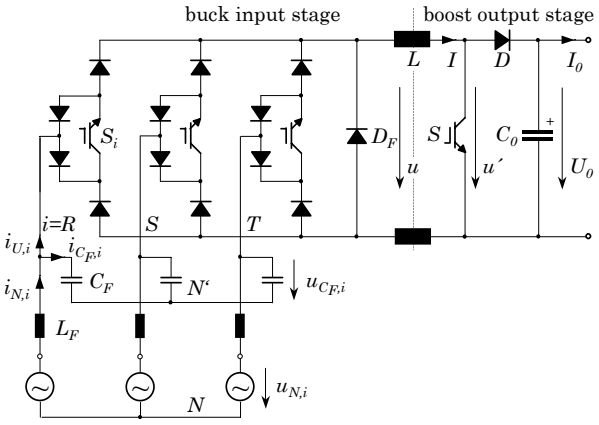

Fig. 1: Power circuit of the three-phase rectifier system with three-switch buck input stage and integrated DC/DC boost output stage.

2 Principle of Operation

In order to obtain a resistive fundamental mains behavior, mains phase currents $i_{N,i}$, $i = R, S, T$, and/or fundamentals $i_{U,(1),i}$ of the discontinuous rectifier input phase currents have to be formed, which are proportional to (lying in phase with) the corresponding mains phase voltages $u_{N,i}$. I.e. the rectifier system has to emulate a three-phase arrangement of ohmic resistors, where G is the conductivity of one phase, if the three phase resistors are arranged in star-connection,

$$i_{N,i} = u_{N,i} \cdot G \approx i_{U,(1),i} = u_{C_F,i} \cdot G. \qquad (1)$$

There, the reactive input filter capacitor current $i_{C_F,i}$ is neglected, i.e. $i_{N,i} \approx i_{U,(1),i}$ is assumed, and the voltage drop across the mains filter inductors L_F is neglected, i.e. $u_{N,i} \approx u_{C_F,i}$[1] (we have $u_{C_F,i} \approx u_{C_F,(1),i}$ for low capacitor voltage ripple). In order to realize (1) proper on-times of the buck input stage power transistors S_i and of the boost output stage power transistor S have to be selected, whereby the buck+boost inductor current (DC link current) is distributed sinusoidally to the mains phases. Furthermore, the reference value of the DC link current has to be set in dependency on the mains voltage condition. A detailed calculation of the DC link current reference value and of the relative on-times of the active switching states of buck input stage and boost output stage are given in [7].

Remark: In this paper, capital letters denote values which are constant over one mains period (e.g. G), the *local* average value (within one pulse period) of a discontinuous value is denoted with a bar (e.g. $\overline{u}$). Furthermore, ripple components with pulse frequency are neglected (e.g. $u_{C_F,i} = u_{C_F,(1),i}$), and continuous instantaneous values are denoted by lower case letters (e.g. u_N). The same is true for reference values which do always show a continuous shape (e.g. $u^* = \overline{u}^*$).

The maximum local average value of the output voltage $\overline{u}_{\max}$ of the buck input stage is defined by the input filter capacitor voltages $u_{C_F,i}$ and a maximum modulation index $M_{\max}$ of the buck input stage [1],

$$\overline{u}_{\max} = \frac{3}{2} \cdot M_{\max} \cdot \sqrt{\frac{2}{3}\left(u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2\right)}, \quad (2)$$

where the input filter capacitor voltages $u_{C_F,i}$ are measured with reference to an artificial neutral point N'. For symmetric mains, the buck stage modulation index M is defined as follows,

$$M = \frac{\hat{I}_N}{i} = \frac{\sqrt{2}}{\sqrt{3}} \cdot \frac{\overline{u}}{U_{N,ll}}, \qquad M \in (0;1), \qquad (3)$$

where $\hat{I}_N$ is the peak value of the mains phase currents and $U_{N,ll}$ is the rms value of the mains line-to-line voltage, cf. [1].

[1] This is valid only if the mains phase voltages do not contain any zero-sequence system.

3 Control Structure

In **Fig. 2** the proposed control structure which allows a reliable operation with sinusoidal mains phase currents and unity power factor under any mains condition is given. The control circuit consists of an outer output voltage control loop and an inner DC link current control loop. The relative on-times δ_j and δ of the active switching states of the buck input stage and of the boost output stage are derived as given in the following:

- The input filter capacitor voltages are measured against an artificial neutral point N' whereby a zero-sequence system which could occur in case of a mains failure is eliminated.
- The output voltage controller output is interpreted as output power demand p^*. In order to suppress low frequency harmonics as occurring in case of a mains failure, the output power reference value is low-pass filtered (corner frequency 5 Hz) and furthermore limited to the rated power P_{lim} of the rectifier system.
- The input conductivity reference value G^* is calculated according to

$$G^* = \frac{P_{lim}^{*\,LP}}{\sum_i \hat{U}_{C_F,i}^2}, \qquad (4)$$

with the limited and low-pass filtered reference value $P_{lim}^{*\,LP}$ of the output power reference value and with the sum of the squares of the input filter capacitor voltage amplitudes,

$$\sum_i \hat{U}_{C_F,i}^2 = \frac{1}{2}\left(\hat{U}_{C_F,R}^2 + \hat{U}_{C_F,S}^2 + \hat{U}_{C_F,T}^2\right). \quad (5)$$

- The DC link current reference value i^* is calculated employing

$$i^* = \begin{cases} \frac{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}{u_0} \cdot G^* & \text{for } u_0 < \overline{u}_{\max} \\ \frac{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}{\overline{u}_{\max}} \cdot G^* & \text{for } u_0 \geq \overline{u}_{\max} \end{cases}. \qquad (6)$$

One has to note that the conductivity reference value G^* is constant over one mains period, however, the DC link current reference value i^* shows a time-dependent behavior within one mains period for unbalanced mains conditions.

- In order to assure that the current stress on the power diodes and transistors does not exceed a maximum admissible level and in order to avoid saturation or overheating of the DC link inductor, the peak value of the DC link current reference value $\hat{i}^*$ has to be limited to a maximum value $\hat{I}_{\max}$, which is defined by the dimensioning of the rectifier system (25 A in this case). In case $\hat{i}^*$ exceeds the limit, the reference value i^* is downscaled by a correcting factor f_c,

$$f_c = \begin{cases} 1 & \text{for } \hat{i}^* \leq \hat{I}_{\max} \\ \hat{I}_{\max}/\hat{i}^* & \text{for } \hat{i}^* > \hat{I}_{\max} \end{cases}. \qquad (7)$$

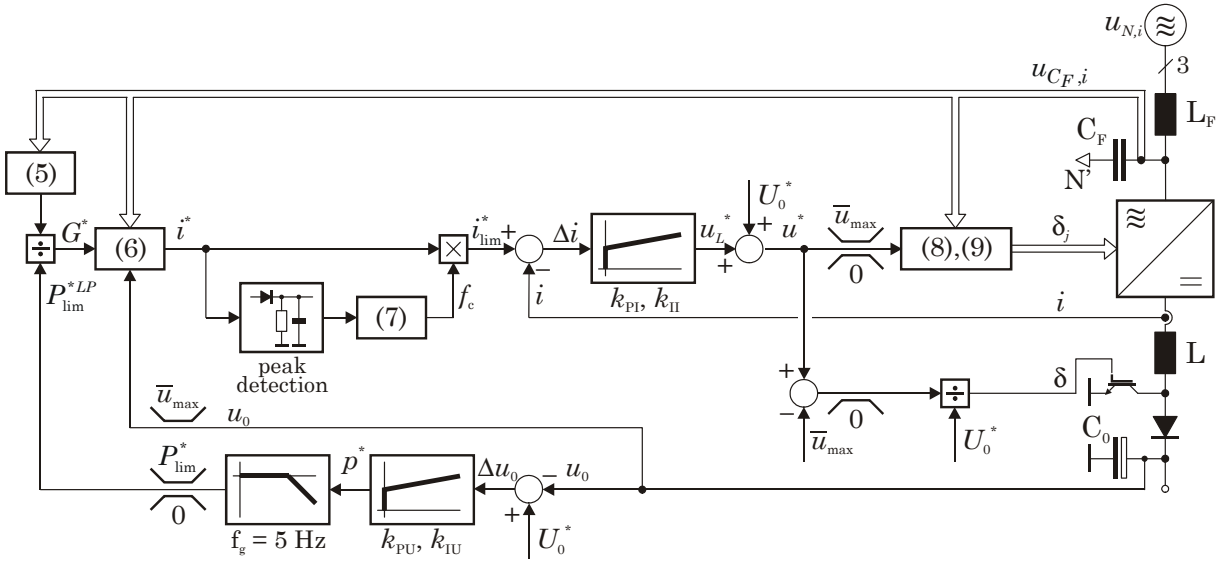

Fig. 2: Control structure guaranteeing unity power factor operation under heavily unbalanced mains.

- The output of the DC link current controller sets the reference value of the voltage across the DC link inductor u_L^* which is pre-controlled with the output voltage reference value U_0^* resulting in the buck stage output voltage reference value u^*.
- The relative on-times of the active switching states of the buck input stage $\delta_{Act,1}$, $\delta_{Act,2}$ are then calculated employing

$$\delta_{Act,1} = -\frac{u^* \cdot u_{C_F,T}}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}, \quad (8)$$

$$\delta_{Act,2} = -\frac{u^* \cdot u_{C_F,S}}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}, \quad (9)$$

  for deactivated as well as for active boost output stage [1], where the buck stage output voltage reference value u^* is limited to $\overline{u}_{\rm max}$, i.e. $u^* \leq \overline{u}_{\rm max}$ is valid.
- Beyond the modulation limit of the buck input stage, i.e. for $u^* > \overline{u}_{\rm max}$, the reference value of the voltage across the DC link inductor can not be generated by the buck stage any longer, therefore, the boost power transistor has to be activated in order to decrease the right hand side potential of the DC link inductor, i.e. for achieving $\overline{u}' < u_0$, where $\overline{u}'$ is the voltage across the boost power transistor. For the boost output stage

$$\overline{u}' = (1-\delta)\, u_0 \quad (10)$$

  is valid for continuous conduction mode. For the voltage across the inductor we have in general

$$u_L^* = \overline{u}_{\rm max} - \overline{u}'; \quad (11)$$

  with this one receives for the relative on-time of the boost power transistor,

$$\delta = 1 - \frac{\overline{u}_{\rm max} - u_L^*}{U_0^*}. \quad (12)$$

  For the calculation of δ $u_0 = U_0^*$ is assumed due to the provided output voltage control. The calculation is realized in the control structure (cf. Fig. 2) by

$$\delta = \frac{u^* - \overline{u}_{\rm max}}{U_0^*}, \quad (13)$$

  where $u^* = u_L^* + U_0^*$. By a limitation of the numerator to a lower value of zero, $\delta = 0$ is realized if the operation of the boost stage is not necessary (deactivated boost stage).

Remark: All equations given are valid within the whole mains period, except (8) and (9), which are only valid for an input filter capacitor voltage condition $u_{C_F,R} > 0 > u_{C_F,S} > u_{C_F,T}$. Equations for other relations of the mains phase voltages could be derived based on [1]. Furthermore, the equations are given for a constant modulation index limit of the buck input stage if $u_0 > \overline{u}_{\rm max}$, i.e. the modulation index is held on a constant value during the mains period, e.g. at the maximum modulation index $M_{\rm max} = 1$ (in case active damping of the input filter is provided [8], the modulation index limit has to be decreased to e.g. $M_{\rm max} = 0.9$ in order to have a margin for control).

4 Experimental Results

The experimental results are carried out on a prototype of the three-phase rectifier system showing the following parameters:

$U_{N,ll}$	= (208..480) V	$U_0^* = 400\,\mathrm{V}$	$P_0 = 5\,\mathrm{kW}$
f_N	= 50 Hz,	$L_F = 130\,\mu\mathrm{H}$	$L = 2 \times 0.9\,\mathrm{mH}$
f_P	= 23.4 kHz	$C_F = 4\,\mu\mathrm{F}$	$C_0 = 750\,\mu\mathrm{F}$,

the dimensions of the rectifier system are $(16 \times 34 \times 11)$ cm^3, the complete control is implemented in a 32-bit floating point digital signal processor ADSP-21061

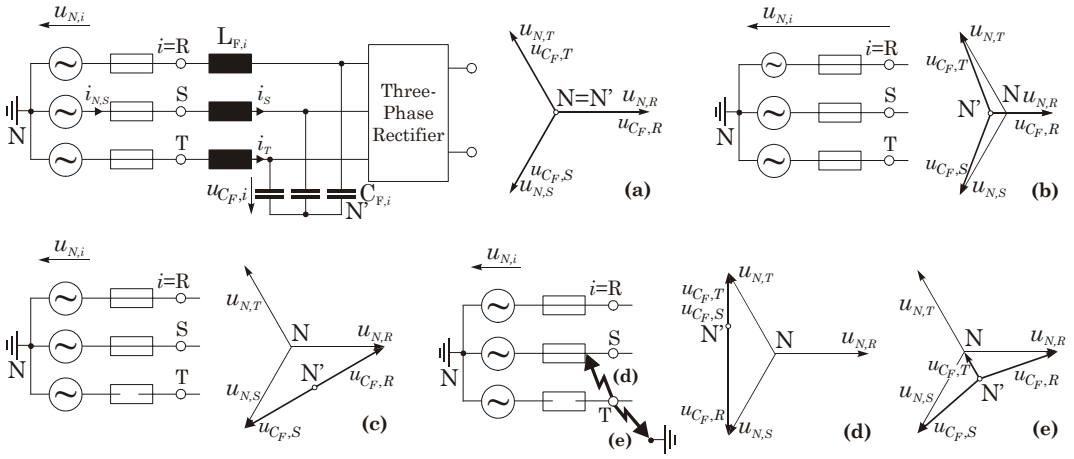

Fig. 3: Mains phase conditions and corresponding phasor diagrams of mains phase voltages $u_{N,i}$ and input filter capacitor voltages $u_{C_F,i}$. **(a)**: symmetric mains condition, **(b)**: mains phase voltage unbalance: $u_{N,R}$ is 50% smaller than for symmetric conditions (for experimental results see Fig. 8). **(c)**-**(e)**: Two-phase operation, **(c)**: loss of phase T, **(d)**: short circuit between phases S and T, and **(e)**: earth fault of phase T.

SHARC (Analog Devices). The inductance values L_F and L (iron powder core inductors) are both given for $i_N = 15$ A and/or $i = 15$ A.

4.1 Investigated Mains Conditions

In **Fig. 3** the different mains conditions and corresponding phasor diagrams which are investigated in this paper are depicted. For symmetric mains (Fig. 3(a)) we have equal amplitudes of the phase voltages (referred to the mains neutral point N) and of the input filter capacitor voltages (referred to the artificial neutral point N') and a phase displacement of the phase quantities of 120°el. Figure 3(b) shows the behavior of the mains phase voltages and of the input filter capacitor voltages in case the voltage in phase R is 50% smaller than under symmetric conditions. If one phase is missing at the rectifier input, e.g. after tripping of a fuse in phase T, the remaining input filter capacitor voltages $u_{C_F,R}$ and $u_{C_F,S}$ are 180°el. out of phase, cf. Fig. 3(c). If one phase (phase T) is connected to another phase (phase S in Fig. 3(d)) as caused by an input voltage short circuit (after tripping of a fuse in phase T) only one line-to-line voltage is remaining for delivering the output power, there, $u_{C_F,S}$ and $u_{C_F,T}$ do show identical shapes and are 180°el. out of phase to $u_{C_F,R}$. Another failure condition is the connection of one phase (phase T after tripping of a fuse in phase T, cf. Fig. 3(e)) to the mains neutral as could be caused by an earth fault.

4.2 Transition between Two Mains Conditions

In **Fig. 4** experimental results which confirm the proposed control method are given. The operating behavior for the disconnection (cf. Fig. 4(a), (b)) and for the reconnection (cf. Fig. 4(c), (d)) of one mains phase (phase T) as well as for the transition from the loss of phase T to a mains phase short circuit from phase T to phase S (cf. Fig. 4(e), (f)) and to short circuit to the mains neutral (i.e. earth fault) (cf. Fig. 4(g), (h)) are given. There, the input filter capacitor voltages $u_{C_F,i}$, the mains phase currents $i_{N,i}$ as well as the output voltage u_0 and the DC link current i are given. The mains phase currents remain proportional to the input filter capacitor voltages at any time, i.e. the rectifier system emulates a three-phase ohmic resistor. The deviation of the voltage from a purely sinusoidal shape is not caused by the rectifier system but is also present for no load operation[2].

As a closer investigation of the rectifier input currents during a short circuit of two phases shows, an uneven partitioning of mains phase current $i_{N,S}$ to phases S and T does occur, i.e. the currents i_S and i_T through the corresponding input filter inductors (cf. Fig. 3(a)) do not show a sinusoidal behavior, cf. **Fig. 5**. The path of the rectifier input currents $i_{U,i}$ is defined by the relative on-times of the active switching states of the buck input stage, which are selected in dependency on the relation of the input filter capacitor voltages (i.e. the actual position in the mains period). In case of a short circuit between phases S and T we have $u_{C_F,S} = u_{C_F,T}$, i.e. we are located at the boundary of two mains intervals[3]. Due to unbalances and/or offsets in the signal electronics (operational amplifiers, resistors, A/D-converters, etc.) a toggling of the interval detection from one interval to the adjacent interval does occur which influences the partitioning of mains phase current $i_{N,S}$ to phases S and T. This effect does not take any influence on the purely resistive mains behavior of the rectifier system (the resulting mains phase current $i_{N,S} = i_S + i_T$ (cf. Fig. 3(a)) is sinusoidal and in phase with the corresponding mains voltage), but a slight re-

[2]This distortion is caused by office machines and computers and/or single phase rectifiers with capacitive smoothing which are connected in high numbers to the supplying mains in the Vienna University of Technology.

[3]For symmetric mains we have 12 mains intervals.

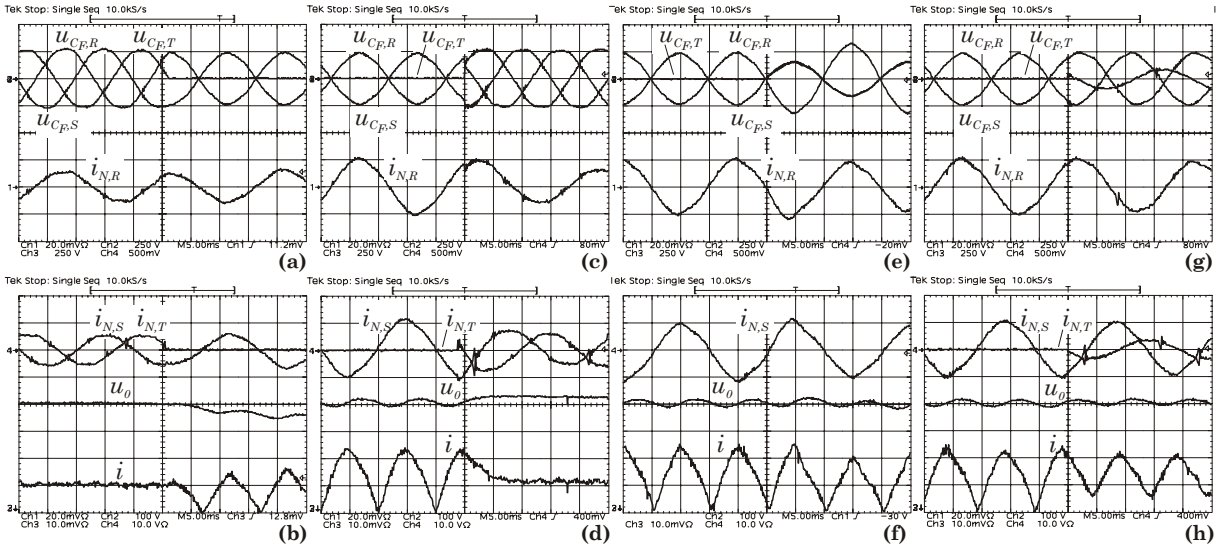

Fig. 4: Experimental results for different mains conditions: **(a), (b)**: Loss of phase T (for the time behavior of $i_{N,S}$ and $i_{N,T}$ over several mains periods see Fig. 6(a)), **(c), (d)**: Reconnection of phase T (return to symmetric mains), **(e), (f)**: Short circuit between phases S and T during loss of phase T and **(g), (h)**: Short circuit to mains neutral during loss of phase T. Operating conditions: 330 V_{rms} line-to-line voltage, 400 V output voltage and 2.2 kW output power. (a), (c), (e), (g): Time behavior of input filter capacitor voltages $u_{C_F,i}$, and mains phase current $i_{N,R}$, (b), (d), (f), (h): mains phase currents $i_{N,S}$, $i_{N,T}$, output voltage u_0 and DC link current i. Voltage scales: $u_{C_F,i}$: 250 V/div, u_0: 100 V/div, current scales: $i_{N,i}$: 10 A/div, i: 5 A/div, time scale: 5 ms/div.

duction of the efficiency could be possible. However, due to the fact that a two-phase operation is only present in case of a failure, the reduction in efficiency can be accepted.

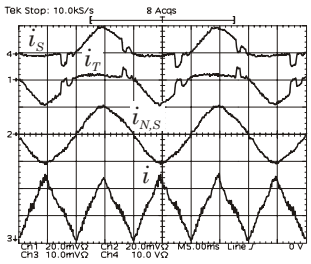

Fig. 5: Current partitioning to phases S and T (given by i_S, i_T) during short circuit of phase S and T and loss of phase T (cf. Fig. 3(d)) and resulting mains phase current $i_{N,S} = i_S + i_T$. Current scales: i_S, i_T, $i_{N,S}$: 10 A/div, i: 5 A/div.

4.3 Behavior of the Output Voltage

Regarding Fig. 4 one can see that no overvoltages and/or overcurrents or any ringing do occur at the transition between the mains conditions. There is only a voltage dip or surge in the output voltage in case of disconnection (cf. **Fig. 6**(a)) or reconnection (cf. Fig. 6(b)) of one mains phase. In case of a phase loss the output voltage dip u_- is approximately 60 V, for the reconnection a voltage surge u_+ of 20 V does occur for 330 V line-to-line voltage and 2.2 kW output power.

In case of a mains failure the output voltage shows a 100 Hz ripple component which is due to the pulsation of the total power taken from the mains due to the relatively low output capacitance of 750 μF. In **Fig. 7** the size of the ripple component is depicted for different types of mains failures and for different levels

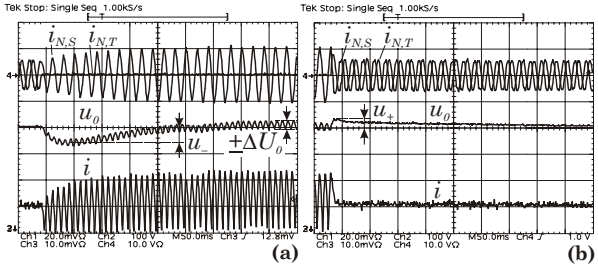

Fig. 6: Time behavior of the output voltage for disconnection **(a)** and reconnection **(b)** of mains phase T. Operating parameters, voltage and current scales as in Fig. 4, time scale: 50 ms/div. $\pm\Delta U_0$ denotes the output voltage ripple with two times the mains frequency.

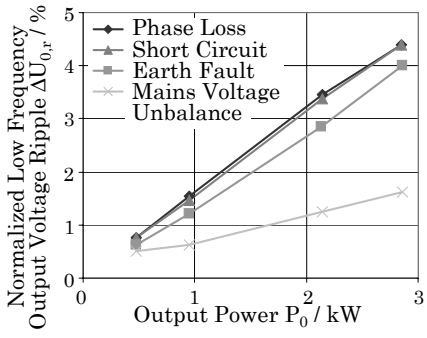

Fig. 7: Normalized output voltage ripple $\Delta U_{0,r}$ in dependency on the output power P_0 for different mains failures for an average value of the output voltage of $U_0 = 400$ V.

of output power, there $\Delta U_{0,r}$ is the amplitude of the low-frequency component ΔU_0 (cf. Fig. 6(a)) with reference to the rated output voltage, i.e. $\Delta U_{0,r} = \Delta U_0 /$ 400 V. One can see that the output voltage ripple shows a linear dependency on the output power and is (ap-

proximately) the same in case of the loss of one phase and of a short circuit of two phases which is due to the fact that in both cases the operation is with a single line-to-line input voltage. In case of a short circuit to the mains neutral the output voltage ripple is approximately 15 % smaller resulting from the modified DC link current behavior (which does not become zero in this case). The smallest output voltage ripple occurs in case of a mains voltage unbalance, however, it is depending on the amount of the unbalance. This results from the fact that for a mains unbalance we have a lower alternating power component than for two-phase operation (cf. Fig. 3(c)-(e)).

The time behavior of input and output quantities for a mains voltage unbalance (cf. Fig. 3(b)) is given in **Fig. 8**. There, voltage $u_{N,R}$ is assumed to be 50% lower than for balanced mains.

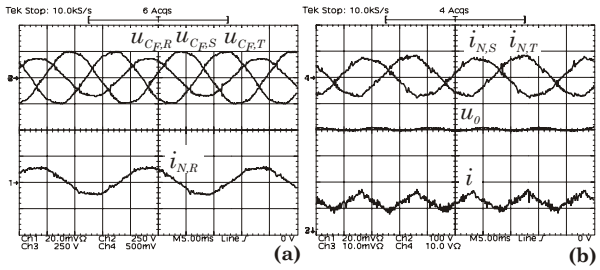

Fig. 8: Experimental results for a mains phase voltage unbalance, where mains phase voltage $u_{N,R}$ is 50% smaller than for symmetric conditions: **(a)**: Time behavior of input filter capacitor voltages $u_{C_F,i}$, and mains phase current $i_{N,R}$, **(b)**: mains phase currents $i_{N,S}$, $i_{N,T}$, output voltage u_0 and DC link current i. Operating parameters, voltage and current scales as in Fig. 4, time scale: 5 ms/div.

4.4 DC Side Current Limitation

In case of a phase loss or short circuit of two phases only one line-to-line voltage is available for delivering the output power, i.e. we have a two-phase operation and a limited output power $P_{\max,2\sim} = P_{\max,3\sim}/\sqrt{3} = 2.9$ kW[4]. The limitation to this maximum admissible value is due to the DC link current limitation (cf. Fig. 2 and (7)). The maximum admissible DC link current value is set to 25 A. Therefore, the limitation concerning the average value is actually 22 A due to the superimposed current ripple. In **Fig. 9** the time behavior of mains phase current $i_{N,R}$, DC link current i and output voltage u_0 are given in case of a loss of phase T. The binary signal $s_{L,DC}$ indicates DC link current limitation, $s_{L,DC} = 0 \rightarrow 1$). One can see that the DC link current limitation results in an output voltage limitation and hence in an output power limitation.

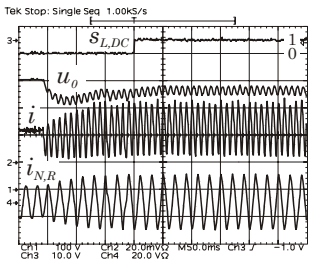

Fig. 9: DC-side current limitation to 22 A peak during phase of phase T, signal indicating limitation $s_{L,DC}$. Operating parameters: load: 73 Ω, line-to-line voltage 208 V_{rms}. Voltage scale: u_0: 100 V/div, current scales: i: 10 A/div, $i_{N,R}$: 20 A/div, time scale: 50 ms/div.

[4]With $P_{\max,2\sim} = 2\,U_{N,2\sim}I_N$ and $U_{N,2\sim} = \sqrt{3}/2\,U_{N,ll}$ (cf. Fig. 3(c)) and with $P_{\max,3\sim} = \sqrt{3}\,U_{N,ll}I_N$.

5 System Characteristics

In this section quantities which do characterize the system behavior, i.e. efficiency η, power factor PF and total harmonic distortion THD_A of the mains phase currents, are given for symmetric mains and for the investigated mains failure conditions for different output power levels of $P_0 \approx (0.5; 1; 2; 3)$kW and 400V output voltage for three mains line-to-line voltages $U_{N,ll} = (208; 330; 450)\,V_{rms}$ representing the lower, middle and upper input voltage range. The operating point for $U_{N,ll} = 208V_{rms}$ and $P_0 \approx 3$kW could not be achieved due to the DC link current limitation (cf. section 4.4).

5.1 Power Factor

The power factor of the PWM rectifier system is given in **Fig. 10**. At low output power and for high mains voltage, the power factor shows lower values than at higher output power and low input voltage. This is due to the lower mains phase current and the higher percentage of the reactive input filter capacitor current. In case of a mains failure, which results in a two-phase operation and/or a higher load on two mains phases, the power factor is increased especially for low output power levels. The relatively low value of the power factor for a mains failure at $U_{N,ll} = 208$V is due to the fact that a resonance of input filter and supplying autotransformer does occur. Generally one can say that the power factor lies between $PF = 0.992$ and 0.998 for an output power $P_0 \geq 2$ kW.

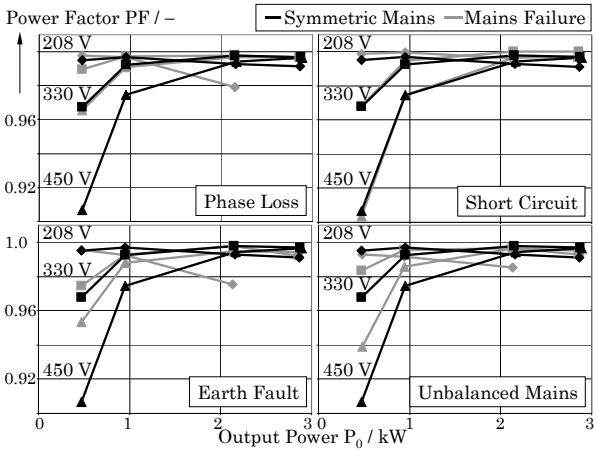

Fig. 10: Power factor PF of the rectifier system for symmetric mains and mains failures and different line-to-line rms voltages $U_{N,ll}$ in dependency on the output power P_0.

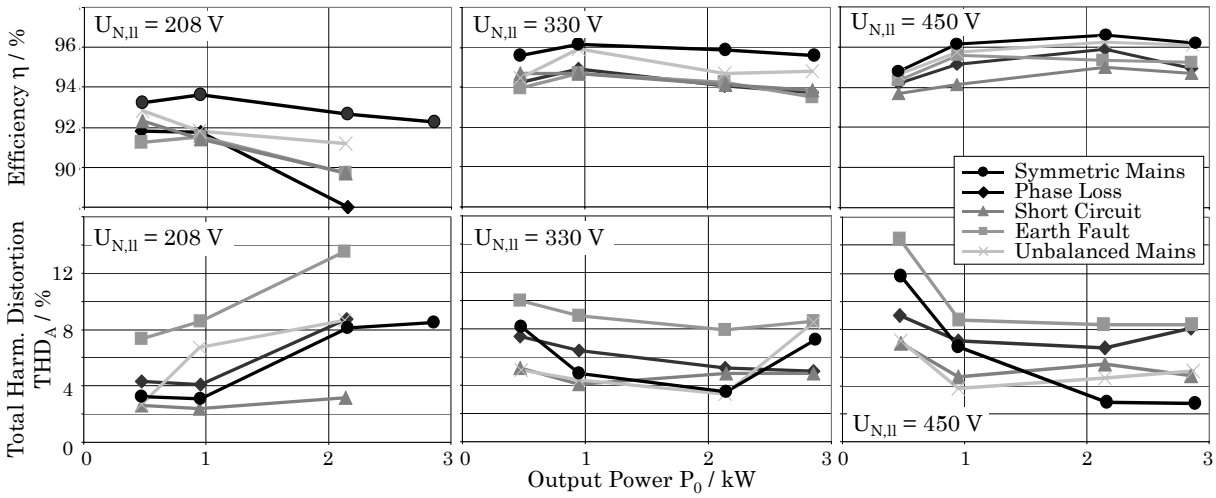

Fig. 11: Efficiency η of the rectifier system and total harmonic distortion THD_A of the mains phase currents for symmetric mains and mains failures and different line-to-line rms voltages $U_{N,ll}$ in dependency on the output power P_0.

5.2 Efficiency

In case of a mains failure, the efficiency is reduced in all operating points. This is due to the fact that for increasing input current (due to two-phase operation) switching and conduction losses in the power semiconductors as well as losses of passive components do increase (cf. **Fig. 11**).

5.3 Total Harmonic Distortion

For low input current values and low output power levels the total harmonic distortion of the mains phase currents shows higher values which is again due to the input filter attracting current harmonics from the mains, for increasing output power the total harmonic distortion is approximately constant, except for low input voltages of $U_{N,ll} = 208$V (i.e. high input currents) where a resonance between input filter and autotransformer does occur (cf. Fig. 11). Remark: For no-load operation, the total harmonic distortion of the mains phase voltages is $\approx (2.0 \ldots 2.3)\%$.

6 Conclusions

A new control concept for reliable operation of a three-phase buck+boost PWM unity power factor rectifier under different mains failure conditions (mains voltage unbalance, loss of one mains phase, short circuit of two mains phases and earth fault) has been presented. The control consists of an outer output voltages control loop which sets the DC link current reference value, and an inner DC link current control loop which provides the control signals for both the buck input stage and the boost output stage. In order to keep all quantities within admissible values also in case of two-phase operation, the DC link current reference value is limited. As shown by experimental results, the rectifier system behaves like a symmetric ohmic load for balanced and unbalanced mains conditions. The input currents show a sinusoidal shape independent on the mains condition, and for the transition from symmetric mains to a mains failure and vice versa no overvoltages or overcurrents or oscillations do occur. It is furthermore shown that there are no major deviations for efficiency, power factor and total harmonic distortion for operation during a mains failure as compared to symmetric mains operation.

The considerations are valid only for continuous conduction mode (CCM). However, at low output power discontinuous conduction mode (DCM) does occur. In order to avoid DCM, the DC link inductor current reference value could be increased by adding an offset. However, this also would result in an increasing system output power. Therefore, in order to keep the desired output power value, the duty cycle δ of the boost stage has to be increased and/or the boost stage has to be activated. In connection with lowering the buck-stage modulation index this does result in a circulating part of the DC link current via the buck stage and the boost switch, whereby an influence on the delivered output power could be compensated.

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