Analysis of the Effects of Non-Idealities of Power Components and Mains Voltage Unbalance on the Operating Behavior of a Three-Phase/Switch Buck-Type Unity Power Factor PWM Rectifier

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Abstract – According to the experimental analysis of a 5kW wide input voltage range three-phase three-switch buck-derived unity power factor PWM rectifier, the ideally constant DC output current does show a low-frequency distortion for open-loop control operation which is translated into low-frequency harmonics of the mains current. This distortion cannot be eliminated completely by closed-loop control since the controller bandwidth has to be limited for stability reasons and/or in order to avoid an excitation of the LC input filter. In this paper the parasitic effects being responsible for the low-frequency distortions of DC output voltage and/or current are analyzed analytically and quantified for different operating conditions. Furthermore, the minimization of the influence of the parasitic effects by proper pre-control is discussed. All theoretical considerations are confirmed by digital simulations.

I Introduction

In [1] the experimental analysis of a 5kW wide input voltage range unity power factor three-phase buck+boost PWM rectifier system [2],[3] with three-switch buck-type input stage and boost-type output stage has been discussed. The investigation has shown clearly that for open-loop operation a low-frequency distortion of the ideally constant buck-stage output current does occur, which does result in a distortion of the currents drawn from the mains (cf. **Fig. 1**). This effect cannot be eliminated completely by an output current control since the controller bandwidth has to be limited for stability reasons and/or in order to avoid an excitation of the buck-stage LC input filter which would result for ideally constant power operation. Therefore, one has to clarify the origin of the non-ideal behavior in order to provide a proper pre-control or hardware adaption for improving the output and mains current quality.

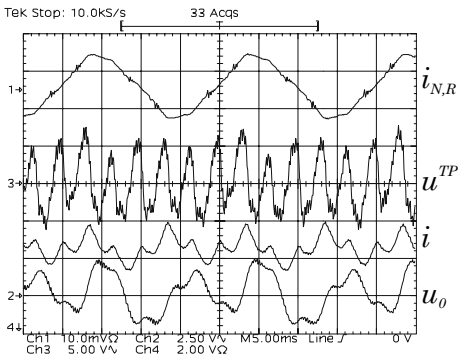

Fig. 1: Time behavior of mains phase current $i_{N,R}$ (5A/div.), of AC components of the buck-stage output voltage u (5V/div), of the system output voltage u_0 (2.5V/div), and of the DC output current i (2A/div) for open-loop operation (output power: 1 kW, $U_0 = 400\,\mathrm{V}$, $U_{N,l-l} = 400\,\mathrm{V}$)

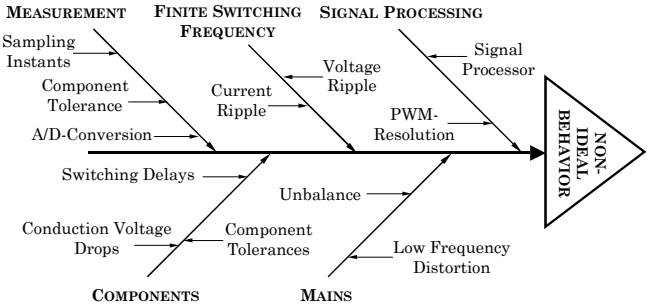

Fig. 2: Origins of the non-ideal behavior of a three-phase/three-switch buck-type PWM rectifier system resulting in AC- and DC-side voltage and current distortion.

In this paper the effect of an

- unbalance or of a low-frequency distortion of the mains phase voltages, of the
- conduction voltage drops of the power semiconductors, of the
- accuracy and resolution of the signal processing, of the
- accuracy of voltage and current measurement, and of the
- switching delays of the power transistors

on the operating behavior of the three-phase three-switch buck-type input stage of the rectifier system is analyzed. A classification of all non-idealities analyzed is shown in **Fig. 2** in the form of a Fishbone-Diagram.

In **section II** the influences of the different non-idealities on the operating behavior are treated analytically where always only a single non-ideality is investigated and/or no mutual interactions of different non-idealities are considered. In **section III** the absolute values of the effects of the non-idealities are given for rated output power, and are shown to be e.g. in the range of 0.1 V to a few volts for the buck-stage output voltage and are comprising a DC component and low-frequency AC components. Finally, in **section IV** measures available for eliminating the undesired effects are discussed with reference to the experimental set-up and results of digital simulations are shown.

II Origins of Non-Ideal Operating Behavior

In this section the origins of the non-ideal stationary operating behavior (cf. Fig. 2) of the three-phase/switch buck PWM rectifier system depicted in **Fig. 3** are analyzed analytically. There, the behavior of buck-stage output voltage u and output current i, and of the mains phase currents $i_{N,i}$, $i = R, S, T$ is investigated, and formulas are given in order to be able to determine the relevance of the different effects.

II.A Conduction Voltage Drops of Power Semiconductors

For achieving a resistive fundamental mains behavior $i_{N,i} \sim u_{N,i}$, $i = R,S,T$, and for neglecting the fundamental of the input filter capacitor currents, i.e. for assuming $i_{N,i} \approx i_{U,(1),i}$, fundamentals of the discontinuous rectifier input phase currents $i_{U,i}$ lying in phase with the corresponding mains phase voltages $u_{N,i} \approx u_{C_F,i}$ have to be formed by setting the relative on-times of the power transistors S_i, $i = R,S,T$, proportional to the instantaneous values of the mains phase voltages [3]. Thereby, the buck-stage output current[1] I is distributed sinusoidally to the mains phases and/or the buck-stage output voltage u is formed by segments of the mains phase-to-phase input filter capacitor voltages.

Within one pulse period there are two active switching states, where current is drawn from the mains, and one free-wheeling state[2], where the buck-stage output current path is via the free-wheeling diode D_F. If we consider the interval of the mains period where a relation of the mains phase voltages is given according to

$$u_{N,R} > 0 > u_{N,S} > u_{N,T}, \tag{1}$$

the active switching states are $j = (110)$ and $j = (101)$[3]. Within each active switching state, there are four power diodes $D_{(N),i}$ and two power transistors S_i involved in current conduction, which is clearly shown in Fig. 3 for switching state $j = (101)$.

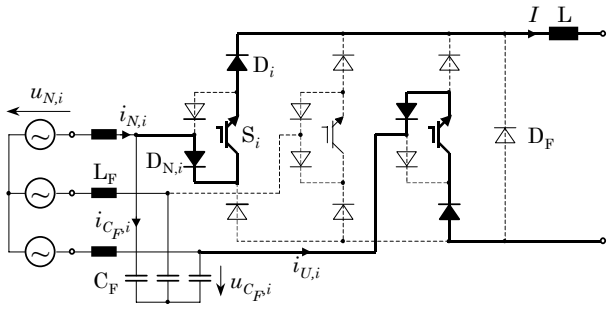

Fig. 3: Structure of the power circuit of the buck-type input stage. The current path for switching state $j = (101)$ is highlighted.

The forward characteristic of the power diodes as known from the data sheet (cf. Fig. 1 in [4]) can be approximated by

$$V_{D,F} = V_{F,0} + r_D\, I, \tag{2}$$

where $V_{F,0} = 0.92\,\mathrm{V}$ and $r_D = 10\,\mathrm{m\Omega}$ is valid. Analogously, considering Fig. 2 in [5] the forward characteristic of the IGBTs can be approximated by

$$V_{S,F} = V_{CE,0} + r_{CE}\, I \tag{3}$$

with $V_{CE,0} = 1.5\,\mathrm{V}$ and $r_{CE} = 22.5\,\mathrm{m\Omega}$. The series connection of power diodes and power transistors does cause a voltage drop reducing the instantaneous values of the buck-stage output voltage u as compared to the ideal value

$$\begin{aligned} j = (101): &\quad u_{(101)} = u_{C_F,RT} - 4V_{D,F} - 2V_{S,F}, \\ j = (110): &\quad u_{(110)} = u_{C_F,RS} - 4V_{D,F} - 2V_{S,F}, \\ j = (000): &\quad u_{(000)} = -V_{D,F}. \end{aligned} \tag{4}$$

[1] In a first step the inductor current can be assumed to be constant and impressed by the output inductor.

[2] The characterization of the switching state of the buck rectifier is given by the combination $j = (s_R\, s_S\, s_T)$ of the phase switching functions. There, a phase switching function s_i does characterize the switching state of the corresponding power transistors S_i, $i = R,S,T$, where $s_i = 0$ denotes the off-state, and $s_i = 1$ denotes the on-state.

[3] Switching state $j = (101)$ is equal to switching state $j = (111)$ within (1).

With this, one receives with the relative on-times δ_j of the switching states for the local average value (within one pulse period) of the buck-stage output voltage

$$\begin{aligned} u(\varphi_U) &= u_{(101)}\,\delta_{(101)} + u_{(110)}\,\delta_{(110)} + u_{(000)}\,\delta_{(000)} = \\ &= \underbrace{\sqrt{3}\,M\,\hat{U}_{N,l-l}/2}_{\text{ideal value}} - \underbrace{[M\,(3\,V_{D,F} + 2\,V_{S,F})\,\cos(\varphi_U) + V_{D,F}]}_{\text{voltage drop}}, \end{aligned} \tag{5}$$

where M denotes the modulation index of the buck input stage being defined by the ratio of the amplitude of the mains phase current to the buck-stage output current,

$$M = \hat{I}_N / I \qquad M \in [0;1]. \tag{6}$$

The first part of expression (5) denotes the ideal and constant value of the buck-stage output voltage, the second term is due to the voltage drops across the conducting power semiconductors which is time-varying over the mains period due to the varying width of the turn-on intervals. For the global average value (within one mains period) of the non-ideal buck-stage output voltage one receives

$$\begin{aligned} U &= \frac{1}{\pi/3}\int_{-\pi/6}^{+\pi/6} u(\varphi_U)\,\mathrm{d}\varphi_U = \\ &= \frac{\sqrt{3}\,M\,\hat{U}_{N,l-l}}{2} - \left[\frac{3\,M}{\pi}\,(2\,V_{S,F} + 3\,V_{D,F}) + V_{D,F}\right]. \end{aligned} \tag{7}$$

The AC-component of the buck-stage output voltage is showing the following harmonic spectrum:

$$\begin{aligned} u(\varphi_U) - U &= \sum_{k=6,12,..}^{\infty} \frac{6M(3V_{D,F} + 2V_{S,F})}{(k+1)(k-1)\pi}\cos(k\varphi_U)(-1)^{k/6} = \\ &= \frac{6M(3V_{D,F} + 2V_{S,F})}{\pi}\left(-\frac{\cos(6\varphi_U)}{35} + \frac{\cos(12\varphi_U)}{143} - \ldots\right) \end{aligned} \tag{8}$$

The effects of the conduction voltage drops of the power semiconductors on the buck-stage output voltage are the reduction of the global average value in dependency on modulation index and output power, and the generation of a 6^{th}, 12^{th},... harmonic in the buck-stage output voltage, leading to a corresponding output current distortion for open loop operation. This distortion is translated into the system input currents, where 5^{th}, 7^{th}, 11^{th}, 13^{th},... harmonics are generated.

II.B Distorted Mains Voltage

The control algorithm of the three-phase buck-type rectifier system is realized such that the local average value of the DC output voltage shows a constant value over the mains period, i.e. constant power is drawn from the mains independent of the mains voltage behavior. Assuming that the feeding mains contains low-frequency harmonics, e.g., a 5^{th} and 7^{th} harmonic, as resulting from heavy loading by single-phase diode rectifiers with capacitive smoothing, the corresponding mains phase current harmonics with ordinal numbers $5, 7, 11, 13\ldots$ (which are not attenuated by the switching frequency LC-input filter) show significant amplitudes [6], [7]. In **Fig. 4** this is confirmed by a digital simulation employing CASPOC® [8], where a 5^{th} harmonic with an amplitude of 5% of the fundamental voltage was impressed. As a spectrum analysis shows (cf. Fig. 4(b)), a purely DC buck-stage output voltage and/or a purely DC output current are resulting, but the mains phase currents do exhibit a significant 7^{th} harmonic. The amplitude $\hat{I}_{N,(7)}$ of the harmonic can be calculated according to [7],

$$\hat{I}_{N,(7)} = \frac{2}{3}\frac{\hat{U}_{N,(5)}\cdot P_0}{\hat{U}^2_{N,(1)}} = \frac{2}{3}\cdot\frac{2.5\mathrm{V}\cdot 50\mathrm{V}\cdot 9.8\mathrm{A}}{(50\mathrm{V})^2} = 0.33\mathrm{A}, \tag{9}$$

which is in good agreement with the simulation result of 0.34 A.

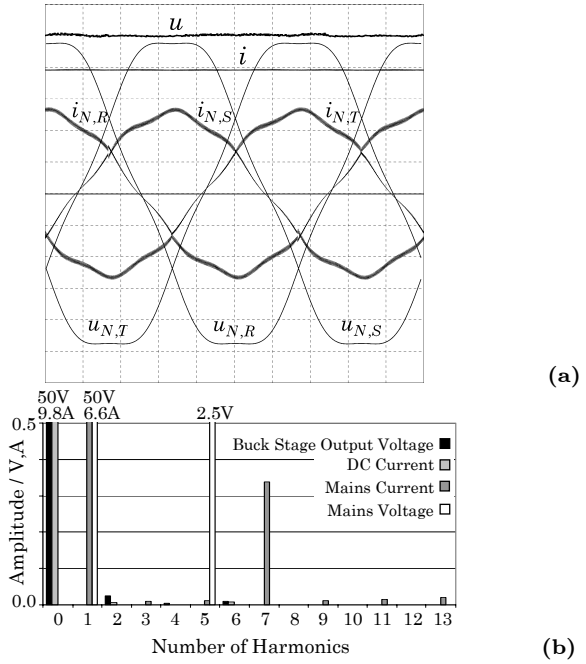

Fig. 4: Simulation of the time behavior of mains phase voltages $u_{N,i}$, mains phase currents $i_{N,i}$, $i = R, S, T$, buck-stage output voltage u and DC current i **(a)**, and related spectra **(b)** for unbalanced mains phase voltages. Time scale: 2ms/div, voltage scale: 10V/div, current scale: 2.5A/div.

II.C Input Voltage Measurement

In order to incorporate the relevant voltages and currents into the system control, a measurement circuit employing differential amplifiers is provided. The accuracy of the signal measurement and/or level adaption is dependent on the tolerance of the resistors, therefore, common-mode and differential-mode errors do occur. In **Fig. 6** the signal adaption circuit and the bandpass-filtering for the input filter capacitor voltages is depicted for phase R, N is an artificial neutral point which is not connected to the mains but formed by the parallel connection of C_f and R_f. For the adapted input filter capacitor voltage one receives

$$\frac{u^{BP}_{C_F,R}}{200} = \left[\frac{u_N\, R_4}{R_3+R_4}\frac{R_1+R_2}{R_1} - (u_{C_F,R}+u_N)\frac{R_2}{R_1}\right]\frac{R_{TP}}{R_{HP}}. \quad (10)$$

If resistors with a tolerance of 0.1 % are employed, the maximum (minimum) error after signal adaption and bandpass-filtering is ±0.7 % of the measured voltage.

Furthermore, a difference in the resistors R_f and capacitors C_f forming the artificial neutral point N causes an unbalance in the measured voltages, which is introduced into the calculation of the relative on-times of the power-transistors resulting in a distortion of the buck-stage output voltage. In order to avoid this influence, a zero sequence system of the measured input voltages is eliminated mathematically in the DSP-program. Therefore, a displacement of the artificial neutral point does not cause a buck-stage output voltage distortion.

II.D Signal Processing

The control of a 5 kW prototype of the three-phase buck+ boost PWM rectifier system is realized using a 32-bit floating point digital signal processor ADSP-21061 SHARC (Analog Devices [9]) [10]. The analog signals are adapted (cf. section II.C) and digitized by 12-bit A/D converters of type AD7892-3 (Analog Devices [11]) having an analog input range of ±2.5 V. The positive (negative) full-scale error is ±4 LSB, which results in a maximum percentage voltage error of

$$|v_{err,ADC}| = 4/2048 = 0.2\,\%. \quad (11)$$

For calculating the relative on-times and for the digital control a signal processor with 32-bit floating point arithmetic is employed, the resulting error therefore can be neglected.

The error resulting from the PWM output resolution is dependent on the quartz oscillator frequency f_Q and/or on the precision of the counters realizing the PWM control as well as on the pulse frequency f_P (during $1/f_P$ a complete switching state sequence is applied to the buck input stage). One receives for the worst-case error

$$|v_{err,PWM}| = \frac{2\sqrt{3}\,f_P}{f_Q}\hat{U}_{N,l-l}. \quad (12)$$

In this case a 12 MHz oscillator and a 8-bit counter are employed, resulting in a pulse frequency of $f_P = 23.4$ kHz and/or in $|v_{err,PWM}| = 0.0068 \cdot \hat{U}_{N,l-l}$.

II.E Switching Delay

The switching time errors result from signal delays of the gate drive units and from turn-on or turn-off delay times of the power transistors. The experimental investigation shows, that a total turn-on delay time of $t_{d,ON} \approx 380$ ns and a total turn-off delay-time of $t_{d,OFF} \approx 470$ ns does occur in the case at hand. In **Fig. 5** the ideal switching signals s_i and the switching signals including the delay times as well as the time behavior of the buck-stage output voltage are given for a pulse period T_P within mains interval (1). The difference of the turn-on and turn-off delay times results in a distortion of the local average value of the buck-stage output voltage. The distortion shows a maximum absolute value of

$$|v_{err,d}| = \frac{t_{d,OFF} - t_{d,ON}}{T_P/2}\sqrt{3}\hat{U}_{N,l-l}, \quad (13)$$

resulting in $|v_{err,d}| = 0.0073 \cdot \hat{U}_{N,l-l}$ for the given system parameters. Furthermore, this local distortion results in low-frequent components of the buck-stage output voltage and in a distortion of the mains phase currents. The distortion is depending on the relative difference between turn-on and turn-off delay time in relation to one pulse period,

$$\Delta\delta_d = (t_{d,OFF} - t_{d,ON})/T_P. \quad (14)$$

In the following, the buck-stage output voltage spectrum is given for

1. equal delay times for all three bridge legs, and for
2. a delay time being present only for one power transistor, while the other power transistors are assumed to show no delay times.

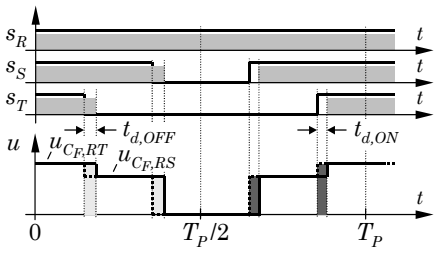

Fig. 5: Switching signals, switching delay times and resulting time behavior of the buck-stage output voltage u within one pulse period T_P valid for mains interval (1). The voltage-time integral errors are shown in grey (light gray: positive error, dark gray: negative error).

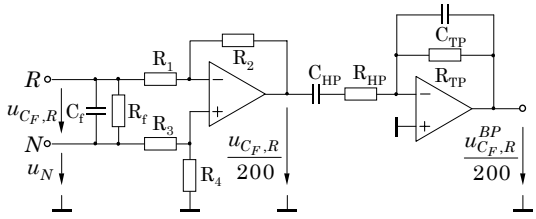

Fig. 6: Signal adaption and bandpass-filtering of the input filter capacitor voltages shown for phase R, N is an artificial neutral point not connected to the mains.

The resulting buck-stage output voltage spectrum for the first case results in

$$u(\varphi_U) = \frac{\sqrt{3}M\hat{U}_{N,l-l}}{2} - \frac{6\Delta\delta\,\hat{U}_{N,l-l}}{\pi}\left[\frac{1}{2} - \frac{\cos(6\varphi_U)}{35} - \frac{\cos(12\varphi_U)}{143} - \frac{\cos(18\varphi_U)}{323} - \dots\right], \quad (15)$$

for the second case one receives

$$u(\varphi_U) = \frac{\sqrt{3}M\hat{U}_{N,l-l}}{2} - \frac{4\Delta\delta\,\hat{U}_{N,l-l}}{\pi}\left[\frac{1}{4} + \frac{\cos(2\varphi_U)}{3} + \frac{\cos(4\varphi_U)}{15} - \frac{\cos(6\varphi_U)}{70} + \dots\right]. \quad (16)$$

The buck-stage output voltage harmonics do cause low-frequent harmonics in the output power which are directly transferred to the mains side (if the rectifier power losses are neglected, the input power equals the output power), hence the mains phase currents are distorted in a way that the pulsation of the power does result. There, the harmonic components are depending on the behavior of the mains phase voltages, furthermore the harmonics content will be different for mains phases R, S, T in the second case (delay time of only one power transistor or time delay of one power transistor being significantly larger than for the other power transistors), i.e. the AC side currents will contain positive and negative phase-sequence systems. E.g. one receives for a 3^{rd} harmonic component

$$\underline{I}_{N,(3)} = \hat{I}^{+}_{N,(3)} \cdot e^{3\jmath(\omega t+\varphi_3^{+})} + \hat{I}^{-}_{N,(3)} \cdot e^{-3\jmath(\omega t+\varphi_3^{-})}. \quad (17)$$

Moreover, an error in the buck-stage output voltage resulting from the different rates of rise of the forward voltage dv/dt at turn-on and turn-off does occur, which is dependent on mains phase voltage rms value and on the point in time considered within the mains period.

II.F Signal Sampling

For controlling the buck+boost PWM rectifier system, the buck-stage output current i and the input filter capacitor voltages $u_{C_F,i}$ are sampled twice per pulse period (sampling frequency: 46.875 kHz). In order to avoid an influence of the signal ripple components on the sampled values, the sampling instants are placed at the beginning of each pulse half period. There, the instantaneous values of DC current $i(t)$ and of input filter capacitor voltage $u_{C_F,i}(t)$ are equal to the local average values i and $u^{BP}_{C_F,i}$, respectively (cf. **Fig. 7**). However, time-delays in the measurement set-up do cause a slight time displacement of the sampling instants, hence the ripple components are not excluded entirely. Therefore, a low-pass filter for the DC current and a band-pass filter for the input filter capacitor voltage (mid-frequency: 50 Hz, cf. Fig. 6) are employed which eliminate the ripple components prior to sampling.

Remark: For designing the bandpass filter one should take into account that the low-frequency harmonics of the mains voltages (e.g., 5^{th}, 7^{th}) should not be attenuated by the bandpass filter in order to ensure a correct calculation of the on-times of the power transistors (cf. section II.B) and/or to guarantee a constant buck-stage output voltage (and/or prevent low-frequency power components).

II.G Finite Switching Frequency

Due to the finite switching frequency ripple components in the input and output quantities do result. As mentioned, the influence of the ripple components on measurement and hence on control can be eliminated by proper signal sampling and filtering. But, the ripple components are transferred from the AC side to the DC side and vice versa.

II.G.1 Input Filter Capacitor Voltage Ripple

As Fig. 7(b) shows, the input filter capacitor voltage ripple is superimposed on the buck-stage output voltage u, whereby a difference in the instantaneous values and an excess or a deficit in the voltage-time integral within one pulse half period occurs. If a switching state sequence is provided which shows a symmetric arrangement of the switching states within each pulse period, the aforementioned excess and deficit is balanced out in the subsequent pulse half period [12]. Therefore, the local and global average value of the buck-stage output voltage is not influenced by the input filter capacitor voltage ripple.

II.G.2 Buck-Stage Output Current Ripple

The DC ripple appears in the discontinuous rectifier input currents $i_{U,i}$ and does cause an excess or a deficit in the current-time-integral which is balanced out in the subsequent pulse half period (if a symmetric switching pattern is employed) (cf. section II.G.1).

For small values of the buck-stage output current (i.e. small output voltage U_0 and/or high load resistance R_0) the PWM rectifier does enter into discontinuous conduction mode (DCM) where the current in the DC side inductor is zero for a part of the pulse period. Therefore, the behavior of the current ripple changes and a 6^{th} harmonic does occur in the buck-stage output current. The harmonic is transferred to the mains, but the current-time integral is still zero within one pulse period. In order to avoid the operation in the discontinuous conduction mode, the boost output stage can be activated, whereby the average value of the DC current is shifted to higher values. DCM therefore will not be considered further in this paper.

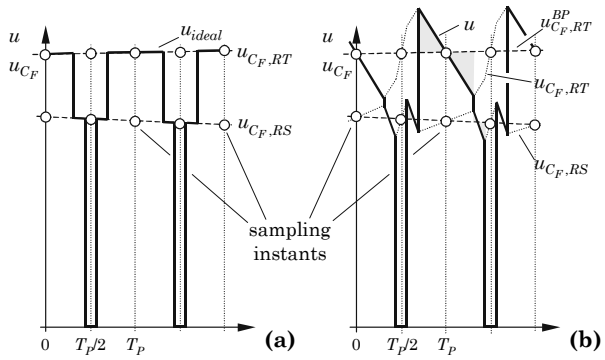

Fig. 7: Behavior of the buck-stage output voltage: **(a)** ideal behavior and **(b)** behavior under consideration of the input filter capacitor voltage ripple, valid for a mains phase interval (1).

Cause	Effect	Remark
Conduction Voltage Drops	0.61 V	Peak-to-peak value of AC components in the buck-stage output voltage
	0.25 V	Amplitude of the 6^{th} harmonic of the buck-stage output voltage
	5.4 V	Reduction of the average value of the buck-stage output voltage
Distorted Mains	≈ 0 V	No influence on the buck-stage output voltage for low-frequent harmonics in the mains
Measurement	2.7 V	Measurement of input filter capacitor voltages employing 0.1% resistors (worst case)
Signal Processing	0.78 V	12-bit A/D conversion (worst case)
	≈ 0 V	32-bit floating point signal processing → negligible effects
	4.6 V	12 MHz PWM signal output (worst case)
Switching Delays	**5.0 V**	Gate drive unit delay time + turn-on and turn-off delay times (worst case)
	0.04 V	Amplitude of the 6^{th} harmonic of the buck-stage output voltage for 1% additional switching delay of the power transistors in all bridge legs
Signal Sampling	≈ 0 V	Lowpass-filtering and bandpass-filtering → negligible effects
Finite Switching Frequency	≈ 0 V	No influence of ripple components on average values
Current Commutation	≈ 0 V	No influence due to additional overlap- times

Tab. 1: Comparison of the different effects causing non-ideal system behavior for a rated output power of $P_0 = 5\,\text{kW}$ at $U_{N,l-l} = 480\,\text{V}$ and $U_0 = 400\,\text{V}$. Significant parasitic effects are shown in bold face, negligible effects resulting in no influence are marked with $\approx 0\,\text{V}$.

II.H Current Commutation

For conventional three-phase (six-switch) current source inverters overlap-times have to be provided for switching the power transistors in order to ensure a continuous current flow in the DC-link inductor. These overlap-times do affect the mains phase currents and the DC-link current harmonics [13]. However, for the three-phase/three-switch buck rectifier there is no need for overlap-times, since the commutation of the DC current is always well defined by the phase-to-phase input filter capacitor voltages. If one considers, e.g., the transition from switching state $j = (110)$ in $j = (111)$ in interval (1), the current has to be commutated from bridge leg S to bridge leg T. This is simply realized by turning on the power transistor in bridge leg T, due to the voltage condition at the buck-stage input side $u_{C_F,RT} > u_{C_F,RS}$ the current is immediately commutated from bridge leg S to bridge leg T (neglecting the gate drive delay time and the power transistor turn-on delay time). Hence, no influence on the mains voltage/current or on the buck-stage output voltage/current is caused by the commutation.

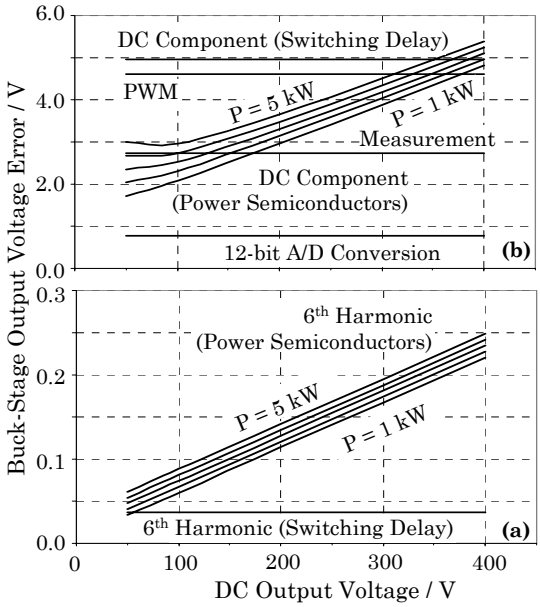

Fig. 8: Comparison of buck-stage output voltage errors for output power levels in the range of $P_0 = (5 \ldots 1)\,\text{kW}$ in steps of 1 kW and for different output voltage levels $U_0 = (50 \ldots 400)\,\text{V}$. **(a)**: Errors in the range of a few 100 mV, and **(b)** errors in the rage of a few Volts.

III Magnitudes of Output Voltage Distortions

In **Tab. 1** the parasitic effects discussed in section II are summarized and magnitudes are given for rated output voltage $P_0 = 5\,\text{kW}$, $U_{N,l-l} = 480\,\text{V}$, and $U_0 = 400\,\text{V}$ in order to provide a quantification of the different effects. Furthermore, the main effects are depicted for different output voltages and output power levels in **Fig. 8** which allows to identify which effect is dominant or negligible at different operating conditions[4].

IV Discussion

In this section, the parasitic effects considered in section II are discussed concerning the amount of influence on the rectifier output behavior based on Fig. 8, and possibilities for compensating the non-ideal behavior are given. Furthermore, the analytical results are confirmed by digital simulations.

IV.A Negligible Non-Idealities

The non-idealities of the input voltage measurement (cf. section II.C) can be neglected since the given errors are worst case values. In practice component tolerances are more evenly distributed, whereby the given errors are reduced. Furthermore, errors due to A/D-conversion (cf. section II.D) show a negligibly small magnitude and can therefore be neglected. The same is true for the harmonics caused by the difference of the turn-off and turn-on delay times (cf. section II.E).

IV.B Conduction Voltage Drops

In **Fig. 9** the simulated time behavior of the buck-stage output voltage and under consideration of semiconductor conduction losses (cf. section II.A) is depicted for an output voltage reference value $U_0^* = 50\,\text{V}$, a load resistance $R_0 = 5\,\Omega$, and a mains line-line voltage $U_{N,l-l} = 60\,\text{V}$. The major effect of the semiconductor voltage drops is a constant DC voltage error of $\approx 5\,\text{V}$, which can be easily compensated also by a low dynamics output current controller. The low-frequency component of the resulting buck-stage output voltage could be avoided by implementing a proper pre-control algorithm adjusting the buck-stage output voltage reference value in dependency on the actual position of the respective pulse period within the mains period, and on the mains voltage and load conditions. There, values for forward voltage and

[4]For low output voltage and high output power the output current would exceed the rated value, i.e. different power semiconductors would have to be employed, whereby the given dependencies would be changed.

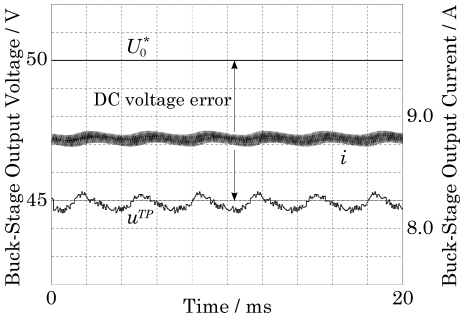

Fig. 9: Time behavior of the average value of the low-pass filtered buck-stage output voltage u^{TP} and of the DC current i for a given output voltage reference value U_0^*.

on-resistance of the power semiconductors have to be known with good accuracy and, furthermore, the dependency of the forward characteristics on the junction temperature has to be taken into account. Nevertheless, a reduction of the low-frequency harmonics in buck-stage output voltage and/or output current of about 50% could be achieved.

IV.C Time Resolution of the PWM Output Signals

The errors due to the finite time resolution of the PWM signal outputs do show significant amount, but could be considered to be evenly distributed, i.e. the actual error will be below the given values. Nevertheless, the effects cannot be neglected; the resolution could be increased by employing a quartz oscillator with two or three times the actual frequency which would decrease the maximum error by the factor of $\frac{1}{2}$ or $\frac{1}{3}$ for unchanged pulse frequency (which has to be generated by an additional frequency divider).

IV.D Switching Delays

The main part of the influence of the switching delays is a reduction of the buck-stage output voltage by a constant DC voltage, which can be controlled to zero. The harmonic components do show a negligible influence and can therefore be neglected in the case at hand (switching frequency of 24 kHz). However, if the switching frequency is set to a substantially larger value, e.g. 50 kHz, the effect of switching delays is linearly increased and cannot be neglected any more. A way of eliminating the influence of switching delays is the implementation of a cycle-by-cycle control [14], [15] or of a charge control [16] which allows to directly control the actual local average value of the DC output voltage and current.

V Conclusions

In this paper different origins for the non-ideal behavior of a three-phase/switch buck-type PWM rectifier system in open-loop operation are determined, classified and analyzed analytically. There, effects due to signal processing and a finite switching frequency, on-state and switching characteristics of power semiconductors, mains phase unbalance and measurement errors are taken into account. In order to get a clear understanding and quantification of the various effects, typical values are calculated for different operating points. As a comparative evaluation shows, the dominant parasitic influences are due to the power semiconductor voltage drops, due to the time resolution of the PWM signal outputs, and due to the turn-on and turn-off delay time of the power transistors. Partially, these effects do result in a constant reduction of the buck-stage output voltage and can therefore be eliminated by closed-loop control. However, the low-frequency components resulting from the non-ideal behavior cannot be fully eliminated by the system control due to limited control bandwidth. Hence, the effects have to be suppressed by proper pre-control methods and/or hardware adaptation, e.g. by increasing the time resolution of the PWM stage.

For verifying the parasitic effects experimentally proper measurement equipment, i.e. differential probes and an oscilloscope with sufficient high resolution is required. Furthermore, by employing an analog power amplifier for generating the three-phase input voltage effects resulting from voltage distortions of the feeding mains can be entirely excluded for the system investigation. Furthermore, the behavior of the rectifier system can then be analyzed for a defined low-frequent harmonic distortion of the input voltage. The experimental analysis will be described in a future paper.

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