A Novel Control Concept for Reliable Operation of a Three-Phase Three-Switch Buck-Type Unity Power Factor Rectifier with Integrated Boost Output Stage under Heavily Unbalanced Mains Condition

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Abstract - In this paper the reliable operation of a three-phase three-switch buck-type PWM unity power factor rectifier with integrated boost output stage under heavily unbalanced mains, i.e. mains voltage unbalance, loss of one phase, short circuit of two phases or earth fault of one phase is investigated theoretically and experimentally. The analytical calculation of the relative on-times of the active switching states and of the DC link current reference value is treated in detail for active and deactivated boost output stage. Based on the theoretical considerations a control scheme which allows to control the system for any mains condition without change-over of the control structure is described. Furthermore, digital simulations as well as experimental results are shown which confirm the proposed control concept for different mains failure conditions and for the transition from balanced mains to a failure condition and vice versa. The experimental results are derived from a 5kW prototype (input voltage range $(208\ldots480)\mathrm{V_{rms}}$ line-to-line, output voltage $400\mathrm{V}_{DC}$ of the rectifier system, where the control is realized by a 32-bit digital signal processor.

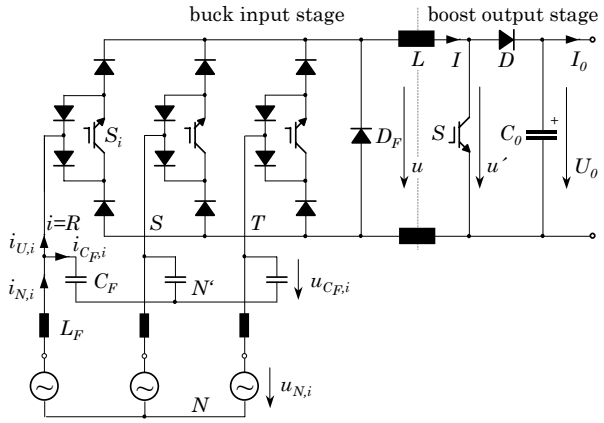

Fig. 1: Power circuit of the three-phase rectifier system with three-switch buck-type input stage and integrated DC/DC boost output stage.

1 Introduction

High power telecommunications power supply modules usually show a two-stage topology, i.e. a front-end three-phase unity power factor rectifier and a DC/DC converter output stage. In [1] a three-phase unity power factor rectifier formed by integration of a three-switch buck-type input stage and a DC/DC boost converter output stage was presented (cf. **Fig. 1**), which allows to control the output voltage to 400 V_{DC} within a wide input voltage range of (280...480) $\mathrm{V_{rms}}$ line-to-line [2]. This results in an advantageous design of the power semiconductors of the rectifier stage and allows the application of a 400 V input DC/DC converter technology being well-known from systems with single-phase AC supply.

According to the required high reliability of telecommunications power supplies the PWM rectifier system should continue in operation also in case of a mains failure, i.e. for a transition from a symmetric to a heavily unbalanced mains voltage condition. In [6] the control for a conventional PWM *boost*-type PWM rectifier was treated for unbalanced mains conditions. The operation of a three-phase/three-level PWM *boost*-type (VIENNA) Rectifier in a wide input voltage range and for the loss of a mains phase was investigated in [3]. There a detection of the phase loss is required and a change-over of the control structure has to be performed in case of a phase loss, which could cause problems for some mains failure conditions. In [4] and [5] a control concept is presented and analyzed experimentally which operates for a general unbalance of the mains phase voltage without change-over, i.e. for mains phase voltages showing different amplitudes and/or a deviation from the symmetric 120° phase displacement as well as for a loss of a mains phase, for an earth fault or for a short circuit between two mains phases.

In this paper the theoretical analysis and the practical realization of a control concept which allows to obtain sinusoidal mains phase currents which are proportional to the mains phase voltages in case of any mains voltage unbalance are described in detail for the three-phase *buck*-type PWM rectifier system with integrated boost output stage (cf. **sections 2** and **3** [7]). The theoretical analysis is verified by digital simulations in **section 4**, **section 5** shows results of an experimental analysis of the proposed control concept for a 5 kW prototype of the PWM rectifier system.

2 Theoretical Analysis

2.1 Basic Principle of Operation

In order to obtain a resistive fundamental mains behavior, mains phase currents $i_{N,i}$, $i = R, S, T$, and/or fundamentals $i_{U,(1),i}$ of the discontinuous rectifier input phase currents have to be formed, which are proportional to (lying in phase with) the corresponding mains phase voltages $u_{N,i}$. I.e. the rectifier system has to emulate a symmetric three-phase arrangement of ohmic resistors, where G is the conductivity of one phase, if

the three phase resistors are arranged in star-connection,

$$i_{N,i} = u_{N,i} \cdot G \approx i_{U,(1),i} = u_{C_F,i} \cdot G. \qquad (1)$$

(index (1) denotes the fundamental). There, the reactive input filter capacitor current $i_{C_F,i}$ is neglected, i.e. $i_{N,i} \approx i_{U,(1),i}$ is assumed, and the voltage drop across the mains filter inductors L_F is neglected, i.e. $u_{N,i} \approx u_{C_F,i}$[1] (we have $u_{C_F,i} \approx u_{C_F,(1),i}$ for low capacitor voltage ripple). For realizing (1) proper on-times of the buck input stage power transistors S_i and of the boost output stage power transistor S have to be selected, whereby the buck+boost inductor current (DC link current) is distributed sinusoidally to the mains phases. Furthermore, the reference value of the DC link current has to be set in dependency on the mains voltage condition.

Remark: In this paper, capital letters denote values which are constant over a mains period (e.g. G), *local* average value (within one pulse period) of a discontinuous value are denoted by bars (e.g. $\overline{u}$). Furthermore, ripple components with pulse frequency are neglected (e.g. $u_{C_F,i} = u_{C_F,(1),i}$), and continuous instantaneous values are denoted by lower case letters (e.g. u_N). The same is true for reference values which do always show a continuous shape (e.g. $u^* = \overline{u}^*$).

The maximum local average value of the output voltage $\overline{u}_{\max}$ of the buck-type input stage is defined by the input filter capacitor voltages $u_{C_F,i}$ and the maximum modulation index $M_{\max}$,

$$\overline{u}_{\max} = \frac{3}{2} \cdot M_{\max} \cdot \sqrt{\frac{2}{3}\left(u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2\right)}, \qquad (2)$$

where the input filter capacitor voltages $u_{C_F,i}$ are measured with reference to an artificial neutral point N'. For symmetric mains, the buck stage modulation index M is defined as follows,

$$M = \frac{\hat{I}_N}{i} = \frac{\sqrt{2}}{\sqrt{3}} \cdot \frac{\overline{u}}{U_{N,ll}}, \qquad M \in (0;1), \qquad (3)$$

where $\hat{I}_N$ is the peak value of the mains phase currents and $U_{N,ll}$ is the rms value of the mains line-to-line voltages, cf. [1].

2.2 Calculation of On-Times and DC Link Current Reference Value

In the following, the calculation of the relative on-times of the switching states of the buck-type input stage and of the DC link current reference value is given. Due to the phase symmetry of the converter structure a detailed analysis of the system behavior can be constrained e.g. to the interval of a mains period which is characterized by $u_{C_F,R} > 0 > u_{C_F,S} > u_{C_F,T}$. This interval is denoted as "interval 1" in the following[2].

Within interval 1, there are two active switching states of the buck input stage, where current is drawn from the mains and/or the DC link current i is distributed to the rectifier input phases. The active switching states $j = (101)$ and $j = (110)$[3] are showing relative on-times $\delta_{(101)}$ and $\delta_{(110)}$ related to one pulse half period. During the free-wheeling state (relative on-time $\delta_{FW} = 1 - \delta_{(101)} - \delta_{(110)}$) the DC link current free-wheels via the diode D_F. For the switching states the following rectifier input current conditions are obtained:

$$\begin{aligned} j = \mathrm{FW} \ : &\quad i_{U,R} = 0, \quad i_{U,S} = 0, \quad i_{U,T} = 0, \\ j = (101) : &\quad i_{U,R} = +i, \ i_{U,S} = 0, \quad i_{U,T} = -i, \\ j = (110) : &\quad i_{U,R} = +i, \ i_{U,S} = -i, \ i_{U,T} = 0. \end{aligned} \qquad (4)$$

Therefore, the rectifier input currents $i_{U,i}$ within one pulse half period can be given as follows,

$$\begin{aligned} \overline{i}_{U,R} &= (\delta_{(101)} + \delta_{(110)}) \cdot i, \\ \overline{i}_{U,S} &= -\delta_{(110)} \cdot i, \\ \overline{i}_{U,T} &= -\delta_{(101)} \cdot i. \end{aligned} \qquad (5)$$

The local average value of the buck stage output voltage can be calculated from the average value of the volt-seconds being switched to the buck stage output terminals,

$$\overline{u} = \delta_{(101)}\left(u_{C_F,R} - u_{C_F,T}\right) + \delta_{(110)}\left(u_{C_F,R} - u_{C_F,S}\right). \qquad (6)$$

With the balance of input and output power (i.e. losses of the buck input stage are neglected, cf. **Fig. 2**)

$$p_{in} = \sum_i i_{N,i}^2 \cdot \frac{1}{G} = \sum_i u_{C_F,i}^2 \cdot G = \overline{u} \cdot i = p_{out}, \qquad (7)$$

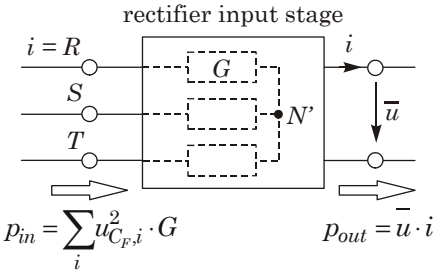

Fig. 2: Equivalent circuit of the input stage of the three-phase rectifier system showing the balance of input and output power.

one receives with (5) for the ratio of buck stage output voltage and the DC link current

$$\frac{\overline{u}}{i} = \frac{2}{G} \cdot (\delta_{(101)}^2 + \delta_{(101)}\delta_{(110)} + \delta_{(110)}^2), \qquad (8)$$

i.e., the buck stage output voltage and the DC link current do show a given proportionality. The relations (1), (5) and (8) can be combined in a system of equations,

$$\overline{u} = \frac{2}{G} \cdot (\delta_{(101)}^2 + \delta_{(101)}\delta_{(110)} + \delta_{(110)}^2) \cdot i, \qquad (9)$$

$$\overline{i}_{U,R} = u_{C_F,R} \cdot G = (\delta_{(101)} + \delta_{(110)}) \cdot i, \qquad (10)$$

$$\overline{i}_{U,T} = u_{C_F,T} \cdot G = -\delta_{(101)} \cdot i, \qquad (11)$$

where the input filter capacitor voltages $u_{C_F,i}$ are measured with reference to the artificial neutral point N', the buck stage output voltage is set by the DC link current controller and the input conductivity is set by the output voltage controller (cf. section 3), while $\delta_{(101)}$, $\delta_{(110)}$ and i are unknown parameters.

[1] This is valid only if the mains phase voltages do not contain a zero-sequence system.

[2] If symmetric mains voltages are considered, this interval equals a $\pi/6$-wide interval of the mains period.

[3] $j = (s_R s_S s_T)$, where s_i, $i = R, S, T$, are the switching functions of the power transistors. $s_i = 0$ denotes the off-state and $s_i = 1$ denotes the on-state of power transistor S_i.

2.3 Control Reference Values

Based on the system of equations (9)–(11), the calculation of the reference values which are needed for the control algorithm can be carried out. The relative on-times δ_j of the active switching states of the buck input stage as well as the DC link current i which is used as reference value i^* are calculated analytically. By solving the system of equations one receives for the relative on-times of the active switching states of the buck input stage and for the DC link current reference value within interval 1

$$\delta_{(101)} = -\frac{u^*}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,T}, \quad (12)$$

$$\delta_{(110)} = -\frac{u^*}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,S}, \quad (13)$$

$$i^* = \frac{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}{u_0} \cdot G^*. \quad (14)$$

There, the DC link current reference value is calculated employing the output voltage u_0. For the calculation of the relative on-times of the active switching states the buck stage output voltage reference value u^* is used, which is due to the proposed control structure (cf. section 3). The reference value of the input conductivity G^* is calculated based on (7),

$$G^* = \frac{P_{lim}^*}{\sum_i \hat{U}_{C_F,i}^2}, \quad (15)$$

with the limited reference value P_{lim}^* of the output power and with the sum of the squares of the input filter capacitor voltage amplitudes,

$$\sum_i \hat{U}_{C_F,i}^2 = \frac{1}{2}\left(\hat{U}_{C_F,R}^2 + \hat{U}_{C_F,S}^2 + \hat{U}_{C_F,T}^2\right). \quad (16)$$

One has to note that the conductivity reference value G^* is essentially constant over one mains period, however, the DC link current reference value i^* shows a time-dependent behavior within one mains period for unbalanced mains conditions.

One has to differ between two cases, which are treated in the following subsections:

- The buck input stage is below its modulation limit, i.e. the voltage reference value u^* can be set by the buck stage ($u^* \leq \overline{u}_{\max}$ and/or $M \leq M_{\max}$). In this case, the boost output stage is not active, i.e. $\delta = 0$;
- The buck input stage is operating at its modulation limit ($M = M_{\max}$), i.e. the buck stage output voltage is limited to $\overline{u}_{\max}$. Therefore, for the calculation of the relative on-times and of the DC link current reference value u^* has to be limited to $\overline{u}_{\max}$. Accordingly, for achieving an output voltage reference value $U_0^* > \overline{u}_{\max}$ the boost output stage has to be activated, i.e. $\delta > 0$.

2.3.1 Deactivated Boost Converter

Since the buck input stage is below its modulation limit ($M \leq M_{\max}$ and/or $u^* \leq \overline{u}_{\max}$), (12), (13) and (14) are incorporated into the calculation of the relative on-times of the active switching states and of the DC link current reference value.

2.3.2 Active Boost Converter

If the buck input stage is operating at its modulation limit ($u^* > u_{max}$), we have two possibilities for controlling the buck stage:

1. The modulation index is limited to a *constant* value, e.g. $M = 1$, within the mains period. For symmetric mains, this results in a constant buck stage output voltage and a constant DC link current.
2. The modulation index is kept on its *maximum* possible value, i.e. it varies in between $M = 1$ and $M = 2/\sqrt{3}$ over a mains period, which results in a time-varying local average value of the buck stage output voltage and of the DC link current also for symmetric mains.

In the following, the relative on-times of the switching states of the buck input stage and of the DC link current reference value are calculated for both cases.

1. Constant Modulation Index Limit

The calculation of the relative on-times $\delta_{(101)}$ and $\delta_{(110)}$ and of the DC link current reference value i^* is equal to the calculation for deactivated boost converter, cf. (12)–(14), where the buck stage output voltage reference value u^* is limited to $\overline{u}_{\max}$, cf. (2),

$$\delta_{(101)} = -\frac{\overline{u}_{\max}}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,T}, \quad (17)$$

$$\delta_{(110)} = -\frac{\overline{u}_{\max}}{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2} \cdot u_{C_F,S}, \quad (18)$$

$$i^* = \frac{u_{C_F,R}^2 + u_{C_F,S}^2 + u_{C_F,T}^2}{\overline{u}_{\max}} \cdot G^*. \quad (19)$$

The modulation index limit can be set to e.g. $M_{\max} = 1$, however, in case active damping of the input filter is provided [8], the modulation index limit has to be decreased to e.g. $M_{\max} = 0.9$ in order to have a margin for control.

2. Maximum Modulation Index Limit

In this case the relative on-time of the free-wheeling state is set to zero, i.e. $\delta_{(101)} + \delta_{(110)} = 1$. There, one receives for the relative on-times of the buck input stage and for the DC link current reference value within interval 1,

$$\delta_{(101)} = -\frac{u_{C_F,T}}{u_{C_F,R}}, \quad (20)$$

$$\delta_{(110)} = -\frac{u_{C_F,S}}{u_{C_F,R}}, \quad (21)$$

$$i^* = \max\{|u_{C_F,i}|\} \cdot G^*. \quad (22)$$

Remark: Due to the fact, that the current reference value i^* shows a constant value for symmetric mains conditions, the control method employing a constant modulation index limit is further investigated in this paper. However, employing the maximum modulation index limit shows advantages concerning switching losses due to the fact that the free-wheeling state is kept to zero. A detailed comparison of both modulation strategies will be the topic of a future paper.

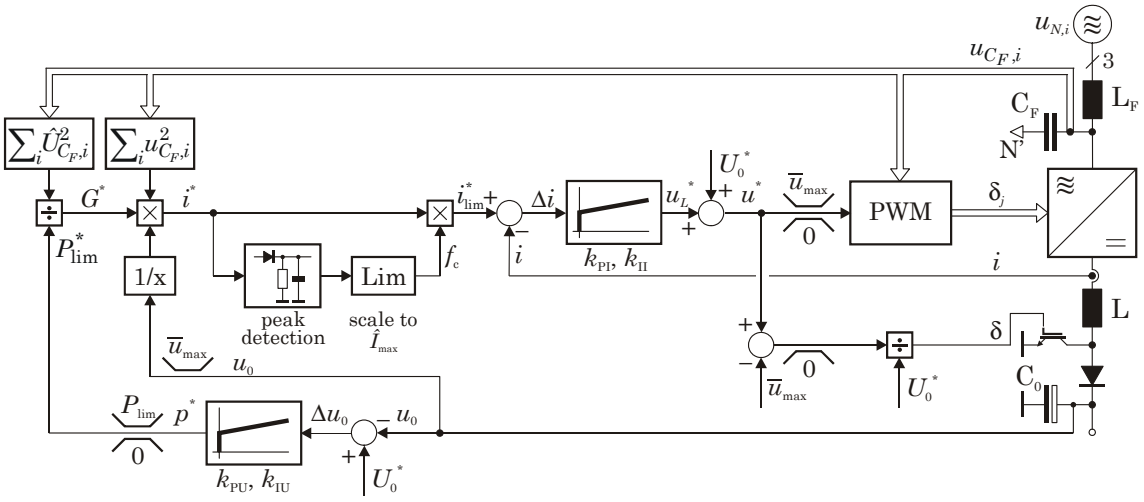

Fig. 3: Control structure guaranteeing unity power factor operation under heavily unbalanced mains.

3 Control Structure

In **Fig. 3** the proposed control structure which allows a reliable operation with sinusoidal mains phase currents and unity power factor under any mains unbalance condition is given. The control circuit consists of an outer output voltage control loop and an inner DC link current control loop. The relative on-times δ_j and δ of the active switching states of the buck input stage and the boost output stage are derived as given in the following:

- The input filter capacitor voltages are measured against an artificial neutral point N' whereby a zero-sequence system which could occur in case of a mains failure is eliminated.
- The output voltage controller output is interpreted as output power demand p^* according to (7). In order to suppress low-frequency harmonics as occurring in case of a mains failure the controller design is for low unity gain open loop bandwidth (typ. 5 Hz), the output power reference value is limited to the rated power P_{lim} of the rectifier system.
- The input conductivity reference value G^* is calculated according to (15).
- The DC link current reference value i^* is calculated employing

$$i^* = \begin{cases} \frac{u^2_{C_F,R}+u^2_{C_F,S}+u^2_{C_F,T}}{u_0} \cdot G^* & \text{for } u_0 \le \overline{u}_{\max} \\ \frac{u^2_{C_F,R}+u^2_{C_F,S}+u^2_{C_F,T}}{\overline{u}_{\max}} \cdot G^* & \text{for } u_0 > \overline{u}_{\max} \end{cases} . \quad (23)$$

- In order to ensure that the current stresses on the power diodes and transistors do not exceed a maximum admissible level and in order to avoid saturation or overheating of the DC link inductor, the peak value of the DC link current reference value $\hat{i}^*$ is limited to a maximum value $\hat{I}_{\max}$, which is defined by the dimensioning of the rectifier system (25 A in this case). In case $\hat{i}^*$ exceeds the limit, the reference value i^* is downscaled by a correcting factor f_c,

$$f_c = \begin{cases} 1 & \text{for } \hat{i}^* \le \hat{I}_{\max} \\ \hat{I}_{\max}/\hat{i}^* & \text{for } \hat{i}^* > \hat{I}_{\max} \end{cases} . \quad (24)$$

- The output of the DC link current controller sets the reference value of the voltage across the DC link inductor u_L^* which is pre-controlled with the output voltage reference value U_0^* resulting in the buck stage output voltage reference value u^*.
- The relative on-times of the switching states of the buck input stage are then calculated employing (12) and (13) for deactivated boost stage as well as for active boost stage (and a constant modulation index limit), where the buck stage output voltage reference value u^* is limited to $\overline{u}_{\max}$.
- Beyond the modulation limit of the buck input stage, i.e. for $u^* > \overline{u}_{\max}$, the reference value of the voltage across the DC link inductor can not be generated by the buck stage any longer. Therefore, the boost stage power transistor has to be activated in order to decrease the right hand side potential of the DC link inductor, i.e. for achieving $\overline{u}' < u_0$, where $\overline{u}'$ is the local average value of the voltage across the boost power transistor. For the boost output stage

$$\overline{u}' = (1-\delta)\, u_0 \quad (25)$$

is valid for continuous conduction mode. For the voltage across the inductor we have in general

$$u_L^* = \overline{u}_{\max} - \overline{u}'. \quad (26)$$

With this one receives for the relative on-time of the boost power transistor,

$$\delta = 1 - \frac{\overline{u}_{\max} - u_L^*}{U_0^*}. \quad (27)$$

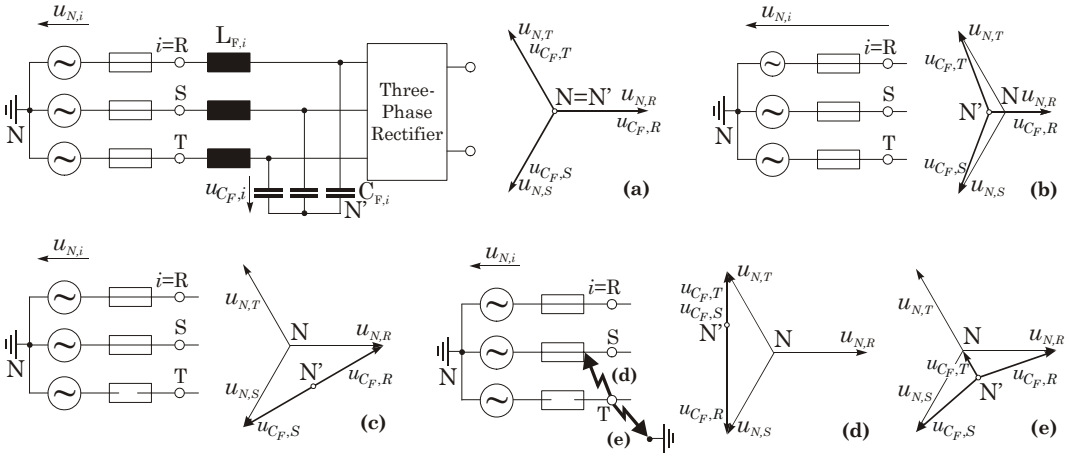

Fig. 4: Mains phase conditions and corresponding phasor diagrams of mains phase voltages $u_{N,i}$ and input filter capacitor voltages $u_{C_F,i}$. **(a)**: symmetric mains condition, **(b)**: mains phase voltage unbalance: $u_{N,R}$ is 50% smaller than for symmetric conditions. **(c)**-**(e)**: Two phase operation, **(c)**: loss of phase T, **(d)**: short circuit between phases S and T, and **(e)**: earth fault in phase T.

For the calculation of δ $u_0 = U_0^*$ is assumed due to the provided output voltage control. The calculation is realized in the control structure (cf. Fig. 3) by

$$\delta = \frac{u^* - \overline{u}_{\max}}{U_0^*}, \tag{28}$$

where $u^* = u_L^* + U_0^*$. By a limitation of the numerator to a lower value of zero, $\delta = 0$ is realized if the operation of the boost stage is not necessary (deactivated boost stage).

Remark: All equations given are valid within the whole mains period, except the equations for calculating the relative on-times, which are only valid for an input filter capacitor voltage condition $u_{C_F,R} > 0 > u_{C_F,S} > u_{C_F,T}$. Equations for other relations of the mains phase voltage instantaneous values could be derived based on [1].

4 Simulation Results

In this section results of digital simulation [9] are given which verify the operation behavior of the proposed control structure for different mains conditions (symmetric mains, unbalanced mains, phase loss, short circuit of two phases and earth fault), cf. **Fig. 4**. There, the rectifier system and the corresponding phasor diagrams of the mains phase voltages $u_{N,i}$ and of the input filter capacitor voltages $u_{C_F,i}$ are shown. The simulations are carried out for a constant modulation index limit $M_{\max} = 1$ for the following system parameters:

$U_{N,ll} = 480\,\mathrm{V}$	$U_0^* = 400\,\mathrm{V}$	$R_0 = 55\,\Omega$
$f_N = 50\,\mathrm{Hz}$	$L_F = 200\,\mu\mathrm{H}$	$L = 2 \times 1\,\mathrm{mH}$
$f_P = 20\,\mathrm{kHz}$	$C_F = 4\,\mu\mathrm{F}$	$C_0 = 750\,\mu\mathrm{F}$,

(f_N denotes the line frequency, f_P the pulse frequency).

4.1 Symmetric Mains

For balanced mains (cf. Fig. 4(a)) we have equal amplitudes of the phase voltages (referred to the neutral point N) and of the input filter capacitor voltages (referred to the artificial neutral point N') and a phase displacement of the phase quantities of 120° el, cf. **Fig. 5(a)**. The mains phase currents $i_{N,i}$ are sinusoidal and in phase with the mains phase voltages, the average value of the DC link current shows a constant value. The boost stage is not active, and the relative on-times of active and free-wheeling states show a similar time-behavior in each interval of the mains period.

4.2 Unbalanced Mains

The behavior of the rectifier system in case one phase voltage shows a lower amplitude is depicted in Fig. 5(b). There, the amplitude of voltage $u_{N,R}$ is assumed to be 50% lower than for symmetric conditions. The resulting input filter capacitor voltages are given, the corresponding mains phase currents are sinusoidal and proportional to the input filter capacitor voltages, i.e. the rectifier system shows a purely ohmic behavior. The DC link current is proportional to the sum of the squares of the input filter capacitor voltages, cf. (23). Due to the time-varying DC link current and the relatively low capacitance of the output capacitor, the system output voltage is not constant but varies by ±1.8% of its global average value. Furthermore, the different operating intervals are shown where the boost transistor is active ($\delta > 0$), and where the boost stage is deactivated ($\delta = 0$). According to the constant modulation index limit ($M_{\max} = 1$) there is a free-wheeling state ($\delta_{FW} \geq 0$) in both operating intervals.

4.3 Loss of One Phase

If one mains phase is missing, e.g. after tripping of a fuse in phase T, cf. Fig. 4(c), the remaining mains phase currents $i_{N,R}$ and $i_{N,S}$ are proportional to the input filter capacitor voltages $u_{C_F,R}$ and $u_{C_F,S}$. Due to the fact that the DC link current becomes zero each half mains period, the output voltage does show a higher ripple (±4.1%) as compared to section 4.2 (cf. Fig. 5(c)). During the time interval where the boost stage is active, the relative on-times of the buck stage switching states are constant, the current is modulated by the boost output stage.

4.4 Short Circuit Between Two Phases

If one phase (phase T, cf. Fig. 4(d)) is connected to another phase (phase S) as caused by an input voltage short circuit

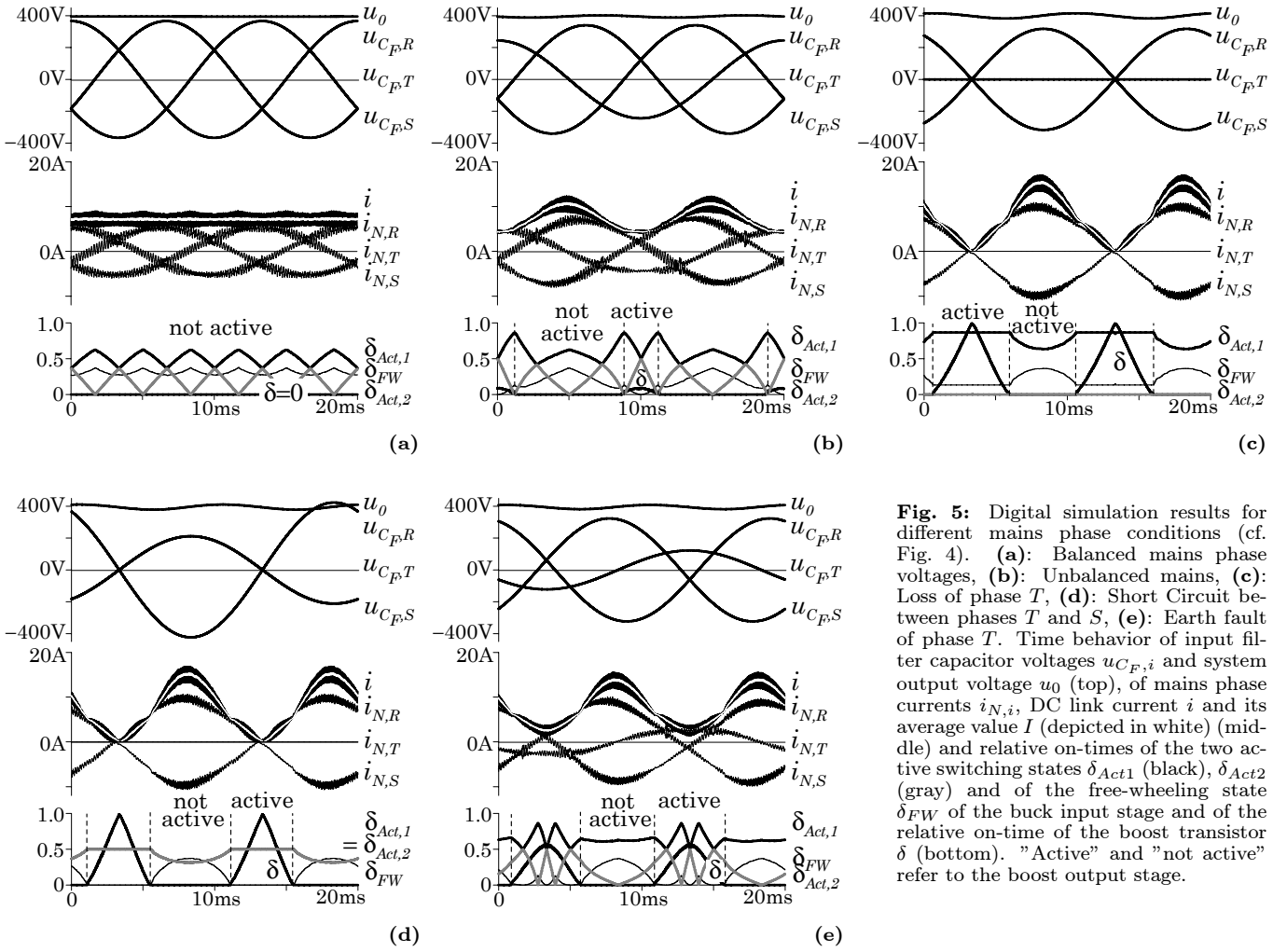

Fig. 5: Digital simulation results for different mains phase conditions (cf. Fig. 4). **(a)**: Balanced mains phase voltages, **(b)**: Unbalanced mains, **(c)**: Loss of phase T, **(d)**: Short Circuit between phases T and S, **(e)**: Earth fault of phase T. Time behavior of input filter capacitor voltages $u_{C_F,i}$ and system output voltage u_0 (top), of mains phase currents $i_{N,i}$, DC link current i and its average value I (depicted in white) (middle) and relative on-times of the two active switching states δ_{Act1} (black), δ_{Act2} (gray) and of the free-wheeling state δ_{FW} of the buck input stage and of the relative on-time of the boost transistor δ (bottom). "Active" and "not active" refer to the boost output stage.

(after tripping of a fuse in phase T) only one line-to-line voltage is available for delivering the output power: In this case the rectifier input phases S and T are operating in parallel and/or have inverse input voltages. Therefore, the relative on-times of the active switching states δ_{Act1} and δ_{Act2} are equal. The mains phase currents are proportional to the corresponding mains phase voltages, the output voltage ripple is the same as for the loss of one phase (±4.1%), cf. Fig. 5(d).

4.5 Earth Fault

If one phase, e.g. phase T (cf. Fig. 4(e)), is connected to the neutral as could be caused by an earth fault (after tripping the fuse in phase T) there is also only one line-to-line voltage available for delivering the output power. Under this mains phase condition, the mains phase currents are again proportional to the corresponding input voltages $u_{C_F,i}$ (cf. Fig. 5(e)). The deviation of the output voltage to its average value within one mains period is approximately ±1.7%, however, this value is depending on the amount of unbalance.

5 Experimental Results

The experimental results are carried out on a prototype of the three-phase rectifier system which has been designed for the following specifications:

$U_{N,ll} = (208..480)\,\mathrm{V}$	$U_0^* = 400\,\mathrm{V}$	$P_0 = 5\,\mathrm{kW}$
$f_N = 50\,\mathrm{Hz}$	$L_F = 130\,\mu\mathrm{H}$	$L = 2 \times 0.9\,\mathrm{mH}$
$f_P = 23.4\,\mathrm{kHz}$	$C_F = 4\,\mu\mathrm{F}$	$C_0 = 750\,\mu\mathrm{F}$;

the inductance values L_F and L (iron powder cores) are both given for $i_N = 15\,\mathrm{A_{rms}}$ and/or $i = 15\,\mathrm{A_{rms}}$, while $L_F = 270\,\mu\mathrm{H}$ and $L = 3\,\mathrm{mH}$ is valid for $i_N = 0\,\mathrm{A_{rms}}$ and/or $i = 0\,\mathrm{A_{rms}}$. The dimensions of the rectifier system are $(16 \times 34 \times 11)$ cm^3 $((6.3 \times 13.4 \times 4.3)$ in$^3)$, the complete control is implemented in a 32-bit floating point digital signal processor ADSP-21061 SHARC (Analog Devices).

In **Fig. 6** experimental results which confirm the proposed control method are given. The operating behavior for the disconnection (cf. Fig. 6(a), (b)) and for the reconnection (cf. Fig. 6(c), (d)) of one mains phase (phase T) as well as for the transition from the loss of phase T to a short circuit of mains phases T and S (cf. Fig. 6(e), (f)) and to a short cir-

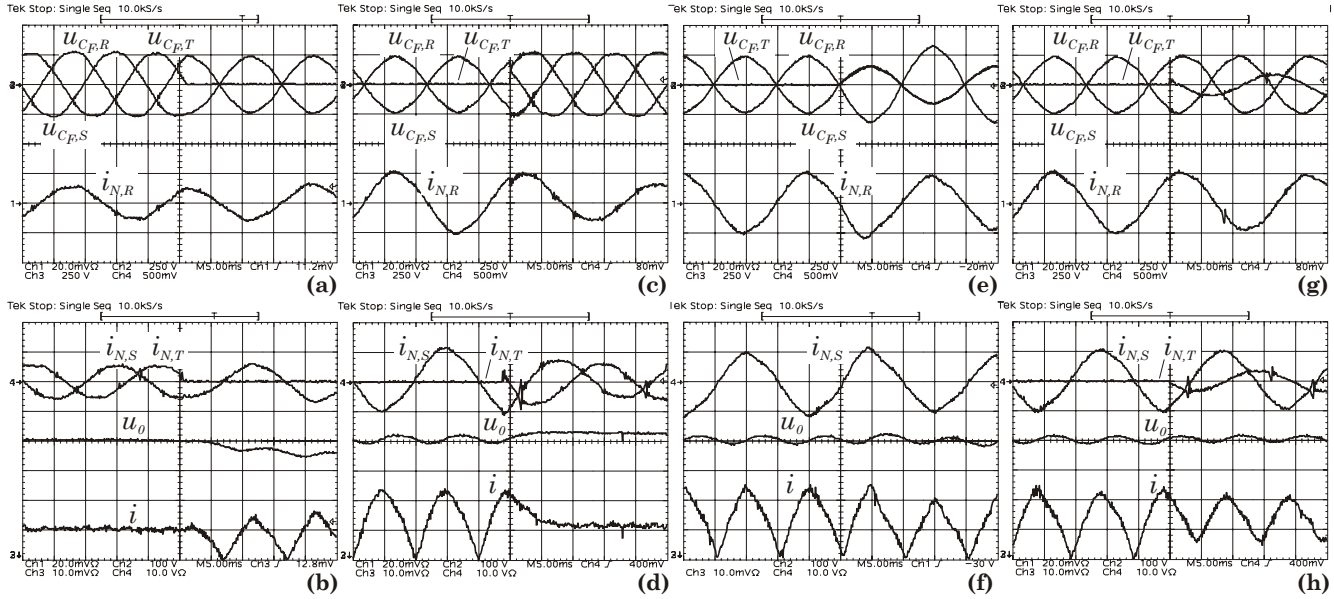

Fig. 6: Experimental results for different mains conditions: **(a), (b)**: Loss of phase T, **(c), (d)**: Reconnection of phase T (return to symmetric mains), **(e), (f)**: Short circuit between phases S and T during loss of phase T and **(g), (h)**: Short circuit to mains neutral during loss of phase T. Operating parameters: 330 V_{rms} line-line input voltage, 400 V output voltages and 2.2 kW output power. (a), (c), (e), (g): Time behavior of input filter capacitor voltages $u_{C_F,i}$, and mains phase current $i_{N,R}$, (b), (d), (f), (h): time behavior of mains phase currents $i_{N,S}$, $i_{N,T}$, output voltage u_0 and DC link current i. Voltage scales: $u_{C_F,i}$: 250 V/div, u_0: 100 V/div, current scales: $i_{N,i}$: 10 A/div, i: 5 A/div.

cuit to the mains neutral (i.e. earth fault, cf. Fig. 6(g), (h)) are given. There, the input filter capacitor voltages $u_{C_F,i}$, the mains phase currents $i_{N,i}$ as well as the output voltage u_0 and the DC link current i are given. The mains phase currents are proportional to the input filter capacitor voltages at any time, i.e. the rectifier system emulates a three-phase ohmic resistor. The deviation of the voltage from a purely sinusoidal shape is not caused by the rectifier system but is also present for no load operation. This distortion is caused by office machines and computers and/or single phase rectifiers with capacitive smoothing which are connected in high numbers to the supplying mains in the Vienna University of Technology.

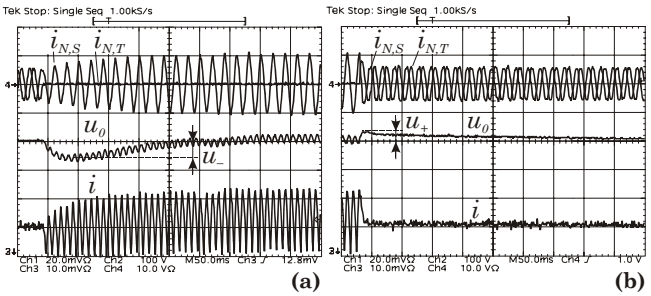

Fig. 7: Time behavior of the output voltage for the disconnection **(a)** and for the reconnection **(b)** of mains phase T. Operating parameters, voltage and current scales as in Fig. 6.

Regarding **Fig. 7** one can see that no overvoltages and/or overcurrents or oscillations do occur at the transition from one mains condition to another. There is only a voltage dip or surge in the output voltage in case of disconnection (cf. Fig. 7(a)) or reconnection (cf. Fig. 7(b)) of one mains phase. In case of a phase loss the output voltage dip u_- is approximately 60 V, for the reconnection a voltage surge u_+ of 20 V does occur for 330 V line-line voltage and 2.2 kW output power.

6 Conclusions

A new control concept for reliable operation of a three-phase/ switch PWM unity power factor rectifier with integrated boost output stage under different mains failure conditions (mains voltage unbalance, loss of one mains phase, short circuit of two mains phases and earth fault) has been presented. The control consists of an outer output voltages control loop which sets the DC link current reference value, and an inner DC link current control loop which provides the control signals for both the buck input stage and the boost output stage. In order to keep all quantities within allowable values, the DC link current reference value is limited and scaled to a maximum admissible value. All calculations which are necessary for control (i.e. relative on-times of the switching states of the power stage and DC link current reference value) are treated in detail in analytically closed form. As shown by simulations and experimental results, the rectifier system behaves like a symmetric ohmic load for balanced and unbalanced mains conditions. The input currents show a sinusoidal shape independent on the mains condition, and at the transition from symmetric mains to a mains failure and vice versa no overvoltages, overcurrents or oscillations do occur.

The considerations given in this paper are valid only for continuous conduction mode (CCM). However, at low output power discontinuous conduction mode (DCM) does occur. In

order to avoid DCM, the DC link inductor current reference value could be increased by adding an offset. However, this also would result in an increased system output power. Therefore, in order to keep the desired output power value, the duty cycle δ of the boost stage has to be increased and/or the boost stage has to be activated. In connection with lowering the buck-stage modulation index this does result in a component of the DC link current circulating via the buck stage and the boost switch, whereby the effect of the high DC link current could be compensated.

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