Design of a 5kW, 1U, 10kW/ltr. Resonant DC-DC Converter for Telecom Applications

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***Abstract* - The demand for decreasing cost and volume and also for increasing efficiency leads to a constantly increasing power density of converter systems. For maximising the power density of a 5kW telecom supply an optimisation procedure that automatically balances the switching frequency, semiconductor and passive losses, and thermal performance has been developed. This procedure and the belonging analytical converter and transformer models are presented in this paper.**

Moreover, the resulting optimised design, which has a power density of 10kW/ltr. and an efficiency of 96% at a height of 1U, is presented.

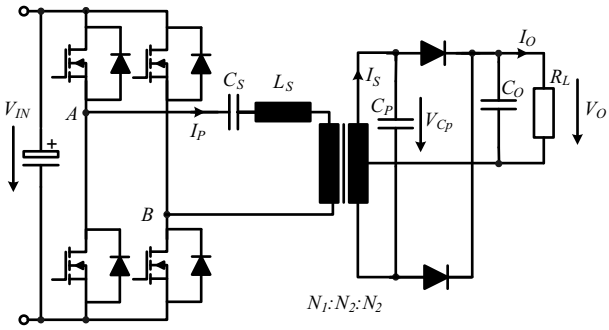
I. Introduction

In the area of power electronic converter systems there is a general trend to higher power densities which is driven by cost reduction, an increased functionality and in some applications by the limited weight/space (e.g. automotive, aircraft). In order to reduce the volume of a system, first the most appropriate topology for the intended application must be chosen.

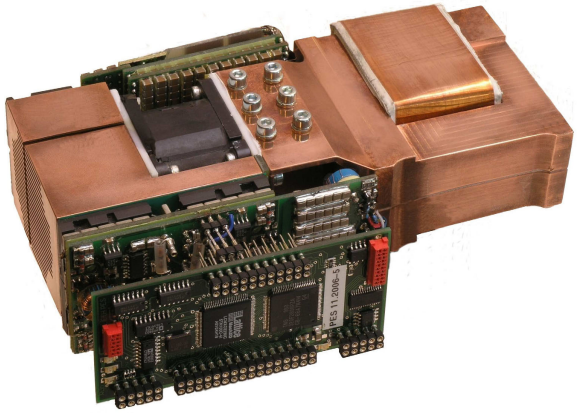
Applying resonant DC-DC converters can help to reduce the switching losses and / or to raise the switching frequency of the power switches. On this account the overall system size in many industrial applications, e.g., telecom power supplies [1], high voltage generators [2] or inductive heating [3] could be reduced and the power density could be increased. Especially, the series-parallel resonant converter, figure 1a), is a promising converter structure since it combines the advantages of the series resonant converter and the parallel resonant converter. On the one hand the resonant current decreases with the decrease of the load and the converter can be regulated at no load and on the other hand good part-load efficiency can be achieved [4], [5]. Furthermore, the converter is naturally short circuit proof.

During the design of a resonant converter one has to determine for example the values of the resonant circuit elements (C_S, L_S and C_P), the turns ratio and the number of primary turns so that the design constraints (temperature rise, operating frequency...) are met for the given specifications (input voltage, output power, load...). In order to find the values for the components which lead to an optimal design (optimal with respect to the given design aim - e.g. minimal converter volume, maximal efficiency, minimal costs...) one needs an automatic optimisation procedure. A possible flowchart for such an optimisation procedure is shown in figure 4.

First, the specifications of the application and the initial values of the resonant circuit elements are fed into the analytic model of the resonant converter. Within the model the operating frequency,



(a) *Schematic of the telecom supply*



(b) *Picture of the converter system*

Fig. 1: Schematic (a) and picture (b) of the telecom power supply.

all voltages and currents of the converter inclusive phase shift and also the flux values in the transformer are computed. With this information the design of the transformer is optimised in an inner optimisation loop (cf. fig. 4) so that the resulting transformer volume is minimal. In parallel the volume of the heat sink for

TABLE I: Specification of the telecom power supply in figure 1.

Input voltage	400V
Input current	13.0A
Output voltage	48-56V
V_{Ripple} at Output	300mV_{pp}
Output current	104A@48V, 90A@56V
Output power	5kW
Maximum ambient temp.	45°C

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the power semiconductors is calculated using the semiconductor losses and an analytic thermal heat sink model. The resulting volumes are fed into the global optimisation algorithm which varies the resonant circuit elements, the cooling conditions and the parameters of the semiconductors until a minimal overall converter volume is obtained.

Before the optimisation procedure is compiled the type of output filter must be chosen. Therefore, the standard LC-filter is compared to a capacitive output filter in section II.

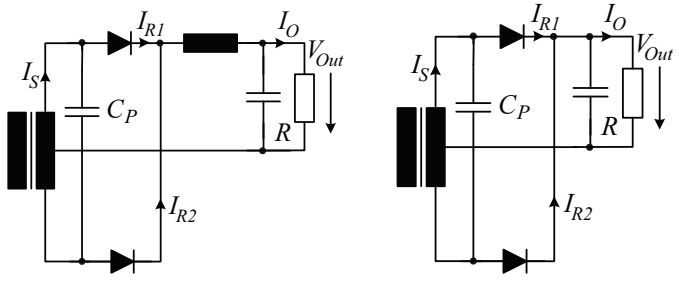
In the following section III the optimisation procedure is described in detailed. For this routine an accurate model for the resonant converter is needed, which must not be too extensive in order to limit the computation time. The used model is based on the extended fundamental frequency analysis and discussed in section IV. There, also the equations for calculating the semiconductor losses, the model for calculating the capacitor volumes and the model for optimising the transformer in the inner optimisation loop are presented.

The resulting design of the optimisation, with a target volume of 10kW/ltr., for the data given in table I is presented in section V. There, also the influence of different parameters on the optimal operating point and measurement results are discussed. Finally, a conclusion is drawn in section VI.

II. LC- vs. Capacitive Output Filter

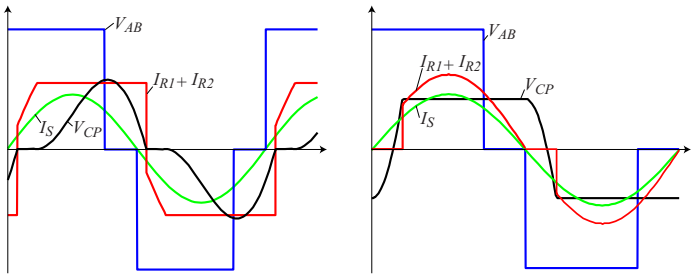
With the chosen series-parallel resonant topology there are basically two different output filter configurations possible: one with a LC low pass filter as shown in figure 2a) and one with a pure capacitive filter as shown in figure 2b). There, the output filter topology influences the behaviour of the DC-DC converter significantly, since the LC-filter acts more like a current source at the output and the capacitive filter as voltage source.

Typical waveforms for the two filter structures are given in figure 3. In case of the LC output filter the continuous (CCV) and the discontinuous (DCV) capacitor voltage mode must be distinguished [6]. Since the DCV-mode usually occurs at heavy load conditions in figure 3a) the waveforms for this mode are shown. There, the voltage waveform of the parallel capacitor V_{Cp} is clamped by the output current to zero for a certain period of time, which leads to a discontinuous and very distorted parallel capacitor voltage V_{Cp}. At the time when V_{CP} falls to zero the resonant current I_S at is smaller than I_O. As long as the resonant current I_S is smaller the capacitor voltage V_{CP} is clamped to zero by the negative difference between I_S and I_O [-(I_S - I_O)] which



(a) *LC-Output Filter* (b) *Capacitive Filter*

Fig. 2: Schematic of the LC- and the capacitive output filter for the telecom supply shown in figure 1.



(a) *LC-Output Filter* (b) *Capacitive Filter*

Fig. 3: Typical waveforms for a series-parallel resonant converter with LC- and capacitive output filter.

TABLE II: Component values of the LC- and the capacitive output filter shown in figure 2 for an output voltage ripple of 300m$V_p p$.

LC-Filter		Capacitive Filter	
C	30μF	C	470μF
-		R_{ESR}	50$\mu\Omega$
L	5μH	-	
$I_{C,Ripple,RMS}$	4.6A	$I_{C,Ripple,RMS}$	52A

flows through the rectifier diodes. From the angle on when I_S is larger than I_O the positive difference between the currents (I_S - I_O) charges the capacitor C_P.

Due to the sinusoidal resonant current and the output inductor the current in the rectifier diodes starts more smoothly resulting in a lower diode turn on stress. In the secondary winding, however, flows a constant DC current plus AC component causing higher transformer losses.

With the capacitive output filter the current in the rectifier jumps from zero to the value of the output current. This could result in higher diode switching losses depending on the diode semiconductor technology and in an increased EMI noise level. The transformer secondary current, however, is lower what results in a compacter transformer design.

Based on the required output voltage ripple of maximum 300mV_{pp} and a maximum inductor ripple current of $\pm$7.5% for the LC-filter, the component values for the two topologies can be determined (cf. table II). The ripple current in the filter capacitor in the topology with capacitive filter is much higher than the one for the LC-filter. Applying electrolytic capacitors this high ripple current results in a large filter volume due to the relatively high ESR/low current carrying capability of electrolytic capacitors. This is shown in the second line of row "LC-Filter Size" in table III. The first line represents the volume of the capacitor if just the capacitance value is considered and the ripple current is neglected. With the ripple current the capacitor volume increases more than by a factor of ten. Both values are based on the cuboid volume of cylindrical electrolytic capacitors.

If the capacitance is realised by ceramic capacitors the volume decreases down to 0.32cm^3 including ripple current considerations. In both cases the volume of the inductor (40.9cm^3) is based on very compact commercially available inductors e.g. [8], [9]. Due to the large inductor volume the size of the LC filter is relatively large and would consume approximately 10% (including interconnection) of the target volume of 0.5dm^3 for the overall system. For achieving a power density above 10kW/ltr.

TABLE III: Comparison of LC- and capacitive output filter with electrolytic or ceramic capacitors. For electrolytic capacitors two volumes are given: The first one gives the volume if just the capacitance value is realised - neglecting the ripple current I_{AC} and the current carrying capability of the capacitors. With the second value also the ripple current is accounted for. The inductor of the LC-filter has a volume of 40.9cm^3.

	Electrolytic		Ceramic	
	Cylindrical	Cuboid	SMD-Device	Mounted
μF/cm^3	170	134	111	90
I_{AC}/cm^3	0.25 A	0.19 A	41.6 A	35.1 A
LC-Filter Size	μF only: **0.22 + 40.9** (L)		**0.32 + 40.9** (Inductor)	
in [cm^3]	I_{AC}: **24.2 + 40.9** (L)		(Max. I_{AC} <11.3A)	
C-Filter Size	μF only: **3.7**, $I_{AC} < 1.5A$		**5.4**	
in [cm^3]	I_{AC}: **273** $\Rightarrow$ C=36mF		(Max. $I_{AC} < 233$A)	

this filter volume is too big.

With a capacitive filter and ceramic capacitors the volume of the filter elements decreases down to 5.4cm^3 including the volume of the PCB for mounting and the maximum thermally possible ripple current increases to 233A. A capacitive filter with electrolytic capacitors would result in a filter volume of 273cm^3 and a capacitance value of 36mF if the ripple current is considered. Taking just the required capacitance value into account this volume decreases to 3.7cm^3.

III. Optimisation Procedure

After the selection of the appropriate topology (cf. figure 1(a)) the components values must be chosen, so that the system volume becomes minimal and the power density maximal. Since the volume of the single components, which are mainly limited by the respective maximum operation temperature, interdepend to some extent on each other, the optimisation of the overall volume is a quite difficult task with many degrees of freedom.

Therefore, an automatic optimisation procedure is applied for determining the optimal component values of the telecom supply.

In figure 4 a possible flow chart of this procedure is given, where the specification of the design parameters like the input and output voltage, the output power, temperature limits, material characteristic, etc. is the starting point of the procedure. These parameters as well as starting values for C_S, C_P, L_S and for the number of turns of the transformer (N_1 and N_2) must be specified by the user.

Based on the values for the series inductance and the turn numbers the reluctance model of the transformer with integrated series inductance is calculated in the next step. Thereafter, the operating point of the DC-DC converter is estimated by an approximated fundamental frequency analysis [7]. With the estimated values the solution space for the analytic converter model (cf. section IV-A) is restricted and the calculation time is reduced. The converter model is based on a set of equations which are derived with the extended fundamental frequency analysis and solved numerically. The solution are the operating frequency, the voltages and currents as well as the flux distribution of the integrated transformer including phase information.

With the frequency and the voltages across the resonant tank capacitors the volumes of these components are calculated. Furthermore, the switching and conduction losses in the MOSFETs and rectifier diodes are determined. These losses, the ambient

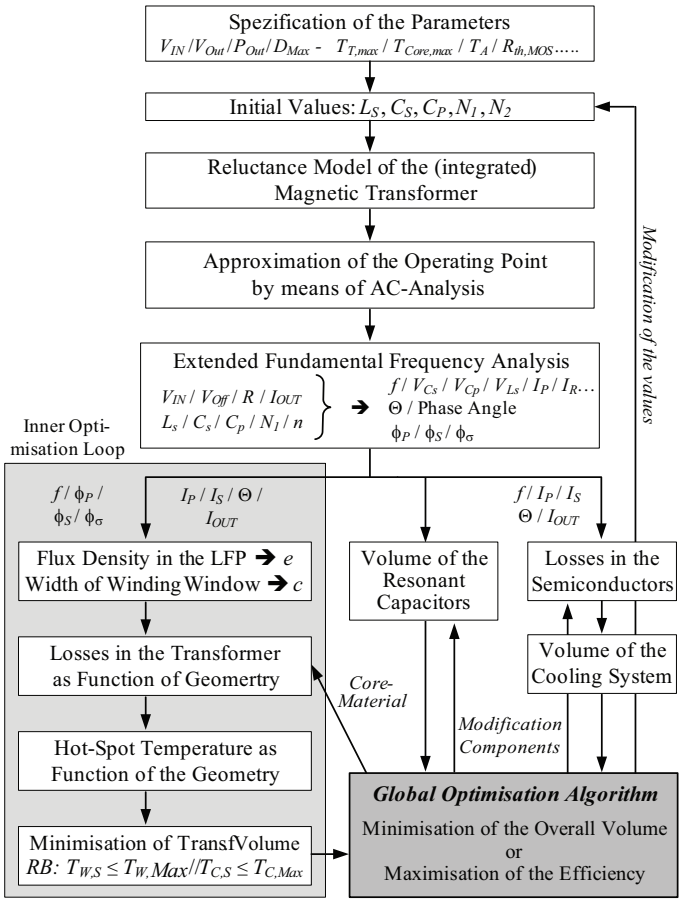


Fig. 4: Automatic procedure for optimising the volume/efficiency of a series parallel resonant converter while keeping the device temperatures below given limits.

temperature and the maximum junction temperatures of the semiconductor devices are used for calculating the volume of the semiconductor heat sink including the fan based on the $CSPI$ (Cooling System Performance Index), which is defined by

$$CSPI\left[\frac{W}{Kdm^3}\right] = \frac{1}{R_{th,S-A}\left[\frac{K}{W}\right] Vol_{HS,Magn.}\,[dm^3]} \qquad (1)$$

and has been introduced in [15].

The volume and the shape of the transformer core and the two windings is determined in a second, inner optimisation procedure. There, the volume of the transformer is minimised while keeping the temperatures below the allowed limits. For this purpose, first two geometrical degrees of freedom are eliminated by setting the flux density in the leakage path to the same value as in the middle leg conducting the main flux and by calculating the core window width using the optimal winding thickness and the turns number [7].

Thereafter, the core and winding losses are calculated as function of the three remaining geometrical variables (a, b, c cf. fig. 7). With the losses and the thermal model of the transformer the temperature distribution in the core and the winding also could be calculated as function of the variables a, b and c/d. The peak temperatures in the windings and the core are together with the maximum allowed temperatures the constraints for the following minimisation of the transformer volume. Furthermore, the variables $a - e$, defining the transformer geometry, can be

restricted in order to preserve certain limitations resulting from the manufacturing process.

In the inner optimisation loop it is also possible to maximise the efficiency of the transformer, if an upper limit for the transformer volume is given.

Together with the volumes of the capacitors/heat sink the minimised transformer volume is passed to the global optimisation algorithm. This algorithm systematically varies the values of the resonant tank elements and the number of turns until a minimal system volume or a maximal efficiency is obtained.

IV. Modelling of the Converter

In the subsequent paragraphs the different models of the optimisation procedure are explained shortly. First, the analytical converter model is derived, then the equations for the semiconductor losses and the model for the resonant tank capacitor volumes. Finally, the loss and the thermal model of the transformer are presented.

A. Analytical Converter Model

The following calculations for the series-parallel resonant converter shown in figure 1 are partly based on the extended fundamental frequency analysis proposed in [14] and [6]. Furthermore, the control method described in [6] (cf. figure 5) with ZVS condition in one leg and ZCS condition in the other leg as well as control by frequency and duty cycle is considered in the equations. This control method reduces the switching losses significantly. For details on the strategy please refer to the mentioned publication.

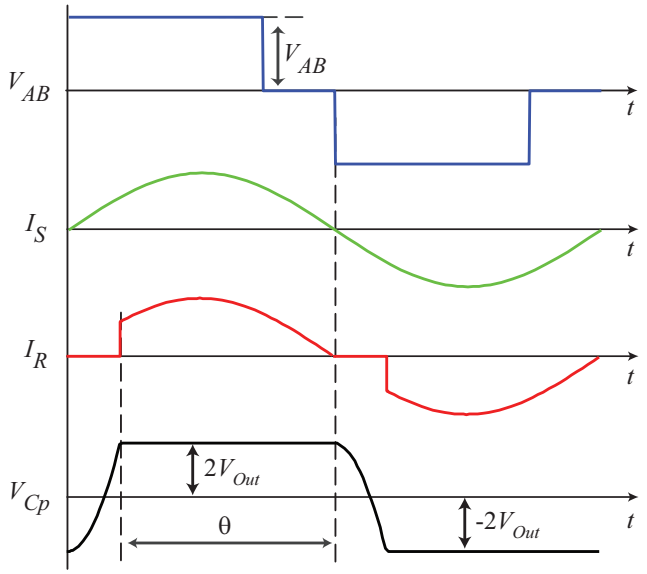


Fig. 5: Converter voltage V_{AB}, resonant current I_S, rectifier current I_R $(= I_{R1} + I_{R2})$ and parallel capacitor voltage V_{Cp}.

The presented calculations are based on the assumptions that both the primary resonant current I_P and the secondary resonant current I_S are sinusoidal with a third harmonic component, that the output voltage is constant and that the components are ideal. The major procedure of the analysis is to determine the fundamental frequency impedance Z_{CpR} of the parallel connection of C_P and the rectifier at first. With this impedance the input impedance Z of the resonant circuit, seen by the H-bridge / voltage source V_{AB} (cf. figure 6), could be calculated. In the impedance Z also the reluctance model of the transformer is included.

In the next step two equations can be set up. The first one describes the relation between the phase shift of the primary current I_P and the fundamental component of the H-bridge voltage $V_{AB(1)}$, which is determined on the one hand by the duty cycle D and on the other hand by Z. The second expression relates the input impedance of the resonant tank to the amplitude of the resonant current. These equations are derived in the following paragraph.

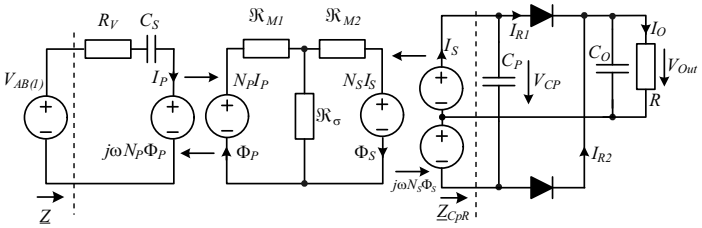


Fig. 6: Equivalent circuit of the series-parallel resonant converter with capacitive output filter.

1) Derivation of the Model: For the derivation of the system equations first the run of the parallel capacitor voltage $V_{Cp}(t)$ is expressed by the analytical function

$$V_{Cp}(t) = \begin{cases} \frac{2V_{Out}}{1+\cos\theta}\left(1-\cos\theta-2\cos\omega t\right) & \text{for} \quad 0 \le \omega t < \pi-\theta \\ 2V_{Out} & \text{for} \quad \pi-\theta \le \omega t < \pi \end{cases}$$

and the current in the resonant tank on the secondary side I_S is described by

$$I_S = I_{S,1}\sin(\omega t) + I_{S,3}\sin(3\omega t). \tag{2}$$

With the current in the resonant tank the average rectifier current is calculated, where it is important to notice that the effective transformer ratio is $N_P : N_S$ while a rectifier diode is conducting and $N_p : 2N_S$ in case no rectifier diode is conducting. Therefore, the resonant current I_S must be multiplied by 2 during the interval from $\pi - \theta$ to π (cf. (3)), since in the equations a transformer ratio of $N_P : 2N_S$ is generally assumed.

$$\begin{aligned} \frac{V_{Out}\pi}{R} &= \int_{\pi-\theta}^{\pi} 2I_{S,1}\sin(\omega t) + 2I_{S,3}\sin(3\omega t)\mathrm{d}\omega t \\ &= 2I_{S,1}\left(1-\cos\theta\right) + \frac{2}{3}I_{S,3}\left(1-\cos 3\theta\right). \end{aligned} \tag{3}$$

Since the average rectifier current must be equal to the load current the rectifier conduction angle θ could be calculated by solving

$$\frac{2I_{S,1}\left(1-\cos\theta\right) + \frac{2}{3}I_{S,3}\left(1-\cos 3\theta\right)}{\pi} = \frac{V_{Out}}{R} \tag{4}$$

for θ, what results in a relatively long expression which is not presented here for the sake of brevity.

In the next step the equivalent load impedance for each harmonic $(\nu = 1, 3)$ is calculated with the harmonics of the parallel capacitor voltage

$$V_{Cp,\nu} = \frac{2j}{\pi}\int_0^{\pi} V_{Cp}(t)e^{-j\nu\omega t}\mathrm{d}\omega t \tag{5}$$

by AC-analysis

$$Z_{CpR,\nu} = \frac{V_{CpR,\nu}}{I_{S,\nu}} \tag{6}$$

With the load impedance and the reluctance model of the transformer described in [6]

$$N_1 \underline{I}_{P,\nu} = \Re_{M1} \underline{\Phi}_{P,\nu} + \Re_\sigma \cdot (\underline{\Phi}_{P,\nu} - \underline{\Phi}_{S,\nu}) \tag{7}$$

$$N_2 \underline{I}_{S,\nu} = -\left(\Re_{M2} \underline{\Phi}_{S,\nu} + \Re_\sigma \cdot (\underline{\Phi}_{S,\nu} - \underline{\Phi}_{P,\nu})\right), \tag{8}$$

the flux in the primary winding $\Phi_{P,\nu}$ and therewith the primary voltage could be calculated. Thereafter, the mesh equation for the resonant tank on the primary side of the transformer could be set up

$$V_{AB,\nu} = \frac{I_{P,\nu}}{j\nu\omega C_S} + I_{P,\nu} R_V + j\nu\omega N_1 \Phi_{P,\nu}, \tag{9}$$

and the input impedance of the resonant tank including the load is given by

$$Z_{AB,\nu} = \frac{V_{AB,\nu}}{I_{P,\nu}}. \tag{10}$$

Based on the input impedance the system equations are given by

$$0 = \frac{\nu\pi}{2}(1-D) - \arctan\left(\frac{\Im(Z_{AB,\nu})}{\Re(Z_{AB,\nu})}\right), \tag{11}$$

for the phase shift of the input current and

$$I_{P,\nu} = \frac{4V_{IN}}{\nu\pi\,|Z_{AB,\nu}|} \cos\left(\frac{\nu\pi}{2}(1-D)\right). \tag{12}$$

for the amplitude of the primary current. By numerically solving these equations the operating frequency and the duty cycle of the converter can be calculated. With the frequency and duty cycle all voltages, currents and also the flux distribution can be determined.

B. Semiconductor Losses

For calculating the volume of the heat sink for the semiconductors with (1) the maximum operating temperature and the thermal resistance between junction and heat sink of the semiconductors are required. These values can be derived from the data sheets. Furthermore, the losses in the 4 MOSFETs including antiparallel diode and the 2 rectifier diodes must be calculated. Due to the different switching conditions in the 2 legs also the losses/current waveforms are different.

With the fundamental component $I_{P,1}$ and the third harmonic $I_{P,3}$ of the resonant current on the primary side the RMS currents in the leg with ZCS and in the leg with ZVS condition can be calculated by

$$I_{T_{ZCS}} = \frac{1}{2}\sqrt{I_{P,1}^2 + I_{P,3}^2} \tag{13}$$

$$I_{T_{ZVS}} = \sqrt{\frac{1}{T}\int_0^{\frac{DT}{2}} \left[I_{P,1}\sin(\omega t) + I_{P,3}\sin(3\omega t)\right]^2 \mathrm{dt}}. \tag{14}$$

With the RMS currents the conduction losses in the MOSFETs can be determined. For the diodes an approximately constant forward voltage drop is assumed, so that for calculating the conduction losses in the antiparallel MOSFET diodes of the ZVS leg and the rectifier diodes the average currents are required. These are given by

$$I_{D_{ZVS}} = \sqrt{\frac{1}{T}\int_{\frac{DT}{2}}^{\frac{T}{2}} I_{P,1}\sin(\omega t) + I_{P,3}\sin(3\omega t)\,\mathrm{dt}} \tag{15}$$

for the MOSFET diodes and by

$$I_{D,Rec} = \frac{3I_{P,1}(1-\cos\Theta) + I_{P,3}(1-\cos 3\Theta)}{3\pi} \tag{16}$$

for the rectifier diodes.

Due to the assumed control method where one leg switches at ZCS and one at ZVS condition the switching losses are relatively low. If the ZCS leg, which should switch at the zero crossing of the resonant current, is switched a bit before the zero crossing, the MOSFET has to turn off a small current. Because of the fast switching and the large output capacitance of the MOSFET this current does not cause relevant turn off losses. In case the turned off current is large enough, so that it charges the MOSFET capacitances during the interlocking delay [6], the opposite MOSFET is turning on at zero voltage. Consequently, the switching losses in the ZCS leg are negligible [7].

In the ZVS leg, the MOSFET has to turn off larger currents, which causes losses in case the current is large enough. In order to determine the losses measurements with APT50M75 MOSFETs from Microsemi (former Advanced Power Semiconductors) have been performed [7]. Based on these measurements the losses can be determined by

$$P_{Sw,ZVS} = 2\left(1.9^{E-7} I_{p,off}^2 - 3.8^{E-6} I_{p,off} + 1.4^{E-5}\right) f_{Sw}$$

in case the turned off MOSFET current is

$$I_{p,off} \geq 15A$$

and they are negligible if the turned off current $I_{p,off}$ is below 15A.

With the presented loss/current equations the overall losses can be calculated by

$$\begin{aligned} P_{Semi} = {} & R_{DS,on}\left(2I_{T_{ZCS}}^2 + 2I_{T_{ZVS}}^2\right) + 2V_{F,D} I_{D_{ZVS}} \\ & + 2V_{F,R} I_{D,Rec} + 2P_{Sw,ZVS}. \end{aligned} \tag{17}$$

To these the losses in the gate drive circuits, which can be calculated with the gate-charge/capacitance and which increase linearly with frequency, must be added.

With the semiconductor losses dissipated via the heat sink and the maximal heat sink temperature T_{Sink} the maximal allowed thermal resistance of the heat sink could be calculated by

$$R_{th,S-A} \leq \frac{T_{Sink} - T_{Amb.}}{P_{Semi}}. \tag{18}$$

There, the heat sink temperature is given by

$$\begin{aligned} T_{Sink} \leq min\{ & T_{J,T_{ZVS},max} - R_{th,T_{ZVS}} P_{V,T_{ZVS}}, \\ & T_{J,T_{ZCS},max} - R_{th,T_{ZCS}}(P_{V,T_{ZCS}} + P_{V,D_{ZCS}}), \\ & T_{J,D_{Rec},max} - R_{th,Rec} P_{V,Rec}\}. \end{aligned}$$

The volume of the semiconductor heat sink directly follows with (1).

C. Resonant Tank Capacitors

In the series and the parallel capacitor of the resonant tank approximately sinusoidal currents with a high amplitude and frequency are flowing. In order to limit the losses and the temperature rise dielectrics with a low loss factor $\tan\delta$ are required. There are basically two good choices: either foil capacitors with polypropylene or ceramic capacitors with COG/NPO material. Since the resulting volume with foil capacitors is significantly larger than with the ceramic ones as could be derived from data sheets, the latter are chosen for the considered telecom power supply.

For calculating the volume required for realising the series and parallel capacitor a commercial 3.9nF/800V COG ceramic capacitor in a 1210 SMD housing from Novacap [10] has been chosen as reference component, since it offers the highest capacitance per volume ratings at AC voltages with a high frequency and amplitude. Based on this capacitor the ratio: volume per capacitance

$$\frac{V_C}{C} = \frac{(3.18{+}0.75)(2.54{+}0.25)(1.65{+}0.75)}{3.9^{E-9}} \left[\tfrac{mm}{F}\right] \qquad (19)$$

has been calculated. There, it has been assumed that the capacitors are mounted on both sides of a double sided 1.5mm standard PCB with a 0.75mm gap in direction of the connections and a 0.25mm gap orthogonal to this direction. Additionally, the volume of the PCB is considered by adding half the thickness of the board to the thickness of the capacitor.

In the optimisation procedure the volume of the resonant tank capacitors is calculated by multiplying the above ratio by the respective capacitance value. Furthermore, the dielectric losses in the capacitors are calculated by

$$P_C = \omega C \tan\delta U_C^2 \qquad (20)$$

and compared with the maximal allowed ones. These can be calculated by multiplying the ratio: losses per capacitance

$$\frac{P_{C,max}}{C_{ref}} = \frac{0.35}{3.9^{E-9}} \left(1 - \frac{T_A - 40°C}{125°C - 40°C}\right), \qquad (21)$$

which is based on the loss limit of 0.35W per 1210 housing (max. operating temperature 125°C), by the capacitance value. In case the losses in the capacitors are too big no feasible design is possible for this set of parameters and the parameters are varied by the optimisation procedure so that the losses are below the limits.

D. Transformer Model

In the optimisation procedure shown in figure 4 also the shape of the transformer is optimised for minimal volume in the inner loop while the hot spot temperatures are kept below the limits. For this inner optimisation loop the volume, the losses and the temperature distribution in the transformer are needed as function of the geometry. The geometry could be described by 5 variables as shown in figure 7, where the construction of the transformer and the definition of the variables are given.

In order to maximise the power density of the transformer an advanced cooling method as described in [11] has been applied. With this method the losses in the windings and the core are transferred via a heat transfer component (HTC) to an additional heat sink for the transformer.

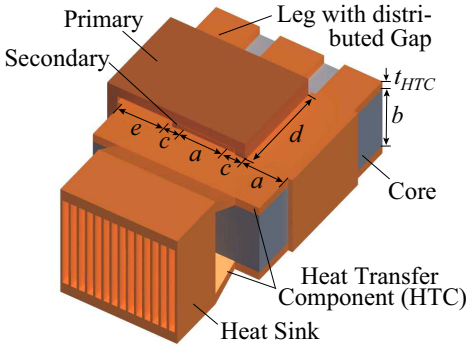


Fig. 7: Geometry of transformer with integrated series inductance and heat transfer component (HTC)/heat sink for cooling.

At the beginning of the inner optimisation procedure the degrees of freedom, i.e. the number of independent variables $a-e$ in figure 7, are reduced. First, the width of the leakage flux path (LFP) e with distributed gap (left leg in fig.7) is chosen so that the flux density in this leg is the same as in the middle leg. Second, the width of the winding window c is determined by the optimal thickness of the foils, the number of turns, the copper fill factor and a fixed mounting space. The optimal thickness of the foils depends on the frequency and the harmonics and can be derived by minimising the copper losses [12]. By eliminating e and c only three independent variables a, b and d are left, which are used for minimising the transformer volume.

In the next step, first the losses in the windings and the core and then the hot spot temperatures are calculated as function of the three remaining variables. In the optimisation algorithm, where the volume is minimised, these functions are used for calculating the hot spot temperatures and keeping them below the maximal allowed operation temperature of the transformer while varying the geometry.

The losses in the different core sections can be calculated by applying the Steinmetz law [13] parameterised (C_m, α, β) with the manufacturer data sheets.

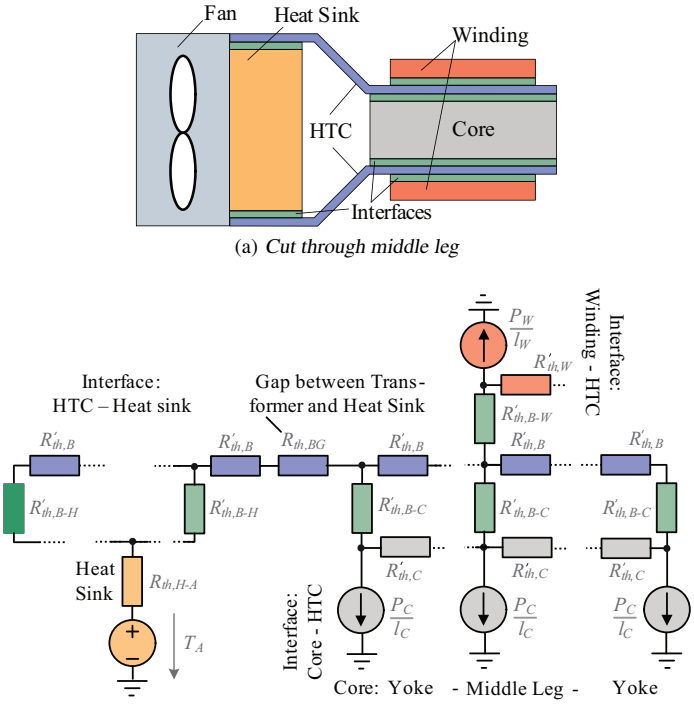
$$P_{Core} = C_m f^{\alpha} B_{\nu,AC}^{\beta} V_{Core,\nu}. \qquad (22)$$

There, $V_{Core,\nu}$ is the volume of the considered core section, which can be expressed by the variables $a-e$.

For analytically calculating the winding losses including the skin- and proximity-effect an 1D approach as for example presented in [7], [12], [16] is applied. Due to the approximately sinusoidal current in the primary winding only the first and the third harmonic of the current are considered in the loss and optimal foil thickness calculation (cf. section IV-A.1).

The current in the two sections of the secondary winding, however, significantly deviates from a sinusoidal shape in contrast to the resulting secondary resonant current I_S (the sum of the currents in the two sections of the secondary). Therefore, higher harmonics (here up to the 12th harmonic) have to be considered in the loss and optimal foil thickness calculations. There, mainly the height of the winding window d and the mean turn length describe the influence of the geometry on the winding losses.

Due to the high secondary currents the losses in the secondary winding dominate the windings losses.



(a) *Cut through middle leg*

(b) *Thermal model*

Fig. 8: (a) Cut through middle leg of transformer with cooling system/heat sink shown in figure 7. (b) Distributed thermal model of the cooling system shown above with the heat sink on the left hand side, a gap between heat sink and transformer and the transformer with winding on the right hand side.

With the losses the temperature distribution in the transformer could be calculated based on the thermal model shown in figure 8. This model describes the heat flow from the winding/core via the thermal interfaces and HTC to the heat sink/ambient by distributed thermal resistances (R_{th} per length). The calculation of the temperature profile is based on transmission line equations, what is described in detail and validated in [11].

For improving the heat flow within the winding made of foil and also from the winding to the HTC a thermally conductive insulating material is used [17]. Moreover, thermal grease between the core and the HTC and a cover pressing the winding on the HTC are used. This cover is not shown in figure 1 for showing more transformer details.

After the volume has been minimised it is passed to the global optimisation algorithm, where it is used for calculating the system volume and for varying the parameters systematically.

V. Resulting Design

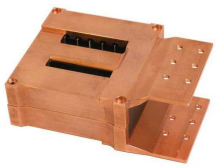
Based in the presented procedure shown in figure 4 a telecom supply with the specification given in table I has been optimised and the results are presented in the following. The data, the component values and a photo of the transformer (with HTC but without winding) of the optimised system are summarised in table IV, where it could be seen that the aimed power density of 10kW/ltr. has been reached and that the efficiency of the system is 96% at rated power. These result for the optimisation is based on the following data/limits:

- Core material: N87 from Epcos ($T_{Max} \leq 115°C$)
- Winding: Foil winding ($T_{Max} \leq 125°C$)
- Centre tapped secondary winding
- MOSFETs: APT50M75 from Microsemi (former APT)
- Rectifier diode: APT100S20 from Microsemi
- Capacitors C_S and C_P: Reference 3.9nF 800V COG series from Novacap
- Cooling system performance index: 23 (transformer and semiconductor heat sink)
- Maximal junction temperature $T_{j,max} \leq 140°C$

A further requirement is the overall height of the supply which should be below 1U (≈44mm). That significantly influences the design of the transformer as well as the cooling system.

TABLE IV: Resulting specification of the optimised 5kW telecom supply.

Volume: 0.49dm^3 Efficiency: 96.1% Power Density: 10.2kW/dm^3



Transformer

• Width	6.4cm
• Breadth	6.4cm
• Height	4.0cm
• Volume	0.21dm^3
• Flux Density	0.23mT

Operation Point

• Output Power	5kW	• Output Voltage	54V (48)
• Output Current	92.6A (104)	• Input Voltage	400V
• Nominal Freq.	92.9kHz (90.1)	• Duty Cycle	0.75

Resonant Circuit

• Series C_S	160nF	• Parallel C_P	120nF
• Series L_S	40μH	• Turns Ratio	7
• Vol. C_s+C_p	3.2cm^3	• Primary Turns	14

In order to judge the sensitivity of the converter volume on the operating frequency the "Global Optimisation Procedure" (bottom box in figure 4) has been replaced by three nested for-next loops. In these loops the component values have been varied within the following range: C_S = 50...300nF / C_P = 100...500nF / L_S = 5...70μH. The result of this is shown in figure 9 where each cross marks the system volume for one set of the three variables $<C_S, C_P, L_S>$. The turns ratio has been fixed to 14:2 since this results in the smallest overall system volume with the given constraints.

As one can see in figure 9 there is a distinct minimum of the volume close to 100kHz. Increasing the operating frequency leads to a larger system volume since the transformer needs a larger volume due to a significant increase in the required window height d (cf. fig. 7) because of the HF-losses in the windings. Also for a decreasing frequency the system volume is increasing due to increasing core sizes. There, the constraints like overall height, materials, etc. significantly influence the position of the minima.

The related data of the converter system is given in table IV. The flux density in the transformer core reaches a peak value of 0.23T at full load. This results in a relatively high power loss density in the core but due to the low core volume the overall core losses are just 27W. The losses in the winding are 5W for the primary and 14.3W for the secondary. Due to the indirect cooling via the HTC and the heat sink the peak temperature in

the core is below 115°C and in the winding below 114°C at an ambient temperature of 45°C.

The losses in the four MOSFETs are 73W and in the two rectifier diodes 84W. In the resonant capacitors only 0.5W are dissipated due to the low loss factor of the ceramic capacitors. Summing up all the losses results in approximately 202W overall losses for the resonant converter at full load.

In figure 11 the back side of the first test setup with the two rectifier diodes, the parallel and the output capacitors are shown. First measurements already have been performed. A oscillogram of the bridge voltage V_{AB}, a gate-source voltage V_{GS} and the resonant current I_P for an output power of 1.2kW and a DC link voltage of 400V is given in figure 10. In the next steps the output power will be increased up to the rated value and efficiency as well as temperature/loss measurements will be performed in order to validate the applied analytic models.

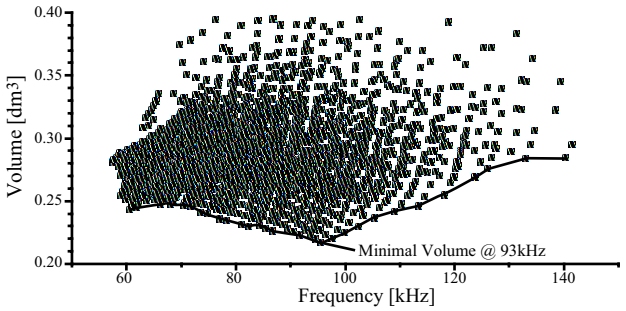


Fig. 9: Volume of the resonant circuit (C_S + C_P + L_S + transformer) for the parameter ranges: C_S = 50..300nF / C_P = 100..500nF / L_S = 5..70μH / N_1 = 14 / N_2 = 2.

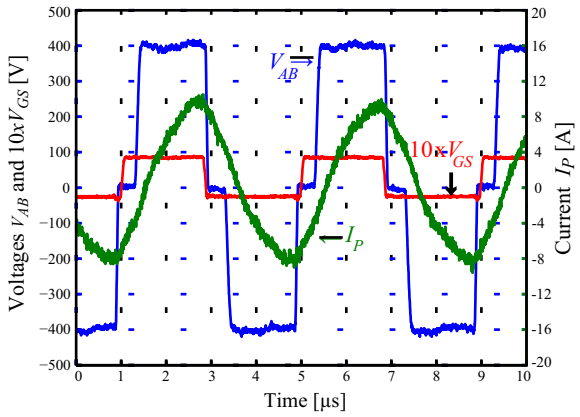


Fig. 10: Measurement results for $V_{IN} = 400V$, $I_{IN} = 3.4A$, $V_O = 44.3V$ and $I_O = 28.2A$.

VI. Conclusion

In this paper the design of a 5kW, 1U series-parallel resonant DC-DC converter for telecom applications has been presented. To meet the demands of high efficiency and low volume resulting in a high power density, an automatic optimisation procedure has been developed and is explained in detail in this paper.

In the optimisation procedure, the model of the converter, with capacitive output filter, is based on extended fundamental frequency analysis.

Furthermore, the control structure, the losses in the semiconductors as well as the thermal and magnetic behaviour of the

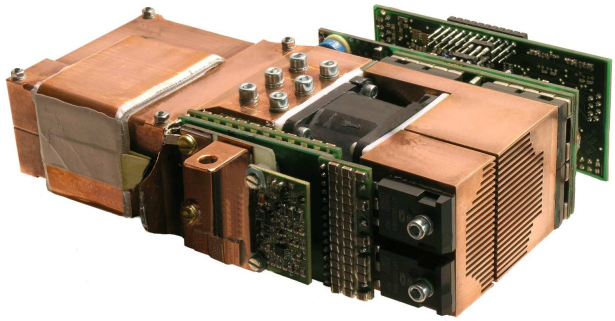


Fig. 11: Backside view of the 5kW, 10kW/dm^3 telecom power supply.

integrated transformer, whose geometry is also optimised within the procedure, are included. With the presented optimisation procedure a 5kW DC-DC converter with a power density of more than 10kW/ltr. has been developed. For validating the analytical models a prototype of the converter has been constructed and measurements are presented in this paper.

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