# Using Transformer Parasitics for Resonant Converters—A Review of the Calculation of the Stray Capacitance of Transformers

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***Abstract*—Parasitic capacitances of conventional transformers can be used as resonant elements in resonant dc–dc converters in order to reduce the overall system size. For predicting the values of the parasitic capacitors without building the transformer different approaches for calculating these capacitances are compared. A systematic summary of the known approaches is given and missing links between the different theories and missing equations are added. Furthermore, a new simple procedure for modeling parasitic capacitances that is based on the known approaches is proposed. The resulting equations are verified by measurements on four different high voltage transformers.**

***Index Terms*—High-voltage transformer, inductor model, parasitic capacitance, resonant converter, transformer model.**

## I. Nomenclature

| | |
|---|---|
| $\varepsilon_D$ | Dielectric constant of wire insulation. |
| $\varepsilon_F$ | Dielectric constant of foil between layers. |
| $\varepsilon_{r,m}$ | Effective dielectric constant. |
| $\delta$ | Thickness of wire insulation. |
| $\delta_{\text{Twist}}$ | Thickness of outer insulation of litz wire. |
| $\delta_{\text{Wire}}$ | Thickness of insulation of a single strand. |
| $b_{\text{Sec}}$ | Breadth of winding section. |
| $C_0$ | Static capacitance between two layers. |
| $C_{\text{Layer}}$ | Equivalent capacitor between two layers. |
| $C_{\text{Sec}}$ | Equivalent capacitor of one section. |
| $C_{\text{Wdg}}$ | Equivalent capacitor of the whole winding. |
| $C_{1.6}$ | Equivalent capacitor general model. |
| $d$ | Distance between successive turns. |
| $d_{W,0}$ | Diameter of a single strand with insulation. |
| $d_{\text{Sec}}$ | Distance between two successive sections. |
| $d_{\text{tt}}$ | Distance between two successive turns. |
| $h$ | Thickness of foil or distance between layers. |
| $d_{\text{eff}}$ | Effective distance between two layers. |
| $k$ | Number of turns in one incomplete layer. |
| $L_L$ | Length of coil (or sum of sections). |
| $l_{w,m}$ | Mean turn length of two the considered layers. |
| $N_S$ | Number of strands of litz wire. |
| $N_{\text{Layer}}$ | Number of all layers of one winding. |
| $N_{L,i}$ | Number of turns in layer $i$. |
| $N_{\text{Sec}}$ | Number of sections. |
| $R_{L_1}$ | Radius of inner layer of considered pair of layers. |
| $R_{L_2}$ | Radius of outer layer of considered pair of layers. |
| $d_i/r_i$ | Diameter/Radius of wire without insulation. |
| $d_0/r_0$ | Diameter/Radius of wire including insulation. |
| $V_{LL}$ | Voltage between two successive layers of one winding. |
| $V_{\text{Wdg}}$ | Voltage of one winding. |
| $V_{\text{tt}}$ | Voltage between two successive turns. |
| $W_{E,LL}$ | Electrical energy stored between two layers. |
| $W_{E,6C}$ | Electrical energy stored in equivalent six-capacitor network. |
| $\text{W}_{E,\text{Wdg}}$ | Electrical energy stored in one winding. |
| $z$ | Number of turns in one complete layer. |

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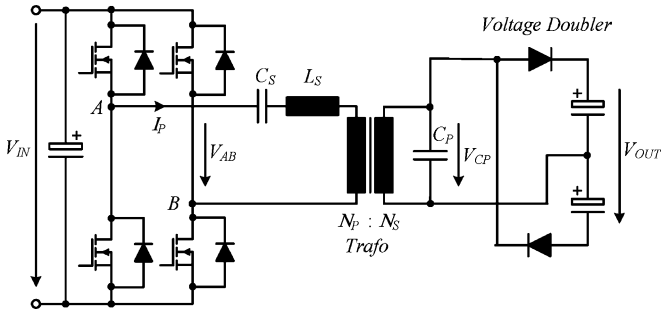


Fig. 1. Series-parallel resonant dc-dc converter.

## II. Introduction

APPLYING resonant dc–dc converters can help to reduce the switching losses and/or to raise the switching frequency of the power switches. On this account, the overall system size in many industrial applications, e.g., telecom power supplies [1], high-voltage generators [2], or inductive heating [3] could be reduced.

In particular, the series-parallel resonant converter, Fig. 1, is a promising converter structure since it combines the advantages of the series resonant and the parallel resonant concept. On one hand, the resonant current decreases with the decrease of the load and the converter can be regulated at no load, and on the other hand, a good part-load efficiency can be achieved [4], [5]. Furthermore, the converter is naturally short-circuit proof.

In order to reduce the overall system size, the series inductance of the resonant circuit could be integrated into the

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transformer by increasing the transformer-leakage inductance by a magnetic shunt as described in [6] and [7]. Also, the series and the parallel capacitors can be integrated in the transformer by using planar cores together with layers of high-permittivity material [7]–[9]. The application of integrated planar cores, however, is limited to power levels up to some kilowatts and is not appropriate for high-voltage applications. There, conventional transformers with wire winding structures are usually used. These transformers also have parasitic capacitances that can be used as integrated parallel capacitor of the resonant circuit.

Different aspects of the calculation of the parasitic capacitance are described in [10]–[51], but a complete structured overview and a comparison of the different calculation methods is missing. This will be presented and completed by deriving missing equations in this paper in order to find the most appropriate algorithm for calculating the "parasitic" parallel capacitance of the transformer, and to find the winding structure that is most suitable for realizing high-capacitance values and, which causes the lowest dielectric losses. Furthermore, the links and dependencies of the different approaches will be revealed.

In high-voltage applications, the number of turns of the secondary winding, which mainly causes the parasitic capacitance $Cp$, is high in order to limit the voltage per turn and to achieve a high-step-up ratio. This fact and the insulation requirements usually result in multilayer and multisection windings. For this reason, the presented algorithms focus on the calculation of the parasitic capacitance of multilayer windings that are divided into one or more sections. As shown in Fig. 2, the stored electric energy for a standard multilayer winding mainly concentrates between two successive layers. In comparison to that, the energy between two turns of the same layer is very small. Thus, the turn-to-turn capacitances of turns in the same winding layer are neglected in this paper.

The equivalent capacitance of single layer coils, whose value mainly depends on the turn-to-turn capacitance, is not covered in this paper, but information could be found in [47]–[51], for example.

All the parasitic capacitance models of windings/transformers are based on the static layer-to-layer capacitance, which could be measured at dc conditions between different layers. There are five different models for the static capacitance presented in literature—two simple approximations: parallel-plate capacitor [10]/cylindrical capacitor and three analytical methods [11], [12]. These models and the calculation methods are described in Section II for windings consisting of solid or litz wire. With the equations for the static layer-to-layer capacitance, the equivalent capacitor of standard and flyback windings (cf. Figs. 7 and 9), and with it a general equivalent model of multilayer windings could be calculated as presented in Section III. This equivalent model also includes incomplete layers. The presented model is verified by a finite element analysis (FEA) simulation result, and is approximately valid just below the first resonant frequency of the winding [18], since it sums up distributed capacitances to a lumped capacitor.

In Section IV, a more general model of two winding layers that could also be used to describe two layers of different wind-

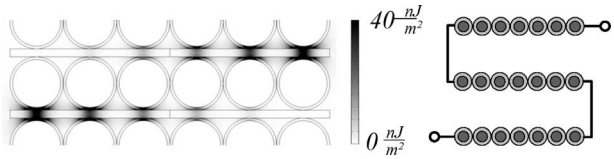


Fig. 2. Energy distribution within a multilayer standard winding.

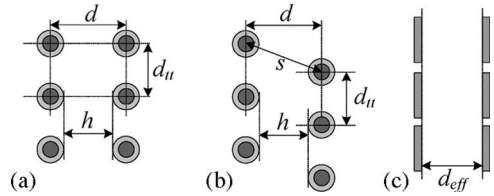


Fig. 3 (a) Orthogonal winding. (b) Orthocyclic winding. (c) Definition of effective distance between plates.

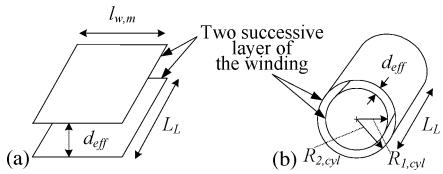


Fig. 4. (a) Parallel-plate capacitor model. (b) Cylindrical capacitor model.

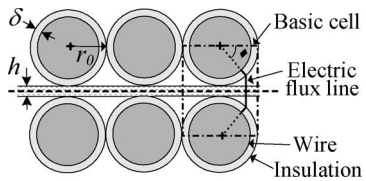


Fig. 5. Analytic field calculation for orthogonal winding.

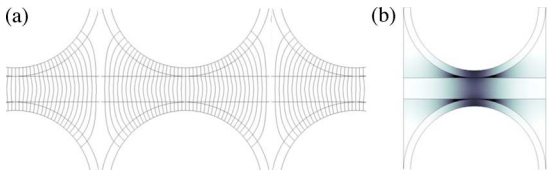


Fig. 6. (a) Electric flux line for orthogonal windings based on FEA. (b) Distribution of electric field strength.

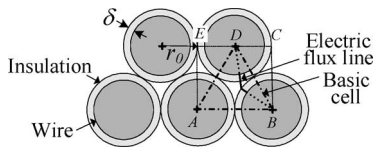


Fig. 7. Analytic field calculation for orthocyclic winding.

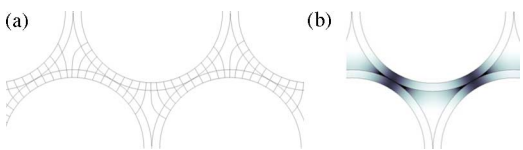


Fig. 8 (a) Electric flux line for orthocyclic windings based on FEA. (b) Distribution of electric field strength.

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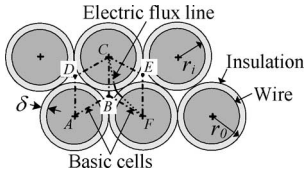


Fig. 9. Second analytic field calculation for orthocyclic winding.

ings or interleaved windings is discussed. The results of the different approaches are verified by measurements of the parasitic capacitance of four different high-voltage transformers in Section V. Finally, a conclusion and topics of future research are given in Section VI.

## III. Static Capacitance Model

All calculations of the equivalent winding capacitance are based on the static layer-to-layer capacitance. With this capacitance the electrical energy is calculated that is stored between two successive winding layers, and that will be used in Section III for calculating the equivalent capacitance. The layer-to-layer capacitance is calculated by assuming that the layers of the winding are equipotential surfaces, i.e., that all turns of one layer are short-circuited and edge effects are neglected. Thus, two successive layers of the winding could be approximated by a cylindrical capacitor [Fig. 4(b)] or a parallel-plate capacitor [Fig. 4(a)].

### A. Parallel-Plate Capacitor Model

For calculating the static capacitance, there are five different approaches. The first one replaces the round wires by flat rectangles, as shown in Fig. 3. In a second step, the flat rectangles can be replaced by an equipotential surface if the electrical connection between the layers is disconnected and dc conditions are assumed. This results in a parallel-plate capacitor, as shown in Fig. 5(a) [10].

The distance $d_{\text{eff}}$ is the effective distance between the plates [cf. Fig. 3(c)]. It is determined by calculating the capacitance of the real arrangement of the wires [Fig. 3(a) or (b)], i.e., the capacitance of the two wire grids and the value of the parallel-plate capacitor [Fig. 4(a)]. By equating these two capacitance values, the effective distance $d_{\text{eff}}$ could be calculated [cf. (1)] as a function of the geometry of the wire grid. The variable $d'$ is given in (2) for orthogonal windings (cf. Section II-C) and in (3) for orthocylcic windings (cf. Section II-D). For the orthocyclic winding, there are two different values for $d'$ depending on the distance of the two layers

$$d_{\text{eff}} = d' - 2.3\,(r_0 + \delta) + 0.26\,d_{\text{tt}} \tag{1}$$

$$\text{Orthogonal (3a)}: \quad d' = d = 2r_0 + h \tag{2}$$

Orthocyclic (3b):

$$d' = \begin{cases} d = 2r_0 + h & h > 0 \\ r_0 + \dfrac{h}{2} + \dfrac{\sqrt{(2r_0+h)^2 + d_{tt}^2/4}}{2} & h \le 0 \end{cases}. \tag{3}$$

The derivation of the relationship for the effective distance is described in [13] and it will not be repeated in this paper for the sake of brevity.

The value of the parallel-plate capacitor could be calculated as

$$C_{0,\text{pla}} = \varepsilon_0 \varepsilon_{r,m} \frac{l_{w,m} L_L}{d_{\text{eff}}} = \varepsilon_0 \varepsilon_{r,m} \frac{l_{w,m} z 2 r_0}{d_{\text{eff}}}. \tag{4}$$

By (5), the effective permittivity $\varepsilon_{r,m}$ and the average turn length of the two layers $l_{w,m}$ that are used in (4) can be calculated. The effective permittivity is determined by equating the voltage across the series connected dielectrics and the voltage across the equivalent dielectrics or by equating the stored energies [52].

$$\varepsilon_{r,m} = \frac{\varepsilon_D \varepsilon_F\,(\delta + h)}{\varepsilon_F \delta + \varepsilon_D h}; \qquad h = R_{2,\text{cyl}} - R_{1,cyl};$$
$$l_{w,m} = \pi\,(R_{1,\text{cyl}} + R_{2,\text{cyl}})\,. \tag{5}$$

*1) Remark:* The author of [22] uses the parallel-plate capacitor model for approximating the relative permittivity by measurement data for wires in the range $r_0 = 0.05\ldots$, 0.35 mm. The result is that $E_R$ varies from 1.3 for thicker wires to 2.2 for thinner ones for orthogonal windings [cf. Fig. 3(a)]. For orthocyclic windings, the permittivity is assumed to be approximately double. Furthermore, the author assumes that in a standard winding, approximately half of the turns are orthogonal and the other half is orthocyclic. With the foregoing assumptions and by assuming further that $h = 0$, the resulting static interlayer capacitance is equal to

$$C_{0,\text{app}} \approx 180 e^{-12} l_{w,m} \frac{z\,(z+1)\,(2z+1)}{6z^2}$$
$$\approx 60\, l_{w,m}\, z \quad \text{pF} \quad (\text{z} >> 1). \tag{6}$$

This equation could be used as a thumb rule for a first guess on the parasitic capacitances of windings.

### B. Cylindrical Capacitor Model

Many windings have a cylindrical shape. Therefore, the second approach replaces the parallel-plate capacitor by a cylindrical capacitor, as shown in Fig. 4(b). Thereby, the round wires of a layer have also been replaced by an equipotential surface (cf. Section II-A, Fig. 3). For the cylindrical capacitor the capacitance is calculated by

$$C_{0,\text{cyl}} = \frac{\varepsilon_0 \varepsilon_{r,m} 2\pi L_L}{\ln\left((R_{1,\text{cyl}} + d_{\text{eff}})/R_{1,\text{cyl}}\right)} = \frac{\varepsilon_0 \varepsilon_{r,m} 2\pi 2 z r_0}{\ln\left((R_{1,\text{cyl}} + d_{\text{eff}})/R_{1,\text{cyl}}\right)}. \tag{7}$$

The radius of the inner cylinder is given as a mean value of the two cylindrical layers minus half of the effective distance $d_{\text{eff}}$.

$$R_{1,\text{cyl}} = \frac{R_{L1} + R_{L2} - d_{\text{eff}}}{2}. \tag{8}$$

For standard values of $R_{1,\text{cyl}}$ and $R_{2,\text{cyl}}$ of high-power transformers, the difference between the parallel-plate and the cylindrical capacitor model is quite small so that the simpler parallel-plate capacitor model could be used in most cases.

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### C. Analytic Capacitance Model for Orthogonal Windings

The remaining three approaches approximate the electric flux lines by straight lines. An example of an approximated electric flux line for an orthogonal winding, whose layers are separated by a foil of thickness $h$, is shown in the basic cell of Fig. 5. In orthogonal windings, the turns of successive layers are orthogonally on top of each other, whereas in orthocyclic windings, the turns of the successive layer are in the gaps between two turns of the preceding layer.

The electric flux line leaves the wire, which is an equipotential surface, approximately orthogonally. Because of the small thickness $\delta$ of the insulation, the flux line approximately runs as a straight line to the border of the insulation [11]. Then, the approximated flux line deviates toward the successive layer and runs as a straight line to the second layer. It crosses the symmetry line (dashed line in Fig. 5) of the two layers orthogonally. The path of the flux line continues symmetrically from the symmetry line to the second wire. This approach is used for all angles $\varphi$ from 0 to 180°, i.e., that within one basic cell, all approximated electric flux lines from one turn to the underlying one are contained.

In Fig. 6, the resulting flux lines of a finite element analysis are shown. The FEA-flux lines correspond quite well with the approximated flux lines especially in the regions where the stored electric energy and, therefore, the parasitic capacitance is high ($\varphi$ is around 90°—cf. Fig. 2— energy).

With the considered path of the flux lines, a given permittivity of the insulation and the foil, and the given voltage between one wire and the underlying wire (layer-to-layer voltage), the electric field strength in the different sections of the approximated flux line could be calculated. Then, the electric field strength could be used for calculating the electric energy that is stored between the two wires lying on top of each other. This energy is equated to the electric energy that is stored in the equivalent capacitor, which leads to the equivalent capacitance of the basic cell. Multiplying this capacitance by the number of turns per layer, $z$ results in the static capacitance of the two layers. The detailed calculation is described in [11].

The result of the earlier described calculation is the static layer-to-layer capacitance for orthogonal windings

$$C_{0,\mathrm{ortho}} = \frac{\varepsilon_0 z l_{w,m}}{1-\delta/\varepsilon_D r_0}\left[V + \frac{1}{8\varepsilon_D}\left(\frac{2\delta}{r_0}\right)^2 \frac{Z}{1-\delta/\varepsilon_D r_0}\right]. \tag{9}$$

with

$$V = \frac{\beta}{\sqrt{\beta^2-1}}\arctan\left(\sqrt{\frac{\beta+1}{\beta-1}}\right) - \frac{\pi}{4}$$

$$Z = \frac{\beta\left(\beta^2-2\right)}{\left(\beta^2-1\right)^{3/2}}\arctan\left(\sqrt{\frac{\beta+1}{\beta-1}}\right) - \frac{\beta}{2\left(\beta^2-1\right)} - \frac{\pi}{4}$$

$$\alpha = 1-\frac{\delta}{\varepsilon_D r_0}; \qquad \beta = \frac{1}{\alpha}\left(1+\frac{h}{2\varepsilon_F r_0}\right). \tag{10}$$

### D. Analytic Capacitance Model for Orthocyclic Windings

A similar analytic approach [11] could be used for an orthocyclic winding which is shown in Fig. 7. There, the basic cell consists of a triangle (ABD) and the path of the approximated electric flux line, which is very similar to the one described in the foregoing section, is given. Again, the analytic electric flux lines correspond very well with the flux lines resulting from finite element analysis (Fig. 8).

For calculating the static layer-to-layer capacitance the analytic flux line is used to calculate the energy that is stored in the basic cell, as done in Section II-C. In order to calculate the complete electric energy that is stored between one turn of the upper layer and the two underlying turns of the lower layer, one also has to consider the energy stored in the two small triangles (ADE and BCD in Fig. 7). This is done by multiplying the energy stored in the basic cell by two, since the two small triangles are half of the two adjacent basic cells.

Again, the complete layer-to-layer capacitance is calculated by a comparison of stored energies (cf. Section II-C). The resulting capacitance is

$$C_{0,\mathrm{cyclic}} = 4\varepsilon_0 z l_{w,m}\left[M_L + \frac{4\delta r_0 - 2\delta^2}{\varepsilon_D\left(2r_0\right)^2} M_D\right]. \tag{11}$$

together with

$$M_L = \int_0^{\pi/6} \frac{\cos^2\psi - \cos\psi\sqrt{\cos^2\psi - 3/4} - 1/2}{2[\cos\psi - (1-\delta/2\varepsilon_D r_0)(\sqrt{\cos^2\psi - 3/4}+1/2)]^2}\,d\psi$$

$$M_D = \int_0^{\pi/6} \frac{\sin^2\psi + \cos\psi\sqrt{\cos^2\psi - 3/4}}{2[\cos\psi - (1-\delta/2\varepsilon_D r_0)(\sqrt{\cos^2\psi - 3/4}+1/2)]^2}\,d\psi \tag{12}$$

*1) Remark:* In order to achieve a better agreement between the calculations and measurements, the authors of [21] introduced an empiric equation for the relative permittivity in (11).

$$\varepsilon_D = 2.5 + \frac{0.7}{\sqrt{2r_i/\mathrm{mm}}}. \tag{13}$$

With this function, $\varepsilon_D$ varies from 2.95 for $r_i = 1.25$ mm to 6 for $r_i = 0.02$ mm.

### E. Second Analytic Capacitance Model for Orthocyclic Windings

A second calculation model for the turn-to-turn capacitance of orthocyclic windings is presented in [12]. The approach is very similar to the one in the foregoing section except for the exact path of the electrical flux line and the shape of the basic cell, as shown in Fig. 9 where the basic cell is a rhombus (e.g., ABCD). See (14), at the bottom of the next page.

In order to calculate the complete energy stored between one turn of the lower layer and two "half" turns of the upper layer, one has to consider two rhombuses (ABCD and BFEC). The area covered by these two rhombuses is a little bit smaller than the one covered by the two triangles of Fig. 7, and the path of the flux line in the region between the insulations of the

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TABLE I
COMPARISON BETWEEN LAYER CAPACITANCE MODELS WITH $l_{w,m} = 1$ m; $\delta = 100\ \mu$m; $r_0 = 0.5$ mm; $z = 1$; $h = 0.15$ mm; $\varepsilon_D = 3$; $\varepsilon_F = 3$

A. Orthogonal Winding

| FEA: 51.8pF/m | Value | Error |
|---|---|---|
| Parallel-Plate (4) | 54.2pF/m | 5.1 % |
| Cylindrical (7) | 54.5pF/m | 4.6 % |
| Orthogonal (9) | 49.2pF/m | -4.9 % |

B. Orthocyclic Winding

| FEA 136.5pF/m | Value | Error |
|---|---|---|
| Parallel-Plate (4) | 54.2pF/m | -60.2 % |
| Cylindrical (7) | 54.5pF/m | -60 % |
| Orthocyclic (11) | 140pF | 2.8% |
| Orthocyclic II (14) | 158pF | 16.8% |
| Orthocyclic – Empiric (11+13) | 146pF/m | 7.8 % |

wire is a bit different. Furthermore, for calculating (11) and (12), the author of [11] made some numerical approximations. This causes slight differences in the result for the static-layer capacitance as compared to (11).

### F. Comparison of Static Layer Models

In Table I, the results of the different models for the static-interlayer capacitance and the result of a FEA-Simulation are compared. For the orthogonal windings, the "orthogonal" model (9) yields good results. The results for the orthocyclic winding also show that the approximation of the flux lines by the "orthocyclic" model (11) causes the smallest errors, and the simple approaches cause a significant error.

*1) Remark:* A too exact modeling of the path of the electric flux lines and the static interlayer capacitance is useless, since the tolerances of the geometric winding parameters are usually large and the positioning of the wire is not deterministic.

### G. Using Litz Wire Instead of Solid Wire

For calculating the static interlayer capacitance $C_0$, the outer diameter $r_0$ of the wire and the nominal diameter $d_i$ are needed. In order to apply the calculations also for inductors and transformers by using litz wire, these parameters have to be derived from the specifications of the applied litz wires, as described in [21]. In Fig. 10 the geometry of a litz wire and the belonging solid wire are depicted.

The nominal diameter $d_i$ could be calculated by subtracting the thickness of the twists' outer insulation and the thickness of the insulation of a single strand from the outer diameter of the

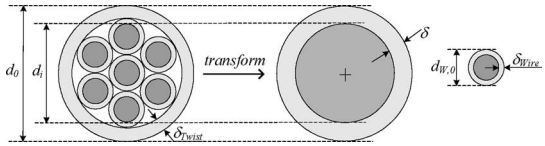


Fig. 10. Transformation of Litz-wire to solid wire.

complete litz wire as

$$r_i = r_0 - \delta = r_0 - \delta_{\text{Twist}} - \delta_{\text{Wire}}. \tag{15}$$

The outer diameter of the litz wire could be taken from the data sheet of the wire or calculated by (16), presented in [21].

$$r_0 = \sqrt{\frac{4N_S}{\pi}}\frac{d_{W,0}}{2}. \tag{16}$$

Another possibility is to use (17) for determining the outer diameter. This equation is presented in [16], and is based on the interpolation of values given in data sheets of different litz wires.

$$r_0 = \frac{135\times 10^{-6}}{2}\left(\frac{N_S}{3}\right)^{0.45}\left(\frac{d_{W,0}-2\delta_{\text{Wire}}}{40\times 10^{-6}}\right)^{0.85} - \delta_{\text{Twist}}. \tag{17}$$

In general, the accuracy of the analytic calculation procedure for determining the equivalent capacitance of inductors or transformers using litz wire is limited, since the winding tension and the shape of the bobbin strongly affect the parasitic capacitance of the winding. Further information on this topic could be found in [21].

## IV. CONNECTION OF LAYERS OF THE SAME WINDING

The static layer-to-layer capacitance does not comprise the voltage distribution between the layers that is dependent on the winding method (standard or flyback—cf. Figs. 7 and 9). According to the applied winding structure, the effective layer-to-layer capacitance changes because the static capacitance is not charged uniformly, but the charge distribution depends on the voltage distribution.

### A. Standard Winding Method (Two Layers)

For the standard winding method (Fig. 11), one side ($x = 0$) of the two layers is shortened and the voltage between the two layers at the other side ($x = L_L$) is double the layer voltage $V_{\text{Wdg}}/N_{\text{Layer}}$ (it is assumed that all layers have the same number of turns $z$ per layer). This fact leads to a relatively high-electric field strengths and dielectric losses at the unconnected side ($x = L_L$) of the layer.

If it is assumed that all turns of the two layers comprise the same magnetic flux, the voltage distribution along the layer [cf. Fig. 11(c] is approximately linear (exact: staircase-shaped).

$$C_{0,\text{cyclic II}} = z\,\varepsilon_0\,l_{w,m}\,\frac{4\varepsilon_r\,\tan^{-1}\{\left(\sqrt{3}-1\right)\left(2\varepsilon_r+\ln\,r_0/r_i\right)\}/\{\left(\sqrt{3}+1\right)\sqrt{\ln\,r_0/r_i\,\left(2\varepsilon_r+\ln\,r_0/r_i\right)}\}}{\sqrt{2\varepsilon_r\,\ln\,r_0/r_i+\left(\ln\,r_0/r_i\right)^2}} \tag{14}$$

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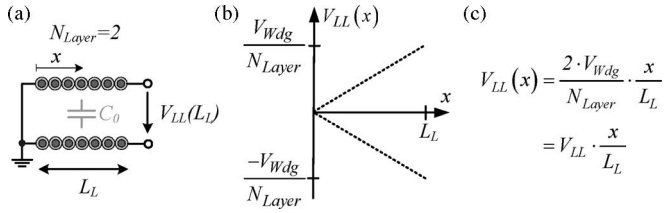


Fig. 11. Layer-to-layer voltage for standard winding method.

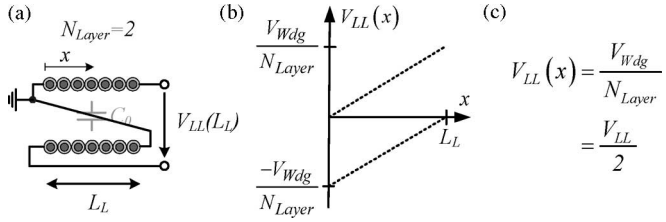


Fig. 12. Layer-to-layer voltage for a flyback winding.

In this case, the leakage flux, which flows through single turns of the layers, is neglected because it is very small for usual winding designs. With the voltage distribution $V_{L_L}(x)$, the stored electric energy could be calculated as (where $V_{L_L} = V_{\text{Wdg}}$)

$$W_{E,LL} = \frac{C_0}{2L_L}\int_0^{L_L} V_{LL}^2(x)\,dx = \frac{2C_0}{3}\left(\frac{V_{\text{Wdg}}}{N_{\text{Layer}}}\right)^2 = \frac{C_{\text{Layer}}V_{\text{Wdg}}^2}{2}. \tag{18}$$

Equating this energy to the energy stored in the equivalent layer capacitor $C_{\text{Layer}}$ [right hand side of (18)] results in the equivalent layer capacitor for the standard winding method $C_{\text{Layer}} = C_0/3$.

### B. Flyback Winding Method (Two Layers)

With the flyback winding method, all layers are wound in the same direction and the voltage between the two layers is constantly equal to the layer voltage $V_{\text{Wdg}}/N_{\text{Layer}}$ (Fig. 12). Therefore, the electric field strength and the dielectric stress are uniformly distributed and the dielectric losses are lower as compared to the standard winding method.

A disadvantage of the flyback winding method is that at the end of one layer, the wire of the winding has to cross all turns of this and the proximate layer. This leads to a lager overall winding length, and to local high-electric field strengths and dielectric losses (locally comparable to the standard winding method). The problem with the local high-electric field strength could be avoided with special arrangements of the "flyback connection" of the layers, but this increases the complexity of the manufacturing significantly.

For calculating the voltage distribution [Fig. 12(c)] along the layer, it is assumed again that all turns of the two layers are linked with the same flux (cf. Section III-A).

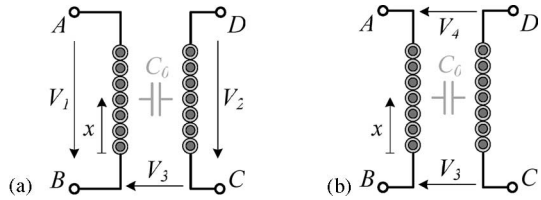


Fig. 13. Layer-to-layer voltage for a flyback winding.

Equating the stored electric energy [(19), where $V_{LL} = V_{\text{Wdg}}$] to the energy that is stored in the equivalent layer capacitor

$$W_{E,LL} = \frac{C_0}{2L_L}\int_0^{L_L} V_{LL}^2(x)\,dx = \frac{C_0}{2}\left(\frac{V_{\text{Wdg}}}{N_{\text{Layer}}}\right)^2 = \frac{C_{\text{Layer}}V_{\text{Wdg}}^2}{2} \tag{19}$$

results in an equivalent capacitor $C_{\text{Layer}} = C_0/4$.

### C. General Approach for Arbitrary Winding Methods (Two Layers)

In Sections III-A and III-B, the voltage distribution between the two layers and therewith, the equivalent layer capacitance is calculated separately for the standard and the flyback winding method. In the following, a more general approach for arbitrary winding connections that is used by many authors [10], is presented.

The voltage between the two layers could be expressed in terms of $V_1$, $V_2$ and $V_3$, or $V_3$ and $V_4$ independently from the winding method [Fig. 13 and (20)]

$$V_{LL}(x) = V_3 + (V_2 - V_1)\frac{x}{L_L} = V_3 + (V_4 - V_3)\frac{x}{L_L}. \tag{20}$$

With the layer voltage, the stored energy is calculated and equated to the energy in the equivalent capacitance (cf. Section III-A) that results in (21) for the equivalent capacitance, where $V_{L_L}$ is the sum of the voltages across the two layers.

$$C_{\text{Layer}} = \frac{C_0}{3}\frac{\left(V_3^2 + V_3V_4 + V_4^2\right)}{V_{LL}^2} = \frac{C_0}{3}\left((V_2 - V_1)^2 + 3V_3(V_2 - V_1) + 3V_3^2\right). \tag{21}$$

Connecting the layers either with the standard or the flyback winding method the general approach provides the same results as calculated in Sections III-A and III-B.

### D. Multilayer Windings

In the preceding sections, the calculation of the equivalent capacitance for two layers for different winding methods is described. With these equations, the equivalent capacitance for multilayer windings with standard or flyback winding method (cf. Fig. 14) could be calculated, as explained in the following.

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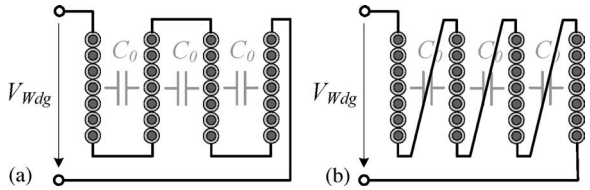


Fig. 14. (a) Multilayer standard flyback. (b) Winding method ($N_{\text{Layer}} = 4$).

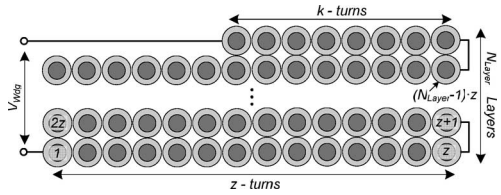


Fig. 15. Winding with incomplete layer.

Again, the equivalent capacitor for the complete winding is calculated by equating the energy stored in this capacitor to the energy that is stored in all the layer capacitors

$$W_{E,\text{Wdg}} = \frac{C_{\text{Wdg}} V_{\text{Wdg}}^2}{2} = \frac{1}{2} \sum_{\nu=1}^{N_{\text{Layer}}-1} C_{\text{Layer},\nu} \left( \frac{2V_{\text{Wdg}}}{N_{\text{Layer}}} \right)^2.$$

$$\Rightarrow C_{\text{Wdg}} = \sum_{\nu=1}^{N_{\text{Layer}}-1} C_{\text{Layer},\nu} \left( \frac{2}{N_{\text{Layer}}} \right)^2. \tag{22}$$

If all layer capacitors $C_{\text{Layer},\nu}$ are equal, the equation for the equivalent winding capacitor simplifies to the well-known equation

$$C_{\text{Wdg}} = 4 \frac{N_{\text{Layer}} - 1}{N_{\text{Layer}}^2} C_{\text{Layer}}. \tag{23}$$

In (22), the calculation of the equivalent winding capacitor $C_{\text{Wdg}}$ is done by equating the stored energies. A different approach uses the impedance transformation rule of autotransformers. There, the equivalent layer capacitor of two layers $C_{i,i+1}$ is transformed into a capacitor at the input of the winding $C'_{i,i+1}$ by multiplying the equivalent layer capacitor $C_{i,i+1}$ by the square of the turns ratio of the two layers to the complete winding resulting in

$$C'_{i,i+1} = \frac{(N_{L,i} + N_{L,i+1})^2}{\left( \sum_{k=1}^{N_{\text{Layer}}} N_{L,k} \right)^2} C_{i,i+1} \Rightarrow$$

$$C_{\text{Wdg}} = \sum_{i=1}^{N_{\text{Layer}}-1} C'_{i,i+1}. \tag{24}$$

The transformed equivalent capacitors are connected in parallel and can be summed up to the equivalent winding capacitor $C_{\text{Wdg}}$ that is in parallel to the winding.

### E. Incomplete Layers

So far, only complete layers with $z$ turns in each layer have been considered. In the following, a winding with $N_{\text{Layer}} - 1$ layers with $z$ turns and the last layer with $k < z$ turns is considered, as shown in Fig. 15 [21].

The interlayer capacitance for the complete layers could be calculated, as described in Section III, and the interlayer capacitance built by one complete and the incomplete layer scales linearly with the number of turns, as

$$C_{\text{Layer},N} = C_{\text{Layer}} \frac{k}{z} \qquad \text{with} \qquad N = N_{\text{Layer}} - 1. \tag{25}$$

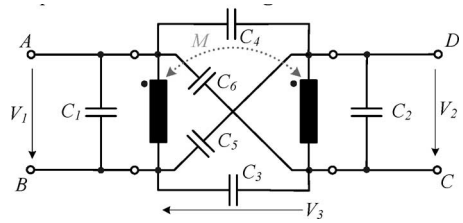


Fig. 16. Equivalent circuit of two arbitrary layers/windings.

The equivalent winding capacitor $C_{\text{Wdg}}$ is calculated by transforming all interlayer capacitors to the connection of the winding by the impedance transformation rule of transformers

$$C_{\text{Wdg}} = \frac{C_{\text{Layer},N} 2k^2 + \sum_{\nu=0}^{N_{\text{Layer}}-2} C_{\text{Layer},\nu} 2z^2}{((N_{\text{Layer}} - 1)\, z + k)^2}. \tag{26}$$

If it is assumed that all interlayer capacitances are the same, the equation simplifies to

$$\text{C}_{\text{Wdg}} = \frac{4C_{\text{Layer}} (N_{\text{Layer}} - 1) \left(z^2 + k^2\right)}{((N_{\text{Layer}} - 1) \cdot z + k)^2}. \tag{27}$$

## V. General Model of Two Layers

In Section III, an equivalent circuit for two or more layers of the *same* winding is calculated, whereas in this section, a model for two *arbitrary* successive layers is presented. This model could be used for calculating the equivalent capacitor of two layers from different windings e.g., primary and secondary winding or interleaved winding structures.

### A. Generalized Capacitance Model of Two Layers

As the authors of [14] have shown the electrostatic behavior of a transformer (what is equivalent to two layers of different windings) could be modeled by a three-input multipole (primary and secondary voltage and the voltage between the windings). In the linear working area, as long as propagation times can be ignored, the electrostatic energy/behavior of this multipole could be modeled by six independent capacitors, as shown in Fig. 16.

The values of the six capacitors in Fig. 16 are again calculated by the energy approach. First, the energy that is stored in the capacitance between the two layers—cf. Fig. 13(a)—is calculated by using the equation of the layer-to-layer voltage (20). The energy is expressed in terms of the three voltages $V_1$, $V_2$,

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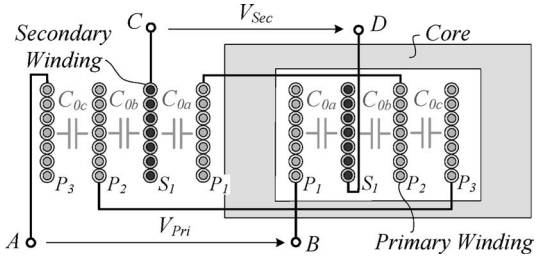


Fig. 17. Transformer with interleaved primary and secondary winding.

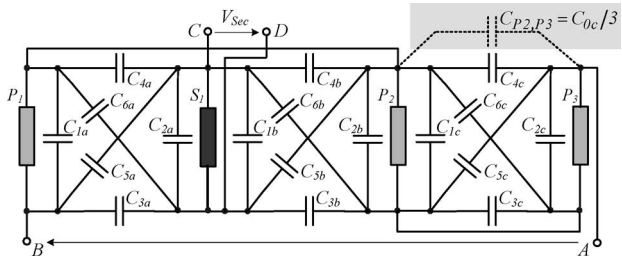


Fig. 18. General equivalent circuit for transformer of Fig. 17.

and $V_3$ in

$$W_{E,LL} = \frac{C_0}{6}\left((V_2 - V_1)^2 + 3V_3\,(V_2 - V_1) + 3V_3^2\right). \quad (28)$$

Second, also the energy stored in the six capacitors of Fig. 16 is calculated in dependence of $V_1$, $V_2$, and $V_3$ as

$$W_{E,6C} = \frac{1}{2}\begin{pmatrix} C_1V_1^2 + C_2V_2^2 + C_3V_3^2 + C_4\,(V_2 + V_3 - V_1)^2 \\ +C_5\,(V_2 + V_3)^2 + C_6\,(V_3 - V_1)^2 \end{pmatrix}. \quad (29)$$

By equating these two energies and comparing the coefficients of the variables $V_1$, $V_2$, $V_3$, $V_1V_2$, $V_1V_3$, and $V_2V_3$, the six capacitors could be expressed in terms of the static-winding capacitance $C_0$. The result is given in (30). The values of these six capacitors can also be determined by three independent measurements, as described in [14] and [15] (where $C_1 = C_2$, $C_3 = C_4$, and $C_5 = C_6$ is assumed).

$$W_{E,L_L} = W_{E,6C} \Rightarrow C_1 = C_2 = -\frac{C_0}{6}; \quad C_3 = C_4 = \frac{C_0}{3}; \quad C_5 = C_6 = \frac{C_0}{6}. \quad (30)$$

### B. Complete Capacitance Model for Transformers or Coils

With the equivalent circuit for arbitrary layers of different windings, it is now possible to model the complete winding structure of transformers. Each pair of successive layers is modeled with an equivalent circuit consisting of six capacitors (Fig. 16) [17]. The result is a quite complex model of the parasitic winding capacitance if the number of layers is larger than two. However, it is always possible to reduce the number of equivalent capacitors to six, as it is shown later.

In the following, the transformer assembly in Fig. 17 is taken as an example. The primary winding consists of three layers (light grey, $P_1$–$P_3$) that are interleaved with one secondary layer (dark grey, $S_1$). First, an equivalent circuit consisting of six capacitors (Fig. 16) is calculated for each pair of layers, as shown in Fig. 18 (where, to each inner layer, two capacitors are connected in parallel—e.g., $C_{2a}$ and $C_{1b}$ to the primary layer—according to the two basic cells on each side of the layer). The value of the static capacitance could be different for each layer.

The layers $P_2$ and $P_3$ of the primary winding are not interleaved with the secondary winding and are connected directly. Thus, the interlayer capacitor $C_{P2,P3}$ could be simply modeled by one capacitor (instead of $C_{1c} - C_{6c}$) and could be calculated as described in Sections III-A and III-B, and as shown in Fig. 18 in the grey shaded part.

In general, the equivalent capacitor for two successive layers belonging to the same winding is directly calculated by $C_{\text{Layer}} = C_0/3$ or $C_{\text{Layer}} = C_0/4$ instead of using the six-capacitor network (Fig. 16). Only two successive layers belonging to different windings must be modeled by the six-capacitor network.

In the second step, the equivalent layer capacitors are transformed to the connection of the winding (A, B, C, and D in Fig. 17) by using the impedance transformation rule of transformers (24). This results in

$$C_{P2,P3} = \frac{C_{0c}}{3} \Rightarrow C_{\text{Wdg}} = C_{AB} = \left(\frac{2}{3}\right)^2 \frac{C_{0c}}{3}. \quad (31)$$

Furthermore, also all six capacitor networks are transformed to the connection of the winding.

This is done by writing the voltages of the six capacitors as a function of the primary and secondary voltage $V_1$ and $V_2$

$$\begin{aligned} V_{C_1} &= (a-b)V_1 \quad V_{C_2} = (c-d)V_2 \\ V_{C_3} &= -bV_1 + dV_2 + V_3 \quad V_{C_4} = -aV_1 + cV_2 + V_3 \\ V_{C_5} &= -bV_1 + cV_2 + V_3 \quad V_{C_6} = -aV_1 + dV_2 + V_3 \end{aligned} \quad (32)$$

by calculating the energy stored in the six original capacitors (Fig. 19) also as a function of $V_1$ and $V_2$ and

$$W_{E,6C\_\text{org}} = \frac{C_0}{12}\Big[-V_{C_1}^2 - V_{C_2}^2 + 2V_{C_3}^2 + 2V_{C_4}^2 + V_{C_5}^2 + V_{C_6}^2\Big] \quad (33)$$

equating this energy to the energy that is stored in the six transformed capacitors (29). By comparing the coefficients of the different terms of $V_1$, $V_2$, and $V_3$, the values of the six transformed capacitors could be calculated as function of the ratios $a$, $b$, $c$, and $d$ (34)

$$\begin{aligned} W_{E,6C\_\text{org}} = W_{E,6C} \Rightarrow \\ C_1 &= C_0/6\left(2a^2 + 2ab + 2b^2 - 3a - 3b\right) \\ C_2 &= C_0/6\left(2c^2 - 3c - 3d + 2d^2 + 2cd\right) \end{aligned}$$

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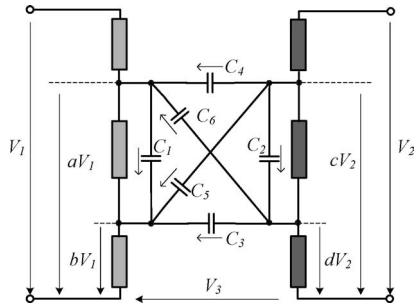



Fig. 19. Transformation of six capacitor network.

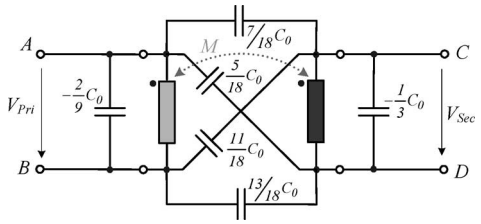



Fig. 20. Resulting equivalent network for transformer of Fig. 17.

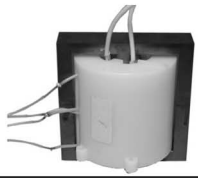
TABLE II
COMPARISON BETWEEN LAYER CAPACITANCE MODELS WITH $R_{L1} = 15$ mm; $\delta = 30\ \mu$m; $r_0 = 0.75$ mm; $z = 30$; $h = 0$ mm; $\varepsilon_D = 2.5$

| $C_{Layer}$ | Winding method | |
|---|---|---|
| | Standard | Flyback |
| Parallel-Plate (4) | 140pF | 105pF |
| Cylindrical (7) | 140pF | 105pF |
| Orthogonal (9) | 133pF | 99pF |
| Orthocyclic (11) | 236pF | 171pF |
| Orthocyclic II (14) | 246pF | 185pF |
| Empirical (plate) (6) | 187pF | 140pF |
| Empirical (cyclic) (11+13) | 209pF | 156pF |

$$
\begin{aligned}
C_3 &= C_0/6\big(-3a + 2ac + ad - 3b + 2bd \\
&\quad + bc - 3c - 3d + 6\big) \\
C_4 &= C_0/6\,(2ac + ad + 2bd + bc) \\
C_5 &= C_0/6\,(-2ac - ad - 2bd - bc + 3c + 3d) \\
C_6 &= C_0/6\,(3a - 2ac - ad + 3b - 2bd - bc)\,. \qquad (34)
\end{aligned}
$$

All transformed six capacitor networks are finally connected in parallel. This is also true for the transformed equivalent layer capacitors of winding 1, which are in parallel to $C_1$, and all transformed equivalent capacitors of winding 2, which are in parallel to $C_2$. Thus, after combining all parallel capacitors to one capacitor, a single six-capacitor network modeling all parasitic capacitances results. For the considered example, the result is shown in Fig. 20, where it is assumed that all static-layer capacitances ($C_{0a} = C_{0b} = C_{0c}$) are equal.

TABLE III
EXPERIMENTAL RESULTS FOR FOUR HIGH-VOLTAGE TRANSFORMERS

| Type | HVT-1 | HVT-2 |
|---|---|---|
| |  |  |
| | Equivalent Secondary Winding Capacitor | |
| Measured | 4.3pF | 12.4pF |
| Orthogonal (9) | 2.45…**2.78**...3.14 pF | 6.4…**7.3**...8.3 pF |
| Orthocyclic (11) | 4.12...**4.75**...5.44 pF | 10.7...**12.4**...14.2 pF |
| Orthocyclic (11 +13) | 3.91…**4.56**...5.28 pF | 9.66…**11.3**...13.2 pF |
| Orthocyclic II (14) | 4.55…**5.17**...5.86 pF | 11.9…**13.6**...15.4 pF |
| Parallel-Plate (4) | 3.68…**4.12**...4.56 pF | 9.7…**10.8**...12.1 pF |
| Type | HVT-3 | PT1 |
| |  |  |
| | Equivalent Secondary Winding Capacitor | |
| Measured | 7.15pF | 4.2pF |
| Orthogonal (9) | 0.99…**1.16**...1.35 pF | 0.83…**1.31**...3.35 pF |
| Orthocyclic (11) | 1.40...**1.70**...2.03 pF | 1.25...**2.15**...6.05 pF |
| Orthocyclic (11 +13) | 1.05…**1.31**...1.57 pF | 1.26…**2.16**...6.1 pF |
| Orthocyclic II (14) | 1.81…**2.09**...2.41 pF | 1.60…**2.44**...6.35 pF |
| Parallel-Plate (4) | 1.29…**1.51**...1.75 pF | 1.25…**2.01**...4.17 pF |

## VI. EXPERIMENTAL VERIFICATION

In Table II, the calculated results for the different approaches for one winding geometry and the two possible winding methods (standard and flyback) are given. Besides the analytic capacitance models, the results for the two empirical methods (6) and (13) are also included. The largest value is obtained for orthocyclic turns, since the distance between the wires is the smallest and the empirical values are close to this value. At the lower end of the range, the values for the orthogonal turns and parallel-plate and cylindrical model can be found since the distance between the wires is large.

In Table III, the measurement and calculation results for four different high-voltage transformers are given. The values, measured with an impedance analyzer HP4294 A from Agilent, agree well with the calculated average values of the transformers if the wire insulation is small in comparison to the wire diameter (HVT-1: $\delta\,/r_0 \approx 11\%$ and HVT-2: $\delta\,/r_0 \approx 10\%$). The range of values is a result of including the tolerances of the mechanical properties of the winding in the calculations.

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For transformers whose wire insulation is large in comparison to the wire diameter (HVT-3: $\delta/r_0 \approx 50\%$ and HVT-2: $\delta\ /r_0 \approx 20\%$), the electric flux not only flows from the layer $L_1$ to the successive layer $L_2$ below but also to the layer $L_3$, which is below layer $L_2$. The flux is flowing through the relatively large areas of insulation between the wires of layer $L_2$. Thus, for calculating the equivalent capacitance of a pair of layers, one has to consider not only the next layer but also the subsequent layer. This must be considered in the equations and will be presented in a future paper.

## VII. Conclusion

A complete survey of the different calculation methods for parasitic transformer capacitances was given and general equations were added. Based on the compiled equations, a simple modeling procedure for the parasitic capacitances of inductors and transformers was presented. The different calculations methods were compared, and verified by FEA simulations and measurement results for high-voltage transformers.

As proved by the measurement results, the equivalent capacitor could be calculated by the presented procedures and predicted without building the transformer. The parasitic capacitance, which is in parallel to the windings of the transformer, could be used as a parallel capacitor in a series–parallel resonant dc–dc-converter as proven by experiment.

Due to the admissible page count of this paper, the influence of the core and shields on the equivalent winding capacitor have been neglected. The corresponding equations and measurement results will be presented in a future paper.

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