Novel Three-Phase Y-Rectifier Cyclic 2 out of 3 DC Output Voltage Balancing

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***Abstract*—A three-phase Y-Rectifier is formed by the star connection of single-phase unity power factor rectifier systems and represents a highly interesting concept for the realisation of the input stage of high-power telecommunications power supply modules using established single-phase technology. However, for stable operation, control and balancing of the independent DC output voltages of the phase rectifier systems is required. A novel, easy to implement DC output voltage control concept is proposed in this paper. There, the mean value of all three DC output voltages is controlled and, in addition, always 2 out of the 3 DC voltages are compared and balanced. The basic operating principle of the control is described and the theoretical limit for the admissible asymmetric loading of the DC voltages is calculated. Finally, the theoretical considerations are verified by measurements on a 3×1kW Y-Rectifier prototype.**

I. Introduction

The input stage of high power telecom power supply modules can be realised with either a direct three-phase rectifier topology, where the DC output voltage is common to all phases as e.g. for the Vienna Rectifier [1], or with a phase oriented approach. There, a star-connection (Y-Rectifier [2], [3] – cf. Fig. 1) or a delta-connection (Δ-Rectifier [4]) of single-phase, boost-type, PWM rectifiers with individual DC output voltages is possible.

The three-level structure of the Vienna Rectifier results in a low blocking voltage stress on the power semiconductors and low volume of the input inductors. This leads to highly compact and efficient rectifier systems. Similar properties are given for the Δ-Rectifier in case the line-to-line modules are realised with three-level single-phase rectifiers [5]. However, for a wide input voltage range of 320…480V$_{RMS,LL}$ the output voltage has to be set for both systems to 800V$_{DC}$. Accordingly, a DC/DC converter stage connected to the rectifier output typically has to be realised by two series connected DC-DC converters [6] in the case where 600V power semiconductor technology is employed.

In contrast, the Y-Rectifier (cf. Fig. 1) has the advantage of a low DC output voltage (400V) of the phase rectifier systems. Therefore, the DC-DC converters can be realised using 600V power MOSFETs and fast recovery diodes as known from single-phase off-line power supplies. Furthermore, the component count is relatively low resulting in a compact and cost effective solution. However, to convert the phase rectifier output voltages $V_{DC,i}$ e.g. into 48V, three independent isolated DC-DC converters, connected in parallel on the secondary side, are required.

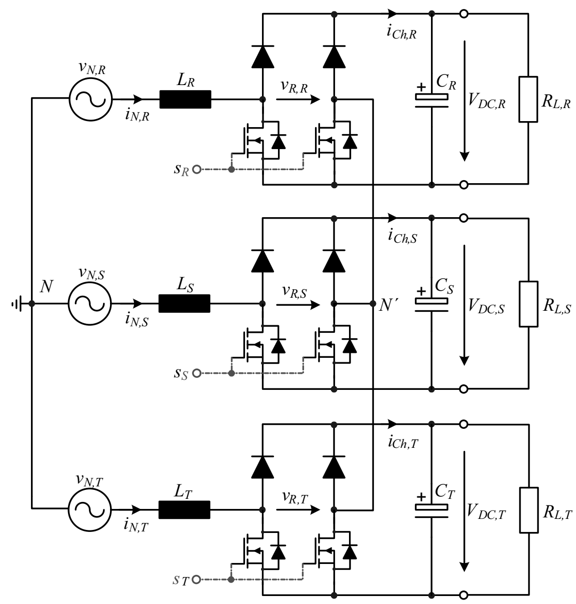

Figure 1. Schematic of the power circuit of the three-phase Y-Rectifier. The switches of a phase are gated simultaneously, i.e. only a single switching signal s_i is employed per phase. The DC-DC converter stages connected to the DC output voltages $V_{DC,i}$ have been replaced by equivalent load resistors $R_{L,i}$.

For ideal conditions the voltages $V_{DC,i}$ show equal values. In practice, however, a balancing control is required accounting for non-idealities like mains phase voltage asymmetries, differences of the losses of the rectifier and DC/DC converter stages and/or for different output currents in case independent loads are supplied from each rectifier output.

In [3] a concept for balancing the phase rectifier systems by measuring the voltage between the mains star point N and the virtual star point N' and correspondingly adjusting the power flow through each DC-DC converter has been proposed. In case of a phase loss the rectifier system and the measuring circuit of the missing phase must be disconnected for a stable operation [7], what represents a significant disadvantage.

Another approach based on transformers to form an artificial star point connected to N' and on a "Current Balancing Unit" to control the fundamental component of the zero sequence current flowing into N' is presented in [8]. There, the transformers must be built for approximately 5% of the rated system power and this increases the system volume by about

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10% and increases the system costs.

The approach presented in [3] balances the phase rectifier systems by individually adjusting the power flow taken by the DC/DC converter stages. In [7], [9] a concept is proposed which directly controls the DC link voltages $V_{DC,i}$ instead of the potential of N' by influencing the mains side power flow of the phases. In contrast to [3] this approach is independent of the load supplied from the DC links and no additional components are required.

However, the concept [7], [9] is of relatively high complexity due to the coupling of the three phase rectifier systems resulting from the open star point N'. Therefore, a novel concept for balancing the DC output voltages is presented in this paper [10]. There, always only two out of the three DC voltages $V_{DC,i}$ are balanced at the same time, which avoids the coupling phenomena. The selected DC link voltages are chosen cyclically depending on the magnitude of the corresponding instantaneous mains phase voltages so that each voltage $V_{DC,i}$ is controlled for two-thirds of a mains period. The proposed concept is confirmed through simulations and experiments on a 3kW laboratory system and this shows that the Y-Rectifier is a highly interesting alternative to the Vienna Rectifier for high-power telecommunications power supply modules.

In the following, basic considerations regarding space vector modulation and switching states of the Y-Rectifier are given in **Section II**. The proposed control method for balancing the DC link voltages is described in **Section III**. Thereafter, the theoretical limits for asymmetric loading of the DC output voltages are calculated in **Section IV**. The theoretical results are verified by measurement in **Section V**.

II. Space vector modulation

For calculating the input inductor current of the single-phase rectifier, the Y-Rectifier AC side equivalent circuit shown in Fig. 2(a) is considered. There, the voltage sources $v_{R,i}$ are the rectifier input phase voltages, which depend on the sign of the corresponding phase current $i_{N,i}$ and on the switching state s_i of the power transistors. The 3 phase voltage system $v_{R,i}$ could be decomposed into a zero sequence component

$$v_{R,0} = \frac{1}{3}\left(v_{R,R} + v_{R,S} + v_{R,T}\right) \tag{1}$$

and a current forming component

$$v'_{R,i} = v_{R,i} - v_{R,0}. \tag{2}$$

Since the star points N and N' are not connected, the sum of the three mains currents is forced to zero, $\sum i_{N,i} = 0$, and $v_{R,0}$ does not influence the phase currents. Therefore, the equivalent circuit could be redrawn as shown in Fig. 2(b) and the current in the boost inductors is defined by ($\underline{v}'_R = \underline{v}_R$)

$$L\frac{\underline{i}_N}{dt} = \underline{v}_N - \underline{v}_R, \tag{3}$$

where $\underline{v}_N$ is the space vector of the mains voltage

$$\underline{v}_N = \widehat{V}_N e^{j\varphi_N} \text{ with } \varphi_N = \omega_N t \tag{4}$$

($\underline{v}_R$ is the space vector of the rectifier input phase voltages and $\underline{i}_N$ denominates the boost inductor current space vector, cf. Fig. 1).

In order to obtain a sinusoidal mains current with amplitude $\widehat{I}^*_N$, which is in phase with the input voltage (resistive mains behaviour),

$$\underline{i}^*_N = \widehat{I}^*_N \frac{\underline{v}_N}{\widehat{V}_N}, \tag{5}$$

ideally a rectifier input voltage space vector

$$\underline{v}^*_R = \underline{v}_N - j\omega_N L \underline{i}^*_N \tag{6}$$

would be required (cf. Fig. 3), and/or a fundamental voltage space vector $\underline{v}_{R(1)} = \underline{v}^*_R$ has to be generated in the time average over a switching period T_P.

In a three phase rectifier system as shown in Fig. 1 each rectifier phase voltage $v_{R,i}$ could basically assume three values: $+\frac{V_o}{2}$, 0 and $-\frac{V_o}{2}$. This would result in $3^3 = 27$ possible states/space vectors. However, the formation of $v_{R,i}$ also depends on the sign of the corresponding phase current

$$v_{R,i} = \begin{cases} 0 & \text{if } s_i = 1 \\ \text{sign}\{i_{N,i}\}\frac{V_o}{2} & \text{if } s_i = 0 \end{cases} \tag{7}$$

since the current flow is via the diodes if the switches of phase i are in the turn-off state (cf. Fig. 1, $s_i = 1$ denominates the turn-on state of the power transistors). Consequently, for a given phase current sign the rectifier stage could switch the input only between 0 and $+\frac{V_o}{2}$ if $i_{N,i} > 0$ or between 0

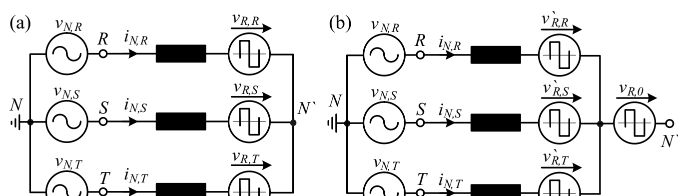

Figure 2. AC side equivalent circuit of the Y-Rectifier (a) shown in Fig. 1 with decomposition of the rectifier phase voltages into a zero sequence component $v_{R,0}$ and a current forming component $v'_{R,i}$ (b).

Table I
Rectifier input voltage space vectors for phase currents $i_{N,R} > 0, i_{N,S} < 0$ and $i_{N,T} < 0$; $(s_R s_S s_T)$ denominates the rectifier switching state, where $s_i = 1$ indicates the turn-on state of the power transistors of phase i; $\underline{a} = e^{j\,2\pi/3}$.

State	Space Vector	Magnitude
(111)	0	0
(110)	$\frac{2}{3}\left(-\underline{a}^2\frac{V_o}{2}\right)$	$\frac{V_o}{6}\left(1+\sqrt{3}\right)$
(101)	$\frac{2}{3}\left(-\underline{a}\frac{V_o}{2}\right)$	$\frac{V_o}{6}\left(1-\sqrt{3}\right)$
(011)	$\frac{2}{3}\frac{V_o}{2}$	$\frac{V_o}{3}$
(100)	$\frac{2}{3}\frac{V_o}{2}\left(-\underline{a}-\underline{a}^2\right)$	$\frac{V_o}{3}$
(010)	$\frac{2}{3}\frac{V_o}{2}\left(1-\underline{a}^2\right)$	$\frac{V_o}{6}\left(1.5+\sqrt{3}\right)$
(001)	$\frac{2}{3}\frac{V_o}{2}\left(1-\underline{a}\right)$	$\frac{V_o}{6}\left(1.5-\sqrt{3}\right)$
(000)	$\frac{2}{3}\frac{V_o}{2}\left(1-\underline{a}-\underline{a}^2\right)$	$\frac{2V_o}{3}$

and $-\frac{V_o}{2}$ if $i_{N,i} < 0$. Therefore, there are only $2^3 = 8$ combinations for each set of phase current signs. This is shown in Fig. 3 where all eight rectifier input voltage space vectors are shown for the phase current set $i_{N,R} > 0, i_{N,S} < 0$ and $i_{N,T} < 0$. These vectors are defining a hexagon which rotates in 60 degree steps counter-clock wise for the six possible combinations of phase current signs (cf. dashed hexagon in Fig. 3).

In order to minimise the current harmonics only space vectors lying in the immediate vicinity of the reference vector $\underline{v}_{R(1)}$ are applied for generating $\underline{v}_R^* = \underline{v}_{R(1)}$ in the pulse period time average. For the position of $\underline{v}_{R(1)}$ shown in Fig. 3 these would be the vectors (100)/(011), (010) and (000) defining the grey shaded subtriangle. The reference vector is formed by geometrically adding the rectifier voltage space vectors

$$\underline{v}_R^* = \underline{v}_{R(1)} = \delta_{(100)}\underline{v}_{R(100)} + \delta_{(000)}\underline{v}_{R(000)} + \delta_{(010)}\underline{v}_{R(010)} + \delta_{(011)}\underline{v}_{R(011)} \qquad (8)$$

weighted by the relative on-times δ_j of the switching states $j = (s_R, s_S, s_T)$. These on-times can be calculated from simple geometrical considerations [7], [11] and are a function of the angle of $\underline{v}_R^*$ and of the magnitude $|\underline{v}_R^*| = \widehat{V}_{R(1)}$ of the reference vector and/or of the modulation index

$$M = \frac{\widehat{V}_{R(1)}}{V_{DC}}; \qquad M \in \left(0, \frac{2}{\sqrt{3}}\right). \qquad (9)$$

It is important to note that for the considered set of signs of the phase currents the two switching states (100) and (011)

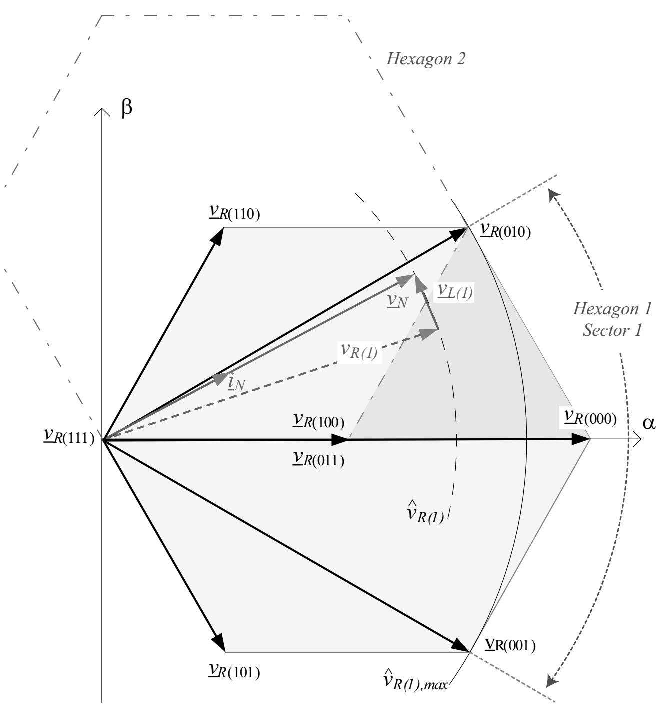

Figure 3. Y-Rectifier input voltage space vectors $\underline{v}_j$, $j = (s_R s_S s_T)$, for $\varphi \in \left(-\frac{\pi}{6}, +\frac{\pi}{6}\right)$ and/or $i_{N,R} > 0$, $i_{N,S} < 0$ and $i_{N,T} < 0$. Furthermore shown: trajectory of the input voltage reference space vector $\underline{v}_R^*$ and/or of the space vector $\underline{v}_{R(1)} = \underline{v}_R^*$ of the rectifier input voltage fundamentals, and space vector $\underline{v}_{L(1)}$ of the fundamentals of the inductor voltages. (Representation not to scale.)

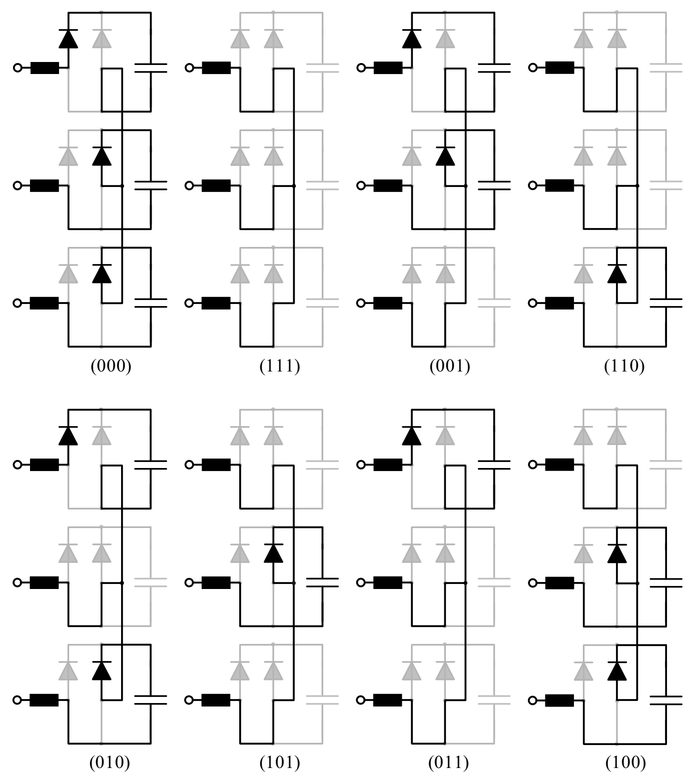

Figure 4. Conduction paths for different switching states $(s_R s_S s_T)$ for $\varphi \in \left(-\frac{\pi}{6}, +\frac{\pi}{6}\right)$ and/or $i_{N,R} > 0$, $i_{N,S} < 0$ and $i_{N,T} < 0$.

result in the same rectifier input voltage space vector as given in Table I if equal DC output voltages $V_{DC,i}$ of the three phase rectifier systems are assumed. Due to the missing connection between the N and N' the current of one phase is not only defined by the respective phase voltage but by all three phase voltages, i.e. by the space vectors $\underline{v}_R$ in combination with $\underline{v}_N$. Consequently, the states (100) and (011) are redundant and from the calculation of the relative on-times only the sum $\delta_{(100)} + \delta_{(011)}$ could be specified. The partitioning of $\delta_{(100)} + \delta_{(011)}$ between the two redundant states therefore represents a degree of freedom of the modulation.

The charging of the output capacitors, however, is directly influenced by the relative on-time partitioning. For $i_{N,R} > 0$, $i_{N,S} < 0$ and $i_{N,T} < 0$ the two capacitors of phases S and T are charged in case of (100) and the capacitor of phase R is bypassed. In contrast, for space vector (011) only the capacitor of phase R is charged and the capacitors of phases S and T are bypassed. Accordingly, in the other sectors different combinations of capacitors are charged and bypassed, so that a balancing of the charging of all three capacitors C_i is possible as will be shown in the following. Consequently, the degree of freedom of the modulation can be used for ensuring equal DC output voltages of all three phases.

Remark: The redundancy of the switching states regarding the rectifier voltage space vector generation is given only for exactly equal output voltages $V_{DC,i}$. This symmetry, which is assumed for the further considerations, is finally guaranteed by the system control (cf. Fig. 8).

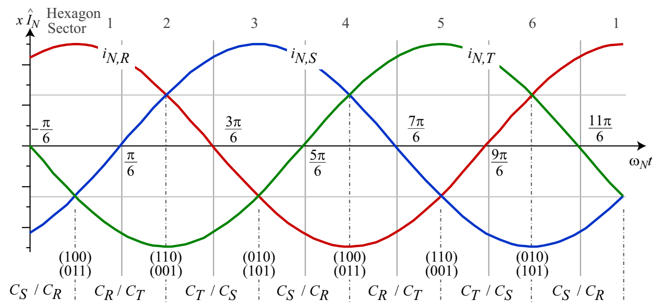

Figure 5. Idealised mains phase currents $i_{N,R}$, $i_{N,S}$ and $i_{N,T}$ (ripple component neglected) for one mains period. The mains period is partitioned into six sectors depending on the combination of the mains currents signs. In sector 1, for example, we have $i_{N,R} > 0$, $i_{N,S} < 0$, $i_{N,T} < 0$ and the rectifier input voltage space vectors $v_{R,j}$ are defining hexagon 1 (cf. Fig. 3). Furthermore given: output capacitors C_i which are mainly charged and redundant switching states.

III. 2 OUT OF 3 DC OUTPUT VOLTAGE BALANCING

In the previous section it has been shown that the current flowing into the output capacitors C_i can be balanced by shifting between redundant vectors. In Fig. 5 the ideal time behaviour of the three phase currents is shown for one mains period. In the interval $\varphi = \omega_N t \in (-\frac{\pi}{6}, \frac{\pi}{6})$ (cf. Fig. 3, ω_N denominates the angular mains frequency) we have $i_{N,R} > 0, i_{N,S} < 0$ and $i_{N,T} < 0$ and the respective rectifier voltage space vectors are defining hexagon 1.

In this interval the switching states (100) and (011) are redundant and it could be chosen between charging C_R or C_S, C_T as explained above (cf. Fig. 4). For the turn-off interval of the switches of phase i ($s_i = 0$) the capacitor charging current $i_{Ch,i}$ is equal to the absolute value of the respective phase current

$$i_{Ch_i} = (1 - s_i)|i_{N,i}|. \tag{10}$$

In case the switches are turned on ($s_i = 1$), the charging current is zero and the capacitor is discharged by the load current. The average of $i_{Ch,i}$ over one pulse period T_P will be denominated as $\bar{i}_{Ch,i}$.

Since in $\varphi \in (0, \frac{\pi}{6})$ the current $i_{N,S}$ in phase S is relatively small compared to the currents in phases R and T, mainly capacitor C_T is charged in case switching state (100) is applied. Thus, if the relative on-time $\delta_{(100)}$ of state (100) is increased and the relative on-time $\delta_{(011)}$ of (011) is correspondingly reduced, capacitor C_T is charged more than C_R. Accordingly, by varying the ratio

$$\rho_{R-T} = \frac{\delta_{(011)}}{\delta_{(100)} + \delta_{(011)}}, \tag{11}$$

i.e. by shifting the total relative on-time $\delta_{(100)} + \delta_{(011)}$ between the two redundant states, e.g. by selecting $\rho_{R-T} \to 0$ or $\rho_{R-T} \to 1$, the voltages $V_{DC,R}$ and $V_{DC,T}$ can be balanced and ρ_{R-T} can be used as an actuating control variable for the balancing of $V_{DC,R}$ and $V_{DC,T}$. The same is true for the voltages $V_{DC,R}$ and $V_{DC,S}$ in $\varphi \in (-\frac{\pi}{6}, 0)$ where $|i_{N,T}|$ is always smaller than $|i_{N,S}|$ and $i_{N,R}$.

Within $\varphi \in (\frac{\pi}{6}, \frac{3\pi}{6})$, where the space vectors are represented by hexagon 2, switching states (110) and (001) are redundant

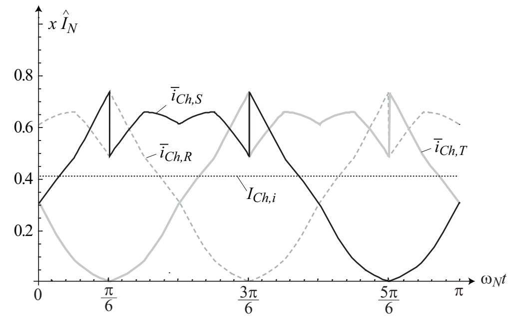

Figure 6. Charging current of the output capacitors C_i for equal partitioning of the on-time of the redundant switching states within each sector of the mains period. Assumed operating parameters: $\widehat{V}_N$ = 327V, $V_{DC,i}$ = 400V and/or M = 0.82 (compare: Fig. 10 & 11).

and one can choose between charging C_T or C_R, C_S. Again, one phase current is smaller in magnitude than the two others; first in $\varphi \in (\frac{\pi}{6}, \frac{2\pi}{6})$ we have $i_{N,S} < i_{N,R}, |i_{N,T}|$. Thus, by shifting ρ_{T-S} between 0 and 1,

$$\rho_{T-S} = \frac{\delta_{(110)}}{\delta_{(001)} + \delta_{(110)}}, \tag{12}$$

either capacitor C_T or capacitor C_R can be mainly charged and/or $V_{DC,T}$ and $V_{DC,R}$ can be balanced. In $\varphi \in (\frac{2\pi}{6}, \frac{3\pi}{6})$ the same is true for $V_{DC,T}$ and $V_{DC,S}$.

Within $\varphi \in (\frac{3\pi}{6}, \frac{5\pi}{6})$, we first have $|i_{N,R}| < |i_{N,T}|$ and then $|i_{N,T}| < |i_{N,R}|$. Accordingly, by varying the relative on-time of (101) and (010),

$$\rho_{S-R} = \frac{\delta_{(101)}}{\delta_{(010)} + \delta_{(101)}}, \tag{13}$$

the voltages $V_{DC,S}$ and $V_{DC,T}$/$V_{DC,R}$ can be balanced.

In case the ratios ρ_{R-T}, ρ_{T-S} and ρ_{S-R} are set to 0.5 within the respective angle intervals the charging currents of all three capacitors show equal average values over a mains period (cf. Fig. 6).

Consequently, it is possible to balance all three output voltages by always balancing two out of three voltages $V_{DC,i}$ within a $\frac{\pi}{3}$-wide interval. Due to the fact, that always one phase current is smaller than the two others, the control is largely decoupled and it is possible to determine the charing of two output capacitors without significantly affecting the third phase. This allows the implementation of a low complexity control method which will be explained in the following. A control considering all three output voltages simultaneously requires a complex consideration of the coupling of the phases and was analysed in [7].

A. Control implementation

With the method described in the previous section a balancing of the three output voltages could be achieved. A possible hardware implementation of the control concept is shown in Fig. 8. There, a common triangular carrier PWM is employed for synchronising the underlying mains current control loops.

On the left hand side the mean value $V_{DC,M}$ of the three output voltages is compared with the reference value V^*_{DC}. With the error signal ΔV_{DC} the amplitude $\widehat{I}^*_N$ of the phase

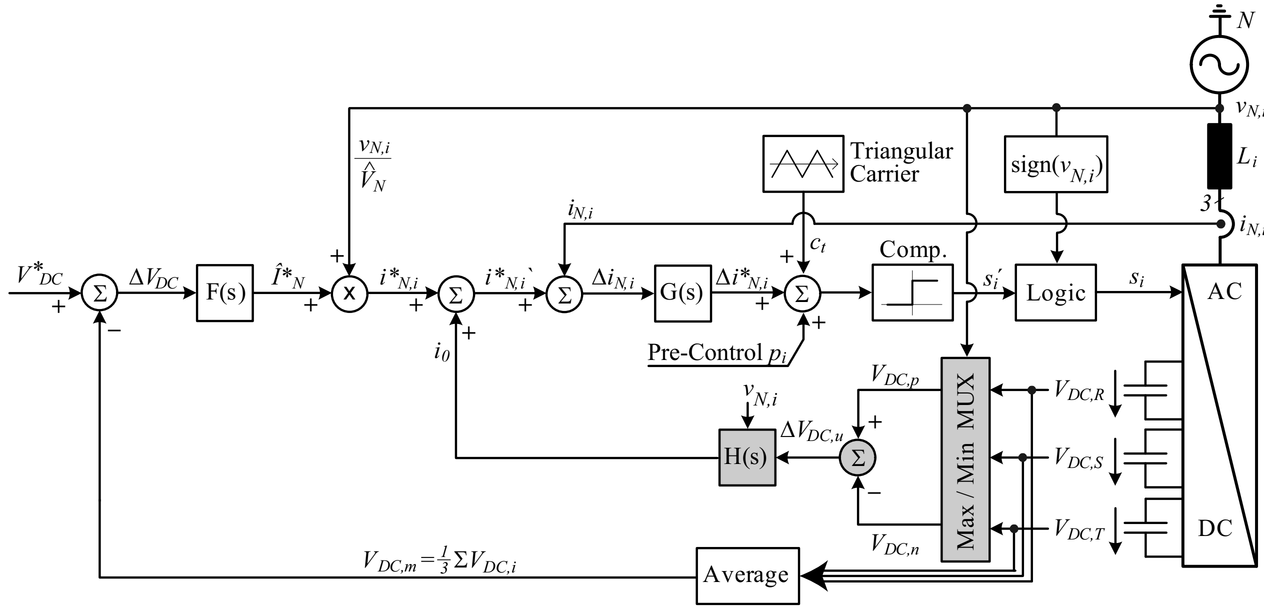

Figure 8. Basic structure of the Y-Rectifier control including the balancing of the DC output voltages of the phase rectifier systems via i_0.

current reference values $i^*_{N,i}$ is calculated. The amplitude $\widehat{I}^*_N$ is multiplied with the normalised mains voltages resulting in current reference values that are in phase with the respective mains phase voltages. Without the output voltage balancing (shaded in grey in Fig. 8) the reference value of each phase current is compared to the corresponding actual current $i_{N,i}$ and the error signal $\Delta i_{N,i}$ is generated. After adding the mains voltage pre-control signal p_i the switching signal is derived from intersection with the triangular carrier c_t. The pre-control signals p_i ensure a low control error also for employing only P-type phase current controllers $G(s)$ [11] and contain a zero sequence component m_3 (cf. (14)) with three times the mains frequency for extending the linear modulation range to $M \in (0, \frac{2}{\sqrt{3}})$ [11]. For purely sinusoidal pre-control $M \in (0, 1)$ would result.

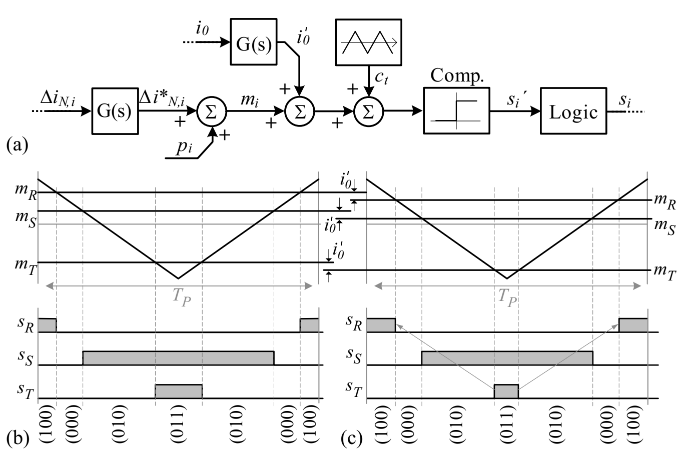

Figure 7. (a) Equivalent circuit of the control structure clearly showing the influence of the balancing signal i_0 on the modulation process. (b) & (c) Shift between the redundant switching states due to the addition of i_0' to the modulating functions m_i. The switching signals of phases S and T are inverted since $i_{N,S}, i_{N,T} < 0$ is given in the considered interval $\varphi \in (0, \frac{\pi}{6})$ [1], [11].

For balancing the DC output voltages $V_{DC,i}$ an additional control loop is added. In this loop the phases showing the most positive and the most negative phase voltage value are determined first. Then the output voltages of these two phases, $V_{DC,p}$ and $V_{DC,n}$, are subtracted resulting in the output voltage unbalance $\Delta V_{DC,u}$, which is the input of a PI-controller $H(s)$ that generates a zero sequence current i_0 at the output. This current is added to the current reference values $i^*_{N,i}$ of all three phases. Since star point N' of the rectifier system is not connected to the mains star point N, i_0 can not be set by the control but only shifts the partitioning the total relative on-time of the redundant switching states. This can be seen in Fig. 7, where a typical pulse pattern, derived from the intersection of modulating functions m_i and the triangular carrier c_t, is shown for a pulse period T_P assuming $\varphi \in (0, \frac{\pi}{6})$.

In Fig. 7(b) the on-times of the different switching states are shown for balanced DC output voltages, i.e. for $i_0 = 0$. In Fig. 7(c) the same situation is depicted for negative i_0. Due to $i_0 < 0$ all modulating functions are shifted downwards and this influences only the relative on-time of the switching states at the beginning and at the end of the pulse period, i.e. of (100) and (011) for the considered case. The on-times of the two remaining switching states (000) and (010) are not influenced as they only depend on the difference of the modulating signals but not on their absolute values. This is also true for the sum of the relative on-times of (100) and (011). As (100) and (011) are the redundant switching states, a zero sequence current i_0 results in a different charging of the output capacitors C_R and C_T and therefore provides a means for balancing the corresponding DC output voltages.

The time behaviour $i_{0,m}$ of i_0 ensuring equal output volt-

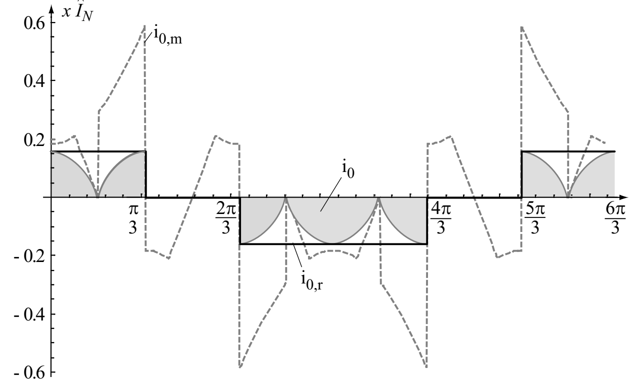

Figure 9. Time behaviour of the balancing signal $i_{0,m}$ allowing the balancing of a maximum asymmetry of the phase loads, i.e. of $P_R = P_{\min,\text{II}}$ and $P_S = P_T = P_{\max,\text{II}}$ in the considered case. Furthermore shown: P-type balancing controller output $i_{0,r}$ and actual zero sequence signal i_0 employed for balancing.

ages in case of a theoretical maximum admissible asymmetry of the phase loads, i.e. in case the output power of phase module R is $P_R = P_{\min,\text{II}}$ and $P_S = P_T = P_{\max,\text{II}}$ (cf. section IV), is shown in Fig. 9. Basically, a scaled version of $i_{0,m}$ could be used for balancing the DC output voltages $V_{DC,i}$ in case of slightly different loads $P_{L,i}$. However, the shape of $i_{0,m}$ is complicated and difficult to implement and also varies with the type of load unbalance and the modulation index M.

If a simple P-type controller would be used for output voltage balancing, a slight unbalance of the output voltages would remain and the balancing signal i_0 would show a rectangular shape $i_{0,r}$ (cf. Fig. 9). As the comparison of $i_{0,m}$ and $i_{0,r}$ indicates, this, however, would lead to overmodulation at the phase current zero crossings and/or at the beginning and at the end of each $\frac{\pi}{3}$-wide sector of the mains period (cf. Fig. 5). Therefore, $i_{0,r}$ has to be modified by multiplication with a signal showing the same zero crossings as $i_{0,m}$. Such signal could be generated as absolute value of

$$m_3 = \frac{1}{2}[\max\{v_{N,i}\} - \min\{v_{N,i}\}], \tag{14}$$

which also is employed in the mains voltage pre-control p_i. (Furthermore, the zero crossings of m_3 are used for determining the boundaries of sectors 1-6, cf. Fig. 5). The resulting actual balancing control signal $i_0 = |m_3| i_{0,r}$ is depicted in Fig. 9 and is highlighted with grey shading.

IV. Theoretical Limits of Load Asymmetries

In section III a concept for balancing the output voltages of the phase rectifier systems has been introduced. Since the balancing is based on the partitioning of the on-times of the redundant switching states, there is a limit for the admissible asymmetry of loading. This limit corresponds to the case where only one of the redundant states is employed in a pulse period. Under this conditions it is still possible to maintain sinusoidal mains currents. Increasing the asymmetry would lead to unbalanced output voltages and mains current distortion.

For calculating the maximal admissible asymmetry of loading, which is equal to the asymmetry in the output powers $P_{L,i}$, the equations for the power flowing to the output capacitors are required. If an approximately constant output voltage is assumed the power $P_{L,i}$ could be calculated by multiplying the currents $i_{Ch,i}$ charging the three output capacitor C_i by the output voltage $V_{DC,i}$. Thus, for determining the maximal admissible load asymmetry, the maximal possible asymmetry of the charging currents must be calculated.

The local average $\bar{i}_{Ch,i}$ of the charging currents $i_{Ch,i}$ can be determined if the relative on-times α_i of the switches are known, since the charging currents are equal to the corresponding mains current in case the switches are turned off,

$$\bar{i}_{Ch,i} = (1 - \alpha_i) i_{N,i}. \tag{15}$$

The on-times α_i can be calculated with (8) for a given reference space vector $\underline{v}_R^*$. For example in sector 1 and/or hexagon 1 we have a switching state sequence of

$$\begin{aligned} ...\big|_{t_\mu=0}(100) \rightarrow (000) \rightarrow (010) \rightarrow (011)\big|_{t_\mu=\frac{T_p}{2}} \\ \rightarrow (011) \rightarrow (010) \rightarrow (000) \rightarrow (100)\big|_{t_\mu=T_p}, \end{aligned}$$

accordingly we have

$$\begin{aligned} \alpha_R &= \delta_{(100)} \\ \alpha_S &= \delta_{(010)} + \delta_{(011)} \\ \alpha_T &= \delta_{(011)}. \end{aligned} \tag{16}$$

Consequently, for determining the charging currents $\bar{i}_{Ch,i}$ in each pulse period T_P the relative on-times $\delta_{(s_R s_S s_T)}$ of the voltage vectors in the vicinity of v_R^* must be calculated. Therefore, the equations for calculating $\delta_{(s_R s_S s_T)}$ must be set up for each sector/hexagon within a mains period (= 6 sectors). In case of the considered trajectory of $\underline{v}_R^*$ in Fig. 3 there are in addition 4 intervals per sector/hexagon. Consequently, there are 24 different space vector sequences and sets of equations for calculating $\delta_{(s_R s_S s_T)}$ and/or the relative on-times α_i.

The mathematical expressions for $\delta_{(s_R s_S s_T)}$ and α_i of the Y-Rectifier are equal to the equations resulting for the Vienna Rectifier (derived in appendix A of [11]), if the output voltage of the Vienna Rectifier is twice the output voltage of the Y-Rectifier. The reason for this is the fact that both rectifiers are generating the same voltage space vectors for the same switching state $(s_R s_S s_T)$.

Basically, there are two types of load asymmetry – Type I: Output R is loaded maximal ($P_R = P_{\max,\text{I}}$) and outputs S & T are carrying minimal load ($P_S = P_T = P_{\min,\text{I}}$); Type II: Minimum load on output R ($P_R = P_{\min,\text{II}}$) and maximum load on outputs S & T ($P_S = P_T = P_{\max,\text{II}}$). Both types of load asymmetry are analysed in the following.

A. Load asymmetry type I

Based on the procedure explained above the time behaviour of the local average $\bar{i}_{Ch,i}$ of the charging currents $i_{Ch,i}$ can be calculated for the case of employing only that redundant

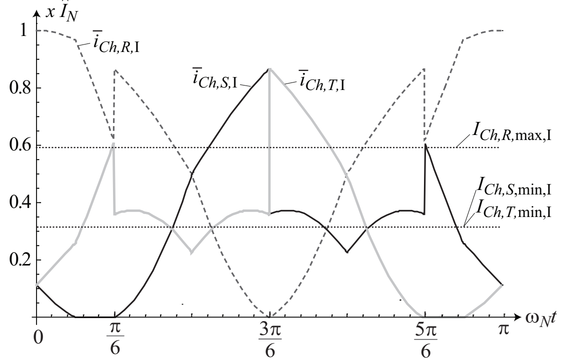

Figure 10. Time behaviour of the local average value $\bar{i}_{Ch,i}$ of the charging currents of the phase rectifier systems for maximum output power on phase R and minimum power supplied to the outputs of phases S and T (load asymmetry type I); $M = 0.82$.

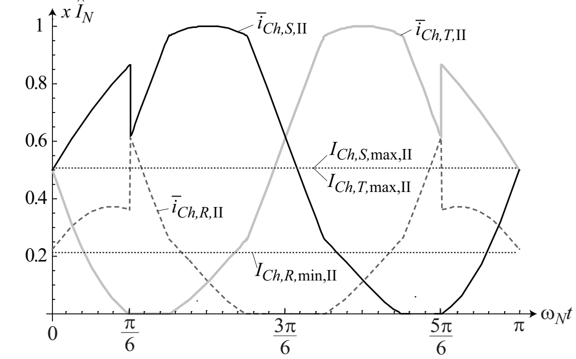

Figure 11. Time behaviour of the local average value $\bar{i}_{Ch,i}$ of the charging currents of the phase rectifier systems for maximum output power on phases S and T and minimum power supplied to the output of phase R (load asymmetry type II); $M = 0.82$.

switching state which (mainly) charges output C_R and bypasses capacitors C_S,C_T within each pulse period (cf. Fig. 10). The resulting global average values $I_{Ch,i}$ over a mains period are also shown in Fig. 10 and it can be seen that $I_{Ch,R}$ is significantly larger than $I_{Ch,S} = I_{Ch,T}$. Accordingly, higher power is supplied to the output of phase R.

The global average value of the charging currents $I_{Ch,i}$ for asymmetry type I are dependent on the modulation index M and can be calculated as

$$I_{Ch,R,\max,\mathrm{I}} = \frac{\widehat{I}_N}{12M\pi}\left(-2\sqrt{3} + 6\left(2 + \sqrt{3 - \frac{1}{M^2}}\right)M - 3\sqrt{3}M^2 + 18M^2 \arcsin\frac{1}{\sqrt{3}M}\right) \quad (17)$$

$$I_{Ch,S,\min,\mathrm{I}} = I_{Ch,T,\min,\mathrm{I}} = \frac{\widehat{I}_N}{24M\pi}\left(2\sqrt{3} - 6\left(2 + \sqrt{3 - \frac{1}{M^2}}\right)M + 3M^2\left(\sqrt{3} + 6\pi\right) - 18M^2 \arcsin\frac{1}{\sqrt{3}M}\right). \quad (18)$$

These equations are valid for $M \in \left(\frac{2}{3}, \frac{2}{\sqrt{3}}\right)$ and/or for the upper modulation range which is especially interesting for a practical realisation since for example typically an output voltage of $V_{DC,i} = 400\mathrm{V}$ is selected for a mains voltage amplitude of $\widehat{v}_{N,i} = 325\mathrm{V}$.

In Fig. 12(a) the charging currents $I_{Ch,i}$ in case of type I load asymmetry are shown in dependence of the modulation index M. The difference between the upper and the lower curve determines the difference in the average power flowing to capacitor C_R and capacitors C_S,C_T and/or to the load resistors $R_{L,R}$ and $R_{L,S}$,$R_{L,T}$.

B. Load asymmetry type II

The local time average $\bar{i}_{Ch,i}$ of the charging currents for load asymmetry type II, where the outputs of phases S and T are carrying maximum load and the output of phase R supplies minimum power, is shown in Fig. 11. Furthermore,

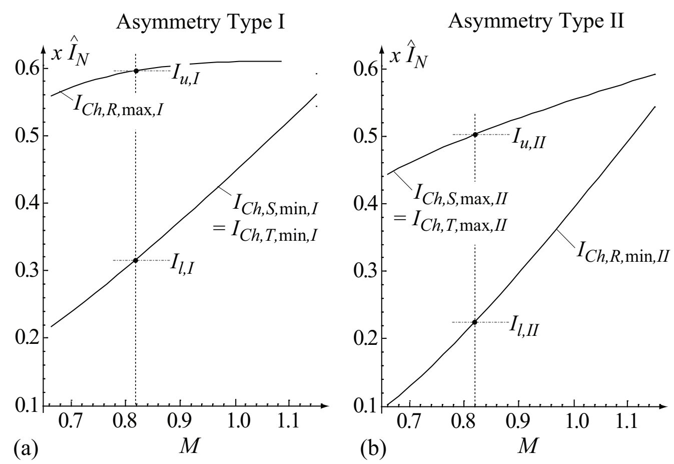

Figure 12. Dependency of the global average charging currents $I_{Ch,i}$ on the modulation index M for load asymmetry type I (a) and type II (b) corresponding to (17), (18), and (19), (20). The currents $I_{u,I}$, $I_{l,I}$, $I_{u,II}$ and $I_{l,II}$ are related to Fig. 10 and Fig. 11 ($M = 0.82$).

the currents $I_{Ch,i}$ averaged over a mains period are depicted there.

The corresponding value of the global average charging currents $I_{Ch,i}$ for load asymmetry type II can be calculated as

$$I_{Ch,S,\max,\mathrm{II}} = I_{Ch,T,\max,\mathrm{II}} = \frac{\widehat{I}_N}{24M\pi}\left(-2\sqrt{3} + 6\left(2 + \sqrt{3 - \frac{1}{M^2}}\right)M - 3M^2\left(\sqrt{3} - 2\pi\right) + 18M^2 \arcsin\frac{1}{\sqrt{3}M}\right) \quad (19)$$

$$I_{Ch,R,\min,\mathrm{II}} = \frac{\widehat{I}_N}{12M\pi}\left(2\sqrt{3} - 12M - 6\sqrt{3 - \frac{1}{M^2}}M + 3\left(\sqrt{3} + \pi\right)M^2 + 18M^2 \arcsin\frac{1}{\sqrt{3}M}\right). \quad (20)$$

The dependency of $I_{Ch,S,\max,\mathrm{II}} = I_{Ch,T,\max,\mathrm{II}}$ and $I_{Ch,R,\min,\mathrm{II}}$ on M is shown in Fig. 12(b).

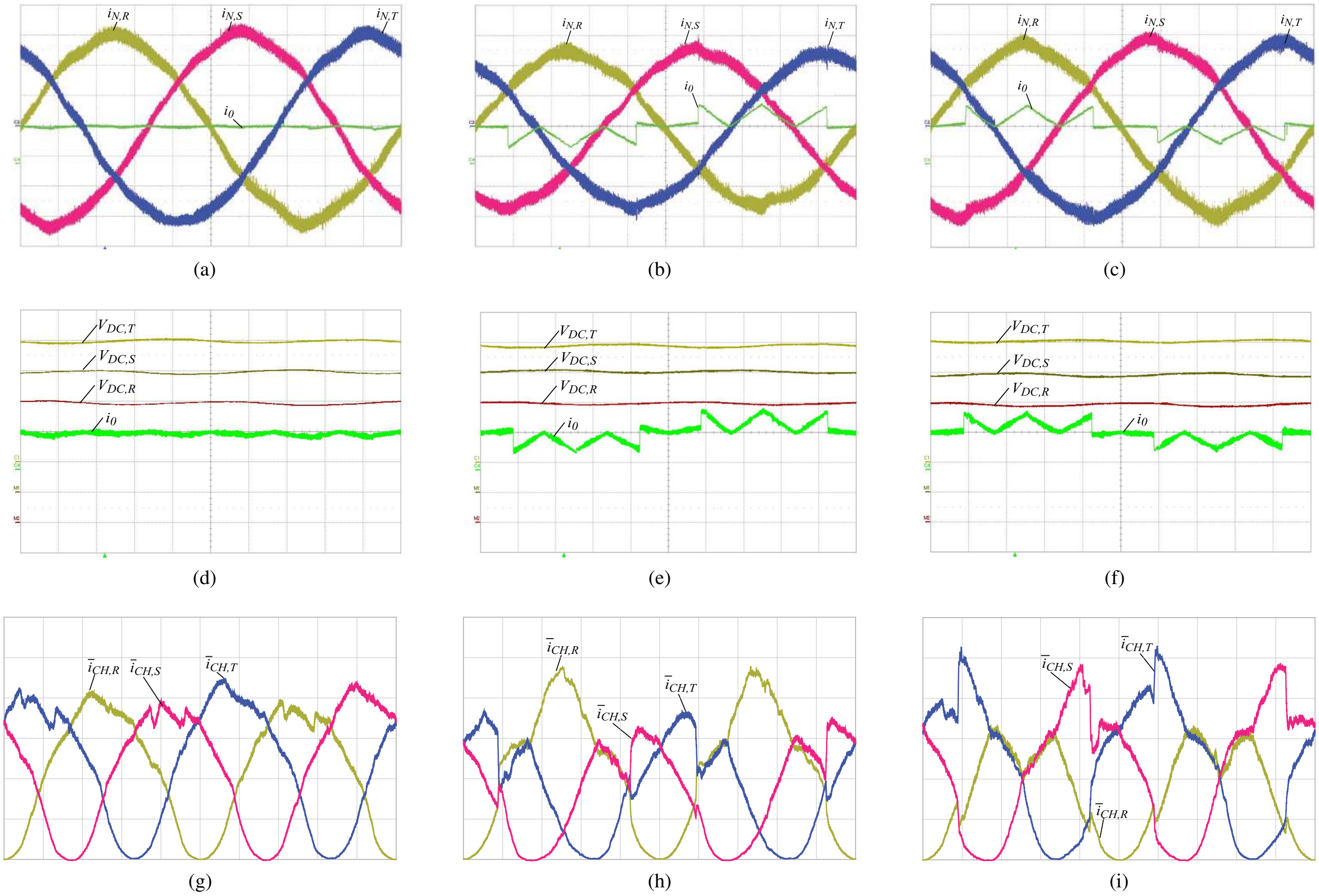

Figure 13. Measurement results for the prototype shown in Fig. 14: *First row*: mains phase currents and balancing control signal i_0. *Second row*: DC output voltages and i_0. *Third row*: local average charging currents $\widehat{i}_{Ch,i}$. Operating parameters: (a), (d), (g), symmetric load ($P_{L,i} \approx 1000$W, $R_{L,i} = 160\Omega$); (b), (e), (h), asymmetric load type I ($P_{L,R} = 1013$W, $P_{L,S} = 731$W and $P_{L,T} = 728$W, $R_{L,R}$=150Ω / $R_{L,S}$=$R_{L,T}$=220Ω); (c), (f), (i), asymmetric load type II ($P_{L,R} = 732$W, $P_{L,S} = 1013$W and $P_{L,T} = 1002$W, $R_{L,R}$=220Ω / $R_{L,S}$=$R_{L,T}$=150Ω). Scales: first row: 2A/div, second row: 100V/div, third row: 1A/div, time: 2ms/div.

V. Measurement results

In order to verify the proposed control concept a 3×1kW Y-Rectifier prototype has been built (cf. Fig. 14) with the specifications given in Table III.

In Fig. 15 the mains phase voltages and in Fig. 13 the mains phase currents $i_{N,i}$ for symmetric load and for load asymmetry type I and II are shown in the first row. The currents $i_{N,i}$ are sinusoidal (proportional to the corresponding mains phase voltages $v_{N,i}$) in case of symmetric load and also in case of asymmetric loading. The second row shows the output voltages $V_{DC,i}$, which are well balanced in any case (note: different reference level), and the balancing current i_0.

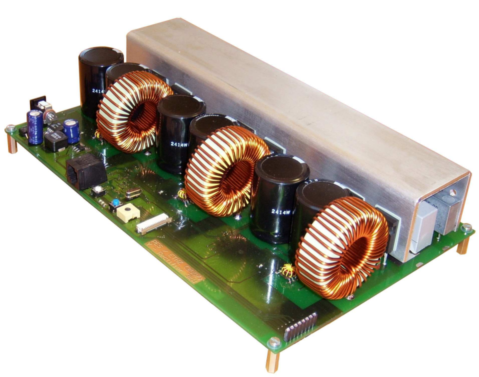

Figure 14. Photo of the 3×1kW prototype of the Y-Rectifier.

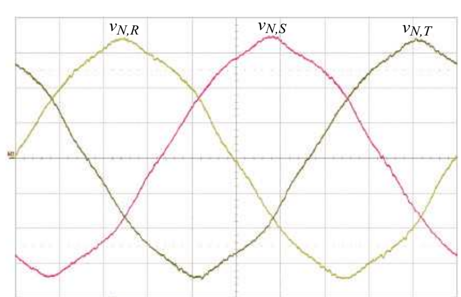

Figure 15. Mains phase voltages for the measurements shown in Fig. 13; scales:(100V/div, 2ms/div).

Numerical results are given in Table II where also the output power levels $P_{L,i}$ are included.

In the third row the local average charging currents $\bar{i}_{Ch,i}$ are depicted which show slightly asymmetric waveforms due to the distorted mains voltage (cf. Fig. 15).

Table II
OUTPUT POWER $P_{L,i}$ AND DC VOLTAGE $V_{DC,i}$ VALUES OF THE PHASES FOR SYMMETRIC LOADING OF THE PHASES AND LOAD ASYMMETRY TYPE I AND II.

	Phase	Symmetric	Type I	Type II
Output Power	R	1005W	1013W	732W
	S	1004W	731W	1013W
	T	1006W	728W	1002W
Output Voltage	R	396V	387V	403V
	S	396V	402V	391V
	T	396V	398V	393V

Table III
SPECIFICATION OF THE RECTIFIER SYSTEM SHOWN IN FIG. 1 WHERE COOLMOS SPW47N60C3 AND DIODES ISL9K3060G3 ARE APPLIED.

Input voltage	200-240V
Switching frequency	58kHz
Output voltage	400V
Output current	2.5A
Output power	3×1kW
Input inductor	2.8mH
Capacitors C_i	660μF
Maximum ambient temp.	40°C

Table IV
THEORETICAL LIMIT OF THE MAXIMAL LOAD ASYMMETRIES TYPE I AND II FOR $V_{DC,i} = 400$, $M = 0.82$, $\hat{I}_N = 20.4$A AND A TOTAL OUTPUT POWER OF $\sum P_{L,i} = 10$KW.

Type I: $R_{L,R}$ = 33Ω and $R_{L,S} = R_{L,T}$ = 62Ω	
$P_{L,R,\max,\mathrm{I}}$	4850W
$P_{L,S,\min,\mathrm{I}}$=$P_{L,T,\min,\mathrm{I}}$	2580W
Type II: $R_{L,R}$ = 88Ω and $R_{L,S} = R_{L,T}$ = 39Ω	
$P_{L,R,\min,\mathrm{II}}$	1820W
$P_{L,S,\max,\mathrm{II}}$=$P_{L,T,\max,\mathrm{II}}$	4100W

VI. CONCLUSION

In this paper a new control scheme for balancing the three individual DC output voltages of a three-phase Y-Rectifier has been proposed. The balancing control is based on redundant switching states, which result in equal rectifier input voltage formation but different power flow to the phase outputs. For example, in a 10kW system approximately 5kW could be supplied by one phase output and 2.5kW by each of the two other phase outputs without impairing the symmetric and purely sinusoidal mains currents shape. Alternatively, two phases could be loaded with approximately 4.1kW and the third phase could supply 1.8kW (cf. Table IV). The control concept is verified by measurements on a 3kW prototype and shows a low realisation effort. In combination with the low number of power semiconductors employed in the power circuit, this makes the Y-Rectifier a highly interesting candidate for the realisation of high power telecommunication rectifier modules, and competitive to the Vienna Rectifier.

In the course of further research the maximum admissible phase load asymmetry in case of unbalanced mains voltages will be analysed and the balancing scheme will be extended to phase loss (two-phase) operation.

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