

Double-Stage Gate Drive Circuit for Parallel Connected IGBT Modules

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Abstract—In more and more pulsed power applications solid state modulators are applied. There, often IGBT modules must be connected in parallel due to their limited power handling capability. For balancing the currents in the IGBTs a control method adapting the gate signal of the single IGBTs has been presented in a previous paper.

Besides the current balancing also the fall and rise times of the voltages/currents are crucial as they significantly influence the pulse shape and the modulator efficiency. For reducing the rise time of the pulse without increasing the maximal over-voltage of the IGBT a double-stage gate driver for parallel connected IGBTs is presented in this paper. In this gate driver also protection circuits for avoiding over-voltages as well as over-currents are included and an improved current balancing method is incorporated. Finally, measurement results revealing the dependency of the rise time/turn off losses on the design parameters of the gate drive are presented.

I. INTRODUCTION

In more and more pulsed power applications solid state modulators are applied. There, often IGBT modules must be connected in parallel due to the limited power handling capability of semiconductor switches. For balancing the currents in the IGBTs a special gate drive has been proposed in [3], which measures the IGBT currents and adapts the gate signals accordingly.

Besides the current balancing also the fall and rise times are crucial as they significantly influence the achievable parameters of the output pulse, which must be within the specifications of the application, and the switching losses and therewith the modulator efficiency.

With conventional gate drive circuits (single-stage driver) the switching losses of the IGBT modules are mainly generated during turn off, because the turn off time could not be decreased to the minimal achievable value due to the over-voltage caused by the parasitic inductances in the commutation path [1]. Therefore, a large value for the gate resistor during turn off has to be utilized for decreasing the current slope, which limits the resulting over-voltage [4], [5]. This results in turn off losses being significantly larger than the minimal achievable.

For reducing the turn off time and therewith the switching losses without increasing the over-voltage, multistage driver concepts [1], [2], [6], [7], which vary the value of the turn off gate resistor during the turn off transient, have been proposed for smaller IGBT devices. Based on this concept and results presented in [3] a new double-stage driver for parallel IGBTs for a 20MW 5μs solid state power modulator as depicted in Fig 1 is presented in the following.

To ensure safe operation of the IGBT modules also collector-emitter-voltage monitoring and protection circuits to avoid over-voltage as well as over-current are included in this gate driver. The monitored IGBT voltages v_{ce} are also used to improve the synchrony of the switching transients. This results in an improved current and voltage balancing between the parallel connected IGBT modules compared to the control method presented in [3].

The basic operating principle and the block diagram of the proposed double-stage driver are explained in **Section II**. Thereafter,

DC Link Voltage V_{DC}	1000V
Output Voltage V_{out}	200kV
Pulse Duration T_{pulse}	5μs
Output Power P_{out}	20MW
Repetition Frequency f_{rep}	200Hz
Turns ratio	1:200

Table I: Specification of the 20MW pulse modulator with four parallel connected IGBT modules.

the additionally implemented over-voltage and over-current protection circuit as well as the combination of the gate driver with an improved zener clamping circuit are presented in **Section III**. There, also the current balancing by means of the voltage edges is discussed. In **Section IV** experimental results for the double-stage gate drive and the dependency of the rise time and the turn off losses on the gate resistor are presented. Furthermore, the minimal achievable rise time/turn off losses for the single stage, for the double-stage and for the two stage combined with zener clamping are evaluated for the modulator system shown in Fig. 1.

II. MULTI-STAGE DRIVER

In many solid state pulsed power systems fast rise/fall times are required by the application. Furthermore, the switching losses are reduced by fast switching transients. Consequently, powerful low resistive/inductive gate drives turning the semiconductors fast on/off are required.

At turn on the falling time/switching losses can be minimized by decreasing the external gate resistor. However, at turn off a high switching speed with high $\frac{dv_{ce}}{dt}$ and high $\frac{di_c}{dt}$ would result in large over-voltages v_{ov} due to the parasitic inductance L_s of the commutation path (cf. Fig. 1a).

$$v_{ov} \sim L_s \frac{di_c}{dt} \quad (1)$$

The over-voltage v_{ov} could be reduced by minimizing the stray inductance L_s of the commutation path, i.e. the series inductance of the input capacitor, the bus bar, and the power module. However, in the existing system the total inductance is already smaller than 40nH and is mainly determined by the components, which can not be influenced by the system designer. Alternatively, the current slope $\frac{di_c}{dt}$ could be decreased with a larger gate resistor (cf. Miller-effect), what results in higher turn off losses E_{off} [5] due to the slower turn off transient.

To avoid the limitation of the $\frac{di_c}{dt}$ due to the over-voltage, double-stage drivers for IGBT modules have been proposed [1], [2], [4], [7]. By utilising more than two stages a further refinement of the turn off control is possible [6]. In the following the operation principle of proposed double-stage driver for high power modules is explained.

A. Operation Principle

Generally, multi-stage driver split the turn off transient in different successive switching sections and apply different gate resistors for

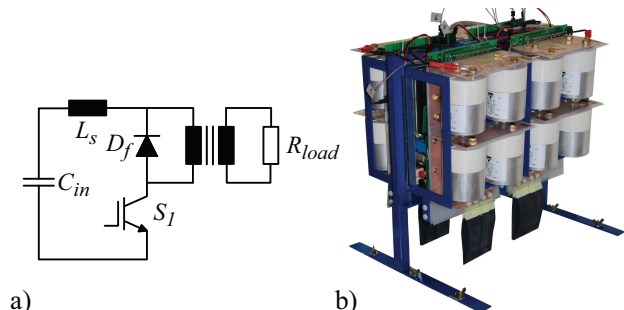


Figure 1: a) Schematic of the solid state pulsed power system. b) 20MW 5μs solid state pulse modulator with four parallel connected IGBT modules.

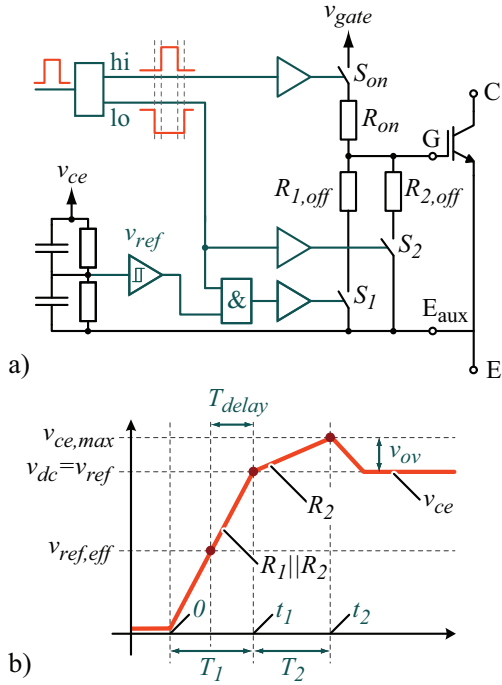


Figure 2: a) Block diagram of the double stage driver circuit and b) resulting voltage and current waveform of v_{ce} and i_c during double-stage turn off.

controlling the rate of gate discharge / $\frac{dv_{ce}}{dt}$ depending on the IGBT voltage v_{ce} .

The proposed double-stage driver consists of a low and high resistive turn off stage splitting the switching operation in two different switching sections as depicted in Fig. 2.

In the first section, during T_1 , the IGBT voltage v_{ce} is below the reference voltage v_{ref} and the gate is quickly discharged to achieve a short turn off time and small switching losses. Consequently, both stages S_1 and S_2 are turned on during T_1 , what results in a turn off resistor $R_{off,1} || R_{off,2}$ (cf. Fig. 2). As soon as the IGBT voltage v_{ce} exceeds the specified voltage level v_{ref} at t_1 the low resistive stage S_1 is turn off and the gate will be discharged only through the high resistive stage S_2 with $R_{off,2}$ during T_2 . Due to the Miller capacitor, the change of the gate resistor from $R_{off,1} || R_{off,2}$ to $R_{off,2}$ results in a decreased current / voltage slope (cf. Fig. 2b)).

The reference voltage v_{ref} is usually set to a value close to the DC-link voltage v_{dc} for achieving a fast turn off as long as possible and for limiting the over-voltage. However, the reference level could be set to arbitrary values in principle. A lower voltage reference v_{ref} leads to lower over-voltage.

Due to the delays in the comparator and driver circuit T_{delay} the effective reference voltage $v_{ref,eff}$ has to be set below the DC-link voltage v_{dc} to achieve a change of the gate resistor at $v_{ce} \approx v_{dc}$. To minimize this effect, the signal delay T_{delay} has to be minimized to guarantee a stable performance for various operating conditions. In the proposed system the signal delay T_{delay} from detection to driver output of the implemented hardware is approximately 40ns.

The IGBT voltage v_{ce} is monitored with a balanced ohmic-capacitive voltage divider, where the overstepping of the reference voltage v_{ref} is detected with a high speed comparator. There, attention has to be paid to the layout to keep the signal disturbances on a minimum level. The reference voltage v_{ref} for the high speed comparator can be adjusted with a potentiometer to an arbitrary value. For more complex systems, where an adjustment also during operation is needed, the reference could be set with a DSP via a digital analog converter. With a fixed reference voltage the complexity of the signal logic for the double-stage driver can be kept low (cf. Fig. 2).

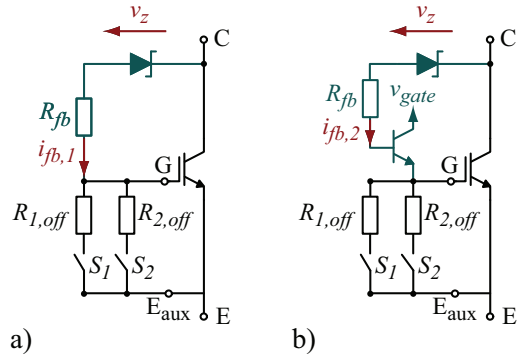


Figure 3: Implementation of a) the conventional zener clamping circuit and b) the improved zener clamping circuit.

III. PROTECTION CIRCUITS

In normal operation the double-stage driver ensures a limitation of the over-voltage to safe values. However, in fault conditions as over-current and the possibility of over-voltages, which comes along with the over-current, the IGBT modules must be protected by additional circuits. There, either passive snubber circuits [1], [10], [12], which generate high losses, or protection circuits which influence the gate voltage as for example zener clamping [1], [10], [11], [12] can be used. Therefore, the proposed double-stage gate-driver is extended by an over-voltage and an over-current protection.

A. Over-Voltage Protection

A well known and commonly applied overvoltage protection is the zener clamping, which directly influences the gate voltage. There, a high voltage or several series connected low voltage zener diodes are inserted between the collector and gate connections to realize a control loop as shown in Fig. 3a).

As soon as the IGBT voltage v_{ce} exceeds the zener voltage v_z , a current determined by the zener characteristic flows to the gate. This current recharges the gate capacitor or reduces the discharge rate of it depending on the value of the turn off resistor $R_{off,2}$. Additionally, to control the influence/value of the feedback current through the zener diodes usually a series resistor R_{fb} is inserted (cf. Fig. 3a)).

In the combination of the zener clamping with the double-stage driver, the current $i_{fb,1}$ flowing through the zener diodes can be limited to small values, due to the high resistance value of the gate driver during T_2 . Therefore, the power dissipation in the zener clamping circuit can considerably reduced compared to a conventional single-state driver with a small value for the turn-off resistor. To further reduce the feedback current $i_{fb,1}$ flowing through the zener clamping circuit a NPN bipolar transistor for current amplification is inserted as shown in Fig. 3b).

With the bipolar transistor, the losses of the zener clamping circuit can be reduced significantly, so that the losses become negligible. Therefore, the zener clamping circuit can also be applied for repetitive switching operation and is no longer limited to protection of the IGBT. By combining the double-stage driver and the improved zener clamping for normal operation it is possible to reduce the switching time as well as the switching losses for a given over-voltage. Furthermore, the zener voltage v_z is almost constant due to the low current $i_{fb,2}$ through the zener diodes. This allows a better prediction of the resulting over-voltage $v_{ce,max}$, so that the devices can be better utilised.

For a safe operation it must be guaranteed, that the double-stage driver changes to the high gate resistor value before a zener current i_{fb} is flowing, which starts when v_{ce} exceeds v_z . The zener clamping circuit with the appropriate series resistor R_{fb} will keep the over-voltage in any case below the maximum allowed over-voltage $v_{ce,max}$. To achieve a high $\frac{di}{dt}$ the over-voltage has to be clamped to the maximum allowable over-voltage $v_{ce,max}$ as long as possible.

B. Over-Current Protection

In the considered pulsed power application the required output power is so high that several IGBT modules must be connected in

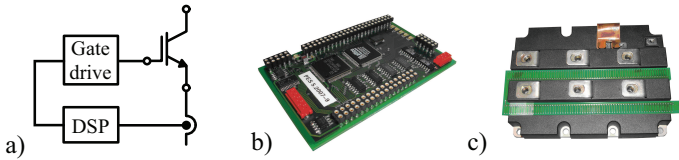


Figure 4: a) Over-current protection loop with b) the applied DSP-board and c) PCB Rogowski coil.

parallel. For balancing the IGBT currents the currents through the IGBTs are measured by Rogowski coils and the gate signals are adapted as presented in [3] (cf. Fig. 4) and shortly discussed in the next section. This simple and low cost measurement circuit is also utilized in the gate drive for over-current protection. In case of an over-current the IGBTs are turned off immediately and the over-voltage is limited by the gate drive as presented above.

This protection circuit has the advantage that the current is always monitored, i.e. also during the switching transients. Most of the circuits presented in literature as for example in [2], [8], [9] just monitor the IGBT current in a specific interval of the switching cycle. For example, circuits monitoring the desaturation of the IGBT can only detect over-currents during the interval, where the IGBT module is fully turned on, but not for example when the IGBT is turned on and the load has a short-circuit or is too high.

C. Current Balancing for Parallel Connected IGBTs

As already mentioned above several IGBT modules must be connected in parallel in the considered application because of the high output power. Due to IGBT tolerances, system asymmetries and variation in propagation delays a joint trigger signal for the parallel connected IGBT modules usually leads to an unbalanced current distribution between the modules. In [3] an active gate signal control was presented, where a balanced current distribution between the IGBT modules can be achieved by detecting the edge times of the currents in the IGBTs and to appropriately shift the turn on and off times of each IGBT for the next pulse. There, the IGBT currents are monitored by PCB Rogowski coils as shown in Fig. 4. With this method a good balancing of the currents could be achieved.

In order to improve the current balancing and the symmetrizing of the voltage edges further, additionally the IGBT voltages v_{ce} , which are monitored for over-voltage protection, are used to detect the edge times $t_{f,1} - t_{f,4}$ and $t_{r,1} - t_{r,4}$ (cf. Fig. 5) of the voltage. In combination with the times for the current edges, this enables to guarantee well balanced IGBT currents and synchronous switching of the parallel IGBTs.

IV. EXPERIMENTAL RESULTS

For testing the proposed double-stage gate drive the prototype shown in Fig. 6 has been built and measurements have been

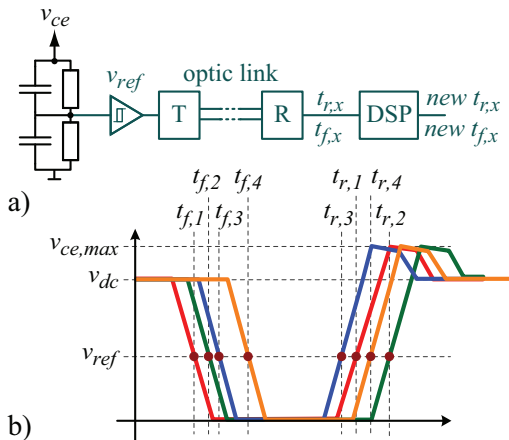


Figure 5: a) Signal processing and b) schematic of the v_{ce} edge detection for switching synchronisation.

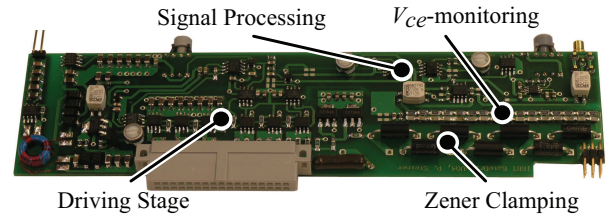


Figure 6: Prototype of the proposed multi-stage gate drive.

performed with $FZ2400R17KE3$ IGBT modules made by Eupec. There, pulse currents of $6000A$ per IGBT module at $1000V$ for $5\mu s$ were generated with the power modulator depicted in Fig. 1.

For comparing the different turn off strategies - single-stage, double-stage and double-stage in combination with zener clamping - measurements of the rise time and the turn off losses at a maximum over-voltage of $1200V$ have been performed. In Fig. 7 the results for t_{rise} of v_{ce} (10%-90%) and the turn off losses E_{off} of the double-stage driver for different turn off resistors R_1 and R_2 are given. Additionally, t_{rise} and E_{off} of the single-stage driver are shown.

As expected, a smaller turn off resistor $R_1||R_2$ in the first stage leads to a faster rise time t_{rise} of v_{ce} , which results in reduced turn off losses E_{off} . If the turn off resistance is reduced below $R_1||R_2 < 0.85\Omega$, the rise time t_{rise} is still decreasing, but the turn off losses E_{off} are increasing, since the voltage is increasing more rapidly than the current is falling resulting in high values $P_L = v_{ce}i_c$. To keep the maximum over-voltage below $1200V$ the resistance of the first stage of the double-stage driver must be $> 0.675\Omega$. Minimal turn off losses for the $FZ2400R17KE3$ IGBT module are achieved with $R_1||R_2 = 0.85\Omega$, where E_{off} is $2360mJ$ and t_{rise} is $516ns$.

With a single-stage driver a turn off resistance of 3.75Ω have to be used to keep the over-voltage below $1200V$. There, the measured turn off losses E_{off} are $4053mJ$ and the rise time is $1.548\mu s$. Therefore, with a double-stage driver the rise time t_{rise} and the turn off losses E_{off} can be reduced by $1.032\mu s$ (66%) respectively by $1693mJ$ (41%), which equals $340W$ per IGBT module at a pulse repetition time of $200Hz$.

The minimum achievable rise time t_{rise} of the double-stage is $444ns$ ($R_1||R_2 = 0.675\Omega$), however, the turn off losses E_{off} increase by $140mJ$ ($28W$ at $200Hz$) compared to the minimal losses.

To further improve the turn off time t_{rise} the double-stage driver has to be combined with the zener clamping circuit. There, the zener clamping voltage was set to $1100V$ and the series resistor R_{fb} has to be adjusted to keep the over-voltage below $1200V$ in order to have

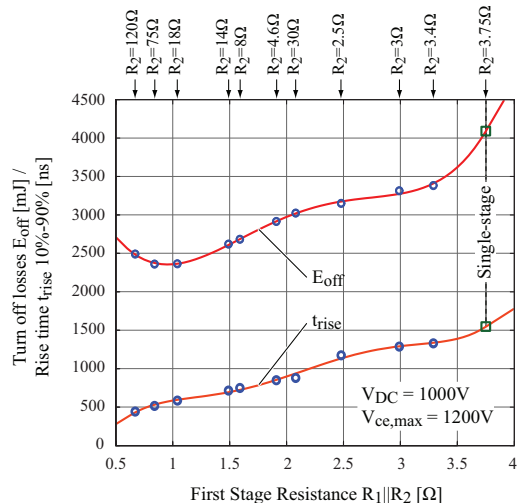


Figure 7: Turn off losses E_{off} and rise time t_{rise} of v_{ce} (10%-90%) of the double-stage driver for different R_1 and R_2 values and for the single-stage driver.

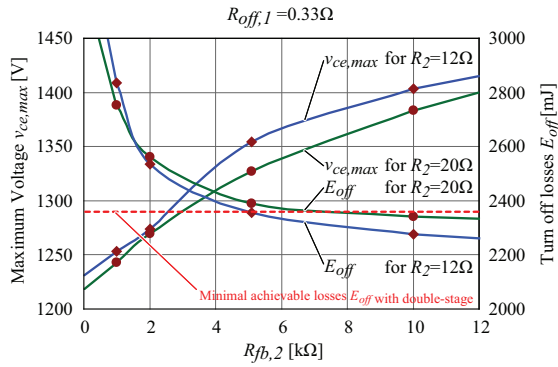


Figure 8: Turn off losses E_{off} and $v_{ce,max}$ of the improved zener clamping for different $R_{fb,2}$.

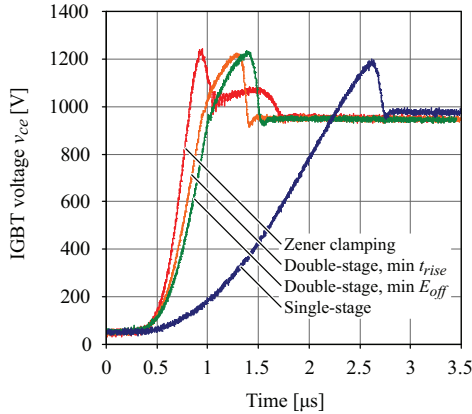


Figure 9: Voltage v_{ce} during turn off for i) single-stage driver, ii) double-stage driver with minimal turn off losses E_{off} , iii) double-stage driver with minimal rise time t_{rise} and iv) driver with combination of double-stage and zener clamping).

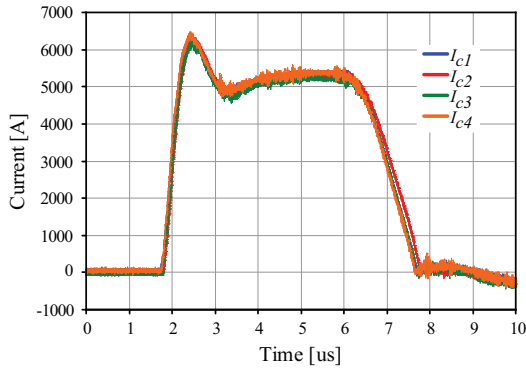


Figure 10: Current waveform of the four parallel connected IGBT modules.

a comparable utilization of the IGBTs for the three gate drives.

In Fig. 8 the turn off losses E_{off} and the resulting over-voltage $v_{ce,max}$ of the improved zener clamping with $V_z = 1100V$ and $R_{off,1} = 0.385\Omega$ for different series resistors R_{fb} are shown. There, the feedback current $i_{fb,2}$ reaches at maximum $160mA$ for $R_{fb,2} = 1k\Omega$ and decreases to $33mA$ for $R_{fb,2} = 10k\Omega$. Therefore, the voltage $v_{R_{fb,2}}$ is $160V$ respectively $330V$. For the improved zener clamping E_{off} is $2507mJ$, which is $147mJ$ ($30W$ at $200Hz$) higher than the minimal achievable losses with the double-stage driver. However, the rise time can be further reduced to $360ns$.

Due to the current amplification of the introduced bipolar transistor the peak power in the zener clamping circuit of $36500W$ for the conventional zener clamping can be reduced to maximum $200W$ for the improved zener clamping, which significantly lowers the stress of the zener diodes. Also the power losses of $7.2mJ$ ($1.44W$ at $200Hz$) in the diodes reduce to $46\mu J$ ($9.2mW$ at $200Hz$).

In Fig. 9 the voltage waveforms v_{ce} for the different turn off strategies are shown. There, the fastest rise time can be achieved with the combination of double-stage driver and zener clamping, which however results in larger turn off losses. The double-stage driver achieves the lowest turn off losses for a given over-voltage and is only slightly slower than the zener clamping.

Besides the switching transients also the current balancing has been tested. In Fig. 10 the resulting, well balanced currents of the active gate control for the four parallel connected IGBT modules are depicted.

V. CONCLUSION

In this paper a compact and cost efficient double-stage gate driver for parallel connected high power IGBT modules in power modulator systems is presented. Besides the current balancing the gate drive also includes an over-current and an over-voltage protection.

With the proposed gate drive a reduction of 66% in the turn off rise time and of 41% in the turn off losses compared to a single stage driver has been achieved. There, the maximal allowed collector emitter voltage was limited to $1200V$ for both drivers and a $FZ2400R17K E3$ IGBT module made by Eupec has been utilized. A further reduction of the rise time by 19% has been achieved by combining the double-stage gate drive with an improved zener clamping circuit. However, the turn off losses slightly increased by 6%.

REFERENCES

- [1] B. Weis and M. Bruckmann, "A New Gate Driver Circuit for improved turn-off characteristics of high current IGBT Modules," Records of IEEE 33rd Annual Industry Applications Conference, IAS 1998, Vol. 2, pp. 1073-1077, St. Louis, MO, Oct. 1998.
- [2] H.-G. Eckel and L. Sack, "Optimization of the turn-off performance of IGBT at overcurrent and short-circuit current," 5th European Conference on Power Electronics and Application, EPE 1993, Vol. 2, pp. 317-322, Brighton, UK, Sept. 1993.
- [3] D. Bortis, J. Biela and J.W. Kolar, "Active Gate Control for Current Balancing in paralleled IGBT Modules in a Solid State Modulator," Proceedings of IEEE 16th Pulsed Power and Plasma Science Conference, PPPS 2007, pp. 1323-1326, Albuquerque, NM, June 2007.
- [4] F. Blaabjerg and J. K. Pedersen, "An optimum drive and clamp circuit design with controlled switching for a snubberless PWM-VSI-IGBT inverter leg," Records of the IEEE 23rd Annual Power Electronics Specialists Conference, PESC 1992, Vol. 1, pp. 289-297, Toledo, Spain, July 1992.
- [5] N. Mohan, T. Undeland, W. Robbins, "Power Electronics - Converters, Applications and Design," Wiley, 1989.
- [6] V. John, B.-S. Suh and T. A. Lipo, "High Performance Active Gate Drive for High Power IGBTs," Records of the IEEE 33rd Annual Industry Application Conference, IAS 1998, Vol. 2, pp. 1519-1529, St. Louis, MO, Oct. 1998.
- [7] R. Sachdeva and E. P. Nowicki, "A novel gate driver circuit for snubberless, low-noise operation of high power IGBT," Records of the IEEE Canadian Conference on Electrical and Computer Engineering, CCECE 2002, Vol. 1, pp. 212-217.
- [8] s. Musumeci et al., "A new gate drive performing Fault Protections of IGBT during short circuit transients," Records of the IEEE 37th Annual Industry Applications Conference, IAS 2002, Vol. 4, pp. 2614-2621.
- [9] C. Licitra et al., "A new driving Circuit for IGBT Devices," IEEE Transactions on Power Electronics, Vol.10 pp. 373-378, May 1995.
- [10] R. S. Chokhawala, S. Sobhani, "Switching Voltage Transient Protection Schemes for High-Current IGBT Modules," IEEE Transaction on Industry Applications, Vol. 33, Dez. 2007.
- [11] J. Saiz et al., "Optimisation and integration of an active clamping circuit for IGBT series association," Records of the 36th Annual Industry Application Conference, IAS 2001, Vol. 2, pp. 1046-1051, Chicago, IL, Oct. 2001.
- [12] H. Riedi, P. Köhli, "SCALE" Driver for High Voltage IGBTs," Power conversion conference, PCIM 99, Nürnberg, Germany, June 1999.