Active Gate Control for Current Balancing of Parallel-Connected IGBT Modules in Solid-State Modulators

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***Abstract*—In modern pulsed power systems, often, fast solid-state switches like MOSFETs and insulated gate bipolar transistor (IGBT) modules are used to generate short high power pulses. In order to increase the pulsed power, solid-state switches have to be connected in series or in parallel. Depending on the interconnection of the switches, parameter variations in the switches and in the system can lead to an unbalanced voltage or current. Therefore, the switches are generally derated, which results in an increased number of required devices, cost, and volume. With an active gate control, derating and preselection of the switching devices can be avoided. In this paper, an active gate control of paralleled IGBT modules, which has been developed for converters with inductive load, is explained in detail and adapted to a solid-state modulator. This paper focuses on achieving a low-inductance IGBT current measurement, the control unit implementation with a field-programmable gate array and a digital signal processor, as well as the balancing of the pulse currents.**

***Index Terms*—Active gate control, current balancing, insulated gate bipolar transistor (IGBT) modules, printed circuit board (PCB)-Rogowski coil, solid-state modulator.**

I. Introduction

OVER THE last few decades, developments in semiconductor technology have led to today's high current and voltage rated insulated gate bipolar transistors (IGBTs). This enables the substitution of older switch technologies (e.g., thyratrons, ignitrons, or spark gaps) in various high-power applications, such as solid-state modulators with several megawatt pulse power. However, due to the lower blocking voltage capability of IGBTs (usually $\leq$ 6.5 kV) compared with that of thyratrons (tens of kilovolts), higher currents (10–20 kA) have to be switched to achieve the same pulsed power level. Another possibility is to connect IGBTs in series, where isolated gate drives are needed.

For large currents, high power IGBT modules [1] have to be connected in parallel. In Figs. 1 and 2, the proposed solid-state modulator schematic and the constructed hardware are shown, respectively. The modulator consists of a pulse generator unit with four paralleled IGBT modules (Eupec, FZ3600R17KE3), which are magnetically coupled by the step-up pulse transformer. In Table I, the specifications of the solid-state modulator are given.

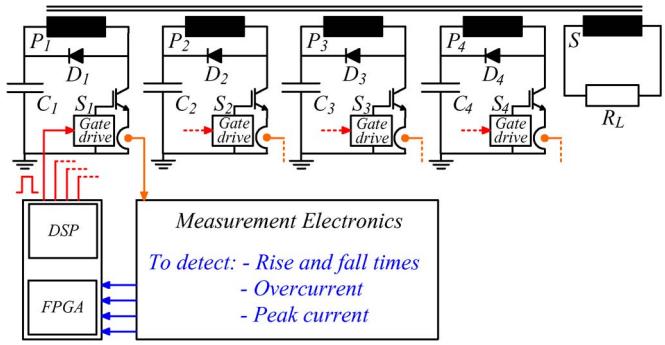

Fig. 1. Schematic of the solid-state modulator containing four magnetically parallel-connected IGBT modules, and the block diagram of the proposed active gate control.

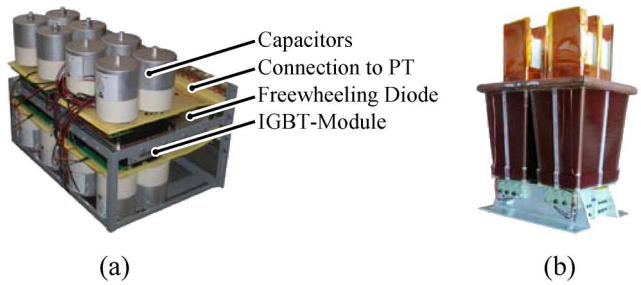

Fig. 2. Solid-state modulator with specifications listed in Table I, which is based on the proposed active gate control. (a) Pulse generator unit, each consisting of a 3.6-kA/1.7-kV IGBT module, storage capacitors, and freewheeling diode, connected to one of the four primary windings of the pulse transformer in (b).

TABLE I
SOLID-STATE MODULATOR SPECIFICATIONS

Pulse generator voltage V_{pulse}	1kV
Pulse generator current I_{pri}	20kA
Pulse duration T_{pulse}	5µs
Pulse repetition frequency f_{rep}	200Hz
Transformer step up ratio	1:170

Due to tolerances in IGBT parameters, geometry of the modulator, and different propagation delays in driver circuits, a symmetric current balancing between parallel-connected IGBTs is not always guaranteed. To ensure a safe operation, the IGBTs have to be derated [2], which results in an oversized design.

Manuscript received September 28, 2007; revised December 20, 2007. First published October 31, 2008; current version published November 14, 2008.

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Digital Object Identifier 10.1109/TPS.2008.2003971

To achieve a better current balancing, the manufacturers commonly preselect IGBTs with the same parameters, or they use devices from one production batch, where smallest parameter deviations are guaranteed [3], [4]. Even with this classification, the maximal power ratings of the IGBT must be reduced.

In [5]–[7], an active gate control to symmetrize the currents in converters with paralleled IGBTs and inductive load is presented, where no derating or preselection of the IGBTs is required. To balance the current between all IGBT modules, the current is first measured with a broadband current probe [8]–[10]. Then, depending on the transient and static currents in each IGBT, the switching times and gate voltages of the individual IGBT are adjusted, which finally results in a balanced current distribution.

In this paper, the active gate control of paralleled IGBTs, based on [5]–[7], is adapted to solid-state modulators. First, in Section II, the active gate control, as implemented for the solid-state modulator, is explained in detail. Thereafter, the low-inductive current measurement of individual IGBT modules, which is a key component of the active gate control, is described in Section III. Due to the short current pulses in the solid-state modulator, a printed circuit board (PCB)-Rogowski coil with additional measurement electronics is utilized. The signals from the measurement circuit are fed to a control unit, based on a digital signal processor (DSP) and a field-programmable gate array (FPGA), which is described in Section IV. In Section V, experimental results of the current measurement circuit and the active gate control are presented.

II. Active Gate Control for Current Balancing

IGBT manufacturers recommend to derate the switching power of parallel-connected IGBTs due to the possible current imbalance between the devices. In order to avoid this derating, two different approaches for achieving an equal current distribution have been proposed.

One possibility is to insert additional components, like series resistances or inductors, in the current path. The series resistances, however, result in additional losses, and inductors slow down the rising and falling edges of the pulse. Alternatively, the currents can be balanced with an active gate control, which does not use series elements. The only drawback of the active gate control is the need of a current measurement circuit for each IGBT and a more complex gate drive circuit.

In Fig. 1, the schematic of a solid-state modulator with four paralleled branches and the block diagram of the active gate control are shown. Each branch can be divided into a power and a control part. The power part consists of a storage capacitor C_i, an IGBT module S_i, a freewheeling diode D_i, and a primary winding P_i, whereas the control loop embodies a gate drive circuit, a current probe, and measurement electronics for detecting the rising and falling edges as well as the peak values of the current pulses. The control loop of each branch is closed with one control unit for all four IGBT modules. To achieve simultaneous turn on and off as well as an equal current distribution, the active gate control is divided into two parts, namely, a rise and fall time control and a peak current control, which will be explained in the following.

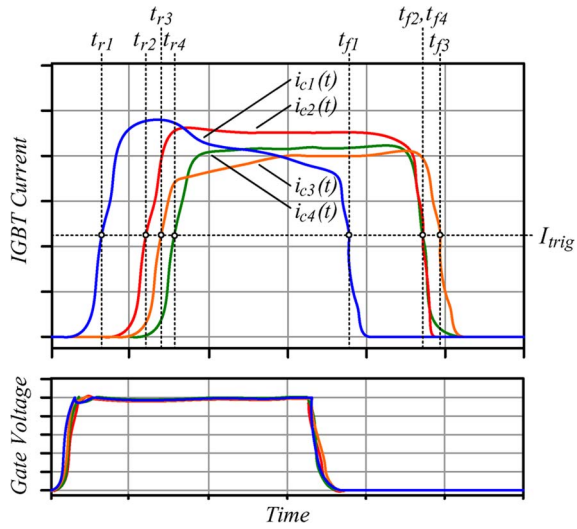

Fig. 3. Example illustration of unbalanced IGBT current pulses produced without the rise and fall time control. Rise and fall time detection at the trigger level I_{trig}.

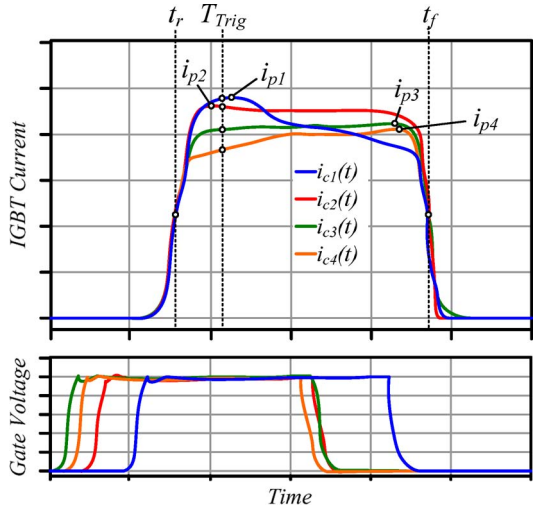

Fig. 4. Example illustration of the IGBT current pulses with synchronized rising and falling edges based on shifted gate signals. Furthermore, the detection of the current amplitudes at the time T_{trig} and the peak currents i_{pi} are shown.

Fig. 3 graphically shows the possible unbalanced current waveforms of the four paralleled branches without active gate control, where all gates are triggered at the same time with the same gate voltage. At a predefined trigger level I_{trig}, the point of time of each rising and falling edge $t_{r1}, \ldots, t_{r4}/t_{f1}, \ldots, t_{f4}$ is detected.

Before the next pulse is triggered, the rise and fall time controller shifts the turn on and off times of the gate signals depending on the time delay compared with a master pulse, whereas any branch can be selected as the master. To achieve the desired pulse duration T_{Pulse}, the turn-off point of time t_{fi} of the master also has to be adapted.

The example current waveforms, as shown in Fig. 4, result with the shifted turn on/off times of the gate signals.

To achieve fast rise and fall times, which are required in many applications, the IGBT modules must be fully turned on/off at the beginning/end of the pulse. Therefore, the IGBTs cannot be

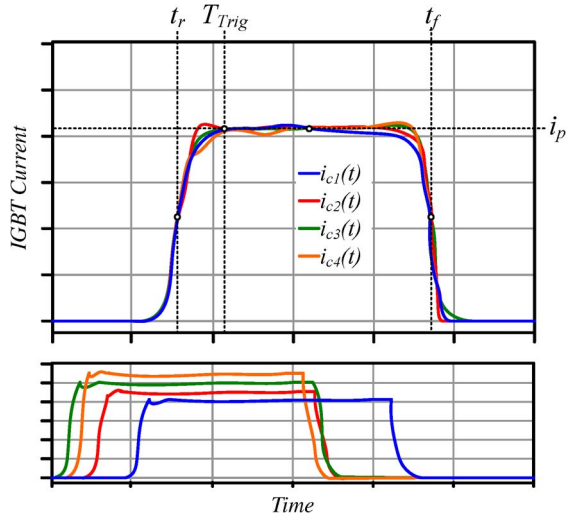

Fig. 5. Example illustrating the IGBT current pulses with synchronized rising/falling edge and synchronized slope of the rising current edge.

operated in the linear mode, and the static current cannot be controlled with the amplitude of the gate voltage, as described in [5]–[7].

Nevertheless, the derivative/slope of the collector current i_{c} can be controlled with the gate voltage ν_{G} based on

$$\frac{di_{\mathrm{c}}}{dt} = \frac{\nu_{\mathrm{G}} - \nu_{\mathrm{th}}}{\frac{R_{\mathrm{g}} C_{\mathrm{gs}}}{g_{\mathrm{m}}} + L_{\sigma}} \tag{1}$$

where operation in the linear mode is avoided, since ν_{G} is always significantly larger than the threshold voltage ν_{th}. In (1), R_{g} is the gate resistance, C_{gs} is the gate–source capacitance, g_{m} is the transconductance of the IGBT, and L_{σ} is the parasitic inductance of one branch (IGBT, C_i, and primary P_i).

Therefore, current balancing at the beginning of the pulse can be achieved by controlling the slope of the current with the gate voltage ν_{G} and synchronizing the rising edge of the pulse as described previously. In cases where IGBTs with positive temperature coefficient are applied (e.g., nonpunchthrough IGBTs), static current balancing is achieved automatically.

In order to determine the current slope/gate voltage ν_{G}, the amplitudes of the IGBT currents are required. These are sampled at the time T_{trig} (cf. Fig. 4), which are defined by the user via the controller. Before the next pulse, the gate voltage ν_{G} is controlled in such a way that, following (1), an equal increase in current in each IGBT is achieved.

Additionally, the absolute maximum values $i_{p1}-i_{p4}$ of the IGBT current pulses are detected (cf. Fig. 5) and monitored, in order to guarantee balanced IGBT currents.

In Fig. 5, the resulting IGBT current pulses with rise and fall time control and slope synchronization are shown. There, the amplitude and the time position of rising/falling edges of the gate signals have been adjusted.

Remarks:

1) Measurement results from the pulse modulator show that adjusting only the turn on and off times results in balanced current distribution. Therefore, the adjustment of the gate voltage provides an additional opportunity to balance currents, if the currents are not evenly distributed.
2) Before operating the modulator at nominal load, the presented active gate control requires a few pulses at reduced output power in order to determine the appropriate time shift of gate signals and, optionally, adjust the amplitude of the gate signal to achieve balanced currents.

During normal operation, the variation of the parameters due to temperature drift and/or voltage fluctuation is relatively small and slow, so that the correction of a measured current imbalance at the successive pulse is sufficient.

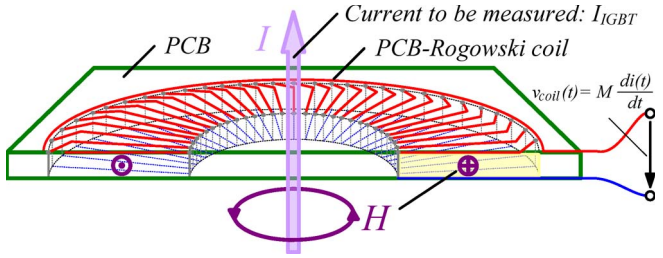

Fig. 6. Measuring principle with a PCB-Rogowski coil. The coil results from routing the PCB track alternating from top to the bottom layer and back. To reduce the stray inductance of the PCB-Rogowski coil, the end is returned to the beginning, following the circumference of the PCB-Rogowski coil.

III. Pulse Current Measurement of IGBT Modules

One of the key elements of the active gate control is a reliable, cost effective, fast, and accurate current measurement. Due to the short pulses generated by the solid-state modulator, only an ac current measurement circuit is required. Furthermore, the parasitic inductance of the modulator (IGBT, capacitors, transformer, and load), which must be very low for proper operation, must not be increased by the current probe. Therefore, a measurement circuit based on a Rogowski coil is used [14].

A. Printed Circuit Board-Rogowski Coil

Rogoswki coils basically consist of a coreless coil, which forms a closed loop. This loop encloses the conductor where the current to be measured flows (cf. Fig. 6) [11], [12].

Consequently, a part of the magnetic field H generated by the flowing current I_{IGBT} flows through the turns of the Rogowski coil.

Whenever the current varies, the amplitude of the magnetic field also varies, and a voltage is induced in the coil (Faraday's law) [8]–[13]. This is similar to a coreless transformer with a single-turn primary. The resulting voltage at the ends of the coil is

$$\nu_{\mathrm{coil}}(t) = M \frac{di(t)}{dt} \tag{2}$$

where M is the mutual inductance of the Rogowski coil and the conductor, which depends on the geometry and the number of turns of the coil. The voltage ν_{coil} at the end of the Rogowski coil is proportional to the derivative of the IGBT current.

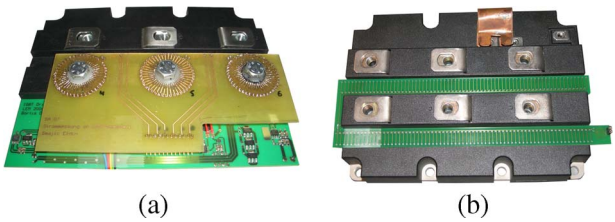

Fig. 7. (a) IGBT module (single switch) with three PCB-Rogowski coils (each containing 45 turns), where one coil encloses one (emitter) terminal of the IGBT. The coils are connected in series for measuring the total switch current. (b) One open and removable Rogowski coil (135 turns) enclosing all terminals of the IGBT module.

The Rogowski coil basically can be wound on a flexible or on a rigid bobbin. To realize a flat and reproducible measurement setup for each IGBT module in the solid-state modulator, a PCB-Rogowski coil is used. This can be designed for the desired specifications and easily be reproduced having always the same signal behavior due to the tight tolerances during the PCB manufacturing process [15]. To reduce the signal distortion and to achieve high signal quality, design rules, like the layout of the return conductor, as described in [8]–[10], have to be applied.

In Fig. 7, the PCB-Rogowski coils, which are used in the considered solid-state modulator, are shown. In order to measure the total current of one switch (= one module) the three coils—each enclosing one of the three parallel-connected IGBT (emitter) terminals—are connected in series. Alternatively, a PCB design with one open and removable coil enclosing all three terminals is shown in Fig. 7(b).

B. Signal Processing Circuit

Due to the operating principle of the Rogowski coil (2), the voltage ν_{coil} must be integrated in order to obtain the IGBT current. For relatively large mutual inductances M, the integration can be done passively with a simple RC low-pass filter. There, the cutoff frequency of the filter defines the lower frequency limit of the current measurement. To achieve a wide measurement bandwidth, a low cutoff frequency of the RC filter is necessary. The low cutoff frequency, however, leads to a high attenuation of the current measurement signal.

In case of small mutual inductances, i.e., small measurement signal amplitudes, this would lead to a low signal quality. Therefore, the signal has to be integrated actively for smaller mutual inductances. Basically, a combination of passive and active integration is also possible [16]–[22].

The integrated voltage, which is proportional to the current, is fed to comparator K_1 (cf. Fig. 8) in order to detect the rising and falling edges of the pulse current. The respective points of time $t_{r1},\ldots,t_{r4}/t_{f1},\ldots,t_{f4}$ (cf. Fig. 3) are later read from the FPGA with a resolution of 10 ns. With comparator K_2, an overcurrent can be detected, and the IGBTs can be directly turned off in order to protect the modulator.

The peak values of the IGBT currents are measured with a peak rectifier and later sampled by the ADC, which is integrated in the DSP. With the additional values sampled at T_{trig}, the total load current is determined, which is divided by the number of paralleled IGBTs in order to obtain a reference value for the

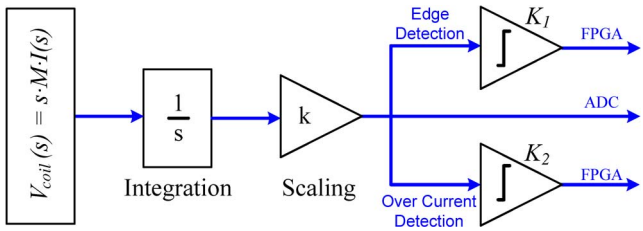

Fig. 8. Block diagram of the measurement and signal processing electronic with edge detection K_1, overcurrent shutdown, and peak value measurement K_2.

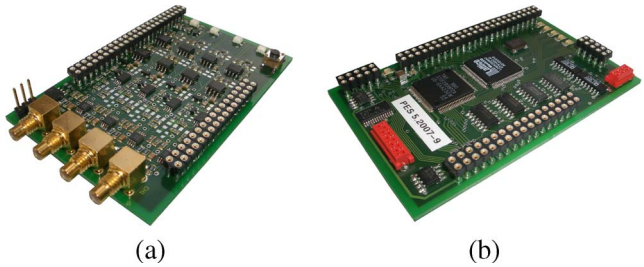

Fig. 9. Photographs of (a) the signal processing electronics and (b) the DSP/FPGA board (credit card size for both boards: 86 mm × 54 mm).

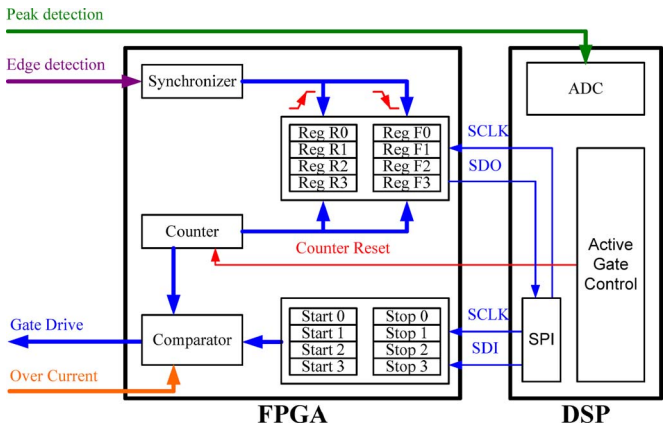

Fig. 10. Block schematic of the implemented active gate controller in the DSP/FPGA. There, the detection of the pulse falling and rising edges, the detection of the peak values, and the generation of the gate signals are shown.

IGBT current. In Fig. 9, photographs of the current measurement electronics for four channels are shown. There, the signal processing electronics [cf. Fig. 9(a)] is mounted on top of the DSP board [Fig. 9(b)] in the final assembly.

It is important to note that, in the explained control scheme, the propagation delay from the current probes to the DSP is not critical as long as the delays of all channels are the same, since a potential current imbalance is compensated in the successive pulse.

IV. Implementation

The active gate control is implemented on the DSP/FPGA board. This board performs the sampling of the signals coming from the measurement electronics in parallel. Due to the clock frequency of 100 MHz, time steps/shifts of the gate voltage of 10 ns are possible.

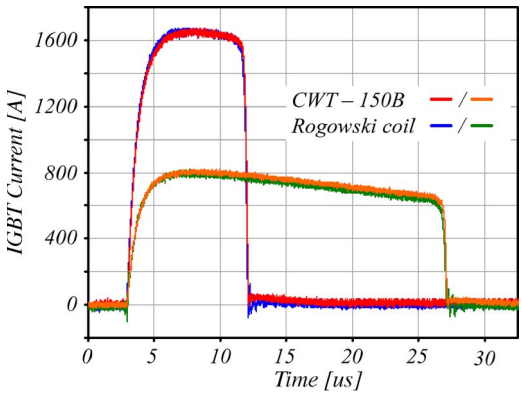

Fig. 11. Comparison of the measurement results of the PCB-Rogowski to the results obtained with a commercial CWT-150B from PEM.

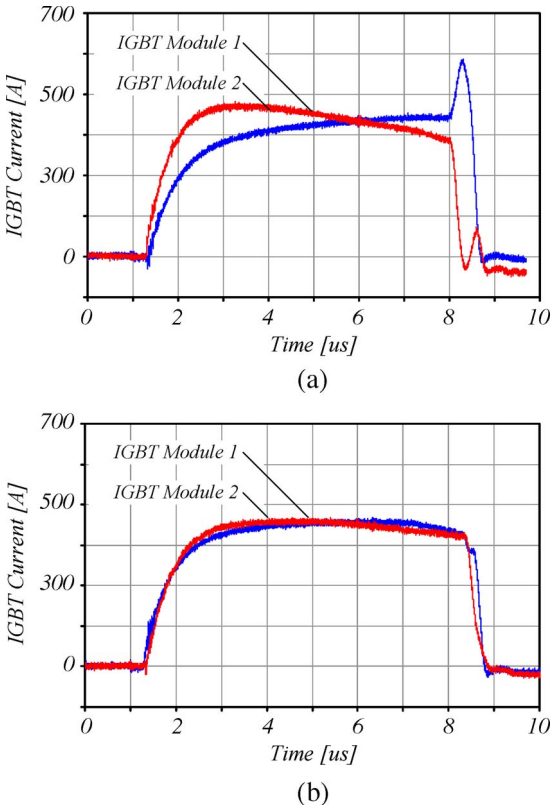

Fig. 12. Current distribution in two direct parallel-connected IGBT modules (Eupec FZ3600R17KE3) (a) without and (b) with active gate control.

The active gate control is initiated by the DSP, which triggers the gate drives at the beginning of the control sequence. Simultaneously, a counter is started on the FPGA. As soon as the rising and falling edges are detected, the FPGA stores the times of the corresponding event in the corresponding register (cf. Fig. 10). Additionally, at the predefined time T_{trig}, the DSP samples the actual current values of each IGBT. Then, the DSP calculates the new turn on and off times, and optionally adjusts the gate voltage of each gate drive and is ready for the next pulse.

If an overcurrent in one of the IGBT modules is detected, the FPGA immediately turns off all of the IGBTs in a time sequence based on the stored turn-off delays in order to ensure a simultaneous turn off.

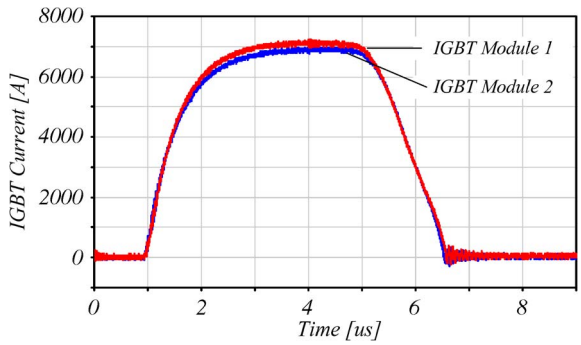

Fig. 13. Seven-kiloampere pulse currents of two direct parallel-connected IGBTs modules with high turn on and off gate resistors ($R_{\mathrm{on}} = 0.9\,\Omega / R_{\mathrm{off}} = 3.75\,\Omega$).

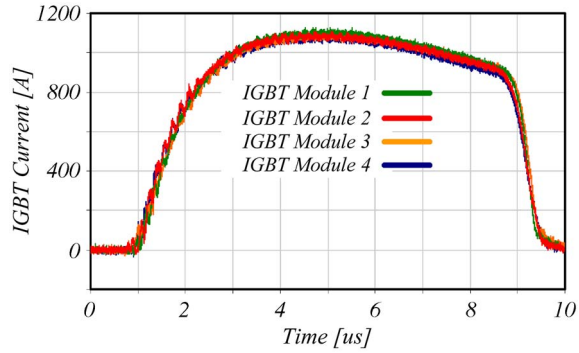

Fig. 14. Current distribution of four IGBT modules, each connected to the corresponding primary winding of the pulse transformer.

V. Measurement Results

In Fig. 11, the resulting signal of the PCB-Rogowski coil with signal processing circuit, as described in the last section, is compared with a commercially available current probe CWT150B from PEM for two different pulselengths and amplitudes. There, it can be seen that the signals of both current probes are in good correspondence.

The performance of the active current balancing circuit is shown in Fig. 12. There, the current distribution for two directly paralleled branches without transformer is shown for operation without active gate control in Fig. 12(a) and with active gate control in Fig. 12(b). These results clearly show the ability of the presented balancing circuit to symmetrize the current distribution while keeping the fast rise and fall times.

In addition, the measurement in Fig. 13 of two directly parallel-connected IGBT modules, each switching 7 kA with high value turn on and off gate resistors, shows an almost perfect current distribution.

Finally, in Fig. 14, the current distribution of four IGBT modules magnetically connected in parallel via the pulse transformer is measured and shows excellent current distribution between all four IGBT modules.

VI. Summary

In this paper, an active gate control for balancing the currents in parallel-connected IGBT modules in a solid-state modulator is presented. The balancing control shifts the rising and falling edges of the gate signals and adjusts the amplitude of the gate

voltage to achieve equally shared IGBT currents. To determine the current distribution, a fast and accurate current measurement system consisting of the PCB-Rogowski coil and the signal processing electronics is described and experimentally verified in this paper.

Furthermore, the implementation of the active gate control in a DSP/FPGA board is described. This is also experimentally verified by pulse current measurements, where, for 20-kA pulses (5 kA per IGBT), the relative error of current sharing is within 5%.

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