25kW 3-PHASE UNITY POWER FACTOR BUCK BOOST RECTIFIER WITH WIDE INPUT AND OUTPUT RANGE FOR PULSE LOAD APPLICATIONS

D. Bortis, S. Waffler, J. Biela and J. W. Kolar
Power Electronics System Laboratory / ETH Zurich,
Physikstrasse 3, Zurich, Switzerland

Abstract - **Pulse loads like solid state pulse modulators often generate short pulses with a high peak power which exceeds the average power 100 to 1000 times depending on the pulse repetition rate. There, the peak power usually is drawn from an energy buffer like a capacitor bank. During the pulse the energy buffer is discharged and has to be recharged between the pulses by a power supply, which is commonly connected to the mains.**
Because of the world wide varying mains voltages and the desired ability to adapt the capacitor voltage of the modulator, the power supply has to handle a wide input and output voltage range. Additionally, the supply often must draw a sinusoidal current from the mains while providing energy to the pulse modulator due to EMI regulations. Therefore, a general control concept for pulse load applications, which guarantees continuous power consumption from the mains and power factor correction (PFC), is described in this paper. For validating the concept measurements on a 3-phase buck boost rectifier are presented.

I. INTRODUCTION

Solid state pulsed power systems containing IGBTs are often operated with input voltages between 100V and 6.5kV due to the maximum allowable blocking voltage of the devices. Nevertheless, high output voltages of several kilovolts can be achieved for example by the use of pulse transformers, an adder topology or a Marx generator configuration ([1] and [2]).

Generally, the pulse power – in the considered case 20MW - is provided from a capacitor bank, whereas the average power (here 20kW) is supplied by a converter [3] connected to the mains, as shown in **Fig. 1**. There, the 3-phase line to line voltage can vary from 177V to 528V for a world wide operation.

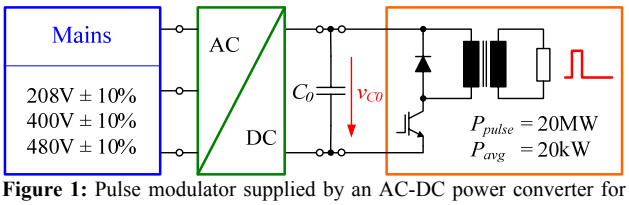


Figure 1: Pulse modulator supplied by an AC-DC power converter for unity power factor and sinusoidal mains currents.

Additionally, a variation of the capacitor voltage v_{C0} of the modulator is often desired. Therefore, a wide input and output voltage range of the rectifier is needed. These requirements can be fulfilled with a 3-phase buck boost rectifier [4] (cf. **Fig. 2**), which operates either in the buck or the boost mode, depending on the ratio of the mains voltage to the capacitor bank voltage v_{C0}. In case of the assumed high repetition rate 500-1000Hz, the recharging of the capacitor bank before the next pulse additionally requires a voltage controller with a high dynamic.

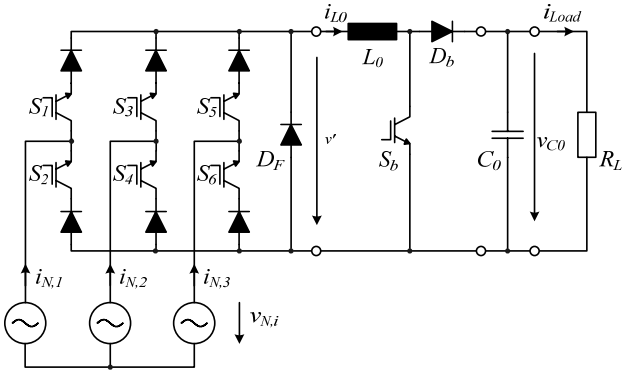


Figure 2: Schematic of the considered buck boost converter. There, the input filter is not shown for the reason of simplicity.

To enable a unity power factor operation of the 3-phase buck boost rectifier, a constant inductor current i_{L0} is required [4]-[6]. The pulse load in combination with a conventional high dynamic voltage control, however, would result in periodic peak currents in the buck-boost inductor and also in the input/mains currents $i_{N,i}$. These current distortions make a unity power factor operation of the converter impossible. Hence, a control strategy for pulse load applications, which achieves a unity power factor as well as an accurate regulation of the output voltage, must be applied in the considered case.

First, in **Section II** the operation principle including the basic structure of the controller [4]-[6] is described. In case a conventional control approach is applied, distorted mains currents result, as described at the beginning of **Section III**. There, also a control method is described, which enables an approximately constant power consumption with unity power factor. For validating the control approach measurement results for the input and output current/voltage waveforms are presented in **Section IV**.

II. BUCK BOOST RECTIFIER

As shown in Fig. 2 the input stage of the buck boost converter consists of six switches S_1-S_6 with series connected diodes, which are connected to a common negative and positive voltage terminal, followed by a boost stage consisting of switch S_b, diode D_b and the inductance L_0. The buck input stage operates as PFC input stage, what results in sinusoidal mains currents.

In case the output voltage v_{C0} is lower than the peak line-to-line mains voltage, only the input stage is used and the converter operates in the buck mode. For higher output voltages, additionally the boost switch S_b must be activated. The prototype, which has been used for validating the control scheme, is shown in **Fig. 3** and the specifications are given in **Table. 1**.

Figure 3: Photo of the 3-phase buck boost rectifier with unity power factor and a wide input and output range.

Table 1: Specifications of the considered buck boost rectifier.

Input voltage v_N	*177V – 528V*
Output voltage v_{C0}	*150V – 450V*
Load current I_{Load}	*55A – 167A*
Average Power P_{avg}	*25kW*

In order to limit the current ripple ΔI_{L0} the converter is operate in the continuous conduction mode (CCM) with an average value I_{L0} of the inductor current i_{L0}. At high switching frequencies and with a large inductance L_0, the ripple current could be neglected for simplification. Assuming a constant current $i_{L0}=I_{L0}$ the duty cycles of the buck stage switches directly can be calculated for achieving unity power factor, what is described in detail in [4]-[6].

In order to obtain a constant output voltage the duty cycles of the switches must be adapted to the input voltage and the load by a controller. For a symmetric set up the control behavior of the 3-phase buck boost rectifier could be modeled by a single phase DC-DC converter with constant input voltage [6], as shown in **Fig. 4**. There, also the cascaded control structure of the converter with an outer voltage control and an inner current loop, which will be assumed in the following, is depicted.

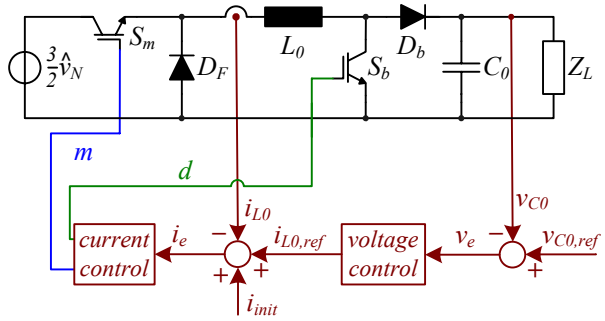


Figure 4: Single phase DC-DC equivalent circuit of the 3-phase buck boost converter with cascaded current and voltage control structure.

For the control of the output voltage the voltage v_{C0} is measured and compared to the reference voltage $v_{C0,ref}$. The voltage difference, which is equal to the voltage error v_e, is the input of the voltage controller. This controller is implemented as PI-controller and its output is the reference current $i_{L0,ref}$ for the inner current control loop. The current error i_e, which is feed into the current control block, is obtained by subtracting the measured inductance current i_{L0} from the current reference $i_{L0,ref}$. With the error signal i_e the duty cycles m and d of the buck and boost stage are calculated in the current controller. In order to achieve a high dynamic an initial current i_{init} can be added to the reference current $i_{L0,ref}$.

III. CONTROL CONCEPT FOR PULSE LOAD APPLICATIONS

The controllers in Fig. 4 are usually designed for continuous loads, where the output voltage is controlled to a constant value. With a constant voltage and a constant load at the output also continuous energy consumption from the mains and sinusoidal mains currents are obtained.

In case of a solid state modulator the power consumption of the load is discontinuous (only a few µs) and has a high peak value (20MW) compared to the average power (20kW). The energy for the pulses is usually provided from capacitor banks (cf. C_0 in Fig. 1) [1], [2]. Due to the large peak power the capacitor voltage v_{C0} drops (here: 1%/10V) below its reference values $v_{0,ref}$ during the pulse (cf. **Fig. 5**). Consequently, the voltage error v_e increases rapidly. Assuming a controller with high dynamic, the "step like" increase of the error signal results in a rapidly increasing inductor current i_{L0} for recharging the capacitor bank up to the reference value $v_{0,ref}$.

As soon as the reference value is reached the controller must decrease the inductor current down to zero again, since the load current is zero in between two consecutive pulses. This control behavior could be observed after every pulse, what would result in a highly distorted pulsating/discontinuous mains current with low power factor.

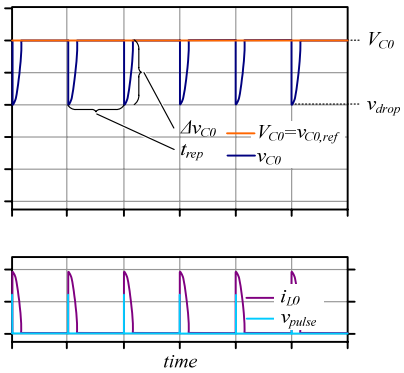


Figure 5: Schematic waveforms of the capacitor voltage v_{C0} and the load current i_{L0} with conventional control and pulse load.

A. Control based on reference signal modulation

In order to achieve sinusoidal currents with high power factor and a continuous power consumption from the mains for pulse load applications a control principle with modulated reference signal is derived in the following. There, two conditions must be fulfilled for proper system operation:

1. For a constant pulse amplitude a constant capacitor voltage v_{C0} at the beginning of the pulse is required.

2. To achieve a unity power factor the converter modulation described in [4]-[6] requires a constant current i_{L0} in the buck boost inductance L_0.. Consequently, the power consumption of the converter ($\sim i_{L0}\, v_{C0}$) is constant only if the voltage drop Δv_{C0} is negligible compared to output voltage v_{C0}.

   Remark: For large voltage drops Δv_{C0} and constant power consumption, the current i_{L0} through the inductance can no longer be constant. Therefore, the modulation strategy must be adapted, which will be presented in a future paper.

The first condition only has to be satisfied at the time steps $n \cdot t_{rep}$ when the pulses are generated. Therefore,

$$v_0(n \cdot t_{rep}) = const. \quad (1)$$

The second condition must be always fulfilled, i.e.

$$i_{L0} = const. \quad (2)$$

For the pulse modulator with a capacitive storage bank C_0 the current respectively the capacitor voltage v_{C0} has to satisfy

$$i_{L0}(t) = \frac{C_0}{(1-d)} \frac{dv_{C0}(t)}{dt} = I_{L0} = const. \quad (3)$$

Generally, the load current can be expressed as a function of an arbitrary complex load impedance Z_{Load}:

$$i_{L0} = f(Z_{Load}) \quad (4)$$

Integrating (3) for v_{C0}(t) and assuming a constant inductor current i_{L0} results in

$$v_{C0}(t) = \frac{(1-d)}{C_0} \int_0^t I_{L0} dt = v_{C0}(0) + \frac{(1-d) I_{L0}}{C_0} \cdot t \,. \quad (5)$$

Consequently, the capacitor voltage v_{C0} must change linearly in order to achieve a constant current i_L for unity power factor. There also (1) has to be fulfilled.

Thus, a linear increasing reference voltage $v_{C0,ref}$ instead of a constant reference voltage V_{C0} is used for the novel control method. The slew rate of the reference voltage $v_{C0,ref}$ could be determined with the pulse repetition time t_{rep} and the voltage drop Δv_{C0} during the pulse since also (1) must be satisfied.

The initial reference voltage $v_{C0,ref}$ at the end of the pulse is set to the minimum actual capacitor voltage v_{drop} (= $v_{C0}(0)$) resulting in

$$v_{C0,ref}(t) = v_{drop} + \frac{\Delta v_{C0}}{t_{rep}} \cdot t = (V_{C0} - \Delta v_{C0}) + \frac{\Delta v_0}{t_{rep}} \cdot t \quad (6)$$

$$\text{for } t = 0 \ldots t_{rep} \,.$$

The waveform of the reference voltage $v_{C0,ref}(t)$ for achieving a constant current i_{L0} and a unity power factor for pulse loads is shown in **Fig. 6**.

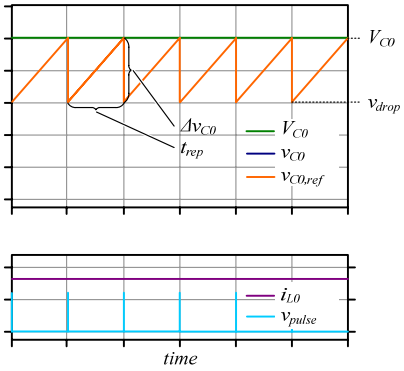


Figure 6: Schematic waveforms of the reference voltage $v_{C0,ref}$, the pulse voltage v_{Pulse} and the inductor current i_{L0} for the novel control method with unity power factor.

B. Beginning of pulse sequence and load steps

The reference voltage in (6) is derived for steady state conditions with a constant load and pulse repetition rate. At the beginning of a pulse sequence, the storage capacitor C_0 is charged up to V_{C0} and the buck boost converter transfers no power to the modulator. After the first pulse is detected, the controller of the buck boost converter resets the reference voltage $v_{C0,ref}$ to v_{drop} and ramps $v_{C0,ref}$ linearly up to V_{C0} to recharge the capacitor C_0 with a constant current i_{L0}. There, the pulse repetition rate t_{rep} must be given by the control of the modulator.

Since the current i_{L0} in the buck boost inductor starts from zero and has a limited slew rate, the current i_{L0} is too small so that the capacitor voltage v_{C0}(t) can not follow the reference value and it does not reach its nominal value V_{C0} until the second pulse (cf. Fig. 7). Therefore, the error voltage v_e(t) is increasing and the pulse voltage is a bit smaller (here app. 4%) than the nominal value at the beginning of the second pulse.

After the second pulse, the voltage reference $v_{C0,ref}$ would be reset again to the actual capacitor voltage $v_{C0}(2t_{rep})$ as described fopr steady state operation. This reset of $v_{C0,ref}$ also would lead to a reset of the voltage error $v_e(2t_{rep}) = 0$ and therefore to a sawtooth shaped waveform of $v_e(t)$ (cf. Fig. 7). Because of the cascaded and highly-dynamic control (cf. Fig. 4) the voltage error v_e would lead to a reference current i_{ref}, which has a similar shape as the error voltage v_e. Consequently, the waveform of the current i_{L0} in the buck boost inductance L_0 also would be sawtooth-like and the mains currents would be distorted at the beginning of a pulse sequence.

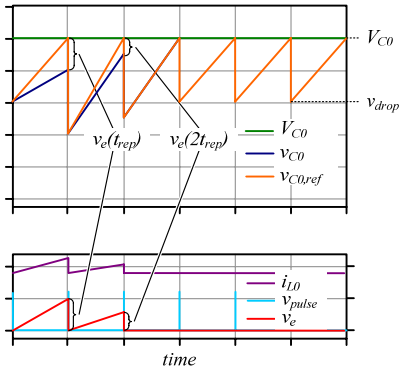


Figure 7: Discontinuous inductance current i_{L0} at the beginning of a pulse sequence and after a load change due to the reset of the reference voltage $v_{C0,ref}$ after each pulse.

In oder to avoid the discontinuities of the error voltage v_e and the current i_{L0}, the initial value of the reference voltage $v_{C0,ref}$ after the pulse has to be reset in such a way, that the error voltage v_e is continuous. Therefore, the error voltage v_e before and after the pulse must be equal.

$$v_e(n \cdot t_{rep}) = v_e(n \cdot t_{rep} + t_{pulse}) \quad (7)$$

This can be achieved by adding the last error voltage v_e (cf. **Fig. 9**) before the pulse to the voltage v_{drop}. Therefore,

$$v_{0,ref}(n \cdot t_{rep}) = v_{drop} + v_e(n \cdot t_{rep} - t_{pulse}) \,. \quad (8)$$

Additionally, the slew rate of the voltage reference $v_{C0,ref}$ must be adjusted because of the shifted initial voltage $v_{C0,ref(0)}$. Therefore, (6) is modified to

$$v_{0,ref}(t) = \left(v_{drop} + v_e(nt_{rep} - t_{pulse})\right) + \frac{(\Delta v_0 - v_e(nt_{rep} - t_{pulse}))}{t_{rep}} t \quad (9)$$

which results in a continuous waveform of v_e and i_{L0} (cf. **Fig. 8**). The described procedure also leads to a continuous error signal v_e and inductor current after a load step.

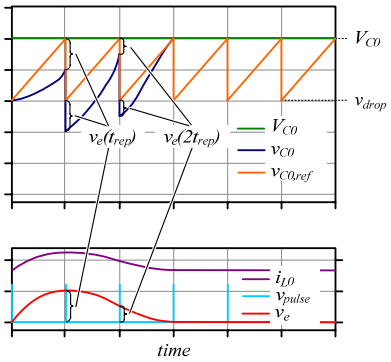


Figure 8: Schematic waveforms of the continuous error voltage v_e and the inductance current i_{L0} at the beginning of a pulse sequence or after a load step.

C. *Disabling the control during the pulse*

For a correct calculation of the reference voltage $v_{C0,ref}$ the converter is synchronized with the trigger signal of the modulator. Additionally, the minimum capacitor voltage v_{drop} has to be detected after receiving the synchronisation signal. Consequently, the reference voltage $v_{C0,ref}$ can not be updated during the pulse until the minimum capacitor voltage v_{drop} has been detected and is therefore fixed at V_{C0} during the pulse as shown in Fig. 9.

Moreover, the voltage error v_e increases rapidly during the pulse and the cascaded control would increase the inductor current i_{L0}. In order to prevent the controller from increasing the current i_{L0} during the pulse, the voltage controller will be disabled, i. e. the current reference $i_{L0,ref}$ and therefore also the current i_{L0} is kept constant, until the voltage reference $v_{C0,ref}$ is updated again.

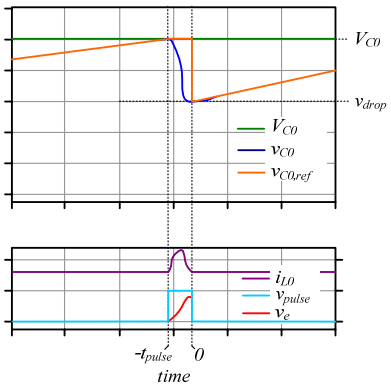
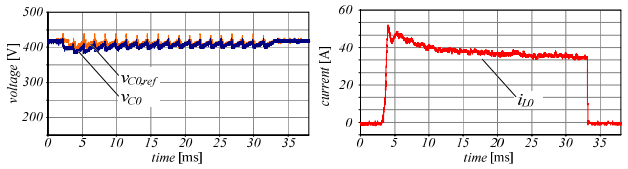


Figure 9: Spike in the inductance current i_{L0} due to the constant reference voltage $v_{C0,ref}$ during the pulse. Disabling the control during the pulse prevents from a current spike.

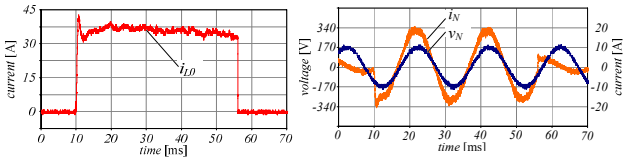
IV. MEASUREMENT RESULTS



(a) **(b)**

Figure 10: (a) Reference voltage $v_{C0,ref}$ and capacitor voltage v_{C0} for a pulse sequence with 20 pulses and 10kW average power. **(b)** Corresponding inductance current i_{L0}.

In **Fig. 10(a)** the reference voltage $v_{C0,ref}$ and the capacitor voltage v_{C0} for a sequence of 20 pulses with a pulse repetition frequency of 720Hz and an average output power of 10kW are shown. At the beginning of the pulse sequence a voltage error, due to the start-up behavior as described before, can be noticed. The corresponding inductance current i_{L0} is depicted in **Fig. 10(b)**. As can be recognized, the current i_{L0} converge to a constant value as soon as the voltage reaches the value V_0.



(a) **(b)**

Figure 11: (a) Measured inductance current i_{L0} and **(b)** corresponding mains current i_N and voltage v_N of one phase.

In **Fig. 11(a)** the inductance current i_{L0} for the same pulse sequence with a pulse repetition frequency of 440Hz and an average output power of 8kW is shown. The corresponding sinusoidal mains current i_N and voltage v_N of one phase are depicted in **Fig. 11(b)**. The measured phase shift is caused by the input filter capacitors and decreases at nominal converter output power.

V. SUMMARY

In this paper a control for AC-DC converters with pulsating loads, like pulse modulators, is explained in detail. This method is based on a modulation of the reference signal, which allows continuous power flow from the mains and sinusoidal mains currents although the power consumption of the load is discontinuous. For validating the theoretical concepts, the control, which is basically independent of the converter topology, has been successfully implemented on a 3-phase buck boost converter and measurement results are presented in the paper.

The concept has been derived for pulse modulators with relatively small variations of the DC link voltage. In case of large variations modified reference values for the capacitor voltage must be applied in order to obtain constant power consumption. These will be presented in a future paper.

VI. REFERENCES

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