A New Dimmable 70W Electronic Ballast for High Pressure Sodium Lamps

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***Abstract*—This paper introduces a dimmable electronic ballast for HPS lamps which uses a new strategy to implement the variation of the lamp's power, based on the variation of the switches' duty cycle. The complete operating principle, theoretical analysis and relevant equations are presented in this paper. The experimental results of a 70W electronic ballast operating at 33 kHz switching frequency are also presented.**

Keywords—high-pressure sodium lamps; electronic ballast; duty-cycle variation.

I. INTRODUCTION

This work presents a new 70W dimmable electronic ballast, which uses a new strategy to improve the power variation of a high-pressure sodium lamp. This electronic ballast must be robust and must have a high power factor. The ballast is commanded by a microcontroller, which has the function of implementing the duty-cycle variation that is responsible for the reduction of the lamp's power during certain daily periods pre-defined by the designer. A very positive point of this innovative proposed strategy is that the soft-switching is preserved throughout the entire range of the duty-cycle's variation.

II. THE CIRCUIT AND OPERATION PRINCIPLE

A. Circuit Description

The topology of the new 70W dimmable ballast is shown in Fig. 1. The ballast consists of two power switches (S1, S2) in a half-bridge inverter configuration, a DC component block capacitor (Cc), an output filter inductor (Lo), an auxiliary inductor (Laux) to implement the soft-switching, and a signal and drive circuit composed basically of a microcontroller and a gate driver integrated circuit. Diodes D1 and D2 are the intrinsical diodes of the power switches.

B. Principle of Duty-Cycle Variation

Defining D as the duty-cycle for switch S1, switch S2 will be driven complementary, meaning that its duty-cycle will be equal to (1-D). This asymmetrical drive of the switches results in a voltage waveform across the auxiliary inductor as shown in Fig. 2, when D is smaller than or equal to 0.5. This waveform will supply the output inductor and the lamp. Since the ballast is operated at a high frequency, 33kHz, the lamp can be modeled as a pure resistance.

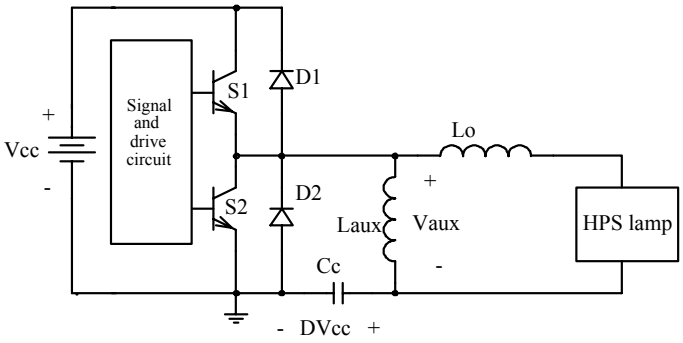


Fig. 1 – Half-bridge inverter topology applied as a HPS-lamp ballast.

The rms value of the voltage, Vaux, shown in Fig. 2 is given by (1).

$$Vaux_{rms} = \sqrt{D \cdot (1-D)} \cdot Vcc \qquad (1)$$

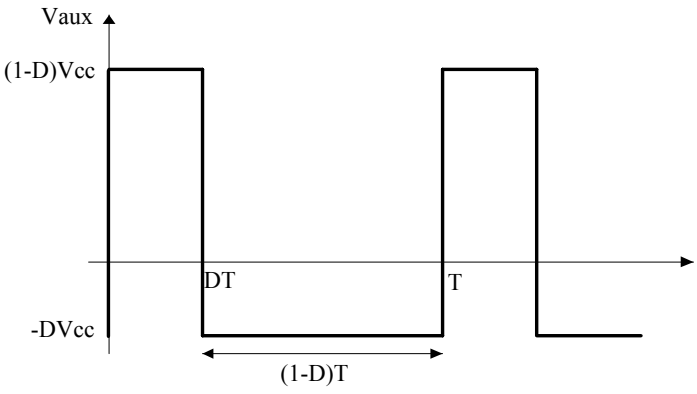


Fig. 2 – Voltage waveform across the auxiliary inductor.

Equation (1) shows that the rms value of voltage Vaux depends on the duty-cycle D. This voltage supplies the output filter inductor and the lamp, which is considered as a resistance. So, using electrical circuit analysis and performing a couple of calculations, it can be proven that the lamp voltage also depends on the duty-cycle. The next section will show an extensive analysis of this dependence.

III. THEORETICAL ANALYSIS

A. Topological Stages

In order to simplify the analysis the following assumptions are made: the circuit operates in steady state; all components are considered ideal; the voltage Vcc supplied by the input pre-regulator is constant and has no ripple; the capacitor, Cc, is always charged with the voltage, DVcc. This voltage has the polarity indicated in the Fig.1, and no ripple; the lamp can be modeled as a pure resistance; the commutation times are equal to zero therefore, the inductor, Laux, will not be considered for this analysis. According to these considerations, the circuit of the Fig.3 represents the simplified model of the inverter.

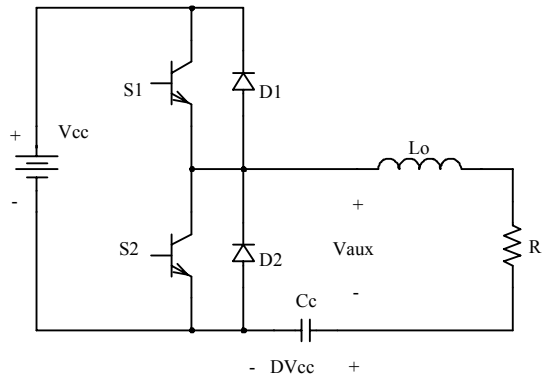


Fig. 3 – Simplified inverter topology for analysis.

First Stage ($t_0 - t_1$) : This stage begins at t_0 when diode, D1, starts conducting with an initial current equal to I_{min}. This current can be aproximated by (2),

$$I_{min}(D) = \frac{D \cdot Vcc}{R} \cdot \left(1 - e^{-\frac{T}{\tau}}\right) \quad (2)$$

where:

T: switching period;

$\tau = \frac{Lo}{R}$: time constant of the circuit;

R: lamp's resistance;

Lo: output inductor.

At this stage, the lamp's current is negative and it decreases exponentially until time t_1, when it reaches zero, finishing the stage. This stage is represented by Fig. 4(a). The voltage Vaux is positive and equal to (1-D)Vcc. The lamp's current for this stage is given by (3).

$$i_1(D,t) = \frac{(1-D) \cdot Vcc}{R} \cdot \left(1 - e^{\frac{-t}{\tau}}\right) - I_{min}(D) \cdot e^{\frac{-t}{\tau}} \quad (3)$$

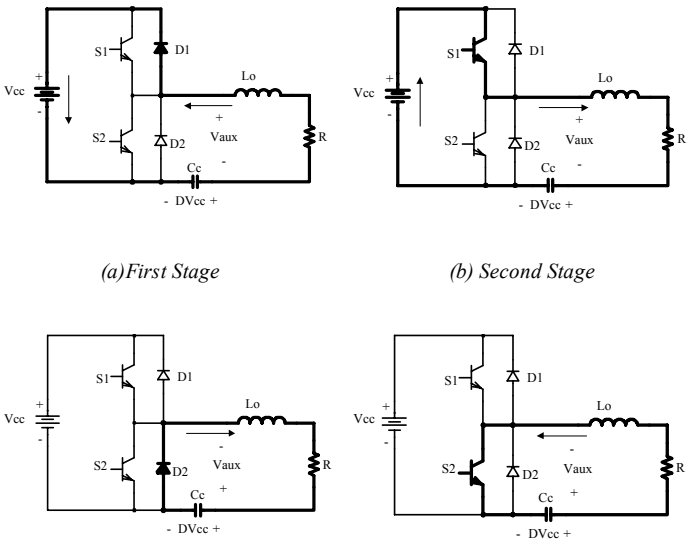
Second Stage ($t_1 - t_2$): At t = t1, S_1 is gated on and it starts conducting the lamp's current as presented in the Fig. 4(b).

This current increases exponentially in positive direction until reaching I_{max} at t_2, that corresponds to time D.T. The current Imax is defined by (4).

$$I_{max}(D) = \frac{(1-D) \cdot Vcc}{R} \cdot \left(1 - e^{\frac{-t_2+t_1}{\tau}}\right) \quad (4)$$

This stage ends at t_2 when S_1 is gated off. The lamp's current for the second stage is given by (5).

$$i_2(D,t) = \frac{(1-D) \cdot Vcc}{R} \cdot \left(1 - e^{\frac{-t+t_1}{\tau}}\right) \quad (5)$$



(a)First Stage *(b) Second Stage*

(c) Third Stage *(d) Fourth Stage*

Fig. 4 - Topological Stages.

Third Stage ($t_2 - t_3$): This stage starts at t_2 when S_1 is gated off and D_2 starts conducting. The lamp's current is positive and it decreases exponentially until reaching zero ending the stage. The output current for this stage is given by (6).

$$i_3(t) = -\frac{Vcc}{2 \cdot R} \cdot \left(1 - e^{\frac{-t+t_2}{\tau}}\right) + I_{max} \cdot e^{\frac{-t+t_2}{\tau}} \quad (6)$$

Fourth Stage ($t_3 - t_4$): At $t = t_3$, S2 is gated on starting the last topological stage. The lamp's current is negative and it increases exponentially until I_{min} completing one switching period.

This stage is represented in Fig. 4(d) and (7) represents the lamp's current.

$$i_4(D,t) = -\frac{D \cdot Vcc}{R} \cdot (1 - e)^{\frac{-t+t_3}{\tau}} \quad (7)$$

B. *Power Variation*

Considering that the lamp can be modeled as a pure resistance, the lamp's voltage for each of the topological stages v_1, v_2, v_3 and v_4 can be obtained multiplying (3), (5), (6), (7) by R, respectively. So, these voltages are also a function of the duty-cycle and of the time. Figure 5 shows the lamp's voltage waveforms for five different duty-cycle values for one switching period.

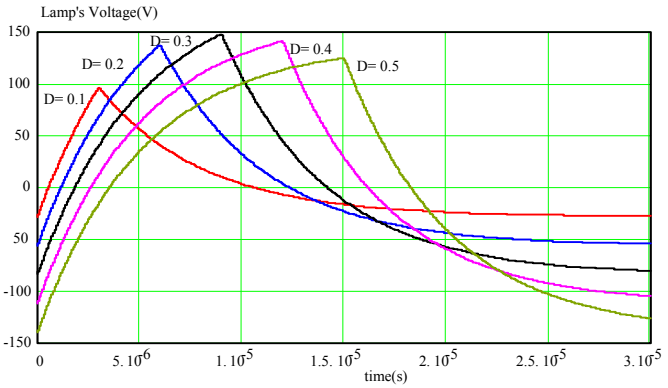


Fig. 5 – Lamp's voltage as a function of duty-cycle and time.

The rms value of the lamp's voltage is defined by (8).

$$Vef(D) = \sqrt{\frac{1}{T} \cdot \left(\int_{t_0}^{t_1} v_1(D,t)^2 dt + \int_{t_1}^{t_2} v_2(D,t)^2 dt + \int_{t_2}^{t_3} v_3(D,t)^2 dt + \int_{t_3}^{t_4} v_4(D,t)^2 dt \right)} \quad (8)$$

The rms value of the lamp's voltage as a function of the duty-cycle is shown in Fig. 6.

Therefore, the power of the lamp is also a function of the duty-cycle.

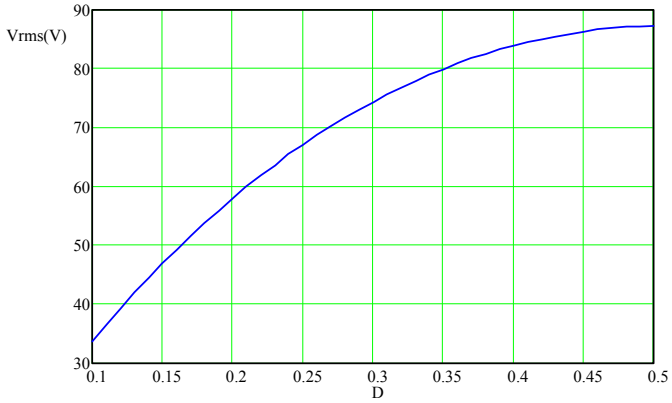


Fig. 6 – Lamp's rms voltage as a function of the duty-cycle.

Figure 7 illustrates how the lamp's power decreases with the duty-cycle's decrement.

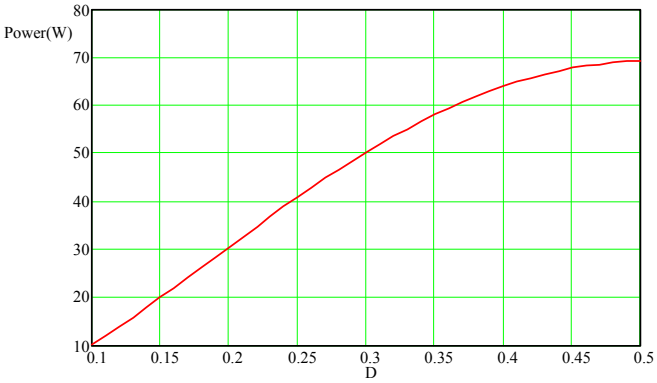


Fig. 7 – Lamp's power as a function of the duty-cycle.

It is important to remember that this innovative strategy preserves the soft-switching throughout the entire range of the duty-cycle's variation.

Another important fact to be considered is that lamps must be operated in the full-power mode for at least fifteen minutes prior to operation in the reduced- power mode. Furthermore, in changing from the full-power mode to the reduced power-mode, the time between full power and reduced power must be no less than ninety seconds, and the rate of change of power at any power level between full power and reduced power must be no greater than that corresponding to a linear reduction between those extremes in a ninety second time interval [4]. If these conditions are not respected, the extinction of the arc of the lamp can occur.

IV. DESIGN PROCEDURE AND EXAMPLE

A. *Input data*

DC bus voltage: 280V;

Rated output power: 70W;

Operation frequency: 33kHz;

Lamp's equivalent resistance: R = 110 Ω;

Maximum duty cycle: D_{max} = 0.5;

Minimum duty cycle: D_{min} = 0.2.

B. *Output Inductance*

The output inductance and the other components of the power stage must be designed for the full-power condition. The output inductance must be related with the DC bus voltage. This occurs because when the lamp becomes older its resistance increases, therefore the inductance must be designed so that when the lamp's resistance increases, its power decreases. Following this principle, the output inductance is equal to 560µH. Figure 8 shows the lamp's power as a function of the lamp's resistance. It can be observed that at the rated value, 110 ohms, the power is equal to 70 W and it is maintained constant until 130 ohms before it starts decreasing.

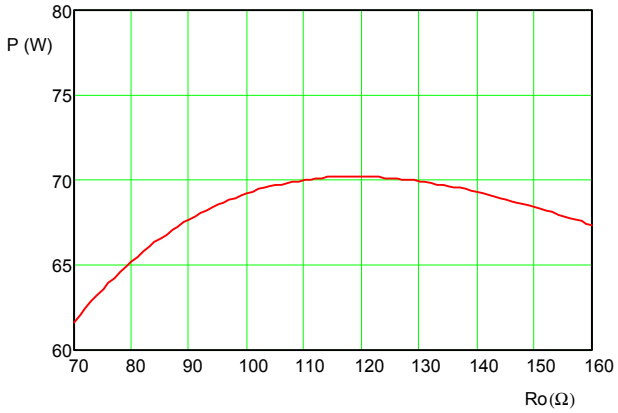


Fig. 8 – Lamp's power as a function of the lamp's resistance.

C. *DC block capacitor*

The DC block capacitor can be determined based on a maximum ripple value, Δv_{Cc}, defined by the designer. Its capacitance is given by (9).

$$Cc \geq \frac{1}{2\cdot\Delta v_{Cc}}\left[\frac{Vcc}{2\cdot R}\left(t_2-\tau\left(e^{\frac{-t_2+t_1}{\tau}}-1\right)-\tau\left(e^{\frac{-t_1}{\tau}}-1\right)\right)+I_{min}\cdot\tau\left(e^{\frac{-t_1}{\tau}}-1\right)\right] \quad (9)$$

For a maximum output ripple of 42 V the chosen capacitance is equal to 330 nF.

D. *Auxiliary inductor*

The auxiliary inductor is necessary in order to discharge the gate- capacitances of the MOSFET's . Before the addition of this inductor the gate voltages had some spikes that gated on the switches inappropriately, causing a short circuit for each commutation. The auxiliary inductor was chosen to be equal to 2mH.

E. *Power switches*

Theoretically, the maximum voltage across the switches would be equal to 280V, that it is the value of Vcc.

However, when the system operates as an open circuit, that is, before the lamp starts, the voltage Vcc reaches 350V. Therefore the maximum drain-to-source voltage across the switches is V_{DSmax} = 350V.

Figure 9 shows the current of the switch S1 for one switching period for five different values of duty cycle. The MOSFET's selection must be done considering the average drain current and rms drain current for the rated conditions. They are given by (10) and (11), respectively.

$$I_{S1avg} = \frac{1}{T}\cdot\left(\int_{t_1}^{t_2} i_2(D,t)dt\right) \therefore I_{S1avg} = 0.344A \quad (10)$$

$$I_{S1rms} = \sqrt{\frac{1}{T}\cdot\left(\int_{t_1}^{t_2} i_2(D,t)^2 dt\right)} \therefore I_{S1rms} = 0.578A \quad (11)$$

The IRF740 MOSFET was chosen as it features the mentioned requirements.

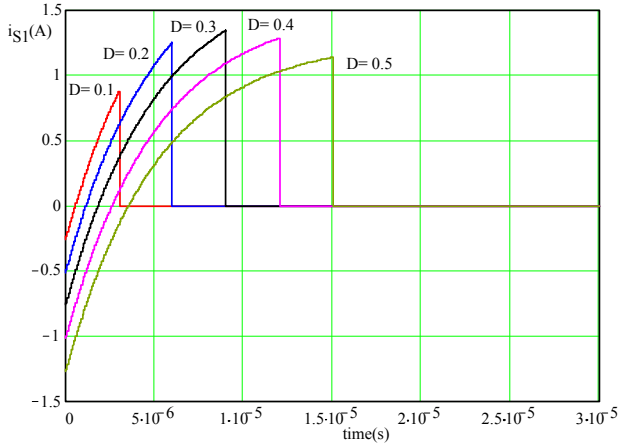


Fig. 9 –Drain current of the switch S_1 for different values of duty cycle.

F. *Signal and drive circuit*

The signal and drive circuit is based on a PIC microcontroller and on an integrated circuit IR2111.

The IR2111 is a high voltage, high-speed power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half-bridge applications. The main connections for the IR2111 are shown in Fig. 10.

The PIC (Peripheral Interface Controller) microcontrollers are RISC-based microcontrollers designed for applications requiring high performance and low cost. The PIC can be reprogrammed many times with a cheap programmer and it is easy to program. For this application, it was chosen the PIC16C62B microcontroller.

The PIC supplies a 5V pulse in the switching frequency and with duty cycle determined by the programmer. This pulse is adapted to 15V and is injected in the input channel of the IR2111 that drives the two switches complementarily.

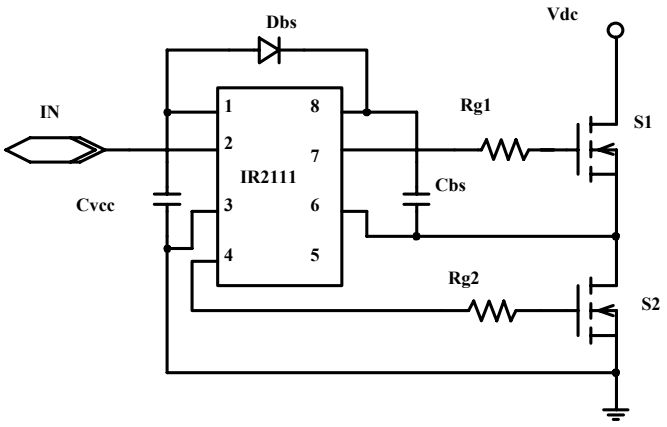


Fig. 10 – Drive circuit IR2111.

An example for the ballast operation sequence is illustrated in Fig. 11.

The circuit is powered on when the daylight decreases activating the photocell of the street lighting. The microcontroller waits 10 minutes before it starts to produce the voltage pulses for the drive circuit. After this time a soft-start is provided and the duty cycle increases from zero to 0.5 in a specified time interval.

The duty cycle is maintained at 0.5, for example, for 6 hours until 00:10 when it is supposed that there are not so many people in the streets anymore so, the luminosity can be reduced. The lamp's power is slowly reduced through the duty-cycle reduction and the lamp will operate at the reduced power until the circuit will be powered off when the morning comes.

This operation sequence can be adjusted for different regions and to implement these adjustments, no hardware changes are necessary: all can be made with a software alteration of the microcontroller.

V. EXPERIMENTAL RESULTS

Based on the theoretical analysis given in Section III, a 70W prototype has been implemented. The power stage of the ballast was implemented using the following components:

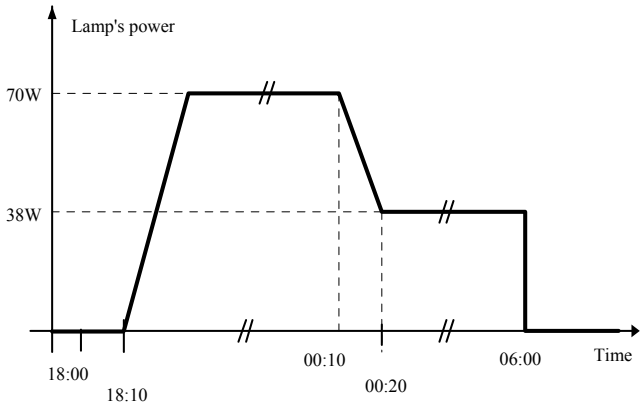


Fig. 11 – Example of time diagram for the ballast operation.

Inverter switches (S_1, S_2): MOSFETs IRF740;

Inverter diodes (D_1, D_2): MOSFET's body diodes;

Auxiliary inductor (Laux): 2mH -Ferrite core E20/6–IP12 (Thornton) - 130 turns /26AWG ;

DC component block capacitor (Cc): 330nF/ 250 V – polypropylene (Epcos);

Output filter inductor (Lo): 560µH -Ferrite core E30/14–IP12 (Thornton) - 76 turns / 6 turns -23AWG.

At rated power, when D is equal 0.5, the gate signal of switch S2 (upper) and the lamp's current (lower) can be viewed in Fig. 12.

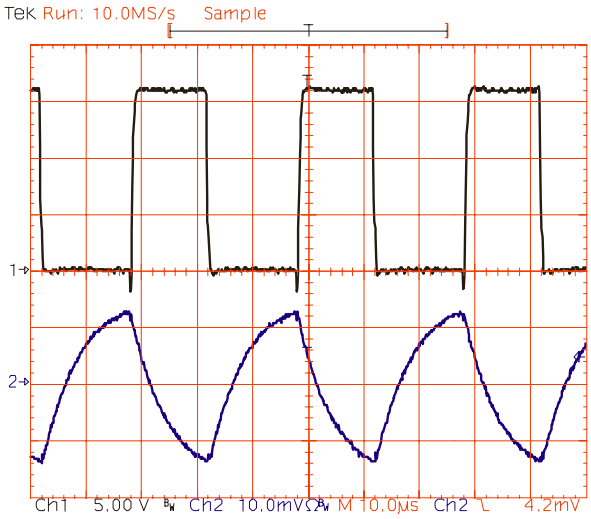


Fig. 12 – Gate voltage and lamp's current for D =0.5.

Voltage scale: 5V/div. Current scale: 1A/div

The lamp's voltage (upper) and current (lower) for rated conditions are shown in Fig. 13.

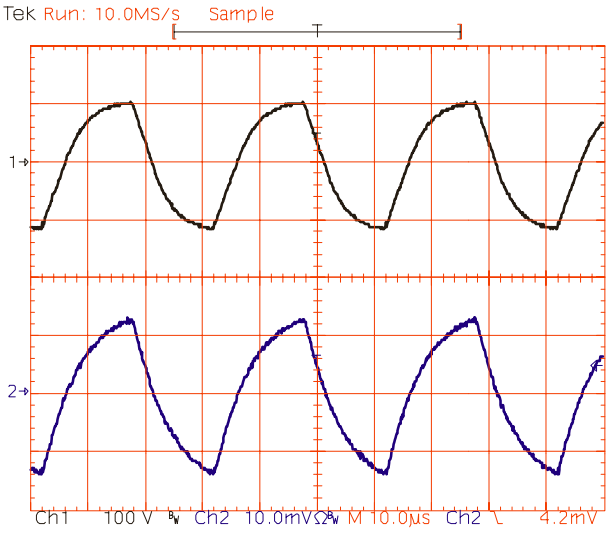


Fig. 13 – Lamp's voltage and lamp's current for D =0.5.

Voltage scale: 100V/div. Current scale: 1A/div

The symmetry between the voltage and current waveforms proves that when the lamp is operated at a high-frequency, it can be modeled as a pure resistance.

At the chosen reduced power, 38W, when D is equal 0.2, the gate signal of switch S2 (upper) and the lamp's current (lower) can be viewed in Fig. 14.

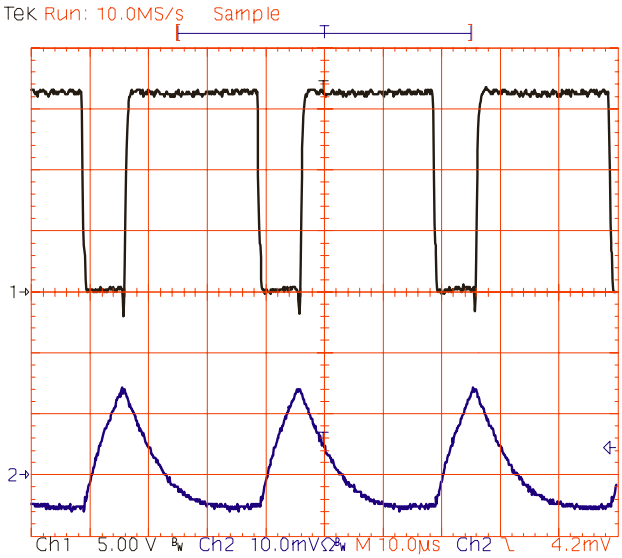


Fig. 14 – Gate voltage and lamp's current for D =0.2.

Voltage scale: 5V/div. Current scale: 1A/div

The lamp's voltage (upper) and current (lower), at 38W of power, are shown in Fig. 15.

Some relevant experimental results for the implemented prototype are presented in Table I.

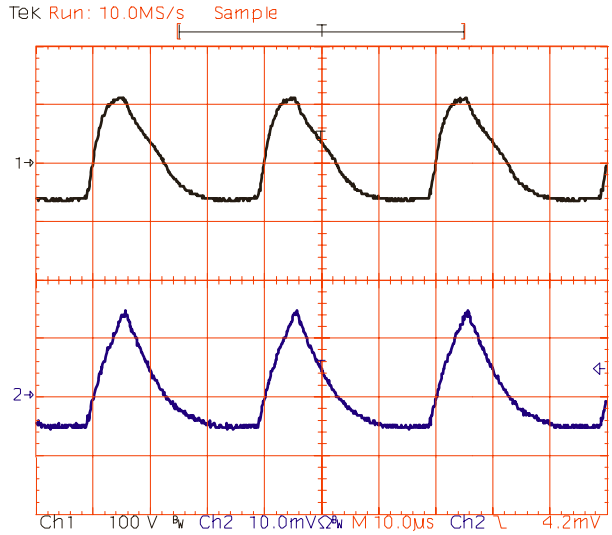


Fig. 15 – Lamp's voltage and lamp's current for D =0.2.

Voltage scale: 100V/div. Current scale: 1A/div

TABLE I.– RELEVANT EXPERIMENTAL RESULTS

	Duty Cycle	
Parameter	***D= 0.5***	***D=0.2***
Lamp's rms voltage	79,3 V	62,5 V
Lamp's rms current	887 mA	626 mA
Lamp's power	70,2 W	38,1 W
Power factor	0,973	0,805
Efficiency	88,41%	87,58%

It can be observed that the ballast efficiency is very high for this power range. It could be observed later with the construction of prototypes for higher power that the converter losses will not increase linearly with the power increase so it will be expected that for higher power the converter efficiency will be significantly better.

VI. CONCLUSIONS

This work presented a new electronic ballast for HPS lamps that uses an innovative strategy to control the lamp's power, throughout the variation of the power switches' duty cycle. The electronic ballast is completely controlled by a PIC microcontroller, which takes care of the duty-cycle's variation.

The new ballast is robust, it has high efficiency and soft-switching is preserved throughout the entire range of the duty-cycle's variation. So, the experimental results showed that the new power variation strategy is appropriate for this application.

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