Design of a 5kW High Output Voltage Series-Parallel Resonant DC-DC Converter

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Abstract — This work presents a comprehensive procedure for designing a high output voltage series-parallel resonant DC-DC converter. The system output voltage control is by a combination of duty-cycle and switching frequency variation, where soft-switching is preserved over the entire operating range. The basic principle of operation of the converter is described and an analytical model is established which does provide a basis for the numerical calculation of the stresses on the power components. Furthermore, a control strategy for minimizing the no-load conduction losses is proposed and the transient behavior in case of load steps including output short-circuit is discussed based on digital simulations.

I. INTRODUCTION

The operation of high output voltage DC-DC converters is considerably affected by transformer non-idealities being caused by the large transformer turns ratio and/or large number of secondary turns. In particular, the leakage inductance and the secondary winding capacitance do take considerable influence on the converter behavior and do potentially reduce efficiency and reliability [1]. Therefore, converter topologies suitable for high-voltage applications should integrate the parasitics of the transformer into the circuit operation. Accordingly, series-parallel resonant converters are frequently employed for the realization of high output voltage DC-DC converter systems. However, the design of resonant converters is involved due to the large number of operating states occurring within a pulse period.

This paper presents a straightforward procedure for designing a full-bridge high output voltage series-parallel resonant DC-DC converter. The approach is based on an extension of the first harmonic analysis proposed in [2]. There, the converter output power is controlled by frequency variation at fixed duty-cycle. In contrast, in the case at hand the output power is controlled by duty-cycle variation where the operating frequency is automatically adjusted for ensuring the commutation of one bridge leg at zero current. As the second bridge leg due to operation above the resonance frequency commutates at zero voltage, soft-switching is preserved in the entire operating range.

Furthermore, in order to guarantee low losses in stand-by mode a control scheme minimizing the converter conduction and switching losses for no load operation is proposed. Also, the transient behavior for step-like changes from rated load to no load operation and to output voltage short circuit is analyzed and a control concept is described which allows to maintain the converter operation above resonance for all kinds of load changes.

In the following, the converter power circuit will be described and subsequently an analytical description of the operating behavior will be given based on the first harmonic concept [2]. Furthermore, the stresses on the main power components as determined by a numerical solution of the nonlinear implicit analytical system description will be shown in graphical form. Furthermore, results of simulations of a 5kW, 23- 62.5kV output converter operating at 250kHz at full load and 450kHz at low load will be given, which fully verify the theoretical considerations.

Finally, a control concept guaranteeing low no-load losses and operation above resonance also in case of highly dynamic load changes will be described.

II. CIRCUIT DESCRIPTION

The topology of the 5kW series-parallel resonant full-bridge DC-DC converter with impressed output voltage operating above resonance is shown in **Fig.1**. The (parasitic) capacitors C_1, C_3 serve for zero-voltage switching of power transistors S_1 and S_3, the resonant inductor L_s is formed by the transformer stray inductance in combination with an auxiliary inductor connected in series. The parallel resonant capacitor C_p is formed by the parasitic capacitance of the high-voltage transformer T_1 secondary winding. As free-wheeling diodes D_1, D_3 the intrinsic diodes of the power MOSFETs are employed; for the bridge leg realized in IGBT technology explicit diodes D_2, D_4 are provided.

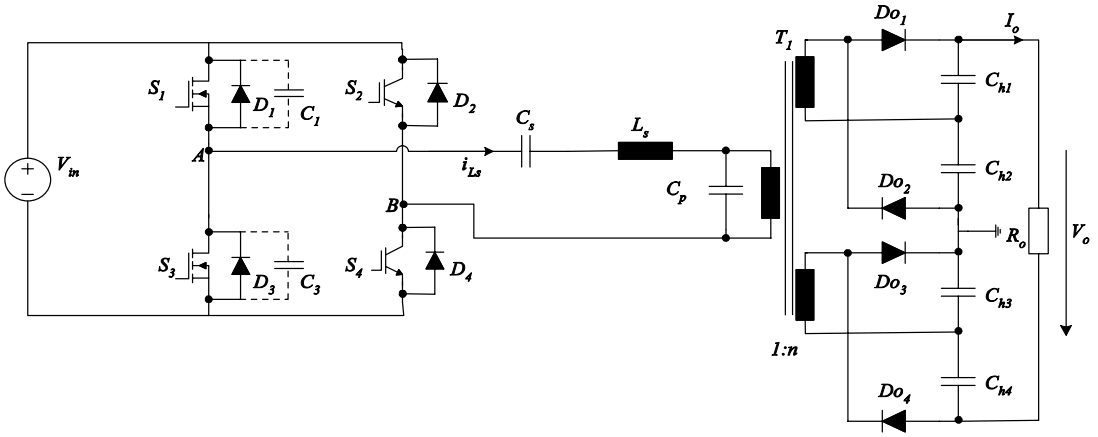


Fig.1: Structure of the power circuit of a series-parallel resonant DC/DC converter with impressed output voltage; C_p denotes the equivalent capacitance of the secondary winding referred to the primary.

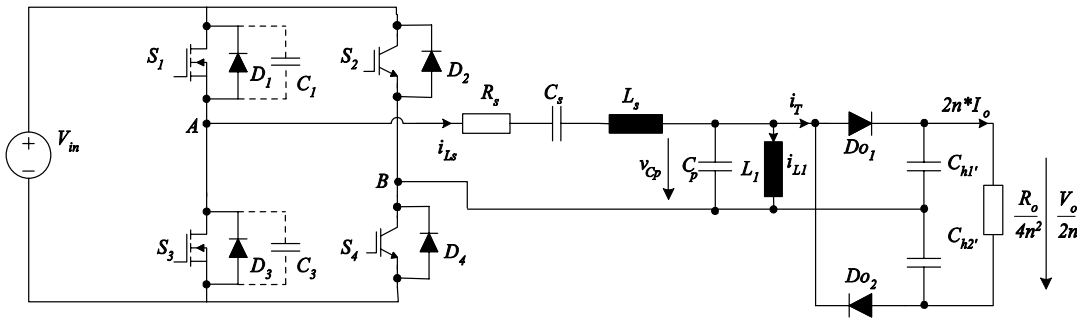


Fig.2: Equivalent circuit of the converter circuit shown in Fig.1 for referring the output quantities to the transformer primary side. The rectifier circuits connected in series on the secondary side are supplied in parallel by the primary winding.

As will be shown in detail in section III the bridge leg S_1, S_3 employing power MOSFETs is operating under zero voltage switching (ZVS) condition, and the bridge leg S_2, S_4 equipped with IGBTs is commutating at zero current (ZCS).

The equivalent circuit of the series-parallel resonant converter is depicted in **Fig.2** where the output quantities are referred to the transformer primary side. There, L_1 represents the transformer magnetizing inductance, the winding losses are considered by a series resistance R_s.

III. THEORETICAL ANALYSIS

In the following, operation of the series-parallel resonant converter above resonance is assumed. There, no direct current commutation from a free-wheeling diode to a power transistor does occur and/or the (intrinsic) anti-parallel diodes of the power MOSFETs which are characterized by a relatively slow reverse recovery behavior can be employed as free-wheeling diodes [3].

The voltage transfer ratio of a series-parallel resonant converter in dependency on the load and on the normalized switching frequency is depicted in **Fig.3**.

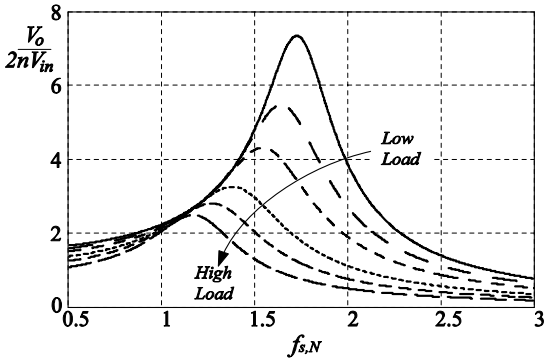


Fig.3: Voltage transfer ratio of a series-parallel resonant converter in dependency on the load and on the normalized switching frequency $f_{s,N} = f_s/f_o$ (normalization with reference to the series resonant frequency $f_o = (2\pi\sqrt{L_sC_s})^{-1}$); n denotes the transformer turns ratio. For low output power the converter characteristic is equivalent to a parallel resonant converter; for high output power the parasitic winding capacitance in a first approximation can be assumed as being short-circuited by the equivalent load resistance [3], accordingly the system shows the characteristic of a series resonant converter.

A. Converter Conduction States

For simplifying the analysis of the converter stationary operating behavior in the following all components are considered ideal and the voltage V_{in} is assumed to show a constant value. Furthermore, the switching frequency ripple of the output voltage is neglected and the load is modeled by an equivalent resistor.

The conduction states of the converter occurring within a pulse period are compiled in **Fig.4** with reference to **Fig.5**.

***First State ($t_0 - t_1$)*:** This state begins at t_0 when the resonant current i_{Ls} crosses zero and switch S_4 is turned on. In the previous stage, S_1 was turned on under ZVS, accordingly S_1 and S_4 do conduct the resonant current. The voltage v_{AB} is positive, the resonant current is positive sinusoid and the output rectifier is turned off as v_{Cp} decreases cosinusoidally from $-V_o/4n$ to zero and continues to increase to positive values. The state ends when v_{Cp} reaches $+V_o/4n$ and the output rectifier starts to conduct again.

***Second State ($t_1 - t_2$)*:** In t_1 the resonant current still flows through S_1 and S_4. The voltage v_{Cp} is clamped to $+V_o/4n$ and v_{AB} is still positive.

***Third State ($t_2 - t_3$)*:** At the beginning of this state S_1 is turned off, accordingly i_{Ls} is directed to the capacitors C_1 and C_3 and charging C_1 and discharging C_3. When the voltage across C_3 reaches zero in t_3 the commutation of S_1 to D_3 is completed.

***Fourth State ($t_3 - t_4$)*:** At time t_3, S_4 and D_3 are conducting. S_3 is turned on at zero voltage (ZVS). The resonant current i_{Ls} is positive and the inverter output voltage v_{AB} is zero. Immediately before the i_{Ls} reaches zero, S_4 is turned off in t_4..

***Fifth State ($t_4 - t_5$)*:** As S_4 has been turned off i_{Ls} flows through D_2 and D_3. Accordingly, we have $v_{AB}<0$. When i_{Ls} reaches zero in t_5, a half switch period is completed.

The system behavior for the second half switching period is analog to the first half period with replacing S_1 and S_4 by S_3 and S_2. Therefore, the second half period will not be described, but only the conduction states are shown in Fig.4 (cf. (t_5–t_{10})).

B. Design Procedure Based on First Harmonic Analysis

In [2], an analytical description of a series-parallel resonant converter with impressed output voltage has been proposed for constant duty cycle operation. This analytical concept will be extended to variable duty-cycle operation and ZCS of one bridge leg and employed for a straightforward system design and/or for analyzing the influence of parameter variations in the following. There, we assume as main specifications of the converter:

output voltage range	$V_o = 23\ldots62.5$kV;
output current range	$I_o = 0\ldots200$mA;
output power range	$P_o = 0\ldots5$kW.

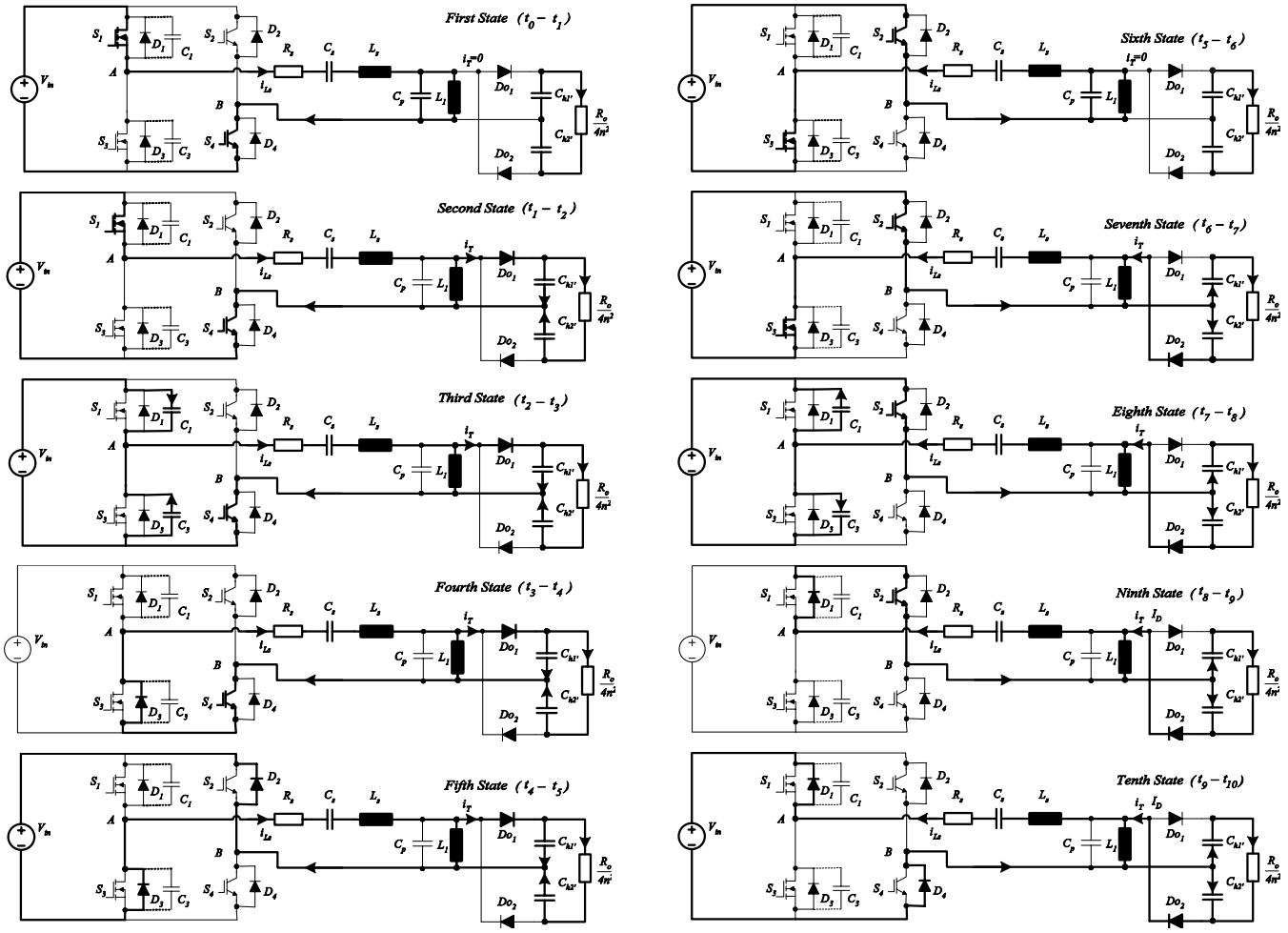


Fig.4: Conduction States of the series-parallel resonant converter within a pulse period (cf. Fig.5).

In a first step of the system design, the components of the resonant circuit have to be determined under consideration of limitations caused by maximum admissible stresses on power components or by parasitic component values. In the case at hand

- the converter switching frequency f_s should not exceed 500kHz in order to limit the complexity of the gate drive and control circuits and to have only a limited influence of the gate drive and signal electronics delay times on the operating behavior;
- the maximum voltage stress on the (low capacitance) series capacitor C_s should be lower than 1kV with respect to the capacitor technology available for high frequency high-current applications;
- the capacitance C_p/n^2 of the parallel resonant capacitor referred to the secondary must be larger than 50pF with respect to the minimum achievable winding capacitance of the high transformer employed in the case at hand.

The procedure for designing the resonant circuit components is iterative and starts from initial values for C_p, α and n (C_p is the capacitance of the parallel resonant capacitor, $\alpha = C_p/C_s$, n denotes the transformer turns ratio). The choice of C_p and n is correlated via $C_p/n^2 \geq 50$pF, accordingly any values which satisfy this condition can be taken as starting values. There, one has to consider that the choice of α takes a large influence on the converter operating frequency range. For lower values of α, the frequency range will be wider than for higher values. This means that the choice of α is related to the upper switching frequency limit.

Following the procedure described in [2] and considering the starting values for C_p, α and n and the effect of the output rectifier stage, we have for the rectifier conduction angle θ (cf. Fig.5)

$$\theta = 2 \cdot \tan^{-1} \sqrt{\frac{4 \cdot n^2}{f_s \cdot C_p \cdot R_o}} \; . \tag{1}$$

According to [2], the combination of the output rectifier, the output capacitor, and the load can be represented by an RC equivalent circuit, R_eC_e. For the sake of clearness, we will maintain notations of quantities defined in [2] in the following although e.g. the variables R_e and C_e do not appear in the circuits presented here. With reference to [2] (cf. Eqs. (17), (21) and section V in [2]) we have

$$k_v = 1 + 0.27 \cdot \sin(\frac{\theta}{2}) \tag{2}$$

$$\beta = -0.4363 \cdot \sin(\theta) \tag{3}$$

$$\omega C_p R_e = \frac{k_v{}^2 \cdot \pi}{4 \cdot \tan(\frac{\theta}{2})^2} \tag{4}$$

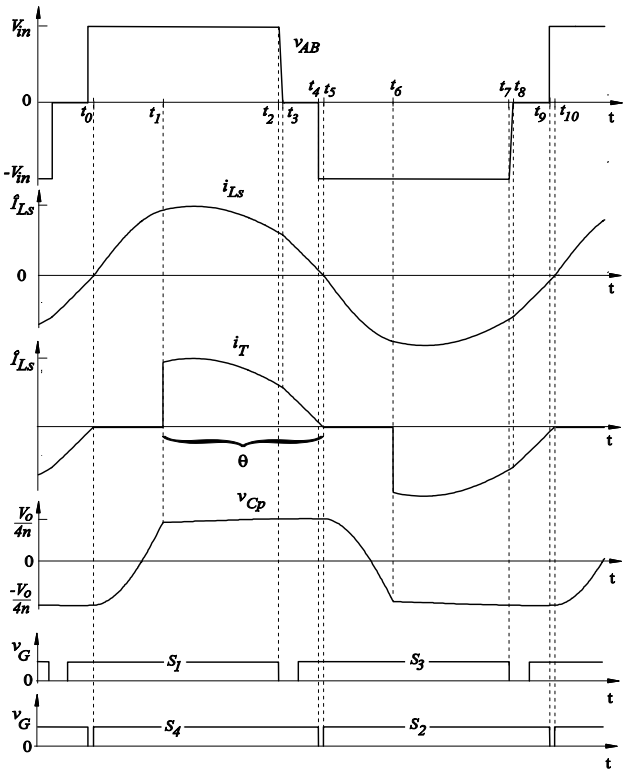


Fig.5: Time behavior of characteristic voltages and currents and of the transistor switching functions (gate drive signals) of a series-parallel resonant converter within a pulse period (t_0–t_{10}).

where

k_v – is a coefficient defining the relation between V_o transferred to the primary and the amplitude of the first harmonic of the transformer primary voltage,

β – denotes the phase displacement of the fundamentals of the primary transformer voltage and current, and

$\omega C_p R_e$ – is a dimensionless parameter.

For the AC voltage transfer ratio, i.e. for the ratio of the amplitudes of first harmonics of the transformer primary voltage and of the voltage v_{AB} we have (cf. Eq. (34) in [2])

$$k_{21} = \frac{v_{Cp(1)}}{v_{AB(1)}} = \frac{1}{\sqrt{[1-\alpha\cdot(f_{s,N}^2-1)\cdot(1+\frac{\tan(|\beta|)}{\omega C_p R_e})]^2+[\alpha\cdot(f_{s,N}^2-1)\cdot\frac{1}{\omega C_p R_e}]^2}} \quad (5)$$

in dependency of θ and of the normalized switching frequency $f_{s,N} = f_s/f_o$ where $f_o = (2\pi\sqrt{L_s C_s})^{-1}$ is the series resonant frequency.

The time behavior of characteristic waveforms as assumed for the analysis in [2] are depicted in **Fig.6**(a). In the case at hand (cf. Fig.6(b)) we have for the amplitude of the first harmonic of the converter output voltage v_{AB}

$$V_{AB(1)} = \frac{4}{\pi}\cdot V_{in}\cdot\cos(\phi)\,. \quad (6)$$

Furthermore, according to Fig.6(b) we have for the phase displacement ϕ of the first harmonic $v_{AB(1)}$ of the converter output voltage v_{AB} and of the first harmonic $i_{Ls(1)}$ of the inverter output current and/or resonant circuit input current i_{Ls}

$$\phi = \frac{\pi}{2} - \frac{D\cdot\pi}{2} \quad (7)$$

where $D = \gamma/\pi$ denotes the converter output voltage duty cycle. Considering (7) and (6) we obtain

$$V_{AB(1)} = \frac{4}{\pi}\cdot V_{in}\cdot\sin(\frac{D\cdot\pi}{2})\,. \quad (8)$$

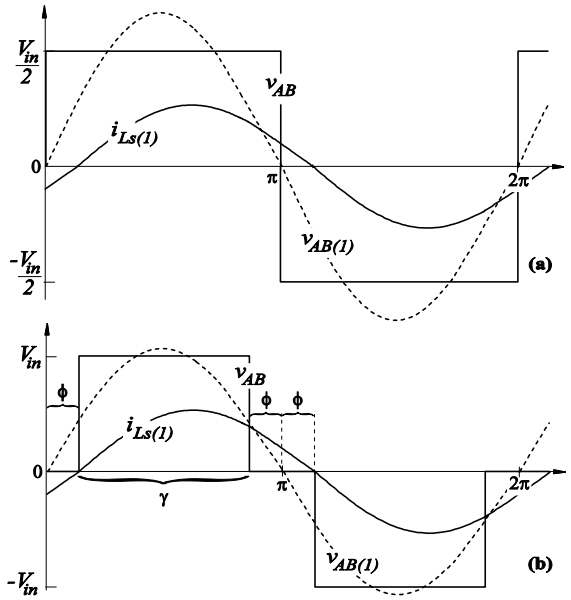


Fig.6: Time behavior of the actual converter output voltage, of the output voltage fundamental (shown dashed) and of the resonant current fundamental as considered for the first harmonic analysis in [2] (cf. **(a)**) and in this paper (cf. **(b)**), the bridge leg comprising IGBTs is switching at the zero crossing of the resonant current, i.e. at i_{Ls}=0 (ZCS).

With the relation for the input phase angle φ(*1*) given in [2] (cf. Eq.(39) in [2]), the duty cycle *D* now can be represented as a function of the normalized switching frequency $f_{s,N}$ and of the rectifier conduction angle θ

$$D = 1-\frac{2}{\pi}\cdot\tan^{-1}(\frac{1}{\omega C_p R_e}\cdot\alpha\cdot\{f_{s,N}^2\cdot[1+(\omega C_p R_e+\tan(|\beta|)^2)]-1\} - [\omega C_p R_e+\tan(|\beta|)]\cdot[1+\alpha\cdot(1+\frac{\tan(|\beta|)}{\omega C_p R_e})]) \quad (9)$$

Finally, also the output voltage can be given as function of $f_{s,N}$ and θ resulting in the voltage transfer characteristic

$$V_o = \frac{16}{\pi}\cdot\frac{k_{21}}{k_v}\cdot n\cdot V_{in}\cdot\sin(D\cdot\frac{\pi}{2}) \quad (10)$$

which is depicted in **Fig.7** for the specifications given in section IV as a function of $f_{s,N}$ and θ .

With decreasing load and/or decreasing output rectifier conduction angle θ, the peak of the resonant characteristic shown in Fig.7 moves to higher frequencies. The converter operating (switching) frequency, which has to be adjusted accordingly in order to ensure operation above resonance therefore shows a pronounced dependency on the load condition. The converter control scheme will be described in detail in section V.

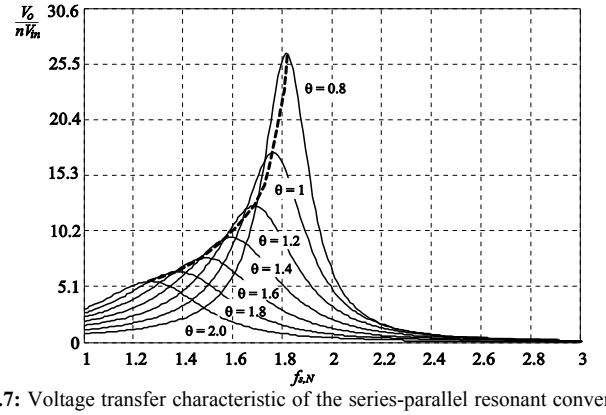


Fig.7: Voltage transfer characteristic of the series-parallel resonant converter in dependency of the normalized switching frequency and the rectifier conduction angle θ.

Now, based on the characteristics shown in Fig.7, with the starting values C_p = 12nF, n = 15 and α = 0.4, the resonant components can be specified. (The starting value for n can be derived with reference to Fig.3 for assuming high output power where the DC gain $V_o/(2nV_{in})$ approaches 2.5; for the given operating conditions (V_{in}=325V, V_o=23.5kV) this results in n≈15).

As can be seen from a finished design (cf. Fig.8(a)) the maximum duty cycle occurs in a first approximation at the maximum output voltage at maximum output current, i.e. at maximum output current and rated power (I_o=200mA, P_o=5kW and/or V_o=25kV, cf. specifications given in section IV).

Ideally, the maximum duty cycle should be set to D = 1, the operating point for the maximum output power then would be placed at the peak of the resonant characteristic. However, as for a practical circuit a dead time has to be considered for the switch-over of an inverter bridge leg and delay times of the gate drive circuits and the signal electronics do occur, we select D < 0.9 with respect to the high switching frequency.

The voltage transfer characteristic (cf. Fig.7) gives a rough idea about the possible operating points so it can be see that for θ = 2 and $f_{s,N}$ ≈ 1.35 it would be possible to achieve V_o=25kV at high output power. Based on (9) and (10) we obtain for operation at 25kV/5kW, θ = 1.995, $f_{s,N}$ = 1.34 and D = 0.831. Substituting θ and R_o= 125kΩ (equivalent to P_o=5kW@V_o=25kV) in (1) we have for the switching frequency f_s = 250kHz. Based on this the series resonant frequency f_o can be calculated and, finally, the inductance of the resonant inductor L_s can be determined. After that, the design proceeds with determining the stresses on the components.

For the above described design of the resonant tank components the variables R_o and θ were employed. However, these variables do not provide a clear representation of the system operating point. For this reason the equations which describe the system operating behavior will be given in dependency of the output voltage and output current in the following.

From a first harmonic analysis of the dependency of the system operating behavior we have for a defined output voltage V_o and output current I_o

$$Q = \frac{V_o}{4 \cdot n^2 \cdot Z_s \cdot I_o} \tag{11}$$

$$\theta = 2 \cdot \tan^{-1} \sqrt{\frac{2 \cdot \pi}{f_{s,N} \cdot \alpha \cdot Q}} \tag{12}$$

$$k_v = 1 + 0.27 \cdot \sin(\frac{\theta}{2}) \tag{13}$$

$$\beta = -0.4363 \cdot \sin(\theta) \tag{14}$$

$$\omega C_p R_e = \frac{k_v^{\,2} \cdot \pi}{4 \cdot \tan(\frac{\theta}{2})^2} \tag{15}$$

$$k_{21} = \frac{v_{Cp(1)}}{v_{AB(1)}} = \frac{1}{\sqrt{[1-\alpha \cdot (f_{s,N}^2 - 1) \cdot (1 + \frac{\tan(|\beta|)}{\omega C_p R_e})]^2 + [\alpha \cdot (f_{s,N}^2 - 1) \cdot \frac{1}{\omega C_p R_e}]^2}} \tag{16}$$

$$D = 1 - \frac{2}{\pi} \cdot \tan^{-1}(\frac{1}{\omega C_p \, R_e} \cdot \alpha \cdot \{f_{s,N}^2 \cdot [1 + (\omega C_p \, R_e + \tan(|\beta|)^2)] - 1\} - [\omega C_p \, R_e + \tan(|\beta|)] \cdot [1 + \alpha \cdot (1 + \frac{\tan(|\beta|)}{\omega C_p \, R_e})]) \tag{17}$$

$$V_o = \frac{16}{\pi} \cdot \frac{k_{21}}{k_v} \cdot n \cdot V_{in} \cdot \sin(D \cdot \frac{\pi}{2}) \tag{18}$$

with the parameters

$Z_s = \sqrt{L_s/C_s}$ – characteristic impedance of the series resonant circuit
Q – normalized load resistance,
$f_o = (2\pi\sqrt{L_s C_s})^{-1}$ – series resonant frequency
$f_{s,N} = f_s/f_o$ – normalized switching frequency
$\alpha = C_p/C_s$.

Some of the above given relations were already presented but are shown again in order to compile the whole set of equations (cf. (11)-(18)) which can be condensed into two nonlinear relations in terms of two variables, i.e. in dependency of the duty-cycle and of the normalized switching frequency. So, for given values of V_{in}, V_o, I_o, n, α, and for specified resonant circuit components, a unique duty cycle D and unique switching frequency $f_{s,N}$ can be determined numerically. Taking a set of values V_o and I_o which covers the whole operating range the variables D and $f_{s,N}$ can be graphically represented as shown in **Figs.8**(a) and (b).

Based on the solutions for D and $f_{s,N}$ and on the time behavior of the voltages and currents shown in Fig.5 and/or Fig.6, now the stresses on all power components can be calculated. There results, e.g., for the peak value of the resonant inductor current

$$\hat{I}_{Ls} = \frac{f_{s,N} \cdot \alpha}{2 \cdot n \cdot (1 + \cos(\theta))} \cdot \frac{V_o}{Z_s}, \tag{19}$$

for the turn-off current of the ZVS bridge leg power transistors

$$I_{Qoff} = \hat{I}_{Ls} \cdot \sin(D \cdot \pi), \tag{20}$$

for the peak value of the series capacitor voltage

$$\hat{U}_{Cs} = \frac{\hat{I}_{Ls}}{2 \cdot \pi \cdot C_s} \tag{21}$$

and for the RMS current stress on the ZVS power MOSFETs

$$I_{QRMS_{ZVS}} = \frac{\hat{I}_{Ls}}{2} \cdot \sqrt{D - \frac{\sin(2 \cdot D \cdot \pi)}{2 \cdot \pi}}. \tag{22}$$

A graphical representation of (19)-(22) is depicted in **Figs.8**(c) - (f), for the parameters specified in section IV. There, it can be verified that the maximum switching frequency is lower than 500kHz, and the maximum voltage across the series capacitor is lower than 1 kV accordingly the design does meet the specifications. In the case of the specifications would not be met the design

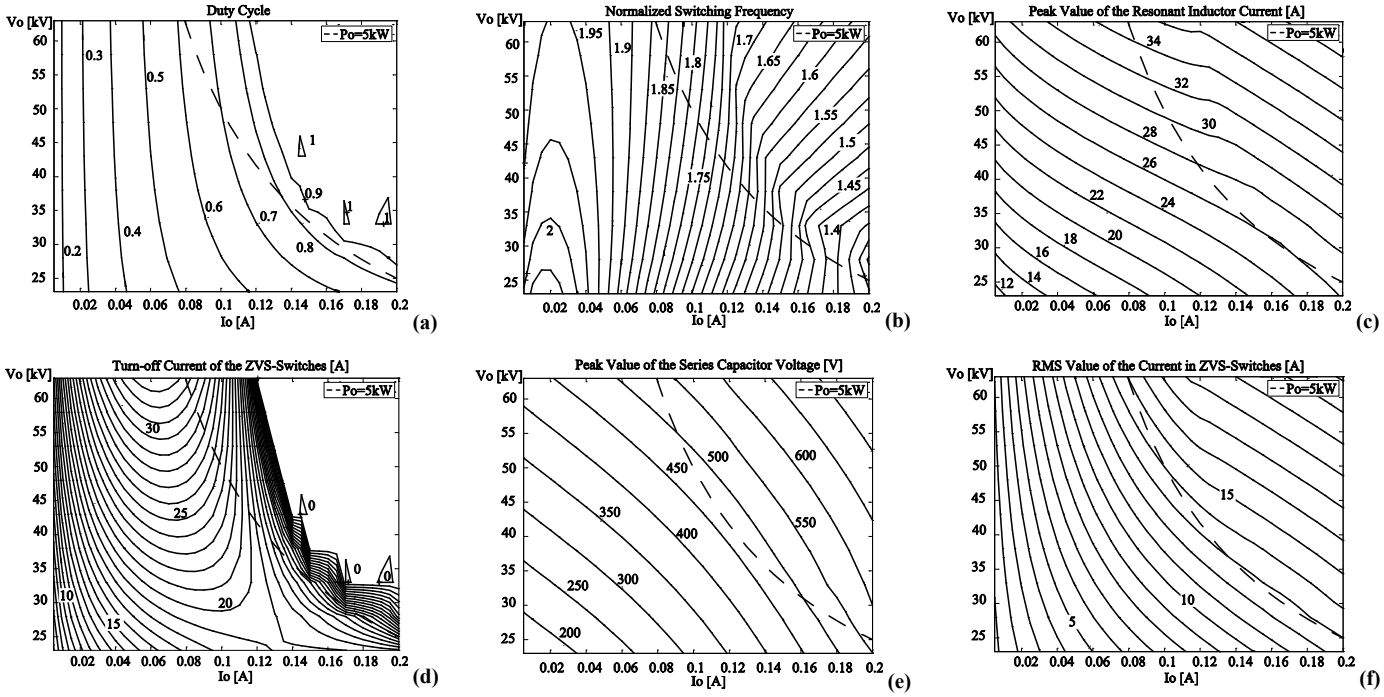
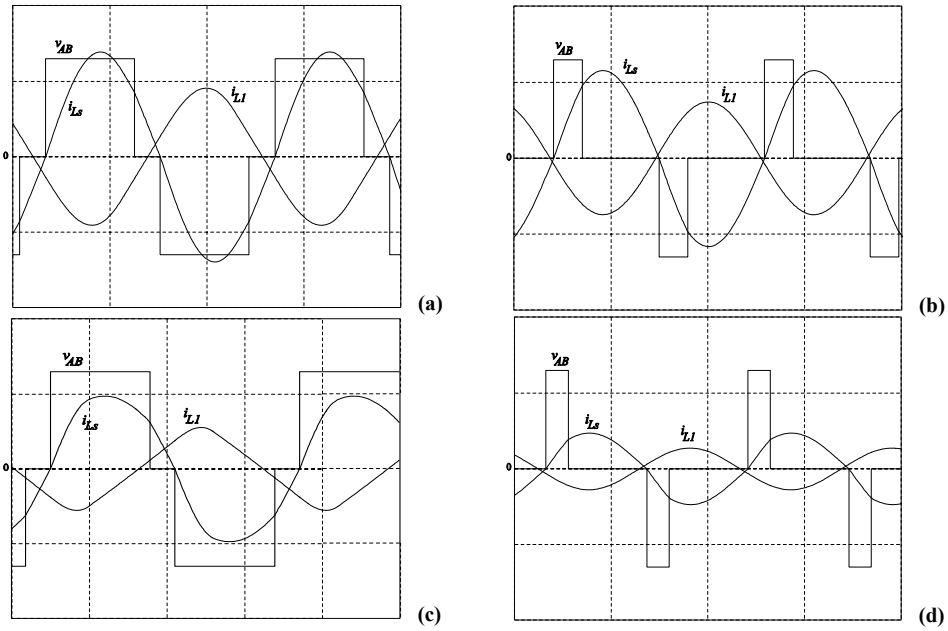


Fig.8: Duty cycle, switching frequency and stresses on the selected power components in dependency of the output current I_o and output voltage V_o.

procedure would have to be repeated with modified initial values C_p, α and n.

IV. SIMULATION RESULTS

Based on the converter design described in section III digital simulations were performed for minimum and maximum output voltage and full load and light load condition. The resulting time behavior of the inverter output voltage v_{AB}, of the resonant current i_{Ls}, and of the transformer magnetizing current i_{L1} is shown in **Fig.9** for operation at rated power and V_o=62.5kV (cf. **(a)**) and V_o=23kV (cf. **(c)**). The system behavior for operation at light load P_o < 500W is depicted in Figs.9(b) (V_o=62.5kV) and (d) (V_o=23kV).



Parameters as used for the simulations (cf. Fig.2):

V_o = 23…62.5kV
I_o = 0…200mA
P_o = 0…5kW
V_{in} = 325V
n = 15
C_1, ,C_3 = 200pF
R_s = 100mΩ
C_s = 30nF
C_p = 12nF
L_s = 24.3µH
L_1 = 1.2mH
C_{h1}', C_{h2}' = 0.5µF.

Fig.9: Digital simulation of the stationary operating behavior; inverter output voltage v_{AB} (250V/div), inverter output current i_{Ls} (25A/div) and transformer magnetizing current i_{L1} (0.5A/div); time scale: 1.25µs/div.

V. CONVERTER CONTROL

For system control and protection a state machine is employed which is not described in detail for the sake of brevity. The turn-on and turn-off of the ZCS power transistors is synchronized with the zero crossing of i_{Ls}. The gate drive signals of the ZVS power transistors are generated by comparing a constant amplitude sawtooth-shaped carrier signal s_T and the controller output voltage v_c. There, the sawtooth frequency has to be properly adjusted for the different points of operation, the amplitude of the sawtooth remains constant for all frequency variations. For generating a sawtooth with those characteristics, a concept proposed in [6] is employed which is based on a double integrator operating in closed loop. There, the reset pulse *RP* is synchronized with the zero crossing of i_{Ls}. A basic schematic of the sawtooth generator is depicted in **Fig.10**.

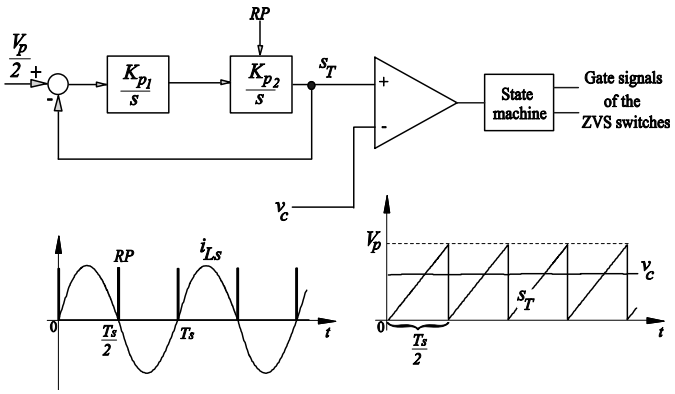


Fig.10: Control of a series-parallel resonant converter according to [6].

In the following two main aspects of the converter control will be described.

A. Operation under No Load Condition

According to Fig. 8(c) the amplitude of the resonant current does not change significantly with the output power level for higher output voltages. That means that the conduction losses under no load condition will be almost as high as for full load. This is an inherent drawback of series-parallel resonant converter systems having a large output voltage range. For solving this problem, the converter operation is switched to burst mode at low load condition. There, the output voltage is maintained in a determined tolerance band around the reference value and the power losses are reduced due to the low relative on-time of the power transistors (cf. **Fig. 11**).

B. Short-circuit Protection and Operation Above Resonance

The output short-circuit and/or overcurrent protection is of special importance in connection with ensuring high system reliability. In order to keep the current below a defined maximum value, a current limiting mode is provided in the state sequence. When the overload or short-circuit ceases, the circuit immediately returns to normal voltage mode operation.

As mentioned before, the resonant frequency of the series-parallel resonant converter is strongly dependent on the load and one has to ensure that the circuit remains operating above resonance and/or with lagging current as otherwise the free-wheeling diodes would be conducting current at the turn-on of the opposite power transistor of a bridge leg. This would result in a large reverse recovery current and/or in excessive switching losses due to the slow reverse recovery behavior of the power MOSFET internal diodes.

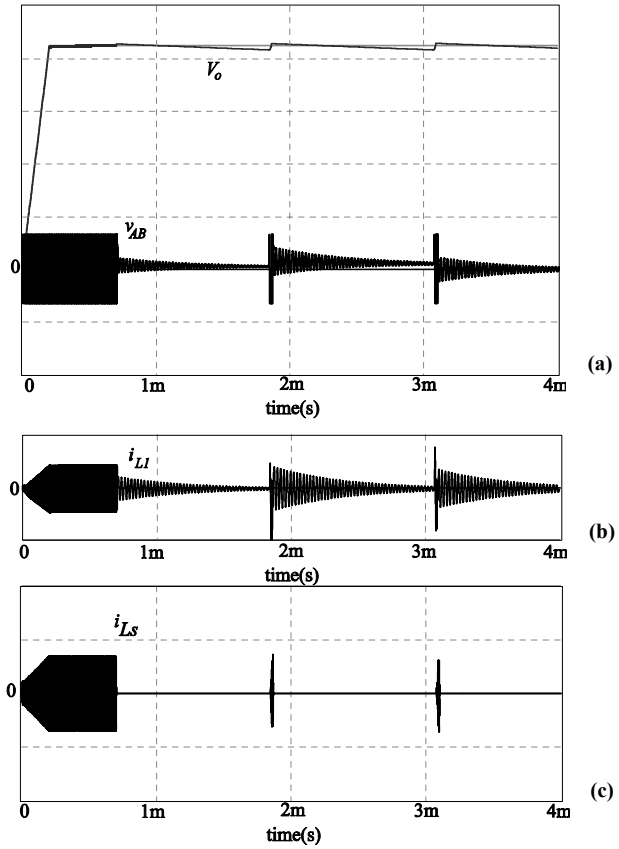


Fig. 11: Discontinuous operation at no load for an output voltage reference value of V_o^*=62.5kV; **(a)** output voltage V_o (15kV/div) and the voltage v_{AB} (500V/div); **(b)** transformer magnetizing current i_{L1} (1A/div); **(c)** resonant current i_{Ls} (50A/div).

According to **Fig.12**, operation below resonance might occur for a large load step. If the operating point changes from A to B (step-like increase of the load), the converter remains operating above resonance. However, for changing from operating point C to D (step-like reduction of the load) operation below resonance is likely to occur. Therefore, in order to ensure operation above resonance for all operating conditions a turn-on of a power transistor is only allowed if the opposite free-wheeling diode is not conducting current.

Operation below resonance could be prevented by monitoring the polarities of the voltage v_{AB} and of i_{Ls}. For regular operation, the voltage v_{AB} is always positive or equal to zero when i_{Ls} is positive. For operation below resonance, for $i_{Ls}>0$ v_{AB} can be positive or negative. So, if the current goes negative and v_{AB} is still positive the system is operating below resonance. In this case the power transistors S_1 and S_4 will be turned-off but S_2 and S_3 will not be turned-on as for regular operation; all switches will remain in the off-state until the next zero-crossing of i_{Ls}, where S_1 and S_4 will be turned-on again, restoring the regular operation above resonance.

However, the problem is alleviated in by the output capacitor, which does prevent an immediate influence of the load change on the resonant circuit and does provide time for the system control to adjust to the load condition by properly changing the duty cycle.

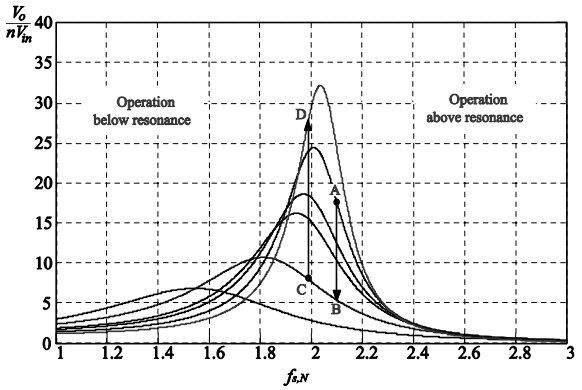


Fig. 12: Possible occurrence of operation below resonance.

The system behavior in case of changing from full load to low load is shown in **Fig. 13** where the smooth transition of the control voltage v_c and of the sawtooth signal s_T can be observed. It is important to point out that if a very faster controller is employed, operation below resonance could become critical again as the controller then does respond immediately to a load change.

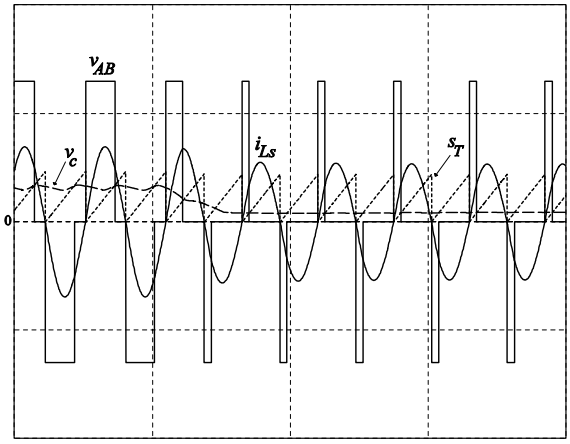


Fig. 13: Converter behavior for load change. Scales: v_{AB}: 250V/div; i_{Ls}: 50A/div; v_c: 25V/div; s_T: 25V/div

VI. CONCLUSIONS

This paper presents a detailed procedure for determining the characteristic values of the power components of a high output voltage DC-DC series-parallel resonant converter. The theoretical considerations are verified by digital simulations. Furthermore, the dynamic control behavior is discussed and a concept for ensuring operation above resonance also in case of large load transients is proposed.

In the course of the continuation of the research, a detailed analysis of the parasitics and/or of the equivalent circuit of the high-voltage transformer will be performed and the theoretical considerations will be verified on an experimental 5kW laboratory model of the system.

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