A Systematic Design Approach to Thermal-Electrical Power Electronics Integration

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Abstract

With the growing demand for integration density of power electronic systems, efficient multi-domain simulations are becoming indispensable design tools. This paper therefore presents a systematic simulation approach for coupled thermal-electrical design of power modules and systems. The presented solution is based on coupled thermal-electrical equivalent circuits and consists of optimized algorithms for accelerating the simulations by orders of magnitude, while keeping the required accuracy. With this type of simulation, load cycles for complete mission profiles can be computed and used for thermal management, reliability and lifetime estimations of power electronic systems.

1. Introduction

Driving forces for future power electronic applications are efficiency increase, size and cost reduction, and reliability. Continuous progress is being done in research, steadily getting closer to the physical power density barriers of today's power semiconductor and integration technologies [1]. Next to the semiconductor physics where new device technologies are being developed, the other important integration disciplines to be considered are: electro-magnetic interferences (EMI), cooling and structure mechanics. More and more multidisciplinary design teams using multi-domain design tools will therefore be required to remain competitive on the power electronics market. In this paper we are therefore presenting a systematic simulation approach, addressing the thermal-electrical design aspect. The proposed solution provides a computationally efficient method to calculate transient temperatures of power semiconductors and therefore to analyze short-term overload conditions and reliability.

If we focus on power modules and power electronic systems, the following design parameters are relevant regarding the thermal-electrical performance:

For power module design: In order to reach the specified high current ratings, transistors are often connected in parallel. The number of chips, their physical location inside the module and their interconnect layout are therefore important design parameters. They directly affect the loss spreading, the thermal coupling between neighbouring chips, the thermal impedance Z_{th} to the cooling surfaces, electrical and electromagnetic interferences, as well as mechanical reliability of materials and solder bonds.

For system design: At system level, thermal-electrical design starts with the underlying circuit topology. Key design parameters are the control schemes to run the application, the switching schemes to balance the losses (especially in multi-level topologies), thermal management of passive components (DC-link capacitors, AC and DC chokes, common mode chokes), EMC filters, as well as the cooling concepts and the dimensioning of heat sinks and cold plates.

One way of concurrently considering all the above design parameters, is therefore to perform coupled simulations of the thermal and electrical behaviour. The modelling requirements for such simulations are determined by the operating conditions, which are related to the application's mission profiles, temperature specifications and lifetime requirements. The main challenge is therefore the wide span of time scales of up to twelve orders of magnitude (Table 1).

Table 1: Typical time scales in power electronics

Description	Time scale [s]
Switching transients of IGBTs	10^{-9} – 10^{-6}
PWM switching schemes	10^{-6} – 10^{-3}
Thermal transients at chip level (T_j)	10^{-6} – 10^{-3}
Thermal transients at module level (e.g. build up and solder layers)	10^{-3} – 10^{+1}
Application load cycles	10^{-3} – 10^{+2}
Application mission profiles	10^{+1} – 10^{+3}

The modelling and simulation approach presented is based on the well known method of coupled thermal-electrical circuit. This work's contribution are solutions for the drawbacks related to this state-of-the-art method, implemented in a software tool to demonstrate the achieved computational efficiency. Addressed topics are:

- Efficient methods to calculate thermal resistance (R_{th}) and thermal capacitance (C_{th}) values
- Algorithms to automatically create thermal impedance matrices (Z_{th}-matrix) [2]
- Connection of electrical losses to thermal equivalent circuits in a SPICE-like circuit simulator
- Poor scaling performance if there are more than few chips modelled [3]
- Efficient and accurate solving of the non-linear electrical components and their switching and stationary losses.

2. Methodology

The basic method consists of combining thermal equivalent networks with electrical networks by connecting the electrical power losses to the loss sources of the thermal circuit. At the same time, the resulting temperatures of the thermal circuit are given back as input parameter to the electrical component models (e.g. T_j, transistor junction temperatures).

As mentioned in the introduction, the difficulties of this method are to calculate the actual R_{th} and C_{th} values of the thermal circuits. In some cases, datasheets provide thermal resistances for T_j to base plate. If more detailed Z_{th} values are needed, complicated measurements or series of thermal simulations must be performed. For that purpose, this work introduces a dedicated numerical solver for thermal conduction, based on the finite element method (FEM) [4]. A simple to use interface allows to build the power module packages with all substrate and solder layers. For each chip on the substrate, an area with a constant or time dependent thermal loss can be defined. Material properties and boundary conditions complete the model (Figure 1). The solver's main feature is to extract each Z_{th} from chip to ambient and from chip to chip and to automatically generate the entire thermal impedance matrix. The thermal equivalent circuit structures in the matrix are curve fitted, Foster-type networks (Figure 2).

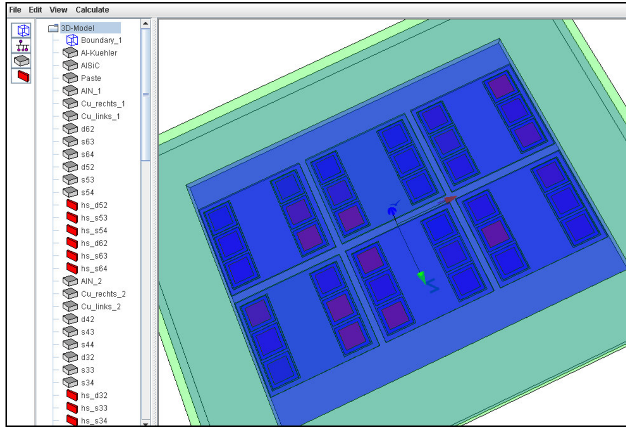

Figure 1: 3D thermal model of power module package with 36 internal chips, used for Z_{th} calculation.

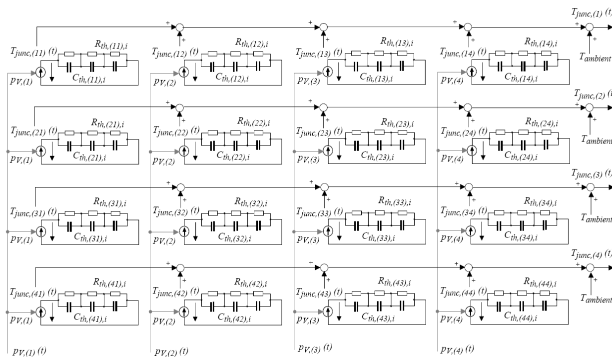

Figure 2: Circuit diagram of a 4 x 4 Z_{th}- matrix, representing 4 internal chips.

Theoretically, any commercial SPICE simulator is capable of solving coupled thermal-electrical circuits. The practical hurdles are the connection of electrical losses to the thermal network, and the poor scaling performance for large Z_{th}-matrices, especially in combination with non-linear elements (transistors and diodes). Therefore a complete new circuit simulator was implemented to solve these problems. Its main features are the direct import of Z_{th}-matrices, a dedicated thermal loss source element that can be assigned to electrical components, and an efficient, fixed-time step solver, optimized for this type of circuits [3]. The device's conduction losses are modelled with temperature dependent equivalent on-state resistors. For switching losses, a more complex approach based on look-up tables with stored switching energies (from measurements or datasheets) is used [5].

The resulting modeling and simulation flow consists now of four steps: 1) using the FEM simulations to optimize the module package, 2) extract the Z_{th}-matrix of the package, 3) import the matrix to the circuit simulator and 4) perform circuit simulations including the thermal package behavior to analyze the system-level performance. This approach allows to organize the thermal-electrical design process in a very systematic way by distributing the different tasks to individual competences, by establishing Z_{th}-matrix libraries, and by applying system simulations at early design stages.

3. Case Study: IGBT Power Module

To demonstrate the presented methodology, a power module for traction applications, is chosen as a case study. The selected device is an ABB HiPak^{TM} IGBT module, rated for 3.3 kV and 1.2 kA [6]. The module functionality consists of a single IGBT switch with an anti-parallel freewheeling diode (Figure 3). The current rating is achieved by parallel connection of 24 IGBTs (3.3 kV / 50 A) and 12 diodes (3.3 kV / 100 A), resulting in a total of 36 chips. The module package consists of six aluminum-nitride (AlN) ceramic substrates soldered on an aluminum-silicon-carbide (AlSiC) base plate. Externally, the IGBTs are connected through three pairs of power terminals for collector and emitter plus a terminal pair for the gate and the auxiliary emitter.

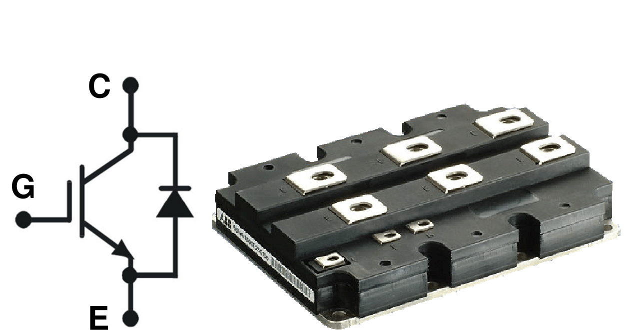

Figure 3: Function diagram and actual photograph of ABB HiPak^{TM} IGBT module.

4. Modeling

The first step is to create a 3D FEM model to extract the Z_{th}-matrix. For this, the complete substrate build-up of the HiPak™ module is modeled, which represents the main thermal path from the chips to ambient and between chips. The complete model includes the 24 IGBTs and 12 diodes (modeled as loss sources), the substrate layer stacks and the base plate. The known heat transfer coefficient of the used cold plate is added as boundary condition underneath the AlSiC base plate. The other faces of the solving space are defined as thermally isolating. The actual numbers used for the model are shown in Figure 4.

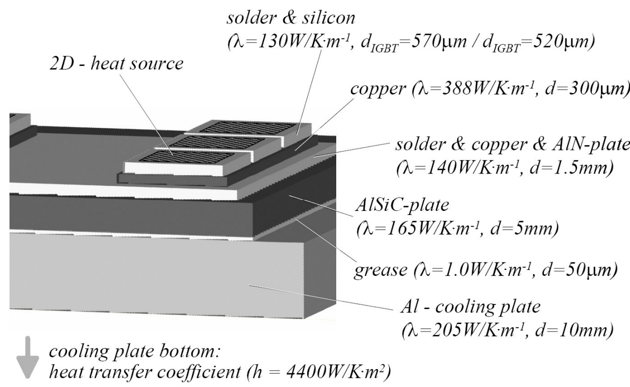

Figure 4: Thermal modeling parameters for the module package layers.

The second step is to import the Z_{th}-matrix to the circuit simulator and to attach it to the electrical circuit (Figure 5). The circuit model consists of an electrical network (left), a thermal network (centre) and the signal scopes (right). In this case, the thermal circuit is the power module symbol (Z_{th}-matrix) with the imported Z_{th}-matrix and the 36 thermal loss ports. Each port is assigned to the corresponding IGBT or diode in the electrical circuit (For the convenience of reading the circuit, the IGBTs and diodes in Figure 5 are arranged the same way as their placement in the module). An extra IGBT-diode pair is added to build a half-bridge circuit with a inductive-resistive load. The simulation parameters are set to t_d = 1 µs for the time steps and t = 2 s for the time duration. The simulation goal is to observe the semiconductor's transient junction temperatures while switching the circuit with f_{switch} = 10 kHz (initial condition are T_j=0°C).

5. Results

Figure 6 plots the two simulated seconds of load current (upper curve) and junction temperatures for two selected IGBTs (IGBT.1 and IGBT.8) and diodes (D.1 and D.9) (see Figure 5 for the location of the chips). The impact of the chip location on its cooling performance is clearly visible through the different speeds at which $T_{j_IGBT.1}$ and $T_{j_IGBT.8}$ are heating up. The mutual thermal coupling can be observed in the temperature rise of the unloaded diodes.

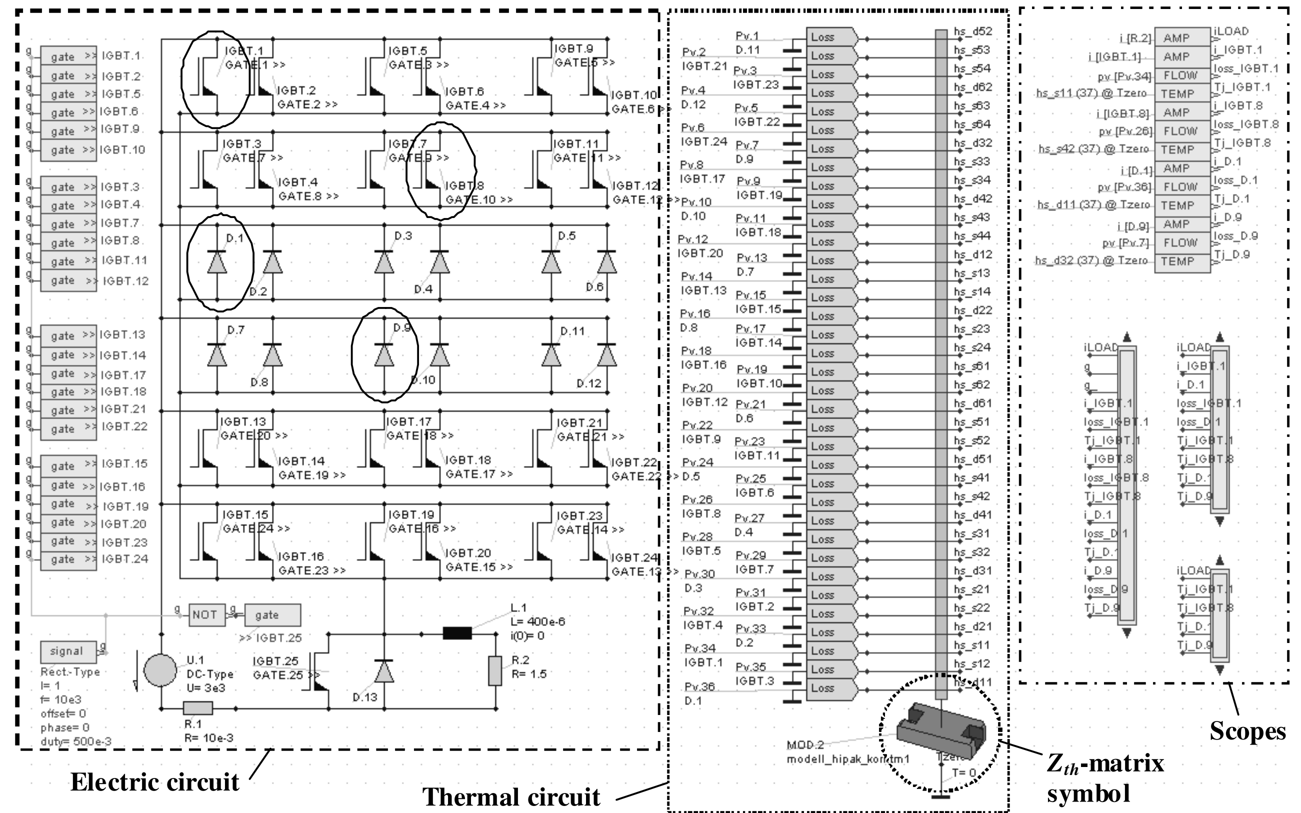

Figure 5: Circuit diagram with the power module symbol for imported Z_{th}-matrices.

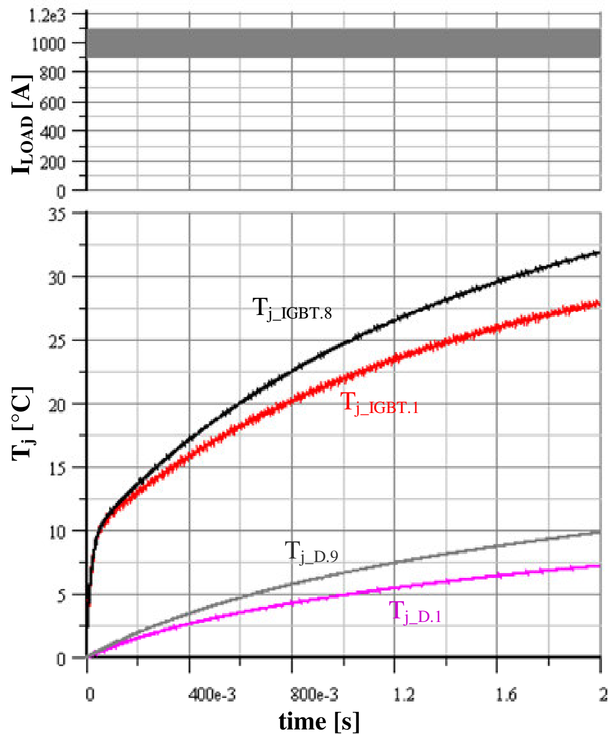

Figure 6: Transient temperature simulation of loaded IGBT and neighboring diode.

The achieved time resolution is shown in Figure 7, displaying the first millisecond of the entire simulation. In the top graph, the typical shape of the switched load and IGBT currents is nicely visible. The middle graph shows the on-state and switching losses of IGBT.1. The lower graph, finally, shows the resulting dynamic junction temperatures for the selected IGBTs and diodes. (Note: The scale of the y-axis makes the temperature peaks appear more severe than they are! The very small temperature ripple of IGBT.1 in the range of 0.010 K is due to numerical inaccuracies of the thermal impedance model.)

6. Verification

The modelling method and the computing accuracy were verified with measurements on an actual HiPak™ IGBT power module. The measurement setup consisted of an open module with removed silicone-gel and under stationary load condition (I_C = 1.2 kA). For the cooling of the dissipated power of P_{loss} = 4.48 kW, we attached the module to a water cooled cold plate (Figure 8). The module temperatures were measured with an infrared (IR) camera with 14 bits dynamic range and 284x288 pixel resolution. The IR camera was calibrated with thermocouples measuring the temperatures at several specific points on the module substrates. Painting the module surface (substrates, chips and bond wires) in black with a dedicated, non-conductive colour, allowed to get uniform emissivity in the infrared range.

The IR camera measurement for the entire IGBT module at stationary temperature is shown in Figure 9.

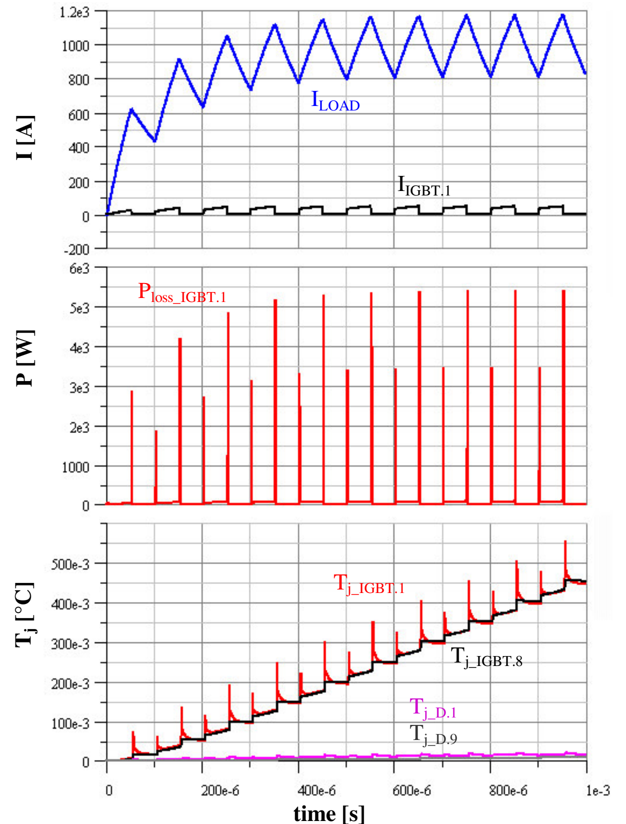

Figure 7: Simulation results detail showing the time domain resolution obtained.

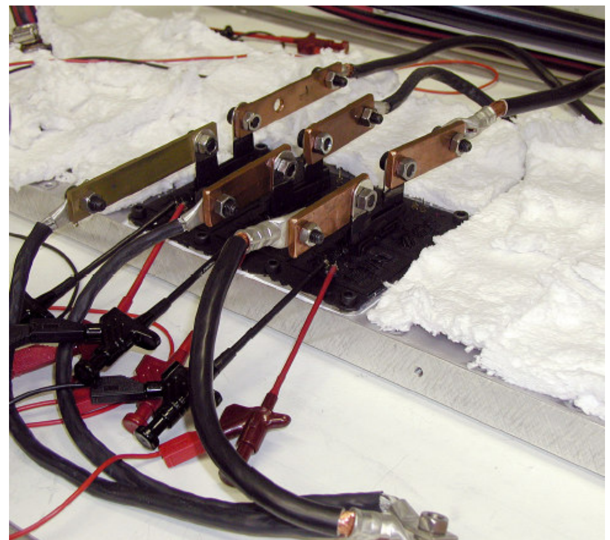

Figure 8: Test set-up for IR camera measurement showing the opened, black painted IGBT module.

The measured temperature distribution is not perfectly uniform across the module. This non-uniformity is the combination of several effects: the statistical parameter distribution of the IGBTs in the module, the not perfectly symmetric connection of the three terminal pairs to the current sources, the lateral (right to left) flow of the cooling water in the cold plate, and some non-idealities of the measurement setup. The only effect that was also

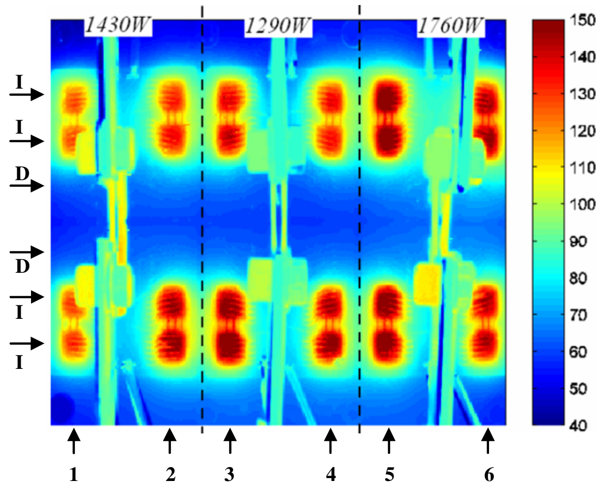

Figure 9: IR camera measurement of all IGBTs at stationary temperatures.

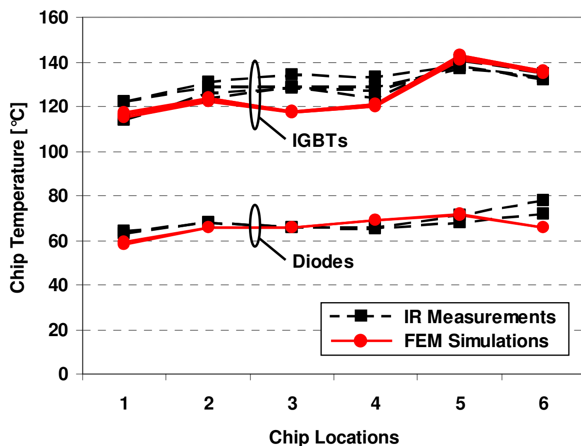

Figure 10: Comparison of measured and simulated chip temperatures across the module.

included in the measurements was the non-symmetric terminal connections, which we measured before.

Figure 10 compares the IR measurement results with the FEM simulations. The individual curves represent the chip temperatures from left to right across the module, according to the labels in Figure 9. As can be seen from the overlaid curves, both, the junction temperatures of the IGBTs as well as the lateral heating of the unloaded diodes are very accurate. Except for the IGBTs in column 3 and 4, the deviation is below 10%. More detailed investigations of the modeling accuracy of thermal coupling is reported in [4].

7. Computing Effort

The major advantage of the method presented, is that it enables efficient design processes for thermal-electrical system dimensioning in industrial power electronics product development.

The implemented 3D FEM solver for thermal conduction can be compared to any other commercial thermal FEM solver. In the case of stationary or transient simulation, the computing speed is the same. The main benefit is the built-in algorithm for automatic extraction of Z_{th}-matrices. This task has otherwise to be done by running several single thermal step responses, and by manually combining the individual curve-fitted results into a convenient form. In the case of the ABB HiPak module, the automatic extraction of the Z_{th}-matrix (36 x 36 elements) took about 50 hours on a desktop computer. As a comparison, building a 6 x 6 Z_{th}-matrix manually (using a commercial FEM solver) took roughly one week.

After the Z_{th}-matrix has been created, it is directly imported to the circuit simulator and further used for large, non-linear system level simulations. As mentioned in the introduction, the method of coupled circuit simulations is highly beneficial, in terms of computing speed, as compared to connecting a FEM model to the electrical circuit. The background idea of implementing own FEM and circuit simulators, was to have full access to the software interfaces and to the solver algorithms. This way, the created Z_{th}-matrix is prepared in a form which is directly readable for the circuit simulator. Furthermore, it allows to use accelerated circuit solver algorithms for coupled thermal-electrical networks. The acceleration procedure used in this work is the *Matrix-Splitting* approach, as presented in [3]. Depending on the size of the Z_{th}-matrix, the speed gain can be of several orders of magnitudes. In the case of the ABB HiPak module with 36 chips, the reduction of computational effort is as high as $1.7x10^6$ [3].

The resulting computing effort of about 45 minutes to simulate two real seconds of the system described in Figure 5, brings this method into an attractive time range for product development. For reliability analysis and lifetime estimation, this means that one real minute of an IGBT module's mission profile can be simulated overnight.

8. Applications

Generally, two ways of applying this method can be considered. The first is to create a detailed, high resolution model as shown in Figure 5 and to analyze the thermal-electrical characteristics of a module package. These results allow to understand the influence of the thermal coupling effects, the electrical switching scheme and the substrate layer stacks, and therefore to optimize the module technology. Secondly, when system level simulations are performed to optimize circuit topologies and control parameters, accurate thermal-electrical macro-models of the relevant circuit components are needed. In this case, the method is used to create the macro-models. Compared to the first type of application, the resolution of the macro-models can be reduced by approximating the behavior of the module with a reduced number of chips and therefore a smaller Z_{th}-matrix, thus gaining further simulation speed.

Great benefits of running such simulations are obtained for applications with critical load profiles, which

require careful dimensioning of the thermal management. Examples are elevators, robots and drilling machines with very short peak loads of few seconds or less. Also in transportation systems like suburban light weight trains, trams and hybrid cars, the cooling systems are dimensioned for an average load with a maximum peak load duration.

Finally, this method allows to compute exact load cycles for each application specific mission profile. These load cycles can then be used to improve the accuracy of lifetime and reliability estimations, with a high resolution at module and system level.

9. Conclusion and Outlook

In this paper we have presented a systematic method to simulate coupled thermal-electrical effects in power electronic modules and systems. The method consists of two basic steps: The first is to run a 3D thermal FEM simulation to extract thermal impedance matrices of relevant system components. The second step is to perform system level thermal-electrical circuit simulations with the imported Z_{th}-matrices. This method was implemented in a software tool, where each step was optimized for maximum computing efficiency: The code provides algorithm for fully automatic impedance matrix extraction, software interfaces for direct import of the extracted matrices, and a circuit solver algorithm optimized for coupled thermal-electrical networks, based on the Matrix Splitting approach. With the achieved computing speed, this method becomes very attractive for industrial product development. Most benefits are obtained in applications with pronounced load peaks and critical thermal management constraints. Future improvement of the method include the integration of reliability and lifetime estimation calculations. This can be realized by applying the computed load cycles to the component's strain-stress curves [7].

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