Thermal Analysis of a Multi-Chip Si/SiC-Power Module for Realization of a Bridge Leg of a 10kW Vienna Rectifier

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***Abstract* – For realizing a three-phase $400V_{AC}/800V_{DC}$ 10kW unity power factor PWM (VIENNA) rectifier system a novel Si/SiC multi-chip power semiconductor modules (IXYS VUM26B) facilitating switching frequencies up to 500kHz is employed. Direct water cooling of the modules base plates does significantly reduce the size of the cooling system. As the heat flow is directly from the power module into the water the cooling system can be realized using non-metal heat sink what does reduce common-mode EMI emissions. In this paper it is shown how the time behavior of the power module semiconductor junction temperatures over a mains period can be calculated with high accuracy by combining simple thermal equivalent circuits and stationary thermal simulations of the cooling system. Furthermore, the determination of the switching losses by circuit simulation based on experimental data is discussed and the power transistor and power diode junction temperatures are investigated for different operating points of the rectifier system.**

1. Introduction

For the simulation of a Vienna Rectifier [1] (cf. **Fig.1**) operating at 500kHz switching frequency, the time step (assumed to be constant) should not exceed $dt=T_P/100=20ns$ (T_P denotes the pulse period) in order to achieve sufficiently accurate results. Accordingly, a period of a 50Hz mains is formed by $1/f_N)/dt=20ms/20ns=1,000,000$ time steps what does result in high execution times even for a circuit simulators being optimized for power electronic systems.

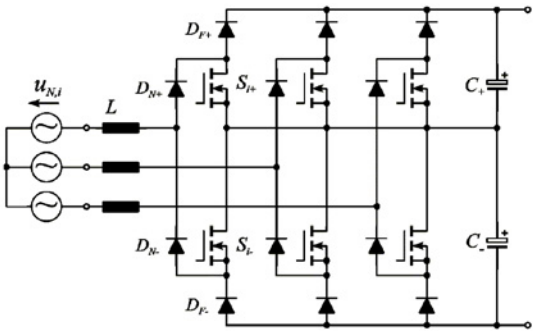


Fig.1: Power circuit of the Vienna Rectifier employing two power transistors in each bridge leg.

For determining the time behavior of the junction temperatures of the power semiconductors the circuit simulation has to be coupled with a thermal simulation. As, there, in generally a three-dimensional analysis has to be performed and often fluid dynamics and/or radiation has to be considered the computational effort of a stationary thermal simulation is extremely high. Another problem besides the required large number of time steps is the large thermal time constant introduced by the cooling system which might be in the order of a few seconds (for direct water cooling) and up to one hour (for a large heat sink with fan). Furthermore, due to numerical stability problems it is often difficult to start the thermal simulation from a stationary operating point what would reduce the effect of large thermal time constants. Therefore, the direct coupling of a circuit simulator and a thermal simulator can be done easily only in theory. In practice, the solution of the directly coupled problem would require weeks instead of hours and is not sensible, therefore.

In this paper it is shown how the time behavior of the junction temperatures of the power semiconductors of a three-phase unity power factor PWM (Vienna) Rectifier system over a mains period can be calculated with high accuracy by combining simple thermal equivalent circuits and stationary thermal simulations of the cooling system. Furthermore, the determination of the switching losses by circuit simulation based on experimental data is discussed and the power transistor and power diode junction temperatures are investigated for different operating points of the rectifier system. All considerations given are related to the realization of a novel Si/SiC multi-chip power semiconductor module (IXYS VUM26B) realizing one bridge leg of a $400V_{AC}/800V_{DC}$ 10kW VIENNA rectifier operated at 500kHz switching frequency.

2. Determination of Semiconductor Losses by Circuit Simulation

The following considerations are referring to the circuit simulator CASPOC [2] which does facilitate a fast and numerically stable simulation of power electronic systems. As CASPOC does not employ special means to determine switching and/or conduction losses of power semiconductors, the proposed concept for loss calculation can be transferred easily to other standard circuit simulators. For the latest CASPOC version it is also possible to vary the parameters of the power switches (voltage drop U_F or on-resistance R_{ON}) in dependency of the calculated junction temperatures what results in very accurate modeling of the system behavior, but is out of the scope of this paper.

The switching losses are dependent on the switching behavior of the transistor and the free-wheeling diode and on the power

circuit layout. Therefore, a sufficiently accurate determination of the switching losses by numerical simulation is not possible with sensible effort. Accordingly, the switching losses are calculated based on measurement derived for the transistor-diode combination to be employed in the power module (cf. **Fig.2**). There, based on previous measurements [3], [4] on a CoolMOS-SiC-free-wheeling diode combination, the dependency of the sum of the transistor turn-on and turn-off switching energy loss on the switched current is described by a loss factor

$$k_{400V/125°C} = k_{SR,ON}\big|_{400V/125°C} + k_{SR,OFF}\big|_{400V/125°C} \approx 5.2\,\frac{\mu Ws}{A} \tag{1}$$

(cf. **Tab.1**).

In Fig.2 the signal block *ZZ1* delays the input signal *SR* by one-time-step time. Combining the output and the input of *ZZ1* by an *XOR* does result in a one-time-step wide output pulse of height *1*. Accordingly, a division by the time step *DT* results in a pulse-time-area equal to one. This pulse is multiplied by the loss factor *K_SR* (cf. Eq.(1)) and the switched current *I_SR* what generates a switching loss power signal *PV_SWITCH_SR*.

Remark: In Fig.2 the normalized pulse does occur for each turn-on and turn-off switching action, but after multiplication with the product (*K_SR* · *I_SR*) all pulses at turn-on instants are eliminated as *I_SR* is still equal to *0* within one time step subsequent to a switching action (cf. Fig.4(b)). Accordingly, despite employing the factor *K_SR* which does characterize the *total* switching losses for the multiplication the switching losses are calculated correctly.

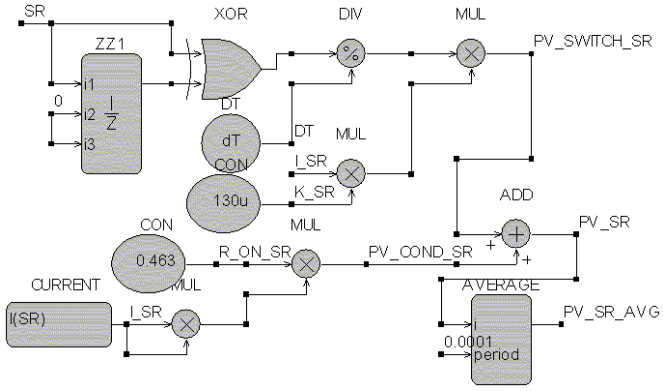


Fig.2: Calculation of the switching losses *PV_SWITCH_SR* and conduction losses *PV_COND_SR* of a power MOSFET in CASPOC. The block *AVERAGE* performs a running average over $T_{AVG}=2/f_P=100\mu s$ (factor 2 improves numerical stability of the averaging), cf. Fig.5; *SR* is the gate signal of the switch with values *0* or *1*.

In order to reduce the simulation time the rectifier switching frequency is reduced by a factor *25* from f_P=*500kHz* to *20kHz*, where the inductance of the input inductors is set to *L=350*µH in order to achieve a largely sinusoidal and/or low ripple current shape. Further simulation parameters are an output power of P_{OUT}=10kW, a DC output voltage of U_{OUT}=800V and a peak value of the mains phase voltages of $\hat{U}_N$=330V (corresponding to a modulation index of $M=2\hat{U}_N/U_{OUT}=0.83$). The simulation time step is increased from *dt=20ns* to *500ns*, where, in order to correctly calculate the switching losses *K_SR* has to be increased by a factor of *25*.

Power MOSFET	Diodes D_F	Diodes D_N
$R_{DS,ON,125°C}$=0.463 Ω	U_{DF}= 1.4V	U_{DN}= 0.85V
$k_{400V/125°C}$=5.2µWs/A	$r_{DF,125°C}$=0.125 Ω	$r_{DN,125°C}$= 0.04 Ω

Tab.1: Characteristics of the power semiconductors to be employed in the module IXYS VUM26B realizing a bridge leg of the 10kW/500kHz Vienna Rectifier. In a first approximation a linear dependency of the total transistor switching energy loss per pulse period (on-off-on switching action) is assumed [5].

The calculation of the conduction losses of the power MOSFET is according to

$$P_{V,COND} = R_{ON,125°C} \cdot I^2_{SWITCH,RMS} \tag{2}$$

(cf. Fig.2). Finally, the total transistor losses $P_{V,SR}$ are calculated by the summation of the switching losses $P_{V,SWITCH}$ and the conduction losses $P_{V,COND}$.

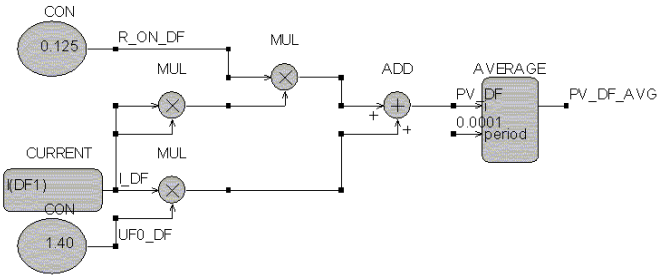


Fig.3: Calculation of conduction losses of a diode.

For the power diodes the switching losses are neglected in a first approximation and the conduction losses are calculated using

$$P_{V,DIODE} \approx P_{V,COND} = U_{F,125°C} \cdot I_{DIODE,AVG} + r_{ON,125°C} \cdot I^2_{DIODE,RMS} \tag{3}$$

as shown in **Fig.3** based on the parameters compiled in Tab.1. **Figure 4** shows the resulting time behavior of the power losses of transistor *SR+*, diode *DF+* and the upper mains diode *DN+* as calculated using circuit simulation (cf. Figs.2 and 3).

Because the thermal time constants of power semiconductors are large compared to a switching period (see section 3.1) the running average value of the power losses (cf. **Fig.5**) is sufficient for defining the time behavior of the dissipated power. The average losses of the power semiconductors and/or of a bridge leg of the rectifier system to be contained in the power module over a mains period are compiled in **Tab.2**.

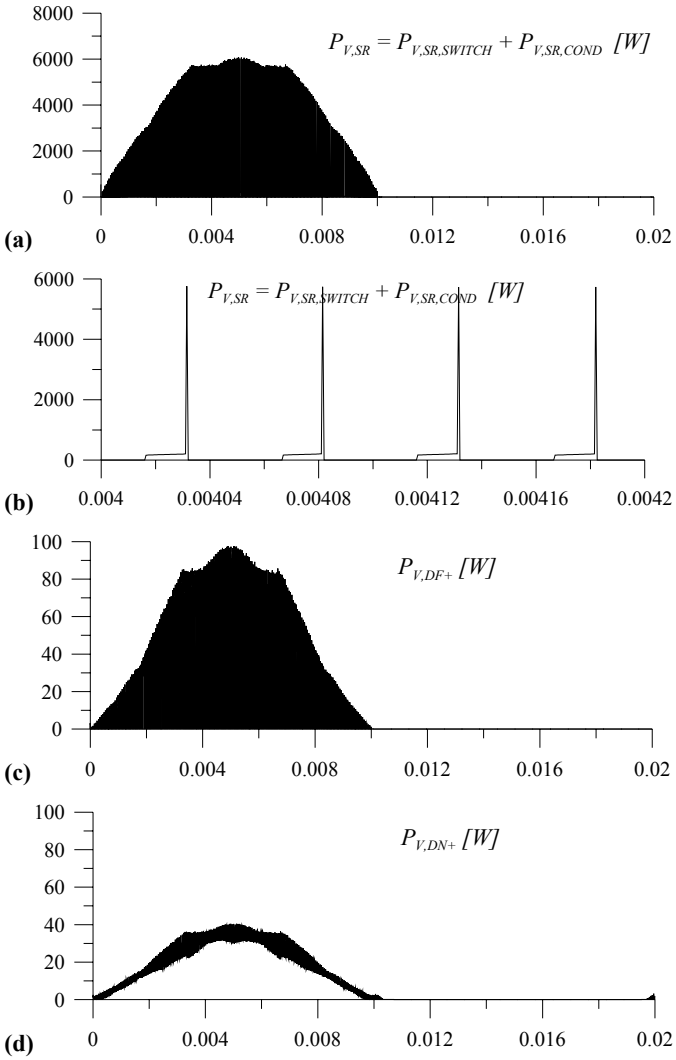


Fig.4: (a) Time behavior of the total power loss of transistor *SR+* within one mains period; **(b)** detail of (a), the height of the pulses modeling the switching energy loss is proportional to the inverse value of the simulation time step *dt=500ns*. **(c)** Time behavior of the conduction losses of the free-wheeling diode *DF+* (diode switching losses are neglected); **(d)** time behavior of the conduction losses of the mains diode *DN+*.

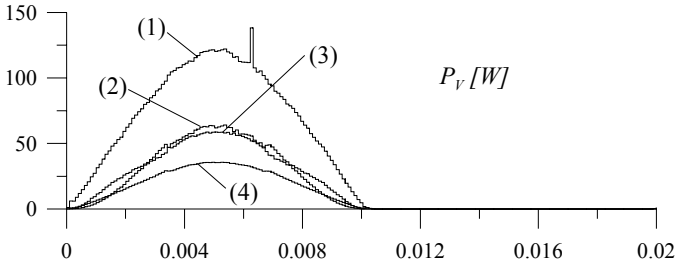


Fig.5: Running average ($T_{AVG}=2/f_P=100\mu s$) of the instantaneous losses shown in Fig.4; (1) total losses of the power transistor *SR+*, (2) conduction losses of *SR+*, (3) conduction (total) losses of diode *DF+*, (4) conduction (total) losses of diode *DN+*. The peak in waveform (1) is a numerical effect of the circuit simulation but does not influence the following thermal simulation because of the large thermal time constants.

Semiconductor Power Losses
$P_{V,SR+,AVG}$ = 36W
$P_{V,DF+,AVG}$ = 15W
$P_{V,DN+,AVG}$ = 10W
$P_{V,MODULE}$ = 122W

Tab.2: Average power losses over one mains period (*20ms*) for one power transistor, one free-wheeling diode, one mains diode of the Vienna Rectifier depicted in Fig.1; furthermore shown: Total losses of the power module (realizing one bridge leg of the rectifier system) based on the numerical simulations according to the parameters given in Tab.1 and/or to the waveforms given in Fig.4 and Fig.5.

3 Thermal Simulation by Computational Fluid Dynamics (CFD) Software ICEPAK

A RC thermal equivalent circuit provides a very accurate model for heat conduction in solid materials. All other heat transfer mechanisms (natural and forced convection, radiation) cannot be modeled that way due to their different physical behavior. For determining the temperature distribution within a system where heat convection cannot be neglected (as typically given for cooling in power electronics), one has to calculate the velocity distribution of the cooling fluid (e.g., air or water) and based on this the thermal resistance of the fluid layers at the boundaries. Complex thermal problems of this kind can be solved using finite-element methods incorporated in computational fluid dynamics (CFD) solvers where also radiation can be taken into account. Accordingly, all relevant heat transfer mechanisms can be simulated, but the numerical calculation of temperature distributions causes a very high computational effort. For the following considerations the CFD software ICEPAK [6] will be employed.

3.1 Direct Water Cooling

For direct water cooling, where the water is in direct contact with the power module base plate, the heat sink can be made from non-metal material (plastic or ceramic) what does significantly reduce common-mode EMI as compared to employing an electrically conductive heat sink. This is especially important for high switching frequency and/or high switching speed.

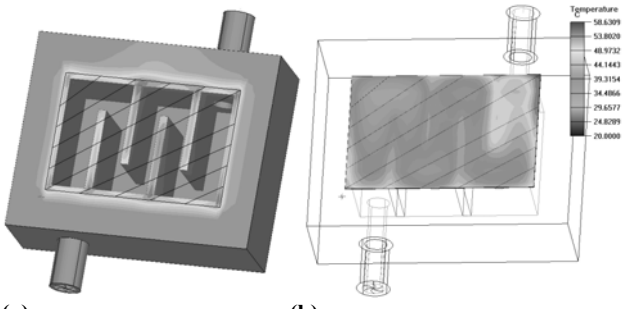


Fig.6: The cooling system including fins for forcing a turbulent water flow is made solely from PEEK material which is easy to manufacture but shows very poor thermal conductivity ($\lambda_{th}=0.25W/Km$); **(a)** geometry of the water cooling system, **(b)** temperature distribution across the thermal power source (*150W*, homogenously distributed) characterizing the base plate of the power module.

In the following the water cooling system shown in **Fig.6** will be analyzed. The system has been designed for achieving turbulent water flow in order effectively remove the thermal power but has not been geometrically optimized concerning minimum thermal resistance in a first step.

The step responses shown in **Fig.7** cannot be taken to set up a useful thermal equivalent circuit model of the direct water cooling system as the temperature distribution across the surface of the rectangular heat source is not uniform but shows differences up to *30°C* (Fig.6(c)) although the heat dissipation is constant over the power source surface. For the actual power module the power losses will be concentrated to the chip areas what will further increase the temperature differences.

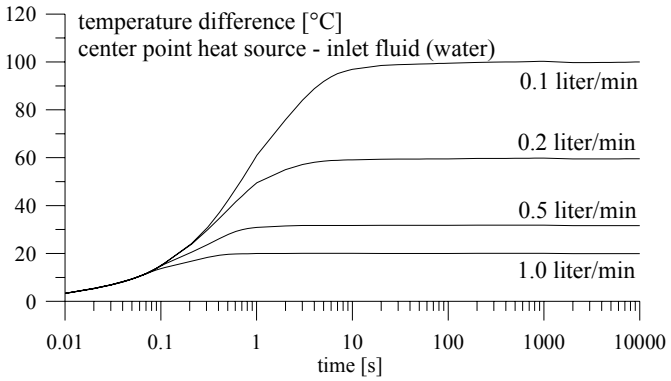


Fig.7: Step response of the temperature at the center of the rectangular thermal power source shown in Fig.6(c) when P_V=*150W* is injected for different water flow rates (water temperature 20°C).

The thermal time constants are much smaller than for solid heat sinks as the temperature drop inside the liquid occurs in a thin liquid layer close to the surface boundaries [7], [8]. This thin liquid layer can be characterized by a thermal resistance and a small thermal capacitance. However, the resulting thermal time constant is still large compared to a mains cycle (*20ms*) so that a stationary thermal system simulation is sufficient for the calculation of the temperature distribution at the interface of module base plate and water (see section 4.2).

3.2 Power Module VUM26B

The internal layout of the power module IXYS VUM26B realizing a bridge leg of a six-switch Vienna Rectifier is depicted in **Fig.8**. There, the freewheeling-diodes are implemented by a parallel connection of three 600V SiC Schottky diodes due to the low current carrying capability of a single device. Two 600V CoolMOS transistors are employed for realizing *SR+* and *SR−*, the rectifier diodes *DN+*, *DN−* and are conventional 600V Si diodes. The power semiconductor chips will be denominated in the following according to the numbers shown in Fig.8.

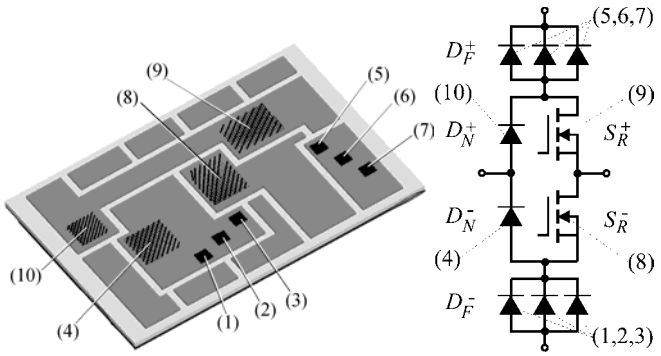


Fig.8: Internal layout of the power module IXYS VUM26B (DCB ceramic substrate, *0.63mm* Al_2O_3 with *0.3mm* Cu layer on both sides); interconnection of the power semiconductors by copper tracks and wire bonds (not shown). *Geometry:* base plate: *25x36mm²*; chips (1,2,3), (5,6,7): *1.5x1.5mm²*; chip (4): *4.5x4.5mm²*; chip (10): *3.3x3.3mm²*; chips (8,9): *4.5x5.7mm²*.

In order to describe the thermal behavior of the power module independent of the type of heat sink, a constant uniform heat sink temperature (*20°C*) has been defined for the thermal simulation. This has been achieved by setting the thermal conductivity of the heat sink material to extremely high values (80 time higher than copper) and cooling the heat sink to *20°C*. As a result, the thermal model of the power module derived in this section is independent of the heat sink and can be coupled with various heat sinks in later investigation (see section 4.3).

The mutual thermal coupling of all power semiconductors is neglected in the following despite the temperature distribution at the interface of the base plate (which is formed by a *0.3mm* Cu layer) to the water is not homogenous (cf. section 4.2). In practice, temperature differences of up to *40°C* do occur across the Cu layer (e.g., for chips (8) and (10)) and do cause heat flow which however remains limited to relatively low values as can be verified by a more detailed analysis. Neglecting the mutual thermal coupling will therefore result in only slightly higher equivalent thermal resistance values.

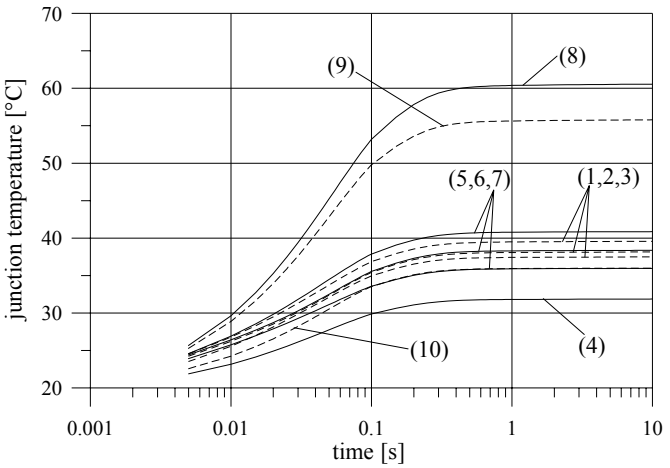


Fig.9: 3D-FEM simulation (ICEPAK) of the step response of the center point temperatures of the semiconductor chips for constant temperature of the heat sink (20°C).

Chip	$R_{th,1}$	$R_{th,2}$	$R_{th,3}$	$C_{th,1}$	$C_{th,2}$	$C_{th,3}$
1	0.454	2.478	0.565	3.4m	7.2m	255m
2	0.623	2.398	0.609	1.6m	11.0m	204m
3	0.845	2.452	0.617	2.4m	9.6m	197m
4	0.256	0.640	0.291	18.2m	21.7m	300m
5	1.058	2.508	0.605	3.1m	9.5m	206m
6	0.660	2.371	0.634	1.4m	11.3m	193m
7	1.752	1.086	0.353	5.7m	40.8m	175m
8	0.196	0.633	0.297	22.3m	21.5m	253m
9	0.115	0.599	0.280	22.0m	20.6m	256m
10	0.532	0.758	0.309	15.7m	22.0m	239m

Tab.3: Thermal resistances $R_{th,i}$ *[K/W]* and thermal capacitances $C_{th,i}$ *[Ws/K]* describing the thermal behavior of the power semiconductors contained in the power module IXYS VUM26B based on Fig.10.

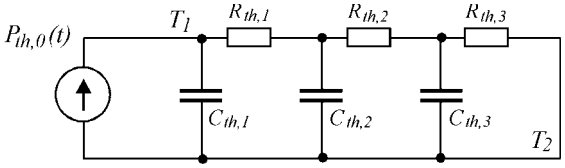


Fig.10: Thermal equivalent circuit employed for each power semiconductor of the power module. T_1 denotes the junction temperature, T_2 is the temperature of the copper layer on the bottom side of the ceramic substrate directly below the chip.

The step response of all chip temperature has been simulated using ICEPAK based on the semiconductor power losses specified in Tab.2. The resulting temperature time behavior is shown in **Fig.9**. The simulation did take about 6 hours and was producing roughly 700MB of data on a 2.2GHz PC. Based on Fig.9 a thermal equivalent circuit according to **Fig.10** has been derived for each power semiconductor; the equivalent circuit parameters were determined by a search algorithm and are compiled in **Tab.3**.

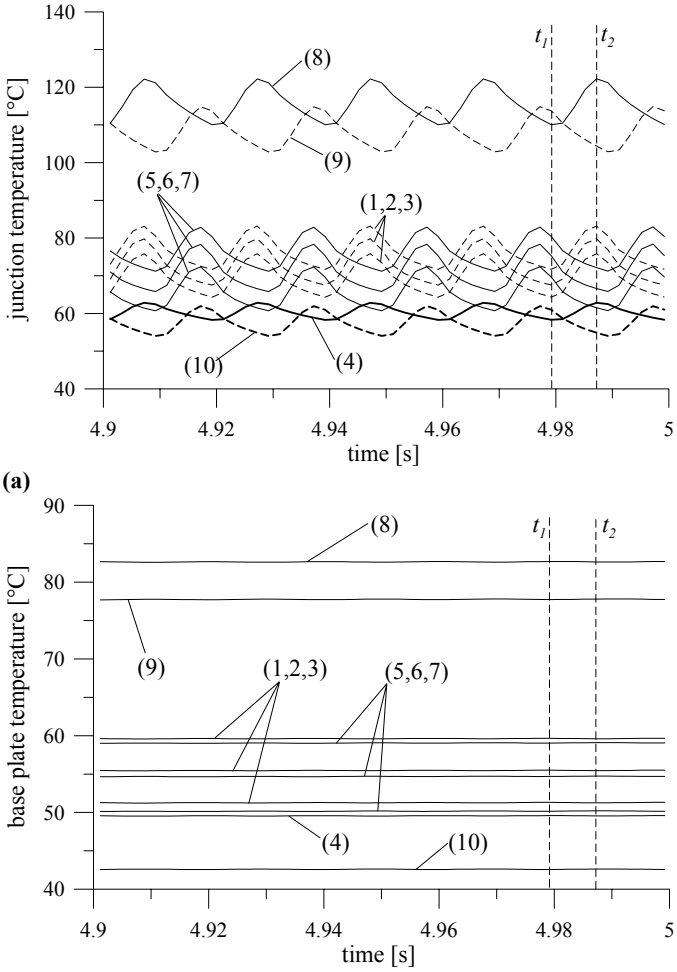
4. Simulation of the Transient Behavior of the Chip Temperatures

4.1 Full Transient Thermal Simulation in ICEPAK

The chip temperatures inside a power module IXYS VUM26B are calculated for direct water cooling according to Fig.6, a water inlet temperature of *20°C* and a mass flow rate of *1.0 liter/min*.

In ICEPAK time step width can be set in dependency of the time, and the time behavior of the power dissipated by a power source can defined. In the case at hand the power semiconductors are modeled as independent power sources where dissipated power is defined by the waveforms shown in Fig.5.

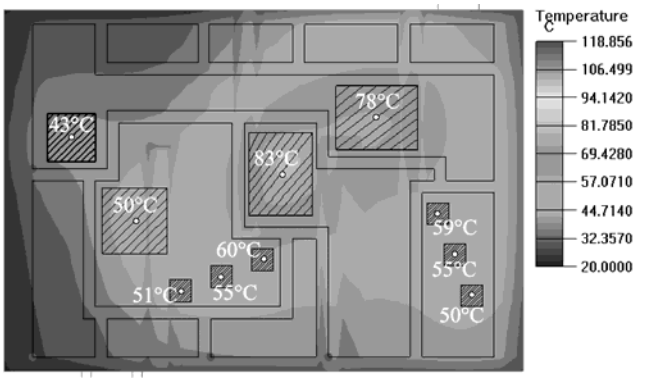
Due to the large thermal time constants of the cooling system (cf. Fig.7) it takes a minimum of about 5 seconds to reach a steady state. Stetting larger time steps for the first 3 or 4 seconds has to be done carefully as the simulator tends to be instable when the time step is suddenly decreased to much smaller values, especially if the fluid behavior is turbulent. The thermal simulation was started with a time step of *dt=30ms* which was finally reduced to *dt=1ms* what is small enough for accurately considering the time behavior of the power losses (cf. Fig.5).



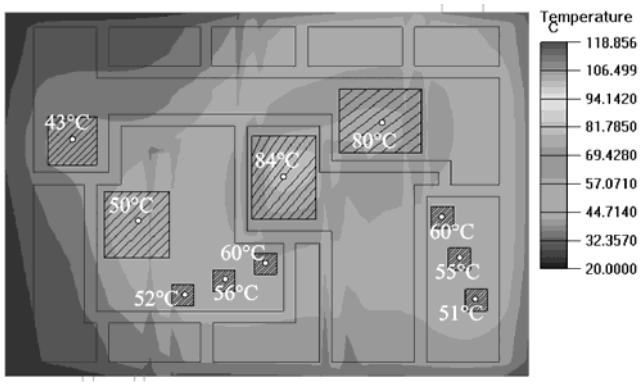
(a)

(b)

Fig.11: Transient thermal simulation of the power module IXYS VUM26B using ICEPAK; losses of the power semiconductors defined according to Fig.5. **(a)** time behavior of the chip junction (center point) temperatures; **(b)** temperatures in the copper layer on the bottom side of the ceramic substrate directly below the center points of the chips.



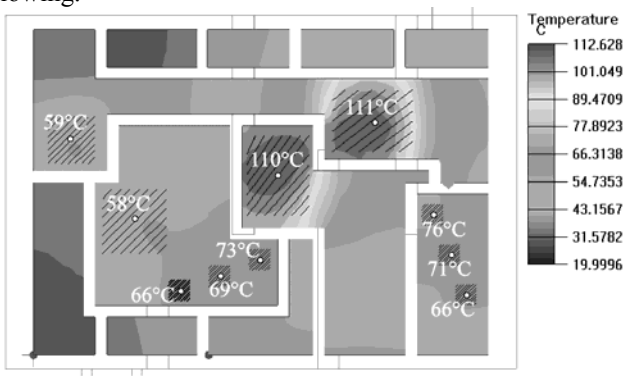
(a)



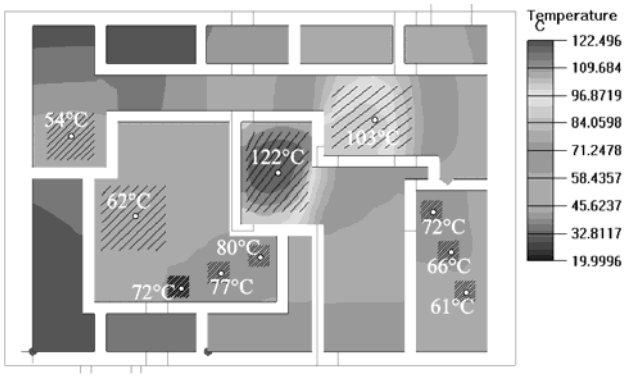
(b)

Fig.12: Temperature distribution at the bottom Cu-layer of the ceramic substrate **(a)** at time t_1 (and/or t_2, temperatures are approximately constant over t, see Fig.11(b)) and **(b)** for a *stationary* simulation; power losses of the individual power semiconductors specified according to Tab.2.

The simulation results are shown in **Fig.11** and snapshots of the temperature distribution at certain instants are depicted in **Fig.12** and **Fig.13**. The simulation took about 10 hours on a 2.2GHz PC and produced more than 3GB data. Therefore, such simulations become impractical for analyzing the influence of different parameters like different mass flow rates of the cooling liquid, different types of water cooling systems, or different operating points of the rectifier system (cf. section 5). An approach significantly reducing the simulation time by combining stationary thermal simulations in ICEPAK with circuit simulations in CASPOC will be presented in the following.



(a)



(b)

Fig.13: Temperature at the center point of each chip **(a)** at time t_1 and **(b)** time t_2 as derived from a *transient* simulation using ICEPAK.

4.2 Stationary Thermal Simulation using ICEPAK

As Fig.12 shows, the temperature is heavily varying over the substrate bottom Cu-layer. Accordingly, for an accurate thermal model of the power module the interface temperature information has to be combined with the RC thermal equivalent circuits of the power semiconductors.

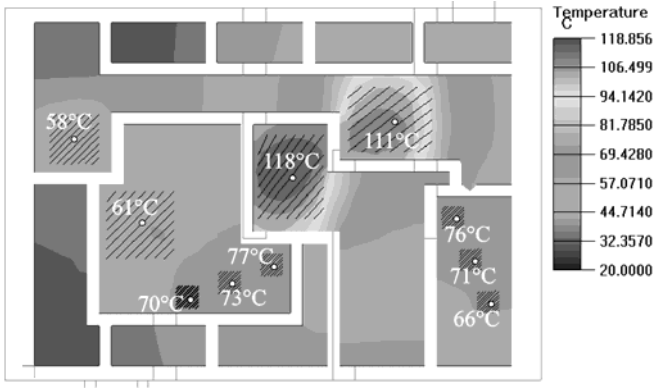


Fig.14: Temperature distribution at the center point of each chip for a *stationary* simulation using ICEPAK where the power losses of the power semiconductors are specified according to Tab.2.

The temperature distribution over the module bottom Cu-layer is in good approximation time-independent and can, therefore, be calculated by a stationary ICEPAK simulation where the thermal power of the chips is defined by the average value over one mains period (cf. Tab.2). There, the simulation time is about 40min what is just 7% of the computational effort required for a conventional transient thermal simulation.

As can be seen from Fig.11(a) and Fig.13 a significant time dependency of the junction temperatures does occur as the thermal time constants are lower that the mains period $T_N=1/f_N=20ms$. Therefore, a stationary thermal simulation (Fig.14) is not sufficient for an accurate determination of the power semiconductor junction temperatures.

4.3 Transient Thermal Simulation by Combination of Thermal RC Equivalent Circuits and Stationary Temperature Information

For neglecting the minor thermal coupling of the different power semiconductors each chip can be modeled by a simple RC equivalent circuit (cf. Tab.3 in section 3.2). There, the temperatures below the chips, i.e. in the Cu-layer on the bottom side of the ceramic substrate (as determined by a stationary thermal simulation, cf. Fig.12(b)) can be used as reference temperatures (cf. **Fig.15**). Based on this, for controlling the current sources of the equivalent circuit (cf. *A1* and *A2* in Fig.15) by the running average of the semiconductor power losses (cf. Fig.5) the transient thermal behavior of the chips of the power module can be simulated in short time using only a circuit simulator.

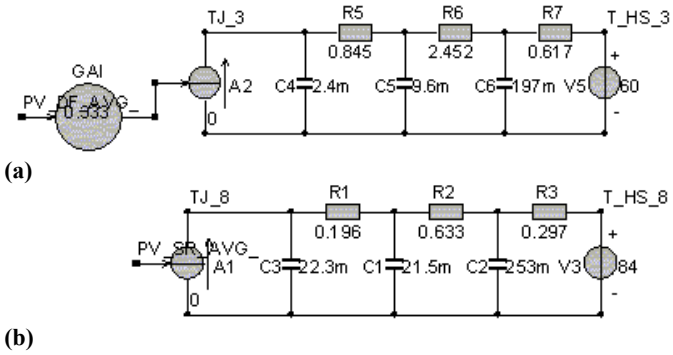


Fig.15: Thermal equivalent circuits of the chips (3) (cf. **(a)**) and (8) (cf. **(b)**) employed for the determination of the time behavior of the junction temperatures by circuit simulation; the reference temperatures are defined by voltage sources *V5* and *V3* with voltage (temperature) values resulting from a stationary thermal simulation (cf. Fig.12(b)). For chip (3) the power losses *PV_DF_AVG_* have to be divided by a factor of 3 (block *GAI*) as the free-wheeling diode *DF–* is formed by a parallel connection of three equal chips (1), (2), (3) (cf. Fig. 8).

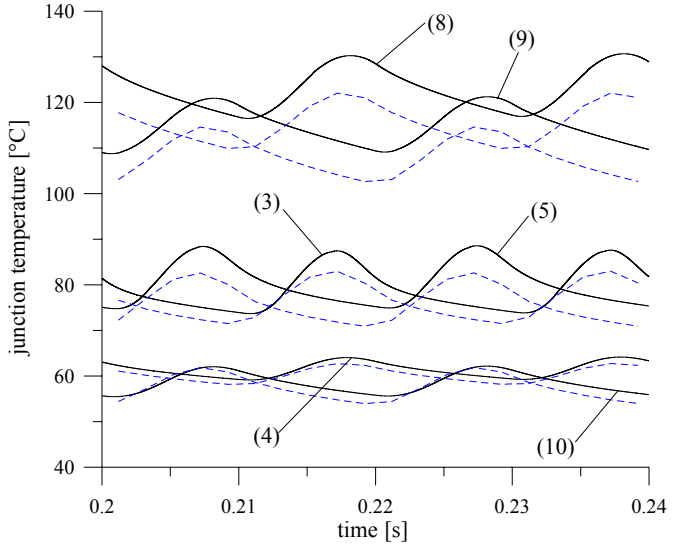


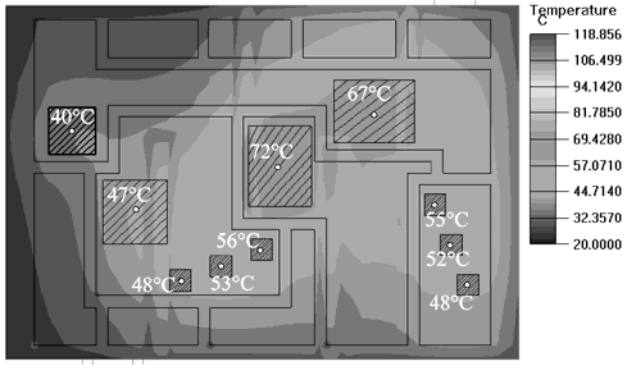
Fig.16: Time behavior of the chip temperatures calculated using circuit simulation (CASPOC) based on thermal equivalent circuits (cf. Fig.15) of the power semiconductors with reference temperatures resulting from a stationary thermal simulation (cf. Fig.15(b)). The results of a conventional transient thermal simulation using ICEPAK are shown by dotted lines.

According to Fig.16 the results of this approach are slightly differing from a conventional transient simulation (shown by dotted lines in Fig.16) only concerning the absolute temperature values while the time behavior of the temperatures are in good correlation. The temperature of chips (8) and (9) are shown to be about *7°C* higher than for the conventional transient simulation, for chips (3) and (5) the temperature error is about *4°C*. The differences of the absolute temperatures are caused by the assumption of a constant temperature of the module bottom Cu-layer for the calculation of the step response of the chip temperatures (cf. section 3.2) and by the neglection of the thermal coupling of the individual power semiconductors when deriving the RC equivalent circuits from the step response data.

For improving the thermal modeling one could refer to the chip temperatures already available from the stationary thermal simulation (cf. Fig.14) and calculate a corrected total thermal resistance for each semiconductor model. The way of adjusting the values given in Tab.3 accordingly without impairing the transient characteristics is currently the topic of further research.

5. Time-Efficient Thermal Analysis of the Power Module IXYS VUM26B for Different Operating States

After deriving the thermal RC equivalent circuits of the power semiconductors what takes about *6 hours* (ICEPAK simulation, cf. section 3.2) the simulation time for a transient analysis of the semiconductor junction temperatures can be reduced significantly. It takes about *1 hour* to perform the stationary thermal simulation for the determination of the temperature distribution at the module bottom Cu-layer, and only *10 minutes* to finally calculate the junction temperatures using the circuit simulation (CASPOC) as described before.



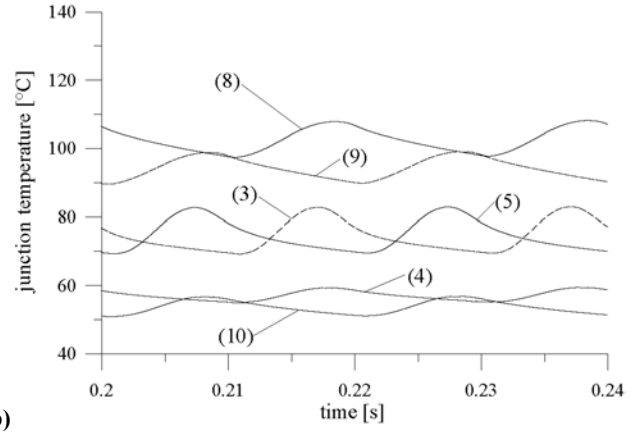


Fig.17: (a) Stationary thermal ICEPAK-simulation of the temperature of the module bottom Cu-layer for determining the reference temperatures of the thermal RC equivalent circuits of the power semiconductors; **(b)** time behavior of chip junction temperatures calculated using the circuit simulator CASPOC as described in section 4.3. Simulation parameters: $M=0.93$, $\hat{U}_N=370V$, $\hat{I}_N=19A$, $P_{OUT}=10kW$; semiconductor losses: $P_{V,SR}=28W$, $P_{V,DF}=15W$, $P_{V,DN}=9W$, $P_{V,MODULE}=104W$.

Accordingly, the temperature distribution can be investigated with sensible effort for different operating parameters of the three-phase rectifier system like different modulation indices as shown in **Fig.17**, **Fig.18** and **Fig.19**. There, the cooling system is still defined according to Fig.6 with a water flow rate of *1.0 liter/minute* and an inlet temperature of *20°C*. With increasing modulation index the relative on time of the power transistor does decrease and/or the free-wheeling conduction time does increase what results in a lower junction temperature difference of the both devices.

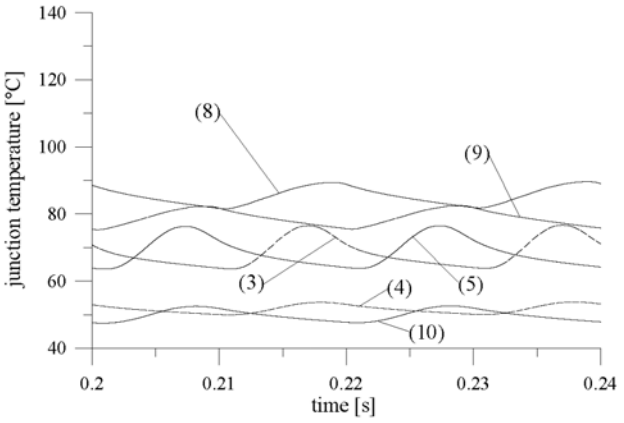


Fig.18: As Fig.17, but for $M=1.03$, $\hat{U}_N=410V$, $\hat{I}_N=17A$, $P_{OUT}=10kW$ and $P_{V,SR}=22W$, $P_{V,DF}=14W$, $P_{V,DN}=8W$, $P_{V,MODULE}=88W$.

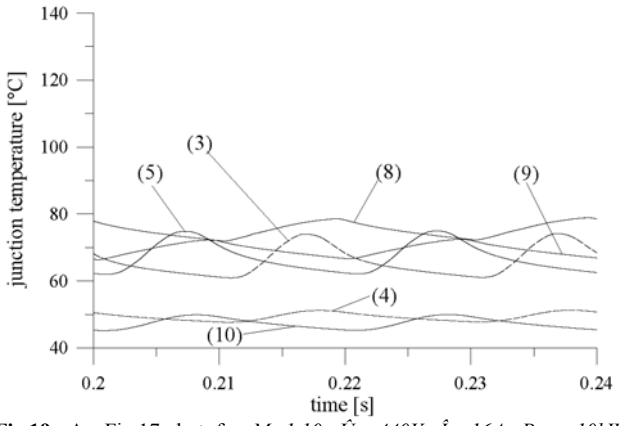


Fig.19: As Fig.17, but for $M=1.10$, $\hat{U}_N=440V$, $\hat{I}_N=16A$, $P_{OUT}=10kW$ and $P_{V,SR}=18W$, $P_{V,DF}=14W$, $P_{V,DN}=7W$, $P_{V,MODULE}=80W$.

Conclusions

A transient thermal simulation of a novel power module to be employed for the realization of a 500kHz/10kW three-phase AC/DC Vienna Rectifier has been performed using ICEPAK where the power semiconductor losses are calculated using a power electronics circuit simulator (CASPOC). For the cooling of the power module direct water cooling is employed.

A conventional transient thermal simulation of the temperatures of the power semiconductors of the module would take about *10 hours*. The procedure proposed in this paper does allow a significant reduction of the simulation time. There, in a first step the time dependent switching and conduction losses of the power semiconductors is determined. In a next step the temperature distribution over the bottom Cu-layer of the module ceramic substrate is calculated by stationary thermal simulation. Furthermore, RC thermal equivalent circuits are derived for the individual power semiconductors based on step response information resulting from transient thermal simulation for constant temperature of the whole module bottom Cu-layer. Finally, the RC equivalent circuits, the time dependent losses and the stationary temperature information are combined and the time behavior of the semiconductor junction temperatures is calculated using circuit simulation. This results in a total simulation time of only about *1hour* (all *calculation times* are given for a 2.2GHz PC) while guaranteeing sufficiently accurate results.

Future research will focus on a verification of the calculated temperature distribution by measurements, and on an analysis of the influence of the thermal coupling of the power semiconductors on the resulting junction temperatures. Furthermore, it will be investigated how the temperature-dependency of power semiconductor on-state and switching losses could be taken into account in order to further improve the accuracy of the simulation.

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