A Novel Bi-Directional Three-Phase Active Third-Harmonic Injection High Input Current Quality AC-DC Converter

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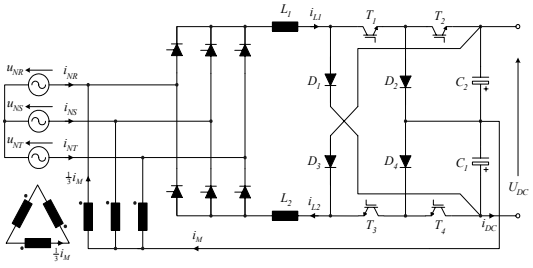
Abstract. A novel bi-directional three-phase AC/DC converter showing sinusoidal input currents is proposed. The system comprises a three-phase thyristor bridge, four turn-off power semiconductors and four diodes and can be thought as integration of the anti-parallel connection of unidirectional active third-harmonic injection (Minnesota) rectifier systems with reduced component count. The paper details the system operating modes, i.e. rectifier operation and/or power flow from the AC to the DC side, and inverter operation and/or power flow from the DC to the AC side and does propose a control scheme guaranteeing a largely sinusoidal shape of the AC currents. Furthermore, analytical expressions for the current stresses on the power component are derived, the semiconductor blocking voltage stresses are determined and the control actions to be taken for changing the direction of the power flow in operation are analyzed. Finally, the novel system is compared to a conventional three-phase voltage DC link PWM converter which represents a well-known technical alternative for bi-directional AC/DC conversion with sinusoidal mains currents. All investigations in the paper are based on numerical simulations.

1 Introduction

Passive rectifier systems employing a thyristor bridge at the mains side can provide bi-directional power flow, controlled output voltage and a very high efficiency (up to *99%*) due to negligible switching losses. However, the drawback of such systems is a significantly distorted mains current waveform and/or the bulky passive input filters for attenuating low order harmonics. In order to avoid such filters the converter mains current has to be actively controlled to a sinusoidal shape by employing pulse width modulation (PWM) at high switching frequencies f_P (*15kHz ... 50kHz*) what, however, does reduce the system efficiency due to switching losses.

In this paper, as an alternative in between a mains controlled thyristor bridge and a complex PWM converter systems, a novel bi-directional three-phase third harmonic injection AC-DC converter system comprising a single thyristor-bridge input stage and four turn-off power semiconductors and four diodes on the DC-side [1] is presented. The topology of the novel system is shown in **Fig.1**(a). The topology depicted in Fig.1(b) is equal in functionality, but does not allow to combine two power transistors (e.g. T_3 and T_4 of (a)) in a standard voltage DC link inverter bridge-leg module. Therefore, the focus of this paper will be on the topology depicted in Fig.1(a).



(a)

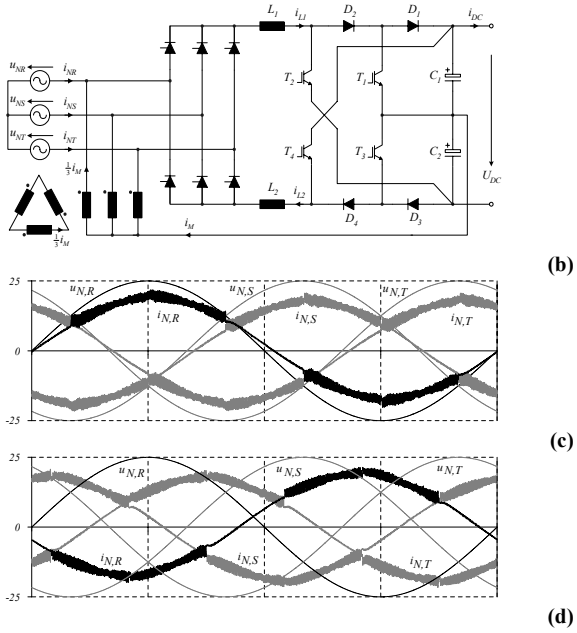


Fig.1: (a) Topology of the proposed bi-directional AC-DC converter with sinusoidal mains currents; **(b)** variation of the topology (a) showing equal functionality; **(c)** time behavior of the mains phase voltages and phase currents for rectifier operation (boost-mode) and **(d)** inverter operation (buck-mode). (*25A/Div*, *330V/Div*, *5ms/Div*)

The novel *bi-directional* converter is able to operate in rectifier and/or boost-mode and inverter and/or buck-mode. Both modes of operation were analyzed individually in [2] - [8] for different *uni-directional* power converter topologies. By employing the proposed converter topology both operating modes are covered while a minimum number of components are employed what does reduce the realization effort and/or cost and does increase the system reliability and opens a wide field of possible applications, e.g. as utility interface of AC drive systems for feeding braking energy back into the mains.

2 Basic Principle of Operation

2.1 Derivation of the DC-Side Reference Current

In **Fig.2** two (out of six) different operating states of the thyristor bridge are shown. The current controller (discussed in Section 4) controls i_{L1} and i_{L2} independently and the difference $i_M=i_{L1}-i_{L2}$ is injected into the AC side via the primary windings of a YΔ-transformer. As the Δ-windings are carrying equal currents, equal currents *1/3* i_M are forced to flow in each of the Y-windings.

For all following discussions we assume a purely sinusoidal symmetric mains

$$u_{N,R} = \hat{u}_N \sin(\varphi)$$
$$u_{N,S} = \hat{u}_N \sin(\varphi - \frac{2\pi}{3}) \quad (1)$$
$$u_{N,T} = \hat{u}_N \sin(\varphi - \frac{4\pi}{3})$$

For rectifier and inverter operation we have in ***sector 34*** where thyristors *3* and *4* are in the on-state (Fig.2(a)),

$$-i_{L2} = i_{N,R} + \frac{1}{3}(i_{L1} - i_{L2})$$
$$i_{L1} = i_{N,S} + \frac{1}{3}(i_{L1} - i_{L2}) \quad (2)$$
$$0 = i_{N,T} + \frac{1}{3}(i_{L1} - i_{L2})$$

what results in

$$i_{L1} = i_{N,S} - i_{N,T} \qquad i_{L2} = i_{N,T} - i_{N,R} \,. \quad (3)$$

Therefore, in order to achieve desired current shapes $i^*_{N,R}$, $i^*_{N,S}$, $i^*_{N,T}$, the currents i_{L1} and i_{L2} have to be controlled according to

$$i^*_{L1} = i^*_{N,S} - i^*_{N,T} \qquad i^*_{L2} = i^*_{N,T} - i^*_{N,R} \,. \quad (4)$$

This means that as long as $i^*_{L1}>0$, $i^*_{L2}>0$ is guaranteed (a basic requirement due to unidirectional current carrying capability of the thyristors) arbitrary waveforms of the AC-side currents can be achieved.

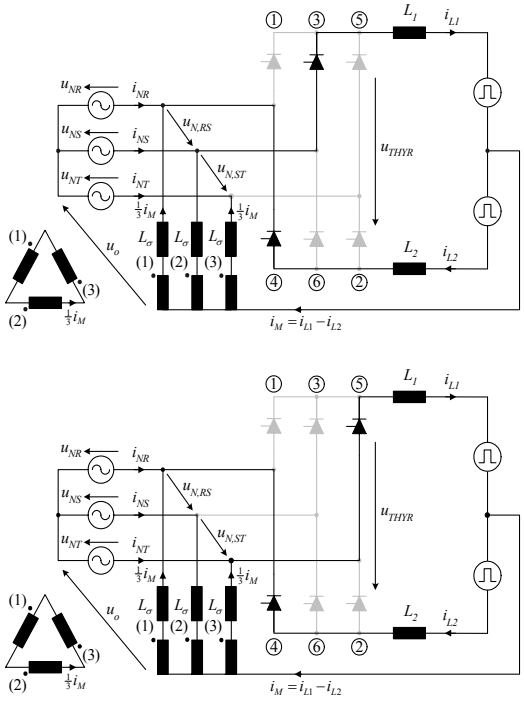


Fig.2: Equivalent circuit for rectifier and inverter operation for calculation of the mains phase current waveforms in **(a)** *section 34* (thyristors *3* and *4* in the on-state) and **(b)** *section 45* (thyristors *4* and *5* in the on-state).

Due the symmetry of the three-phase system the analysis can be limited to a 2π/3-wide interval of a mains period. In the following ***sector 45*** (where thyristors *4* and *5* are in the on-state) is considered in analogy to *sector 34*. There, we have

$$-i_{L2} = i_{N,R} + \frac{1}{3}(i_{L1} - i_{L2})$$
$$i_{L1} = i_{N,T} + \frac{1}{3}(i_{L1} - i_{L2}) \quad (5)$$
$$0 = i_{N,S} + \frac{1}{3}(i_{L1} - i_{L2})$$

what does result in the relationships for the DC-side current reference values

$$i^*_{L1} = -(i^*_{N,S} - i^*_{N,T}) \qquad i^*_{L2} = -(i^*_{N,R} - i^*_{N,S}) \,. \quad (6)$$

In the following, in Sections 2.2 and 2.3, the phase current reference values $i^*_{N,RST}$ are assumed to show a sinusoidal shape. In rectifier and/or boost-mode the AC voltages and currents should be in phase ($\cos\varphi=1$) while in inverter and/or buck-mode $\cos\varphi=-1$ is desired. After defining the mains reference currents (with reference to the mains voltages as defined in (1)) the DC-side reference currents can be calculated directly using (4) and (6) where $i^*_{L1}>0$ and $i^*_{L2}>0$ has to be considered as necessary condition.

It will be shown in the following that $\cos\varphi=1$ can be achieved for rectifier mode while $\cos\varphi=-1$ cannot be realized exactly due to a remaining minor phase shift of voltage and current fundamentals in this operating mode caused by the limitation of the thyristor bridge firing angle required for ensuring a safe commutation in inverter mode.

2.2 Rectifier Operation (Boost-Mode)

For delivering power from the AC-side to the DC-side the power transistors T_2 and T_4 are remaining in the off-state. The firing angle of the thyristor bridge is $\alpha=0°$, and the topology of Fig. 1(a) can be redrawn as shown in **Fig.3**. There, the thyristor bridge operates like a diode bridge. The inductors L_1 and L_2, the power transistors T_1 and T_3, and the diodes D_1 and D_3 are forming two DC-DC boost converters which do allow to modulate the DC-side current according to the waveform shown in **Fig.4**(b). The resulting current difference $i_M=i_{L1}-i_{L2}$ is fed back to the AC-side via the YΔ–transformer.

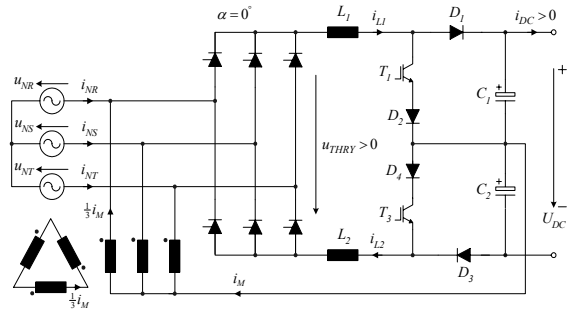


Fig.3: Equivalent circuit of the system shown in Fig. 1(a) for rectifier operation (boost-mode, and/or energy transfer from the AC- to the DC-side). Power transistors T_2 and T_4 are remaining in the turn-off state).

The mains phase voltages $u_{N,RST}$ as defined in (1), the mains current reference values $i^*_{N,RST}$, and the DC-side reference currents i^*_{L1} and i^*_{L2} as defined in (4) and (6) are shown in Fig.4 for rectifier operation (boost-mode). There, "*6&1*" describes *sector 61* with thyristors *6* and *1* in turn-on state, the following sectors are described accordingly. Since i^*_{L1} and i^*_{L2} do not show negative values, the AC-side currents $i_{N,RST}$ can follow their reference currents $i^*_{N,RST}$ without distortion for employing proper current control.

A digital simulation of the system behavior (the assumed operating parameters are compiled in section 3.2) for employing a current controller as described in section 4 is shown in **Fig.5**. There, the time behavior of i_{L1} and i_{L2} (cf. Fig.5(b)) is according to the reference values shown in Fig.4(b). The spectrum $c_{f,norm}=c_f/c_{50Hz}=c_f/\hat{i}_N$ of the phase current $i_{N,R}$ normalized to the

mains current amplitude $\hat{\imath}_N$ is shown in Fig.5(d). Multiples of the switching frequency f_P=*16kHz* are dominant while the amplitudes of the low-frequency harmonics are lower than *1.0%*.

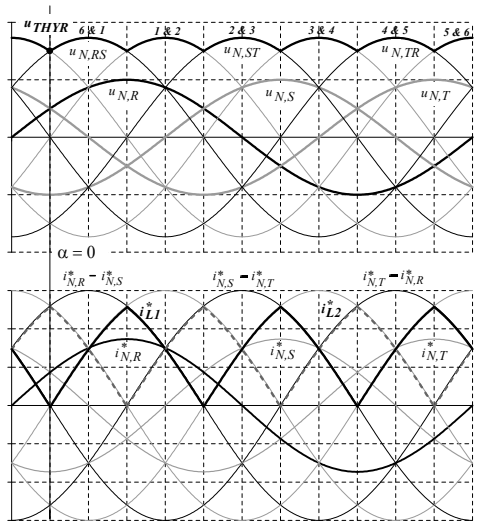


Fig.4: Time behavior of the normalized DC-side current reference values i^*_{L1} (black) and i^*_{L2} (dashed) as required for achieving sinusoidal phase currents in phase ($\cos\varphi$=*1*) with the corresponding mains phase voltages in rectifier operation (boost-mode) over a mains period (π*/6 rad/Div*).

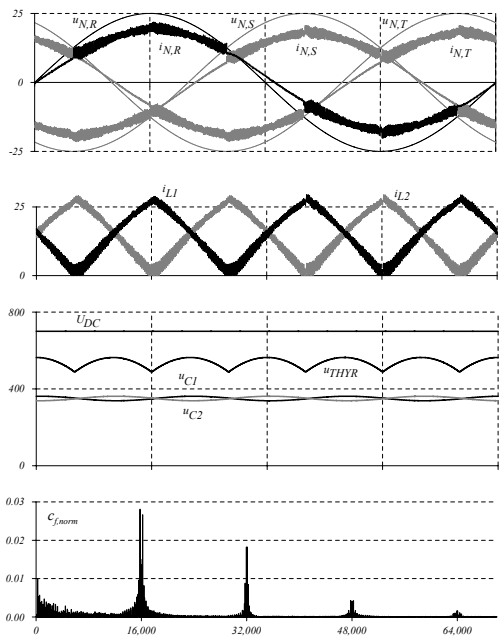


Fig.5: Numerical simulation ($\hat{u}_N$=*327V*, $\hat{\imath}_N$=*18A*, U_{DC}=*700V*, *P=9kW*, f_P=*16kHz*) of the system behavior for rectifier operation (*25A/Div*, *5ms/Div*); **(a)** mains phase currents $i_{N,RST}$, $i_{N,R}$ and the corresponding phase voltage $u_{N,R}$ (*330V/Div*) are shown in black, while the other two phase quantities are shown in grey; **(b)** i_{L1} and i_{L2} are controlled according to Fig.4; **(c)** DC-side voltages U_{DC}, u_{C1}, u_{C2} and u_{THYR} (*400V/Div*); **(d)** normalized spectrum $c_{f,norm}=c_f/c_{50Hz}=c_f/18A$ of $i_{N,R}$ (omitting $c_{50Hz,norm}$=*1.0*, the ordinal number of the harmonics is shown on the horizontal axis).

The time behavior of the relative on-times d_1 and d_3 of power transistors T_1 and T_3 which are active in the boost-mode are called *modulation functions*. The modulation functions are employed as pre-control signals for the current control shaping i_{L1} and i_{L2} according to Fig.4(b) (cf. section 4). Furthermore, the modulation functions are the basis of the analytical calculation of the current stresses on the power semiconductors (cf. section 3.1).

The derivation of the modulation functions for rectifier operation is based on the equivalent circuit shown in **Fig.6**. Assuming a continuous shape of i_{L1} the local average value (referred to a switching cycle $T_P=1/f_P$) is equal to $u_{C1}\cdot(1-d_1)$.

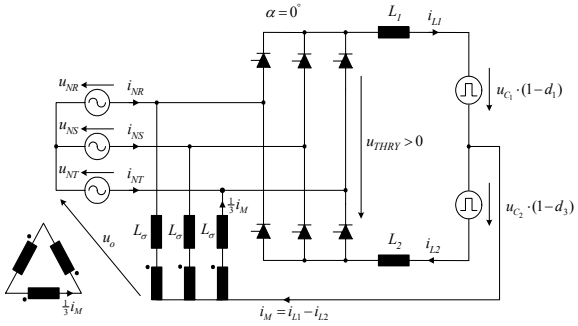


Fig.6: Equivalent circuit for rectifier operation providing the basis for the calculation of the modulation functions d_1 and d_3 (time behavior of the relative on-times of transistors T_1 and T_3).

According to Fig.4(b) and/or (4) and (6) in ***sector 34*** the DC-side reference currents are

$$i^*_{L1,34}=\sqrt{3}\,\hat{\imath}_N\,\sin(\varphi-\frac{3\pi}{6}) \qquad i^*_{L2,34}=\sqrt{3}\,\hat{\imath}_N\,\sin(\varphi-\frac{7\pi}{6})\,. \tag{7}$$

With $d_{1,34}$ and $d_{3,34}$ as the relative on-times of the transistors T_1 and T_3 in *sector 34*, there results based on the equivalent circuit of Fig.6

$$\begin{aligned}-(1-d_{1,34})u_{C1}&=-(u_{N,S}-u_0)+L_1\frac{di_{L1,34}}{dt}\\(1-d_{3,34})u_{C2}&=-(u_{N,R}-u_0)-L_2\frac{di_{L2,34}}{dt}\end{aligned}\,. \tag{8}$$

In the following the partial voltages u_{C1} and u_{C2} will be assumed constant what is ensured in practice with good approximation by a voltage control loop. Furthermore, the inductances L_1 and L_2 are assumed to show equal inductance,

$$u_{C1}=u_{C2}=\frac{1}{2}U_{DC} \qquad L_1=L_2=L\,. \tag{9}$$

Based on the currents $i_{L1,34}$ and $i_{L2,34}$ the voltage drop across the transformer stray inductance L_σ can be calculated as

$$u_{0,34}=L_\sigma\frac{d}{dt}(\frac{1}{3}(i_{L1,34}-i_{L2,34}))=\omega L_\sigma\hat{\imath}_N\,\sin(\varphi-\frac{11\pi}{6}) \tag{10}$$

what finally results in relative on-times

$$\begin{aligned}d_{1,34}&=1-M_1\,\sin(\varphi-\frac{2\pi}{3})-M_2\,\cos(\varphi-\frac{3\pi}{6})+M_3\,\sin(\varphi-\frac{11\pi}{6})\\d_{3,34}&=1+M_1\,\sin(\varphi)+M_2\,\cos(\varphi-\frac{7\pi}{6})-M_3\,\sin(\varphi-\frac{11\pi}{6})\end{aligned} \tag{11}$$

with modulation indices defined as

$$M_1=\frac{\hat{u}_N}{U_{DC}/2} \qquad M_2=\sqrt{3}\,\frac{\omega L\,\hat{\imath}_N}{U_{DC}/2} \qquad M_3=\frac{\omega L_\sigma\hat{\imath}_N}{U_{DC}/2}\,. \tag{12}$$

The analysis of ***sector 45*** gives in analogy

$$i^*_{L1,45}=\sqrt{3}\,\hat{\imath}_N\,\sin(\varphi-\frac{9\pi}{6}) \qquad i^*_{L2,45}=\sqrt{3}\,\hat{\imath}_N\,\sin(\varphi-\frac{5\pi}{6}) \tag{13}$$

$$\begin{aligned}-(1-d_{1,45})u_{C1}&=-(u_{N,T}-u_0)+L_1\frac{di_{L1,45}}{dt}\\(1-d_{3,45})u_{C2}&=-(u_{N,R}-u_0)-L_2\frac{di_{L2,45}}{dt}\end{aligned} \tag{14}$$

$$u_{0,45}=L_\sigma\frac{d}{dt}(\frac{1}{3}(i_{L1,45}-i_{L2,45}))=\omega L_\sigma\hat{\imath}_N\,\sin(\varphi-\frac{7\pi}{6}) \tag{15}$$

and/or

$$d_{1,45} = 1 - M_1 \sin(\varphi - \frac{4\pi}{3}) - M_2 \cos(\varphi - \frac{9\pi}{6}) + M_3 \sin(\varphi - \frac{7\pi}{6}) \quad (16)$$

$$d_{3,45} = 1 + M_1 \sin(\varphi) + M_2 \cos(\varphi - \frac{5\pi}{6}) - M_3 \sin(\varphi - \frac{7\pi}{6})$$

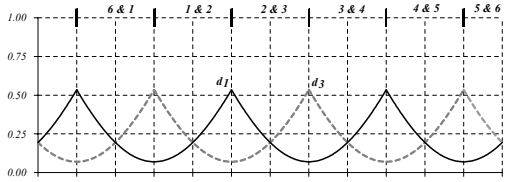


Fig.7: Time behavior of the rectifier-mode modulation functions d_1 and d_3 over one mains period ($\pi/6$ *rad/Div*) according to (11) and (16) for M_1= *327/350= 0.94* neglecting M_2 and M_3.

Due to the symmetry of the three-phase system *sectors 34* and *45* are sufficient for deriving the modulation functions for T_1 and T_3 over the whole mains period. Neglecting the typically very small values of M_2 and M_3 and/or the influence of the voltage drop (low-frequency components) across L_1, L_2, L_σ the modulation functions are shown in **Fig.7** for the parameters given in section 3.2.

2.3 Inverter Operation (Buck-Mode)

For feeding power back from the DC-side to the AC-side the power switches T_1 and T_3 are remaining in the on-state. The firing angle of the thyristor bridge is close to α=*180°*, and the topology of Fig.1(a) can be redrawn as shown in **Fig.8**. The diodes D_1 and D_3 are in permanent off-state and are therefore not shown in Fig.8. The DC-side currents i_{L1} and i_{L2} are shaped according to **Fig.9**(b) by proper control of the transistors T_2 and T_4.

The basic reason for the occurrence of negative reference values i^*_{L1} and i^*_{L2} is the thyristor bridge firing angle α which has to be lower than *180°* for ensuring safe commutation. The angle difference is denoted by ζ and defined in (17). In Fig.9(b) and for all numerical simulations of this paper $\zeta=\pi-\alpha$=*15°* has been assumed. Shifting the reference current system in Fig.11 by ζ results in a reference current system $i^*_{N,RST}$ which guarantees both reference currents i^*_{L1} and i^*_{L2} to be positive over the whole mains period (as shown in Fig.9). In inverter operation (buck-mode) we therefore have in general a power factor lower than *1*.

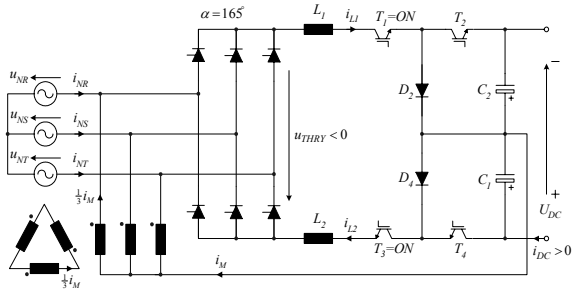


Fig.8: Equivalent topology of Fig.1(a) for inverter operation (buck-mode) and/or feedback of energy from the DC to the AC side. Power switches T_1 and T_3 are remaining in the on-state.

Figure 9 shows the time behavior of the AC-side phase voltages $u_{N,RST}$ as defined in (1), the reference mains currents $i^*_{N,RST}$ for inverter operation (buck-mode), and the DC-side reference currents i^*_{L1} and i^*_{L2} as defined in (4) and (6). If the currents $i^*_{N,RST}$ are defined according to $cos\varphi$=*-1* the reference currents i^*_{L1} and i^*_{L2} would have to show negative values in short intervals. This is shown in **Fig.11** where the according current segments are highlighted. As the thyristor bridge and the DC-side power semiconductors do not allow a reversal of i_{L1} and i_{L2} this will result in distortions of the mains phase currents $i_{N,RST}$.

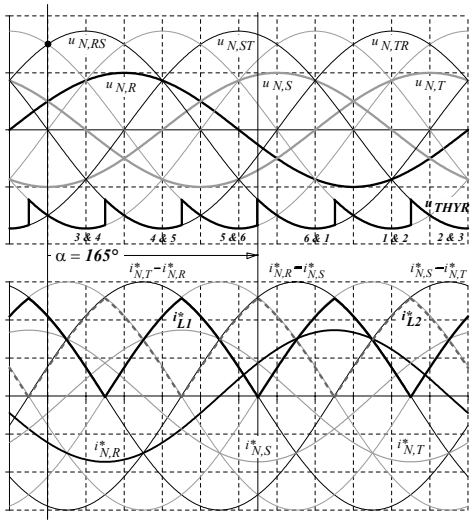


Fig.9: Time behavior of the DC-side reference currents i^*_{L1} (shown in black) and i^*_{L2} (dashed grey) over one mains period ($\pi/6$ *rad/Div*) as required for achieving sinusoidal phase currents in inverter operation (buck-mode).

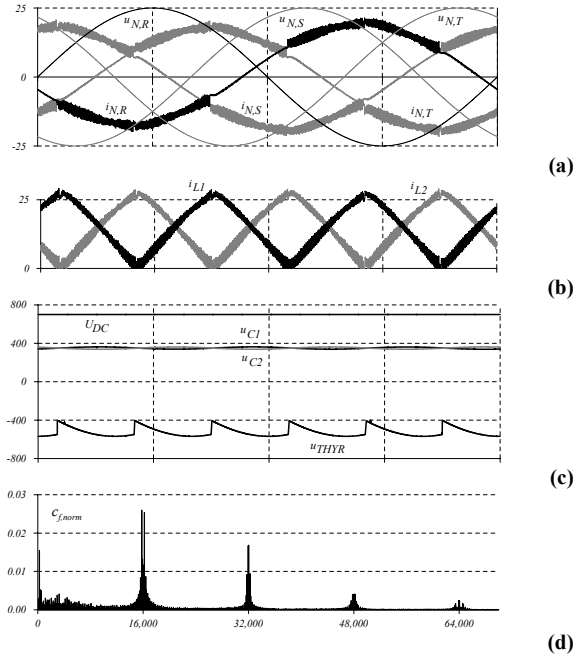


Fig.10: Numerical simulation ($\hat{u}_N$=*327V*, $\hat{\imath}_N$=*18A*, U_{DC}=*700V*, *P=9kW*, f_P=*16kHz*, *L=0.6mH*) of inverter operation (*25A/Div*, *5ms/Div*); **(a)** mains current $i_{N,RST}$, phase voltage $u_{N,R}$ (*330V/Div*) and the corresponding phase current $i_{N,R}$ are shown in black, while the other phase quantities are shown in grey; **(b)** currents i_{L1} and i_{L2} are controlled according to Fig.9; **(c)** DC-side voltages U_{DC}, u_{C1}, u_{C2} and u_{THYR} (*400V/Div*); **(d)** normalized spectrum $c_{f,norm}=c_f/c_{50Hz}=c_f/18A$ of current $i_{N,R}$ (omitting $c_{50Hz,norm}$=*1.0* in the diagram), the ordinal number of the harmonics is given on the horizontal axis.

A numerical simulation (the assumed operating parameters are given in section 3.2) employing a current controller as described

in section 4 is presented in **Fig.10**. The time behavior of i_{L1} and i_{L2} in Fig.10(b) is according to the reference values shown in Fig.9(b). The normalized spectrum $c_{f,norm}=c_f/c_{50Hz}=c_f/\hat{i}_N$ of phase current $i_{N,R}$ (normalization with reference to the amplitude $\hat{i}_N$ of the fundamental) is depicted in Fig.10(d). Harmonics with switching frequency f_P=*16kHz* are dominant while the low-frequency harmonics show amplitudes lower than *1.5%*.

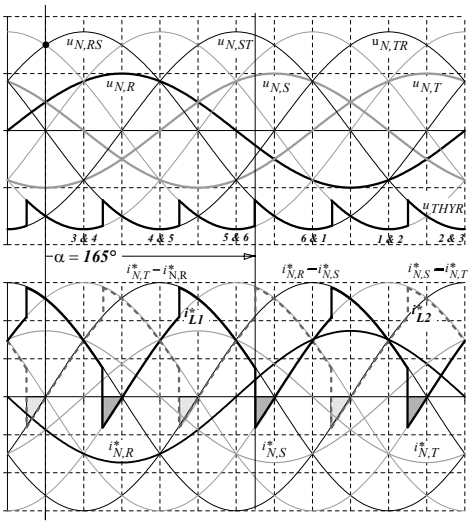


Fig.11: Time behavior of the DC-side reference currents i^*_{L1} (black) and i^*_{L2} (dashed grey) as theoretically required for achieving $cos\varphi$=*-1* in inverter operation over one mains period (π*/6 rad/Div*).

The derivation of the time behavior of the relative on-times d_2 and d_4 of the transistors T_2 and T_4 being active in inverter-mode is based on **Fig.12** and analogous to section 2.2.

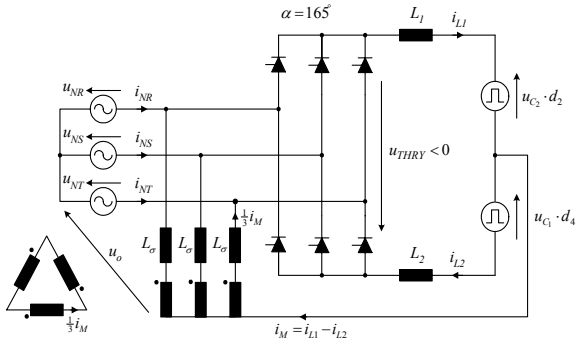


Fig.12: Equivalent circuit for inverter operation (buck-mode) for the derivation of the modulation functions d_2 and d_4 (relative on-times of the power transistors T_2 and T_4).

Assuming a continuous shape of i_{L1} the local average value of the upper partial voltage in Fig.12 is $u_{C2}\cdot d_2$ .With

$$\zeta = \pi - \alpha \tag{17}$$

we receive considering ***sector 34*** according to Fig.9(b) and/or (4) and (6)

$$i^*_{L1,34} = \sqrt{3}\,\hat{i}_N\,\sin(\varphi+\zeta-\frac{9\pi}{6}) \quad . \tag{18}$$
$$i^*_{L2,34} = \sqrt{3}\,\hat{i}_N\,\sin(\varphi+\zeta-\frac{\pi}{6})$$

With $d_{2,34}$ and $d_{4,34}$ as relative on-times of T_2 and T_4 in *sector 34*, we have based on the equivalent circuit shown in Fig.12

$$d_{2,34}\,u_{C2} = -(u_{N,S}-u_0) + L_1\frac{di_{L1,34}}{dt} \quad . \tag{19}$$
$$-d_{4,34}\,u_{C1} = -(u_{N,R}-u_0) - L_2\frac{di_{L2,34}}{dt}$$

Assuming again

$$u_{C1} = u_{C2} = \frac{1}{2}U_{DC} \qquad L_1 = L_2 = L \tag{20}$$

the voltage drop across the transformer stray inductance L_σ is

$$u_{0,34} = L_\sigma\frac{d}{dt}(\frac{1}{3}(i_{L1,34}-i_{L2,34})) = \omega L_\sigma\hat{i}_N\,\sin(\varphi+\zeta-\frac{5\pi}{6}) \,. \tag{21}$$

The relative on-times $d_{2,34}$ and $d_{4,34}$ are calculated based on (19) as

$$d_{2,34} = -M_1\,\sin(\varphi-\frac{2\pi}{3}) + M_2\,\cos(\varphi+\zeta-\frac{9\pi}{6}) + M_3\,\sin(\varphi+\zeta-\frac{5\pi}{6}) \tag{22}$$
$$d_{4,34} = M_1\,\sin(\varphi) + M_2\,\cos(\varphi+\zeta-\frac{\pi}{6}) - M_3\,\sin(\varphi+\zeta-\frac{5\pi}{6})$$

(for the definition of the M_1, M_2, and M_3 see (12)). The analysis of ***sector 45*** results in

$$i^*_{L1,45} = \sqrt{3}\,\hat{i}_N\,\sin(\varphi+\zeta-\frac{3\pi}{6}) \tag{23}$$
$$i^*_{L2,45} = \sqrt{3}\,\hat{i}_N\,\sin(\varphi+\zeta-\frac{11\pi}{6})$$

$$d_{2,45}\,u_{C2} = -(u_{N,T}-u_0) + L_1\frac{di_{L1,45}}{dt} \tag{24}$$
$$-d_{4,45}\,u_{C1} = -(u_{N,R}-u_0) - L_2\frac{di_{L2,45}}{dt}$$

$$u_{0,45} = L_\sigma\frac{d}{dt}(\frac{1}{3}(i_{L1,45}-i_{L2,45})) = \omega L_\sigma\hat{i}_N\,\sin(\varphi+\zeta-\frac{\pi}{6}) \tag{25}$$

and/or in relative on-times

$$d_{2,45} = -M_1\,\sin(\varphi-\frac{4\pi}{3}) + M_2\,\cos(\varphi+\zeta-\frac{3\pi}{6}) + M_3\,\sin(\varphi+\zeta-\frac{\pi}{6}) \,. \tag{26}$$
$$d_{4,45} = M_1\,\sin(\varphi) + M_2\,\cos(\varphi+\zeta-\frac{11\pi}{6}) - M_3\,\sin(\varphi+\zeta-\frac{\pi}{6})$$

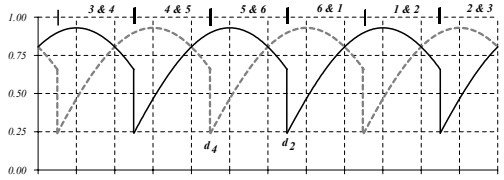


Fig.13: Time behavior of the buck-mode modulation functions d_2 and d_4 over one mains period (π*/6 rad/Div*) according to (22) and (26) for M= *327/350= 0.94* neglecting M_2 and M_3.

Due to the symmetry of the three-phase system the analysis of *sectors 34* and *45* is sufficient for deriving the modulation functions for T_2 and T_4 over the whole mains period. For neglecting the typically small values of M_2 and M_3 and, therefore, the influence of the voltage drops (low-freq. components) across L_1, L_2,L_σ the modulation functions shown in **Fig.13** do result (the assumed operating parameters are detailed in Section 3.2).

3 Stresses on the Components

3.1 Analytical Calculations of Current Stress

Details of the calculations resulting in the analytical expressions given in **Fig.14**, **Fig.15** and **Fig.16** are compiled in the Appendix.

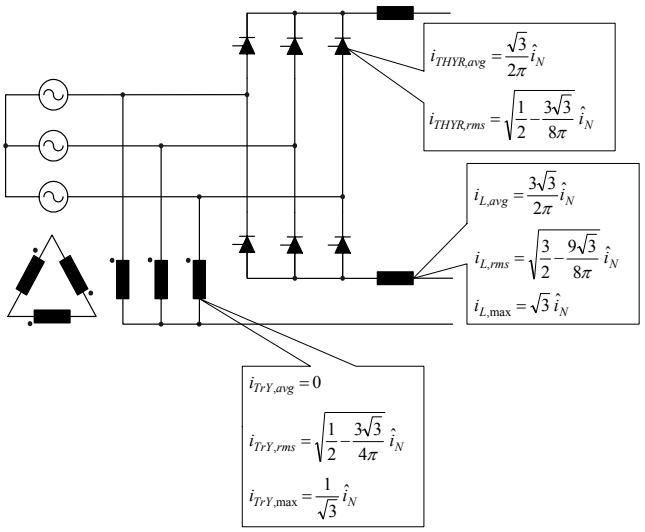


Abb.14: Current stresses on the valves of the thyristor bridge and the magnetic components resulting for rectifier operation (boost-mode) and inverter operation (buck-mode).

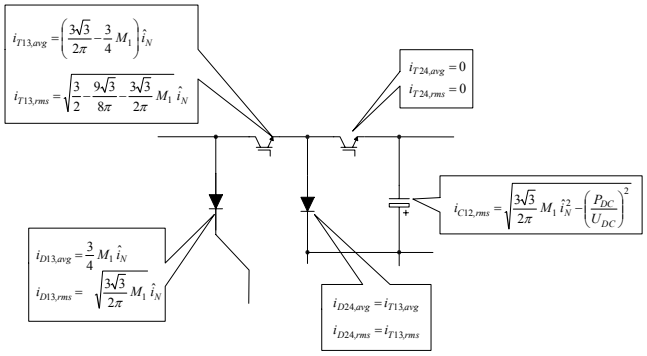


Abb.15: Current stresses on the DC-side power semiconductors for rectifier operation (boost-mode).

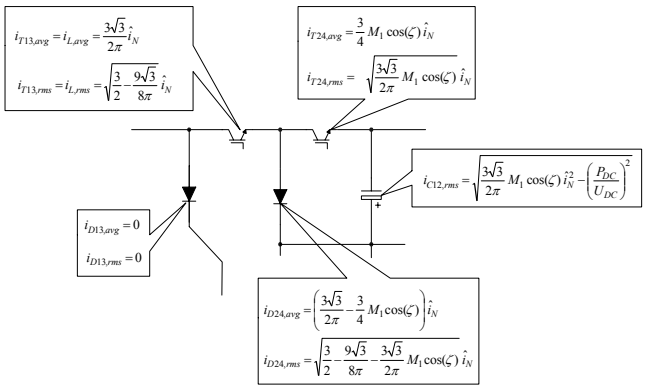


Abb.16: Current stress on the DC-side power semiconductors for inverter operation (buck-mode).

3.2 Simulations

All simulations and calculations in this paper are based on the following set of operating parameters.

$\hat{u}_N = 327\ V$	mains phase voltage amplitude
$\hat{i}_N = 18\ A$	mains phase current amplitude
$U_{DC} = 700\ V$	DC-side voltage
$P = 9.0\ kW$	output power
$L_1 = L_2 = 0.6\ mH$	DC-side inductances
$C_1 = C_2 = 1.0\ mF$	DC-side capacitors
$L_{Trafo} = 1.0\ H$	transformer main inductance
$L_\sigma = (1\text{-}k)\ L_{Trafo} = 2\ mH$	transformer stray inductance
$f_P = 16\ kHz$	switching frequency
$\alpha_{BUCK} = 165°$	firing angle in inverter-mode.

	Rectifier Operation			Inverter Operation		
	AVG	RMS	MAX	AVG	RMS	MAX
$i_{T,13}$	2.5 *(2.3)*	6.2 *(5.9)*	28.3 *(31.2)*	14.9 *(14.9)*	17.0 *(16.9)*	29.2 *(31.2)*
$i_{T,24}$	0 *(0)*	0 *(0)*	0 *(0)*	12.5 *(12.2)*	15.9 *(15.6)*	29.0 *(31.2)*
$i_{D,13}$	12.6 *(12.6)*	15.9 *(15.8)*	29.5 *(31.2)*	0 *(0)*	0 *(0)*	0 *(0)*
$i_{D,24}$	2.4 *(2.3)*	6.2 *(5.9)*	28.3 *(31.2)*	2.5 *(2.7)*	6.3 *(6.6)*	27.7 *(31.2)*
i_{THYR}	5.0 *(5.0)*	9.9 *(9.7)*	28.8 *(31.2)*	4.9 *(5.0)*	9.7 *(9.7)*	28.1 *(31.2)*
$i_{L,12}$	15.1 *(14.9)*	17.1 *(16.9)*	29.5 *(31.2)*	15.0 *(14.9)*	17.1 *(16.9)*	29.0 *(31.2)*
i_{TrafoY}	0 *(0)*	5.4 *(5.3)*	9.0 *(10.4)*	0 *(0)*	5.4 *(5.3)*	8.9 *(10.4)*
$i_{C1,2}$		9.4 *(9.3)*			10.0 *(9.5)*	

Tab.1: Current stresses on the power components as determined by simulations in comparison to the results of analytical calculations (shown in brackets) according to section 3.1.

Comparing the calculated component stresses based on the equations given in section 3.1 with the results of digital simulations, the deviation is typically lower than 5%. The analytical calculations therefore do provide an excellent basis for the design the converter power circuit.

3.3 Power Semiconductor Blocking Voltage Stress

For inverter operation the (nominal) blocking voltage stress on the diodes D_1 and D_3 is the total DC output voltage U_{DC} , the blocking voltage stress on all other DC-side power semiconductors is $U_{DC}/2$. For rectifier operation all DC-side power semiconductors including the diodes D_1 and D_3 are subject to a blocking voltage of $U_{DC}/2$. As shown in **Fig.17** this is valid also during switch-over from rectifier to inverter mode and vice versa.

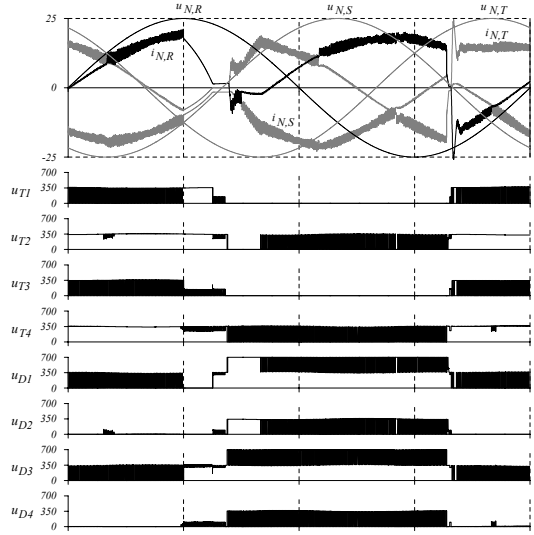


Fig.17: Numerical simulation of the blocking voltage stresses on all DC-side power semiconductors for *rectifier operation*, for the switch-over to *inverter operation*, for *inverter operation*, and for switching back to *rectifier operation*. Only diodes D_1 and D_3 are facing U_{DC}=*700V* for inverter operation. (*25A/Div*, *5ms/Div*, *top: 330V/Div*).

4 System Control

4.1 Control Structure

For achieving sinusoidal mains currents $i_{N,RST}$ the DC-side inductor currents i_{L1} and i_{L2} have to be controlled according to (4) and (6). The block diagram depicted in **Fig.18** shows how to define the time behavior of the reference current waveforms i^*_{L1} and i^*_{L2}.

The amplitudes $\hat{i}^*_{L1}$ and $\hat{i}^*_{L2}$ are derived from the mains current reference amplitude $\hat{i}^*_N$ where an offset i_{CORR} is added for balancing the neutral point of the DC output voltage. The normalized reference currents $i^*_{L1,norm}$ and $i^*_{L2,norm}$ are generated by the controller according to Fig.4 and/or Fig.9 dependent on the operating mode (rectifier or inverter mode) and are synchronized to the mains voltage.

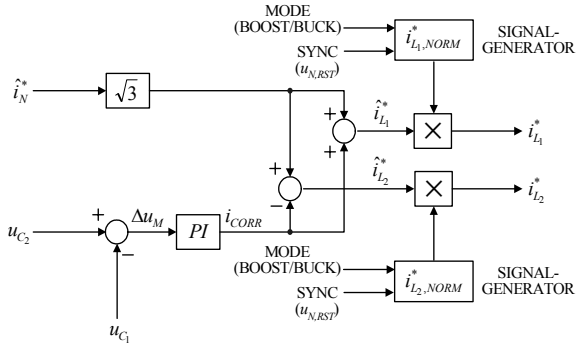


Fig.18: Block diagram of the generation of the DC-side reference currents i^*_{L1} and i^*_{L2}.

The structure of the control of i_{L1} and i_{L2} is shown in **Fig.19** where pre-control signal $vst_{(L1,2)}$ dependent on the mode of operation (rectifier or inverter) are added to the controller outputs.

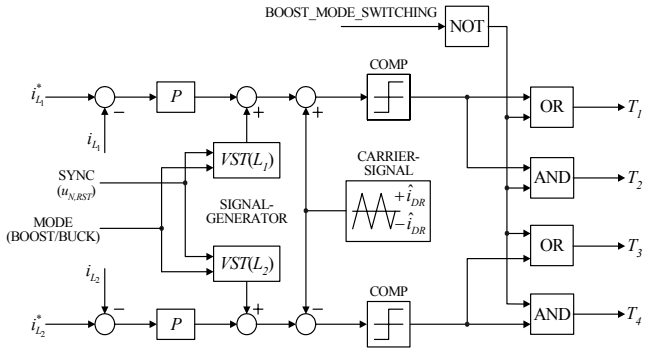


Fig.19: Block diagram of the control of i_{L1} and i_{L2} including the combinatorial logic for switching between rectifier and inverter mode. The pre-control signals $vst_{(L1)}$ and $vst_{(L2)}$ are synchronized with the mains voltages and generated according to (27).

Assuming a low control error, the relative on-times of the power transistors are determined by the intersection of the carrier signal with switching frequency and the pre-control signals according to

$$vst_{(L1,BOOST)} = \hat{i}_{DR}\,(1-2\,d_1) \qquad vst_{(L2,BOOST)} = \hat{i}_{DR}\,(1-2\,d_3)$$
$$vst_{(L1,BUCK)} = \hat{i}_{DR}\,(1-2\,d_2) \qquad vst_{(L2,BUCK)} = \hat{i}_{DR}\,(1-2\,d_4) \qquad (27)$$

(cf. **Fig.20**(a)). By employing pre-control signals simple proportional-type current controllers with low gain are sufficient for guaranteeing low control errors. There, for a practical realization of the system the influence of the voltage drops (low-freq. comp.) across L_1, L_2, L_σ can be neglected for calculation of the pre-control signals based on (11), (16), (22), (26) and (27).

In Fig.19 the current controllers do employ triangular carrier signal with reversed signs. This results in transistor on-times being phase-shifted by half a pulse period as shown in Fig.20(a) for rectifier operation and/or in a significantly reduced current ripple.

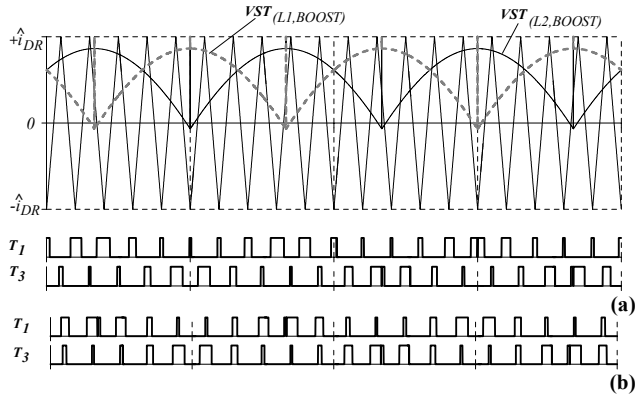


Fig.20: Rectifier operation over one mains period; **(a)** intersection of the pre-control signal $vst_{(L1,BOOST)}$ and the triangular-shaped carrier signal for defining the switching pattern for transistor T_1; the switching pattern of transistor T_3 is generated by intersection of $vst_{(L2,BOOST)}$ and the inverted carrier signal (not shown); **(b)** *non-optimum* switching signal generation employing only a single carrier signal resulting in increased mains current ripple. ***Note:*** The frequency of the carrier signal has been reduced in order to clearly show the system behavior.

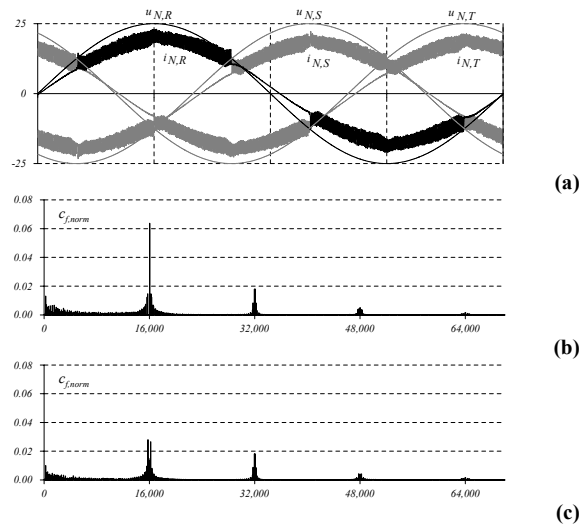


Fig.21: (a) Time behavior of mains currents for employing a *non-optimum* current controller, i.e. no inversion of the carrier signal employed by the i_{L2}-control is performed (*25A/Div*, *330V/Div*, *5ms/Div*); **(b)** corresponding normalized mains phase current spectrum $c_{f,norm}$, and **(c)** normalized mains phase current spectrum $c_{f,norm}$ resulting for inversion of carrier signal according to Fig.19. *Note:* $c_{50Hz,norm}=1.0$ is omitted in (b) and (c).

In case only a single carrier signal is employed by both current controllers and/or the three-level characteristic of the DC side converter part is not utilized a significantly higher current ripple does result as shown in **Fig.21**(a).

4.2 Reversal of the Energy Flow - Changing from Rectifier to Inverter Mode

For reversing the energy flow the system has to be switched from rectifier to inverter mode where special care has to be taken in order to avoid an uncontrollable over-current condition. In contrast switching from inverter to rectifier mode does not pose any problems.

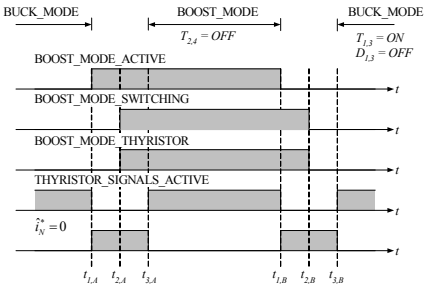


Fig.22: Sequence of control signals for the switch-over from rectifier operation to inverter operation and for switching back to rectifier operation.

The switching sequence for changing the operating mode from rectifier and/or boost- to inverter and/or buck-mode is shown in **Fig.22**. There, *BOOST_MODE_ACTIVE* denotes the signal which defines the desired operating state. If *THYRISTOR_SIGNALS_ ACTIVE* is set to zero, all thyristor firing signals are blocked; however, some thyristors will remain in one-state as long as they continue to conduct current. If NOT(*THYRISTOR_SIGNALS_ ACTIVE)=1* is valid, the reference value of the mains current amplitude $\hat{i}^*_N$ is set to zero. The signal *BOOST_MODE_ SWITCHING* defines the state of the DC side power transistors for rectifier and inverter mode according to Fig.19. For *BOOST_MODE_THYRISTOR=1* the firing angle of the thyristor bridge is set to $\alpha=0°$ (rectifier-mode) and for *BOOST_MODE_ THYRISTOR=0* to $\alpha=165°$ (inverter operation). Furthermore, the *BOOST_MODE_THYRISTOR* signal does switch-over the outputs of the signal generators shown in Figs.18 and 19 to the corresponding norm. time behavior of the reference currents i^*_{L1} and i^*_{L2} and to the corresponding pre-control signals $vst_{(L1)}$ and $vst_{(L2)}$.

For preventing an over-current condition the thyristors which have been conducting current in rectifier operation must have gained their blocking capability in $t_{2,B}$ (Fig.22). The minimum necessary duration $\Delta t=t_{2,B}-t_{1,B}$ for reaching this condition is strongly dependent on the value of the current i_M at the time the switch-over is performed and is calculated in (28)-(34).

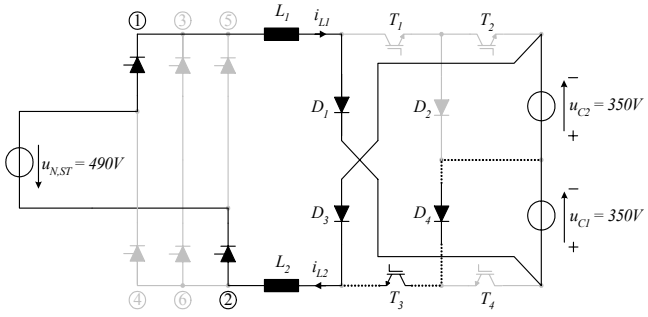


Fig.23: Active current path and voltage levels at the beginning of the switch-over from rectifier- to inverter-mode. As shown in Fig.25 for the assumed switching instant current i_{L2} is significantly larger than i_{L1}, which decays to zero within δt. The current path shown is valid for the interval δt in $\omega t=[5\pi/6 \ldots 5\pi/6+\delta t]$.

The following analysis is based on the time behavior of the currents and voltages resulting for the change-over from rectifier to inverter operation (cf. **Fig.25**). The simulation describes a worst-case condition where the switch-over is activated when transformer current i_M shows its peak value of $i_M=1.732\ \hat{i}_N$. In this case maximum energy is stored in the stray inductances L_σ of the transformer. The corresponding active current path (omitting the transformer) is shown in **Fig.23**. While i_{L2} is at maximum, i_{L1} is close to zero (cf. Fig.25(b)).

As $\hat{i}^*_N=0$ both transistors T_1 and T_3 are in the off-state and the voltage $u_{L1,2}= -(u_{C1}+u_{C2})+u_{N,ST}=-700V+490V=-210V$ is rapidly reducing the currents in L_1 and L_2.

In case T_3 would be turned on, u_{C2} would be bypassed and $u_{L1,2}= +140V$ would result (see dotted current path in Fig.23). Accordingly, i_{L1} and i_{L2} would again increase what finally would result in an over-current condition. Accordingly, T_1 and T_3 must remain in the off-state what is guaranteed by setting $\hat{i}^*_N=0$.

Note: The voltage $u_{L1,2}$ is varying over the mains period. However, as the change-over time is typically small, assuming a constant voltage is valid in a first approximation. This will also be done in the following without further notice. Only in case of switching-over from rectifier to inverter operation where a relatively long transition period does result the time-dependency of $u_{L1,2}$ is taken into account (as shown in Fig.25 and (28) – (34)).

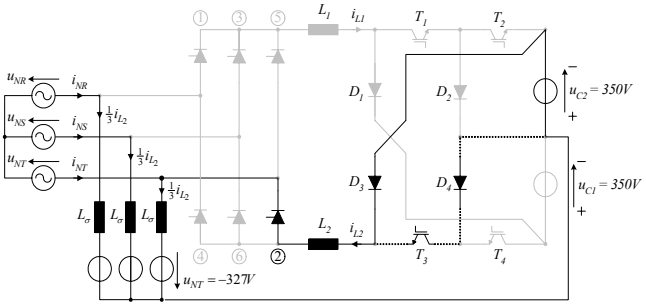


Fig.24: Active current path and voltage levels in $\omega t=[5\pi/6+\delta t \ldots 5\pi/6+\Delta t]$ after i_{L1} has reached zero (cf. Fig.23, $\delta t \approx 0$ is assumed, cf. also Fig.25).

As i_{L1} is already close to zero at the beginning of the change-over the current path shown in Fig.23 is valid only for a very short time interval δt and therefore is not indicated in Fig.25. The converter conduction state being present after i_{L1} has reached zero is shown in **Fig.24**. For a high modulation index ($M_I=0.93$) as assumed for the simulations the voltage $u= u_{N,T}-u_{C1}= 327V-350V= -23V$ reducing i_{L2} is very small what results in a relatively long decay time Δt. The decay time Δt is calculated in (28)–(34) in general form and specified numerically for the assumed operating parameters in (35) where $\Delta t=1.24ms$ results what is identical to the result of the digital simulation shown in Fig.25.

$$L_\sigma \frac{d}{dt}\left(\frac{1}{3}i_{L2}\right) + L_2 \frac{d\,i_{L2}}{dt} = -(u_{N,T} + u_{C2}) \tag{28}$$

$$u_{N,T} = \hat{u}_N \sin\left(\omega t - \frac{4\pi}{3}\right) \qquad u_{C2} = \frac{U_{DC}}{2} \tag{29}$$

$$i_{L2}\left(\omega t = \frac{5\pi}{6}\right) = \sqrt{3}\,\hat{i}_N \tag{30}$$

$$\omega = 2\pi f_N \tag{31}$$

$$i_{L2}(t) = \frac{\hat{u}_N \cos(\omega t - \frac{4\pi}{3}) - \frac{U_{DC}}{2}(\omega t - \frac{5\pi}{6})}{\omega(L_2 + L_\sigma/3)} + \sqrt{3}\,\hat{i}_N \qquad (32)$$

$$i_{L2}(t_0) = 0 \qquad \Delta t = t_0 - \frac{5\pi/6}{\omega} \qquad (33)$$

$$(\omega\Delta t) - M_1 \sin(\omega\Delta t) = \frac{\omega(L_2 + L_\sigma/3)\sqrt{3}\,\hat{i}_N}{U_{DC}/2} \qquad (34)$$

$$(100\pi\Delta t) - 0.93\sin(100\pi\Delta t) = 0.0364 \Rightarrow \quad \Delta t = 1.24\,ms\,. \qquad (35)$$

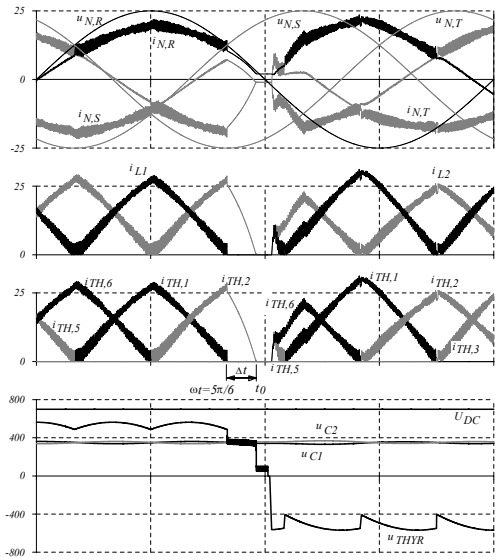


Fig.25: Simulation of the switch-over from rectifier to inverter operation at the maximum of current $i_M = 1.732\ \hat{i}_N$ (worst case concerning the switch-over time) at $\omega t = 5\pi/6$ resulting in $\Delta t = 1.24ms$ (*25A/Div*, *5ms/Div, top: 330V/Div, bottom: 400V/Div*). *Note:* The mains current flow being present for $i_{L1,2}=0$ is due to the magnetizing current of the YΔ-transformer.

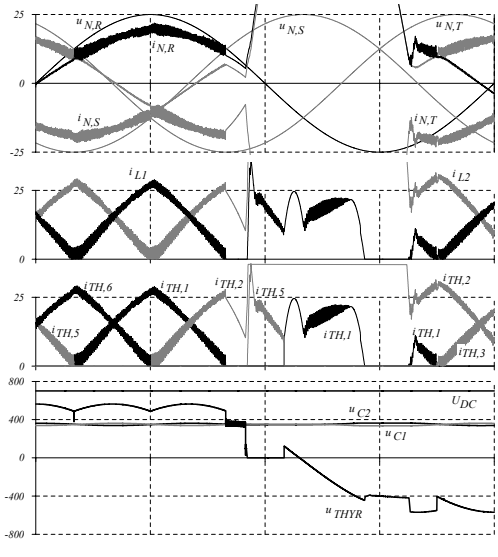


Fig.26: Simulation of the switch-over from rectifier to inverter operation at the maximum of current i_M (worst case concerning the switch-over time). If the inverter mode switching sequence is activated when the thyristors are still conducting an over-current condition does result. (*25A/Div*, *5ms/Div, top: 330V/Div, bottom: 400V/Div*).

If *BOOST_MODE_SWITCHING* would be set to zero before $t_{2,B}$ (where the thyristor bridge is still conducting current) transistor T_3 would be turned-on and u_{C2} would again be bypassed (see dotted current path in Fig.24). Accordingly, a voltage $u = +327V$ would occur across L_σ and L_2 what would result in an overcurrent condition as shown in **Fig.26**.

If the change-over from rectifier to inverter-mode is triggered at $i_M \approx 0$, i_{L1} and i_{L2} will rapidly decay to zero as shown in **Fig.27**. The corresponding conduction state is shown in Fig.23. If the change-over is triggered at $0 < i_M < 1.732\ \hat{i}_N$ the conduction states shown in Figs.23 and 24 do occur subsequently.

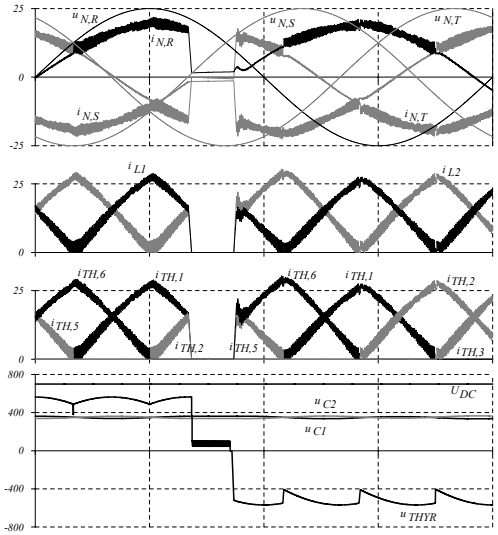


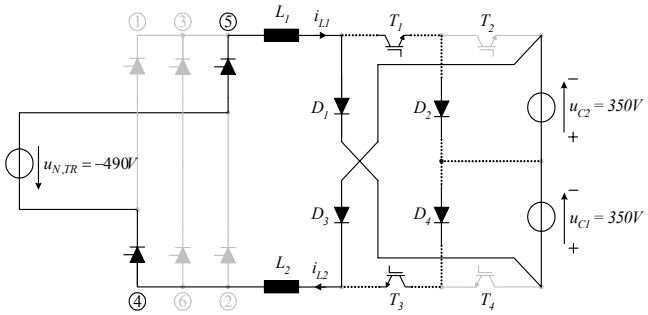
Fig.27: Simulation of the switch-over from rectifier to inverter operation at $i_M \approx 0$ resulting in a very short duration of the change-over interval. (*25A/Div*, *5ms/Div, top: 330V/Div, bottom: 400V/Div*).

In summary changing from rectifier to inverter mode might require in the worst case a minimum duration Δt according to (34). The mode-change has to be performed according to the control signal sequence given in Fig.22 in order to prevent an overcurrent condition. In general for safely changing from rectifier to inverter operation the switch-over has to be initiated only after the thyristors conducting current in rectifier mode have regained their blocking capability.

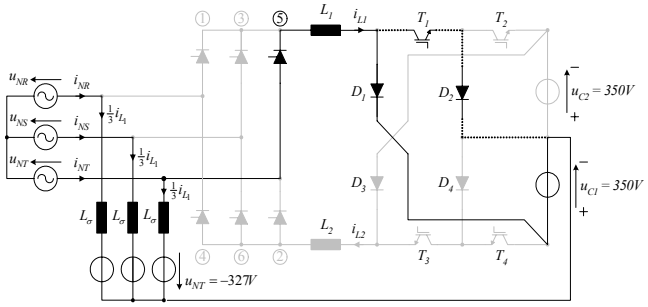
4.3 Reversal of the Energy Flow - Changing from Buck- to Boost-Mode

As shown in the following no thyristor zero current condition has to be considered for switching from inverter to rectifier operation. Therefore, the change of the operating mode can be performed significantly faster than for switching over form rectifier to inverter mode.

The switch-over from inverter to rectifier mode is triggered in $t_{1,A}$, cf. Fig.22. There, e.g. i_M shows the maximum value $i_M = 1.732.\hat{i}_N$, i_{L2} is close to zero and $i_{L1} = 1.732.\hat{i}_N$ and the thyristors *4* and *5* are conducting current (cf. **Fig.29**). The corresponding conduction state is shown in **Fig.28**(a). There, *BOOST_MODE_SWITCHING*=0 is still valid (cf. Fig.22) and/or T_1 and T_3 are in continuous on-state. Accordingly, the resulting voltage drop across the inductors shows a large negative value ($u = u_{N,TR} = -327V$) what results in a rapid decay of i_{L1} and i_{L2} (dotted current path in **Fig.28**(a)). In case the transistors T_1 and T_3 would be switched off the decay of the current would be even faster as then $u = u_{N,TR} - u_{C1} - u_{C2} = -490V - 700V = -1190V$ would be present.



(a)



(b)

Fig.28: (a) Conduction state and voltage levels at the beginning of the switch-over from inverter to rectifier operation (cf. also Fig.29). Current i_{L2} is assumed to be significant larger than i_{L1}, which rapidly approaches zero; **(b)** conduction state and voltage levels after the smaller current i_{L1} has reached zero.

The converter conduction state being present after the smaller current i_{L2} has reached zero is shown in Fig.28(b). There, $u = u_{N,T} = -327V$ does remain. If T_1 would be turned off the rate of decay of i_{L1} would increase as u would then increase to $u = u_{N,T} - u_{C1} = -327V - 350V = -677V$.

In summary, the analysis shows that changing from inverter to rectifier operation is not critical concerning over-current as the voltage drop across the inductances shows a large negative value for all switching states of the power transistors.

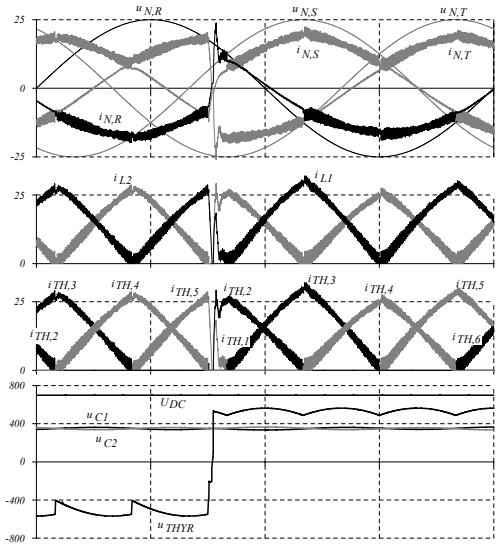


Fig.29: Simulation of the switch-over from inverter to rectifier operation at the maximum of current i_M , $i_M = 1.732\ \hat{i}_N$. (*25A/Div*, *5ms/Div, top: 330V/Div, bottom: 400V/Div*).

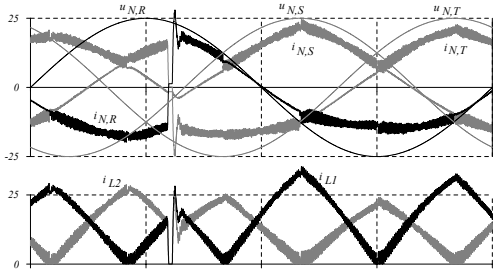
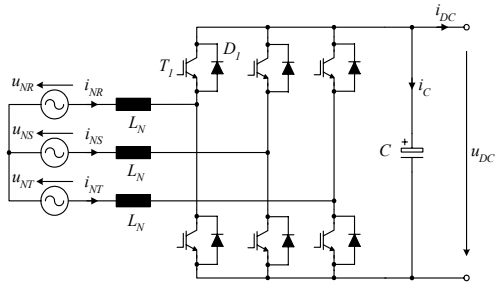


Fig.30: Simulation of switch-over from inverter to rectifier operation at zero current $i_M \approx 0$. (*25A/Div*, *330V/Div*, *5ms/Div*).

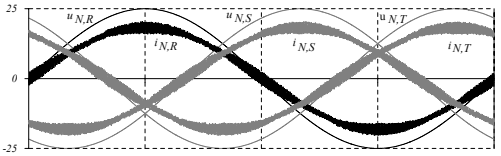
5 Comparative Evaluation of the Proposed System

Conventional three-phase voltage DC link (six-switch) PWM converter systems (cf. **Fig.31**(a)) are characterized by sinusoidal input current and are widely employed for bi-directional AC-DC energy conversion. In this section the proposed converter system will be comparatively evaluated against the six-switch converter based on characteristic quantities defined in [9].

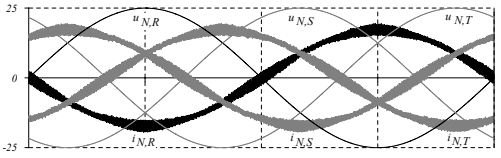
The comparison is for equal AC-side current amplitudes and voltage levels, and equal power levels, and equal switching frequencies of both systems. Furthermore, the AC side inductances L_N of the six-switch converter are set to values which result in an AC side current ripple $\Delta i_{N,i}$ of about equal amplitude as given for the proposed converter (compare Figs.5(a) and 9(a) to Figs.31(b) and (c)). The resulting current stresses on the power semiconductors of the six-switch converter are compiled in **Tab.2**.



(a)



(b)



(c)

Fig.31: (a) Topology of a conventional DC voltage link (six-switch) PWM converter and **(b)** digital simulation of mains current $i_{N,RST}$ (phase voltage $u_{N,R}$ and the corresponding phase current $i_{N,R}$ are shown in black, while the other two phase quantities are shown in grey (rectifier operation for $\hat{i}_N = 18.0A$); **(c)** inverter operation for $\hat{i}_N = 17.4A$ ($\cos\varphi = -1$) to be compared to operation at $\cos\varphi = \cos(15°) = -0.966$ of the proposed converter system. (*25A/Div*, *330V/Div*, *5ms/Div*).

The parameters assumed for the conventional voltage DC link PWM converter (Fig.31(a)) are

$\hat{u}_N = 327\ V$	mains phase voltage amplitude
$\hat{i}_N = 18\ A$	mains phase current amplitude
$U_{DC} = 700\ V$	DC-side voltage
$P = P_{DC} = 9.0\ kW$	system output power
$L_N = 1.3\ mH$	AC-side inductance
$C = 1.0\ mF$	DC-side capacitance
$f_P = 16\ kHz$	switching frequency

	Rectifier Operation			Inverter Operation		
	AVG	RMS	MAX	AVG	RMS	MAX
$i_{T,1}$	0.8	2.9	18.4	4.8	8.2	19.4
$i_{D,1}$	5.0	8.6	20.4	0.7	2.8	17.5
$i_{L,N}$	0	12.9	20.3	15.0	12.2	19.5
i_C	0	7.0	20.2	0	6.3	19.4

Tab.2: Current stresses on the power components of the conventional voltage DC link inverter as derived by digital simulations.

As discussed in detail in [9] a direct comparison of different three-phase PWM converter systems can be based on the following characteristic quantities

$$\text{transistor utilization} = \frac{P_0}{\sum_n u_{T,\max,n}\, i_{T,\max,n}} \tag{36}$$

$$\text{transistor conduction losses} = \frac{1}{I_0}\sum_n i_{T,avg,n} \tag{37}$$

$$\text{transistor switching losses} = \frac{1}{P_0}\sum_n (i_{T,env})_{avg,n}\, U_{T,off,n} \tag{38}$$

$$\text{diode utilization} = \frac{P_0}{\sum_n u_{D,\max,n}\, i_{D,avg,n}} \tag{39}$$

$$\text{diode conduction losses} = \frac{1}{I_0}\sum_n i_{D,avg,n} \tag{40}$$

$$\text{capacitor current stress} = \frac{1}{k_{ESR}}\frac{i_{C,rms}}{I_0}\,. \tag{41}$$

There, the total output power is denoted by P_0 ($P_0=P=P_{DC}$), I_0 is the DC side current ($I_0=P/U_{DC}$), and $i_{T,env,avg}$ is the average value (over one mains period) of the time-varying envelope of the transistor current i_T. In case the switching frequency f_P is higher than *10kHz* the frequency dependency of the equivalent series resistor of electrolytic capacitors is onsidered in (41) by $k_{ESR}=1.5$ while $k_{ESR}=1.0$ is assumed for $f_P<10kH.$.

Comparison with emphasis on the fast switching devices (thyr. bridge *not* considered)	**Bi-direct. Converter**		**Six-switch Converter**	
	rect.	inv.	rect.	inv.
number of transistors	4		6	
transistor utilization	0.44	0.42	0.11	0.10
transistor conduction losses	0.39	4.42	0.38	2.32
transistor switching losses	1.19	1.21	2.73	2.73
number of fast recov. (f.r.) diodes	4		6	
(f.r.) diode utilization	0.83	4.86	0.42	2.89
(f.r.) diode conduction losses	2.34	0.40	2.34	0.34
output capacitor current stress	0.49	0.54	0.36	0.34

Tab.3: General comparison of the proposed converter and the six-switch converter.

6 Conclusions

A novel bi-directional three-phase converter system with largely sinusoidal input currents has been proposed. The system does employ a single thyristor bridge and four turn-off power semiconductors which face only half of the DC output voltage as nominal blocking voltage stress. The system can be considered as an integration of two unidirectional versions of the Minnesota Rectifier with reduced component count.

The comparison of the system to a conventional voltage DC link converter indicates a high utilization of the DC-side power semiconductors. Therefore, the system is interesting for a wide area of applications like AC drive systems and high-power UPS. A 10kW prototype of the system is currently under construction, experimental results will be published in near future.

Appendix

Analytical Calculation of Current Stresses on the Power Components

The current stresses on the power components can be calculated based on the modulation functions defined by (11), and (16) for rectifier mode and by (22), and (26) for inverter mode. The current stresses on the thyristors, on the DC-side inductors L_1,L_2 and on the YΔ-transformer are independent of the operating mode (rectifier or inverter operation).

$$i_{THYR,avg} = \frac{1}{2\pi}\left[\int_{7\pi/6}^{9\pi/6} i^*_{L2,34}(\varphi)\, d\varphi + \int_{9\pi/6}^{11\pi/6} i^*_{L2,45}(\varphi)\, d\varphi\right] = \frac{\sqrt{3}}{2\pi}\hat{i}_N = 0.276\,\hat{i}_N \tag{A.1}$$

$$i^2_{THYR,rms} = \frac{1}{2\pi}\left(\int_{7\pi/6}^{9\pi/6} (i^*_{L2,34}(\varphi))^2\, d\varphi + \int_{9\pi/6}^{11\pi/6} (i^*_{L2,45}(\varphi))^2\, d\varphi\right) = \left(\frac{1}{2} - \frac{3\sqrt{3}}{8\pi}\right)\hat{i}^2_N = 0.293\,\hat{i}^2_N \tag{A.2}$$

$$i_{L,avg} = 3\, i_{THYR,avg} = \frac{3\sqrt{3}}{2\pi}\hat{i}_N = 0.827\,\hat{i}_N \tag{A.3}$$

$$i^2_{L,rms} = 3\, i^2_{THYR,rms} = \left(\frac{3}{2} - \frac{9\sqrt{3}}{8\pi}\right)\hat{i}^2_N = 0.880\,\hat{i}^2_N \tag{A.4}$$

$$i_{L,\max} = \sqrt{3}\,\hat{i}_N \quad . \tag{A.5}$$

For the Y-windings of the transformer we receive

$$i_{TrY,avg} = \frac{1}{2\pi/3}\left(\int_{7\pi/6}^{9\pi/6} \frac{1}{3}(i^*_{L1,34}(\varphi) - i^*_{L2,34}(\varphi))\, d\varphi + \int_{9\pi/6}^{11\pi/6} \frac{1}{3}(i^*_{L1,45}(\varphi) - i^*_{L2,45}(\varphi))\, d\varphi = 0\right) \tag{A.6}$$

$$i^2_{TrY,rms} = \frac{1}{2\pi/3}\left(\int_{7\pi/6}^{9\pi/6} \left(\frac{1}{3}(i^*_{L1,34}(\varphi) - i^*_{L2,34}(\varphi))\right)^2 d\varphi + \int_{9\pi/6}^{11\pi/6} \left(\frac{1}{3}(i^*_{L1,45}(\varphi) - i^*_{L2,45}(\varphi))\right)^2 d\varphi\right) = \left(\frac{1}{2} - \frac{3\sqrt{3}}{4\pi}\right)\hat{i}^2_N = 0.087\,\hat{i}^2_N \tag{A.7}$$

$$i_{TrY,\max} = \frac{1}{3}\sqrt{3}\,\hat{i}_N = \frac{1}{\sqrt{3}}\hat{i}_N = 0.577\,\hat{i}_N \quad . \tag{A.8}$$

In case of rectifier operation the avg- and rms-values of the DC-side power semiconductor currents are different to inverter-mode and are calculated as

$$i_{T13,avg} = \frac{1}{2\pi/3}\left(\int_{7\pi/6}^{9\pi/6} (d_{3,34}(\varphi))\, i^*_{L2,34}(\varphi)\, d\varphi + \int_{9\pi/6}^{11\pi/6} (d_{3,45}(\varphi))\, i^*_{L2,45}(\varphi)\, d\varphi\right) = \left(\frac{3\sqrt{3}}{2\pi} - \frac{3}{4}M_1\right)\hat{i}_N \tag{A.9}$$

$$i_{T13,rms}^2 = \frac{1}{2\pi/3}\Big(\int_{7\pi/6}^{9\pi/6}(d_{3,34}(\varphi))\,(i_{L2,34}^*(\varphi))^2\,d\varphi + \int_{9\pi/6}^{11\pi/6}(d_{3,45}(\varphi))\,(i_{L2,45}^*(\varphi))^2\,d\varphi\Big) = \Big(\frac{3}{2} - \frac{9\sqrt{3}}{8\pi} - \frac{3\sqrt{3}}{2\pi}M_1\Big)\,\hat{i}_N^2 \quad \text{(A.10)}$$

$$i_{T24,avg} = 0 \qquad i_{T24,rms}^2 = 0 \quad \text{(A.11)}$$

$$i_{D13,avg} = \frac{1}{2\pi/3}\Big(\int_{7\pi/6}^{9\pi/6}(1-d_{3,34}(\varphi))\,i_{L2,34}^*(\varphi)\,d\varphi + \int_{9\pi/6}^{11\pi/6}(1-d_{3,45}(\varphi))\,i_{L2,45}^*(\varphi)\,d\varphi\Big) = \frac{3}{4}M_1\,\hat{i}_N \quad \text{(A.12)}$$

$$i_{D13,rms}^2 = \frac{1}{2\pi/3}\Big(\int_{7\pi/6}^{9\pi/6}(1-d_{3,34}(\varphi))\,(i_{L2,34}^*(\varphi))^2\,d\varphi + \int_{9\pi/6}^{11\pi/6}(1-d_{3,45}(\varphi))\,(i_{L2,45}^*(\varphi))^2\,d\varphi\Big) = \frac{3\sqrt{3}}{2\pi}M_1\,\hat{i}_N^2 \quad \text{(A.13)}$$

$$i_{D24,avg} = i_{T13,avg} \qquad i_{D24,rms}^2 = i_{T13,rms}^2 \quad \text{(A.14)}$$

$$i_{C12,rms}^2 = i_{D13,rms}^2 - I_{DC}^2 = \frac{3\sqrt{3}}{2\pi}M_1\,\hat{i}_N^2 - \Big(\frac{P_{DC}}{U_{DC}}\Big)^2. \quad \text{(A.15)}$$

For inverter operation the thyristor bridge firing angle α is close to π (the difference is denoted by $\zeta=\pi-\alpha$, cf. (17)). There, the power component current stress is

$$i_{T13,avg} = i_{L,avg} = \frac{3\sqrt{3}}{2\pi}\hat{i}_N = 0.827\,\hat{i}_N \quad \text{(A.16)}$$

$$i_{T13,rms}^2 = i_{L,rms}^2 = \Big(\frac{3}{2} - \frac{9\sqrt{3}}{8\pi}\Big)\,\hat{i}_N^2 = 0.880\,\hat{i}_N^2 \quad \text{(A.17)}$$

$$i_{T24,avg} = \frac{1}{2\pi/3}\Big(\int_{\pi/6-\zeta}^{3\pi/6-\zeta} d_{4,34}(\varphi)\,i_{L2,34}^*(\varphi)\,d\varphi + \int_{3\pi/6-\zeta}^{5\pi/6-\zeta} d_{4,45}(\varphi)\,i_{L2,45}^*(\varphi)\,d\varphi\Big) = \frac{3}{4}M_1\cos(\zeta)\,\hat{i}_N \quad \text{(A.18)}$$

$$i_{T24,rms}^2 = \frac{1}{2\pi/3}\Big(\int_{\pi/6-\zeta}^{3\pi/6-\zeta} d_{4,34}(\varphi)\,(i_{L2,34}^*(\varphi))^2\,d\varphi + \int_{3\pi/6-\zeta}^{5\pi/6-\zeta} d_{4,45}(\varphi)\,(i_{L2,45}^*(\varphi))^2\,d\varphi\Big) = \frac{3\sqrt{3}}{2\pi}M_1\cos(\zeta)\,\hat{i}_N^2 \quad \text{(A.19)}$$

$$i_{D13,avg} = 0 \qquad i_{D13,rms}^2 = 0 \quad \text{(A.20)}$$

$$i_{D24,avg} = \frac{1}{2\pi/3}\Big(\int_{\pi/6-\zeta}^{3\pi/6-\zeta}(1-d_{4,34}(\varphi))\,i_{L2,34}^*(\varphi)\,d\varphi + \int_{3\pi/6-\zeta}^{5\pi/6-\zeta}(1-d_{4,45}(\varphi))\,i_{L2,45}^*(\varphi)\,d\varphi\Big) = \Big(\frac{3\sqrt{3}}{2\pi} - \frac{3}{4}M_1\cos(\zeta)\Big)\,\hat{i}_N \quad \text{(A.21)}$$

$$i_{D24,rms}^2 = \frac{1}{2\pi/3}\Big(\int_{\pi/6-\zeta}^{3\pi/6-\zeta}(1-d_{4,34}(\varphi))\,(i_{L2,34}^*(\varphi))^2\,d\varphi + \int_{3\pi/6-\zeta}^{5\pi/6-\zeta}(1-d_{4,45}(\varphi))\,(i_{L2,45}^*(\varphi))^2\,d\varphi\Big) = \Big(\frac{3}{2} - \frac{9\sqrt{3}}{8\pi} - \frac{3\sqrt{3}}{2\pi}M_1\cos(\zeta)\Big)\,\hat{i}_N^2 \quad \text{(A.22)}$$

$$i_{C12,rms}^2 = i_{T24,rms}^2 - I_{DC}^2 = \frac{3\sqrt{3}}{2\pi}M_1\cos(\zeta)\,\hat{i}_N^2 - \Big(\frac{P_{DC}}{U_{DC}}\Big)^2. \quad \text{(A.23)}$$

The voltage drops (low-frequency components) across the inductances L_1, L_2 and L_σ has been taken into account in all calculations but does take only minor influence on the final results.

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