Theoretical Converter Power Density Limits for Forced Convection Cooling

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Abstract. Power density, defined as ratio of converter output power and converter volume, is an important parameter characterizing the compactness of power electronic systems. Employing water-cooling, converters in the kW-range with power densities up to *10kW/liter* have already been built. Higher power densities up to *50kW/liter* are under discussion. There is often a desire to employ air-cooling instead of water cooling. In this paper the theoretical converter power density limits for forced convection cooling are investigated. Since the cooling system contributes significantly to the overall converter volume, the paper is restricted to an investigation of the cooling system. The main idea is to increase the power semiconductor junction temperature and, therefore, the heat sink temperature in order to make the heat transfer via forced convection much more effective, thus resulting in a smaller heat sink. This beneficial effect of higher temperatures is partly offset by increased system losses and reduced efficiency. To design thermally optimized heat sinks for today's commercially available fans is shown to be one key to a converter system optimized in terms of power density. It is shown that by employing SiC-devices, power densities of the converter's cooling system (not of the whole converter system) of up to *83kW/liter* are possible for forced air-cooling.

1 INTRODUCTION

With the integration of power converters into large and complex systems like machinery, airplanes or cars, there is a strong desire to reduce the size of the converter while, at the same time, to increase the output power. The ratio of output power and converter volume is called the power density [*kW/liter*] of the system, which characterizes the compactness of the converter design. While today converters in the kW-range have already been built with power densities up to *10kW/liter* by employing water cooling (e.g. [1], [2]), higher power densities in combination with forced air cooling are under discussion. Since the cooling system contributes significantly to the total volume of the converter, the theoretical power density of the cooling system (converter output power divided through the converter's cooling system volume) indicates one important theoretical limit of the whole converter system's power density.

In section (2) there is a detailed discussion about optimization of air cooled heat sinks. A general mathematical optimization scheme is introduced, and the results are verified via numerical simulations and experiments. Defining a cooling system performance index allows simple and direct comparisons between different heat sink types (concerning power density), and shows that heat sinks employed today in power electronics could be improved significantly.

In section (3) modern power semiconductors are investigated concerning their switching- and conduction loss in dependency on the junction temperature. For temperatures up to *150°C* a combination of a CoolMOS transistor and SiC-diodes is discussed. For higher temperatures up to *300°C*, SiC-diodes in combination with SiC-transistors are considered. All semiconductor data is derived from datasheets and literature.

In section (4) the theoretical converter system power density is discussed under the assumption that the cooling system contributes significantly to the total converter volume. To determine the theoretical power density limit it is important to employ thermally optimized heat sinks as discussed in section 1. The central idea in section (4) is to increase the junction temperature and, therefore, also the heat sink temperature in order to increase the convective cooling and thus results in a reduced heat sink volume. As a counter-effect the system efficiency will decrease with increased junction temperatures due to higher semiconductor losses, which will make a larger heat sink necessary. Based on the semiconductor data presented in section (3), the converter power density for junction temperatures up to *300°C* will be investigated.

2 OPTIMIZING AIR-COOLED HEAT SINKS

2.1 Optimization Strategy for Achieving High Power Density

For determining the theoretical limits of the power density of the cooling system, the air-cooled heat sink has to be optimized. The optimization is performed based on theoretical assumptions (section 2.2), tested by numerical CFD simulations (ICEPAK) and verified experimentally (section 2.3).

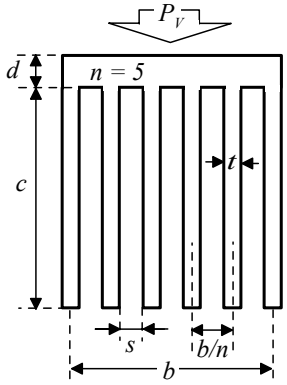


Fig.1: Geometry of an extruded heat sink with six fins and five channels (n=5).

Using the definitions of the heat sink geometry as shown in **Fig.1**, we define for the following discussions the fin spacing ratio as

$$k = \frac{s}{b/n} \qquad (1)$$

with values between zero and one, characterizing the cross-section of the heat sink available for air flow.

Generally, the following effects have to be considered when designing a heat sink for maximum power density:

- The fan size defines the heat sink front geometry. Only fins that are facing a fan, and, therefore, air flow, contribute to convective heat transfer. Choosing, e.g., a *40×40mm²* fan results in a heat sink geometry *b=40mm* and *c=40mm* in order to fully utilize the fan.
- The heat sink base plate size must provide sufficient space for the power semiconductors. This gives a good estimation of the minimum heat sink base plate size (heat sink width *b* and heat sink length *L*) needed for a converter system.
- The heat sink base plate (with thickness *d*) acts as heat spreader to avoid hot spots and to homogenously distribute the

heat from the power semiconductors to the fins. Increasing thickness *d* improves homogenous heat distribution but also increases the thermal resistance of the heat sink. An optimum thickness *d* has to be found.

- The fin spacing ratio *k* (and/or cannel width *s* plus channel number *n*) of the heat sink design defines together with the characteristic of the chosen fan an operating point (air flow at a certain pressure drop). The resulting convective heat transfer is strongly dependent on this operating point.
- The fin thickness *t* has to be large enough to allow heat flow through the whole length *c* of the fin. If *t* is too thin, the heat will not be equally distributed over the whole fin surface, which reduces the effective fin surface and might make a part of the fin (and the according heat sink volume) useless.
- The heat sink material has a strong impact on the optimum heat sink design. If a heat sink (with sufficient fin thickness *t*) made of, e.g., aluminium is made of copper instead, the thermal conductivity of the material will nearly double. But for unchanged heat sink geometry the thermal resistance of the heat sink will hardly be reduced because for a well designed heat sink the convective thermal resistance from fin surface to air in the channel is much larger than the thermal resistance of base plate and fins. On the other hand, because the thermal conductivity of the material doubles, the fin thickness could be reduced by a factor of two. Therefore, the number of fins can be increased so that the total fin surface increases accordingly while the fan operating point remains unchanged at the optimum. This means that by replacing, e.g., aluminium with copper, the heat sink geometry must be adapted in order to reduce the total heat sink volume but achieving equal thermal resistance. The potential of volume reduction can be indicated in approximation by the ratio of the thermal conductivities of the involved materials ($\lambda_{Cu}/\lambda_{Al} = 380/210 \approx 1.8$).
- Increasing the length *L* of the heat sink in air flow direction increases the total fin surface and, therefore, the heat transfer. But also the air pressure drop in the channels is increased, which changes the fan operating point and results in a reduced air flow which increases the air temperature in the channels. This effect encounters the gain of the increased fin surface.
- High air flow velocity results in a high Reynolds number indicating improved heat transfer which can be achieved by small channel width *s*. Small channel width *s*, on the other hand, means low volume flow. The volume flow of air transports away the heat and is inverse proportional to the temperature rise of the air from channel inlet to channel outlet. Therefore, a small channel width *s* gives a large Reynolds number resulting in a large Nusselt number. This means good convective heat transfer from surface into air (small convective thermal resistance), but due to the small volume flow the temperature rise along the channel will encounter this desired effect and increase the thermal resistance of the heat sink.
- If the temperature rise along the channel is very high (small channel width *s* and/or large heat sink length *L*), the temperature gradient between fin surface and channel air will be very small after a certain length $L_x < L$. The resulting heat flow at this location of the channel will be accordingly small, and the remaining length $\Delta L = L - L_x$ of the heat sink will not contribute to heat transfer. It will not only add useless volume but will also create an additional pressure drop with negative impact on the fan operating point.
- With an extruded heat sink fin shape the optimum fan operating point can be arbitrarily set by defining the heat sink geometry. Employing different fin shape configurations (e.g., pin fins) might result in different fin surface and fan operating point (air flow at a certain pressure drop) for the same given fan, but will not show significant overall thermal performance improvement. Therefore, all optimizations in the following can be restricted to the extruded fin shape configuration as shown in Fig.1.
- Very small fin thickness *t* and/or very small channel width *s* might result in increasingly high and even unacceptable manufacturing effort. Generally, a low fin number is desired to keep fin thickness *t* and channel width *s* large. One has to check if the design optimization provides sub-optima of the thermal resistance of the heat sink for low fin numbers that are only slightly worse than the overall thermal optimum might be at a higher fin number.

Generally, there is always an optimum geometric design for a fan/heat sink configuration employing forced convection cooling resulting in maximum cooling and/or minimum thermal resistance. For a selected fan (defining *b* and *c* of the heat sink) the fan characteristic, three different geometry design parameters (*k*, *n*, *L*) and the heat sink material ($\lambda_{HeatSink}$) provide a complex optimization problem. How to find the optimum heat sink design is discussed in the following section theoretically and verified experimentally. As will be shown, a careful heat sink optimization can result in significant improvement of the power density of the cooling system.

2.2 Analytical Optimization of a Heat Sink Geometry

Convective heat transfer can be calculated by solving a set of five scalar partial differential equations including the Navier-Stokes equations (three scalar components of a vector equation) describing fluid flow, and two more equations describing mass and energy conservation. Solutions can be numerically found by 3D CFD (computational fluid dynamics) software. Unfortunately, such calculations are very time-consuming, often show numerical instability, and optimization can only be performed by systematic parameter variations (very time-consuming try-and-error procedure with no guarantee to find all local optima). As an alternative, empirical equations are available (e.g., in [3]) describing a large range of different geometries. These equations are based on experimental data and/or analytical solutions of the heat transfer differential equations and generally describe problems employing three normalized parameters called Reynolds number *Re* (normalized fluid flow), Nusselt number *Nu* (normalized convective heat transfer) and Prandtl number *Pr* (fluid characteristics). These empirical equations are accurate and very useful to simply describe complex convective heat transfer problems in dependency of geometric parameters. Therefore, a systematic optimization can be analytically performed with no need to solve complicated fluid dynamics equations analytically.

The calculations in the following are described in more detail in [1] where the fluid was water. The heat sink geometry is basically the same, and some geometry parameters have been renamed. The only essential change is setting the Prandtl number for air (there is a weak temperature dependency of *Pr*, here we set an air temperature of *80°C*) with $Pr = Pr_{AIR(80°C)} = 0.7083$ instead of the one for water with $Pr_{H20(40°C)} = 4.328$.

The fan characteristic can be described by a 5th order approximation (dashed curve in **Fig.2**) as

$$\Delta p_{SanAce40}(\dot{V}) = 335 + 4374 \cdot \dot{V} - 40.9 \cdot 10^{6} \cdot \dot{V}^{2} + 1.07 \cdot 10^{10} \cdot \dot{V}^{3} - 1.04 \cdot 10^{12} \cdot \dot{V}^{4} + 3.43 \cdot 10^{13} \cdot \dot{V}^{5} \quad (2)$$

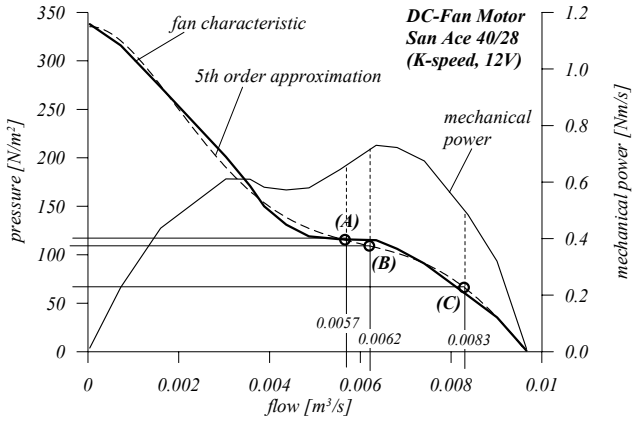


Fig.2: Fan characteristic of a DC-Fan Motor San Ace 40/28 (K-speed, 12V) as given in the datasheet [4]. A 5th order approximation of the characteristic is shown as dashed line and given in (2). While the electrical power consumption of the fan is not very much dependent on the operating point, the mechanical power of the air flow is strongly dependent on the air flow. For three different heat sink designs (introduced in section (2.3)) the optimum operating points (A), (B), (C) are shown.

Defining the hydraulic diameter of one channel

$$d_h = \frac{2s \cdot c}{s + c} \tag{3}$$

for a given fin geometry, the total air flow through all channels creates a pressure drop along the heat sink length L which is given for laminar flow as ((3.221) in [3])

$$\Delta p_{lam}(\dot{V}) = 1.5 \cdot \frac{32\,\rho \nu L}{n(s \cdot c) d_h^2}\ \dot{V} \tag{4}$$

with number of channels n. The air density at *80°C* is $\rho_{80°C}$ = *=0.9859 kg/m³* and the cinematic viscosity of the air is $\nu_{80°C}$ = $=213.5 \cdot 10^{-7} m^2/s$. The correction factor *1.5* in (4) takes into account the non-quadratic channel shape characterized by $s << c$. In case of turbulent flow the pressure drop is given as ((3.261) in [3])

$$\Delta p_{turb}(\dot{V}) = \frac{L \frac{s+c}{2s \cdot c} \rho \frac{1}{2} \left(\frac{\dot{V}}{n(s \cdot c)}\right)^2}{\left(0.79 \cdot \ln\left(\frac{2\dot{V}}{n\,(s+c)\nu}\right) - 1.64\right)^2} \tag{5}$$

with the average Reynolds number Re_m defined for this problem as (page 351 in [3])

$$Re_m = \frac{w_m \cdot d_h}{\nu} = \frac{2\dot{V}}{n(s+c)\nu}\,. \tag{6}$$

If the Re_m is smaller than *2300*, the flow is laminar, otherwise turbulent. Laminar flow means that oscillations of air particles are damped out while in case of turbulent flow oscillations of air particles are amplified. Therefore, turbulent flow creates better energy exchange between neighbor particles resulting in better heat transfer, but on the other hand increases the pressure drop associated with the flow through the channels. The fan is facing the front side of the heat sink (Fig.1) where only the cross section area $A_{CROSS} = k \cdot b \cdot c$ is available for air flow. This is considered by multiplying the effectively available air pressure of the fan with the fin spacing ration k (7). Here lies potential for further optimization of the heat sink by sharpening the fins at the heat sink inlet in air flow direction in order to increase the pressure available for air-flow. According research activities are currently performed.

Employing (2) and (4), one can calculate the flow volume in case of laminar flow from (7). If the resulting Reynolds number (6) is smaller than *2300*, the assumption of laminar flow is justified, otherwise (7) has to be rewritten for turbulent flow employing (2) and (5) to find the correct flow and Reynolds number of the design problem.

$$k \cdot \Delta p_{SanAce40}(\dot{V}) = \Delta p_{lam}(\dot{V}_{lam}) \rightarrow \dot{V}_{lam} \rightarrow Re_{m,lam} < 2300\,? \tag{7}$$

For laminar flow the average Nusselt number Nu_m can be calculated as ((3.250), (3.255) in [3])

$$Nu_{m,lam} = \frac{3.657\left[\tanh\left(2.264X^{1/3} + 1.7X^{2/3}\right)\right]^{-1} + \frac{0.0499}{X}\tanh(X)}{\tanh\left[2.432\ Pr^{1/6}X^{1/6}\right]} \tag{8}$$

with

$$X = \frac{L}{d_h Re_m Pr} \tag{9}$$

and for turbulent flow (Re_m *> 2300)* as ((3.260), (3.261) in [3])

$$Nu_{m,turb} = \frac{\{8 \cdot (0.79 \cdot \ln(Re_m) - 1.64)^2)\}^{-1}\,(Re_m - 1000)\ Pr}{1 + 12.7\sqrt{\{8 \cdot (0.79 \cdot \ln(Re_m) - 1.64)^2)\}^{-1}}\,(Pr^{2/3} - 1)} \cdot \left(1 + \left(\frac{d_h}{L}\right)^{2/3}\right) \tag{10}$$

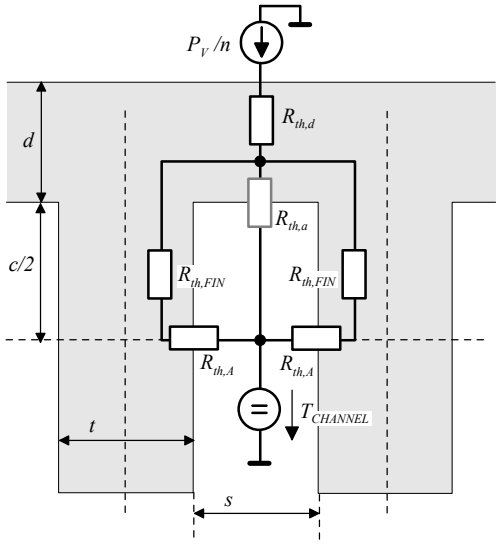


Fig.3: Thermal network describing (stationary) heat conduction between heat sink base plate and the air in the channel (temperature $T_{CHANNEL}$).

The network of thermal resistances in **Fig.3** describes the heat transfer from the heat sink base plate into the air for one channel. The convective thermal resistance $R_{th,a}$ is for geometries $s << c$ much larger than $R_{th,A}$ and will be neglected in the following. With the heat transfer coefficient h (11), the thermal resistance $R_{th,A}$ between fin surface and air channel temperature can be calculated (12). The total thermal resistance $R_{th}^{(n)}$ per channel is calculated from (15). For n channels the thermal resistance of the heat sink $R_{th,S\text{-}a}^{(HS)}$ from base plate surface to ambient (air temperature at the heat sink *inlet*) is calculated from (16), where the second term on the right side of the equation represents the average temperature rise of the air in the channel due to the heat transported away via convection.

$$h = \frac{Nu_m \cdot \lambda_{air}}{d_h} \tag{11}$$

$$R_{th,A} = \frac{1}{h \cdot L \cdot c} << R_{th,a} = \frac{1}{h \cdot L \cdot s} \tag{12}$$

$$R_{th,FIN} = \frac{\frac{1}{2}c}{\frac{1}{2}t \cdot L \cdot \lambda_{HS}} \tag{13}$$

$$R_{th,d} = \frac{d}{\frac{1}{n} A_{HS} \lambda_{HS}} \tag{14}$$

$$R_{th}^{(n)} = R_{th,d} + \tfrac{1}{2}(R_{th,FIN} + R_{th,A}) \tag{15}$$

$$R_{th,S-a}^{(HS)} = \tfrac{1}{n} R_{th}^{(n)} + \frac{0.5}{\rho_{air} c_{P,air} \dot{V}} \tag{16}$$

All equations (2) – (16) can be solved numerically. By variations of k and n the minimum thermal resistance of the heat sink $R_{th,S\_a}^{(HS)}$ is found for a selected fan. Results are given in the next section (2.3).

2.3 Experimental Results

Heat sinks for different operating conditions are optimized for a *10kW* Vienna Rectifier with *500kHz* switching frequency [2], see section 4. With a system efficiency of *96%* the power loss per module [5] is assumed to be *150W*.

With an ambient temperature T_a*=45°C* and a target temperature of the heat sink surface of T_S*=110°C*, a heat sink with a thermal resistance of

$$R_{th,S-a}^{(HS)} = \frac{110-45}{3 \cdot 150} = 0.144 \tfrac{K}{W} \tag{17}$$

has to be designed. Selecting the fan San Ace 40/28 (K-speed, 12Vdc) [4] guarantees a flat heat sink design with *c=40mm*. Employing the design procedure described in the previous section shows that it is necessary to employ two such fans in parallel to meet requirement (17). The resulting optimized heat sink (aluminium) is shown in **Fig.4**. The heat sink, labeled "Type (A)" in the following, shows according to (2) – (16) a local optimum at (*n=42/ s=1.1mm/ t=0.79mm* → R_{th,S_a}*= =0.177K/W*), at (*n=60/ s=0.9mm/ t=0.43mm* → R_{th,S_a}*= =0.170K/W*) and at (*n=70/ s=0.8mm/ t=0.34mm* → R_{th,S_a}*= =0.170K/W*). Since the manufacturing of the prototype Fig.4 (b,c) becomes increasingly difficult with higher channel numbers (increasingly thinner fins and smaller channels) the "Type (A)" heat sink was designed at a sub-optimum (*n=40/ s=1.0mm / t=0.98mm*). The according fan operating point is shown in Fig.2 resulting in an air flow of *0.0057m³/s*.

The optimum design parameters derived analytically from (2) – (16) were verified by numerical ICEPAK-calculations (3D-FEM CFD). The analytical equations proved to give highly accurate design guidelines for finding the optimum. On the other hand, the absolute values of the thermal resistance of the heat sink differ by up to *20%* from the measurements. The analytical calculations predict higher thermal resistance values than measured. This might be due to the use of the fin spacing ratio k in (7) which is just a rough approximation of the pressure loss at the channel inlet. Future research will be concentrated on finding a more accurate approximation of this effect by employing a correction factor and/or function. The thermal resistance calculated analytically above is, therefore, higher than the target value given in (17). This is true for all heat sink optimizations in this section.

With the same ambient temperature T_a*=45°C* and a higher target temperature of the heat sink surface T_S*=160°C*, a heat sink with a thermal resistance of

$$R_{th,S-a}^{(HS)} = \frac{160-45}{3 \cdot 150} = 0.256 \tfrac{K}{W} \tag{18}$$

has to be designed. There is an additional temperature drop from semiconductor junction to case and another one from case to heat sink surface due to the thermal grease between power module and heat sink surface. Therefore, the junction temperature will be in the range of *175°C* which can be realized by employing SiC power semiconductors. Again, selecting the fan San Ace 40/28 (K-speed, 12Vdc) [4] gives *c=40mm*. One fan is sufficient to meet the requirements resulting in *b=40mm*. The optimized heat sink (aluminium) is shown in **Fig.5**. The heat sink "Type (B)" shows a local optimum at (*n=16/ s=1.5mm/ t=0.94mm* → R_{th,S_a}*=0.33K/W*), at (*n=22/ s=1.3mm/ t=0.50mm* → R_{th,S_a}*= =0.31K/W*) and at (*n=30/ s=0.9mm/ t=0.42mm* → R_{th,S_a}*= =0.30K/W*). With easy manufacturing of the prototype in mind, the "Type (B)" heat sink was designed at the sub-optimum at (*n=16/ s=1.5mm / t=0.94mm*). The according fan operating point is shown in Fig.2 resulting in an air flow of *0.0062m³/s*.

Alternatively to "Type (B)" with the same thermal resistance as given in (18), a third heat sink is made of copper with a much higher thermal conductivity (λ_{Cu}*=380W/Km* as compared to λ_{Al}*=210W/Km*). This "Type (C)" heat sink can have much thinner fins due to the significantly increased thermal conductivity of the heat sink material which allows a higher number of fins and, therefore, a much higher total fin surface for convective heat transfer. Therefore, the heat sink will show a much smaller volume. For further optimization the "Type (C)" heat sink has two opposite base plates (**Fig.6**) allowing a better heat distribution over the fins because the heat flow path from the base plate into the fins is reduced by *50%*. The disadvantage of this configuration is that a three-phase converter system comes with three power modules that cannot be equally distributed over two base plates. Even if the all internal power semiconductor chips are approximately equally distributed over the two base plates, the electrical connections of some chips might create very high stray inductances. Therefore, "Type (C)" is a more theoretically concept in order to demonstrate the limits of cooling. The two base plates together show a surface reduced by about *30%* compared to the base plate surface of "Type (B)", but this is still sufficient to employ all internal semiconductor chips of the three power modules [5].

Again, selecting the fan San Ace 40/28 (K-speed, 12Vdc) [4] gives *c=40mm* and *b=40mm*. The "Type (C)" heat sink shows a local optimum at (*n=22/ s=1.09mm/ t=0.70mm* → R_{th,S_a}*=0.31K/W*), at (*n=24/ s=1.0mm/ t=0.64mm* → R_{th,S_a}*= =0.30K/W*), at (*n=30/ s=0.93mm/ t=0.39mm* → R_{th,S_a} *=0.26K/W*) and at (*n=40/ s=0.7mm/ t=0.29mm* → R_{th,S_a} *=0.24K/W*). With easy manufacturing of the prototype in mind, the "Type (C)" heat sink was designed at the sub-optimum at (*n=21/ s=1.0mm / t=0.86mm*). The according fan operating point is shown in Fig.2 resulting in an air flow of *0.0083m³/s*.

2.4 "Cooling System Performance Index" Describing the Power Density of Cooling Systems

The output power of a converter system is defined as

$$P_{OUT,SYS} = \frac{\eta_{SYS}}{1-\eta_{SYS}} P_{V,SYS} \tag{19}$$

with the system efficiency η_{SYS} and total system losses $P_{V,SYS}$. The power density d_{SYS}*[kW/liter]* of the converter system

$$d_{SYS} = \frac{P_{OUT,SYS}}{V_{SYS}} = \frac{\eta_{SYS}}{1-\eta_{SYS}} \frac{P_{V,SYS}}{V_{SYS}} = \frac{\eta_{SYS}}{1-\eta_{SYS}} \frac{\Delta T_{S-a}^{max}}{R_{th,S-a} V_{SYS}} \tag{20}$$

is derived by dividing converter system output power through the converter system volume V_{SYS}, and is proportional to the maximum acceptable temperature drop $\Delta T_{S\text{-}a}^{max}$ from heat sink surface to ambient. One has to additionally consider the voltage drop from power semiconductor junction to heat sink surface in order not to exceed the maximum tolerable junction temperature.

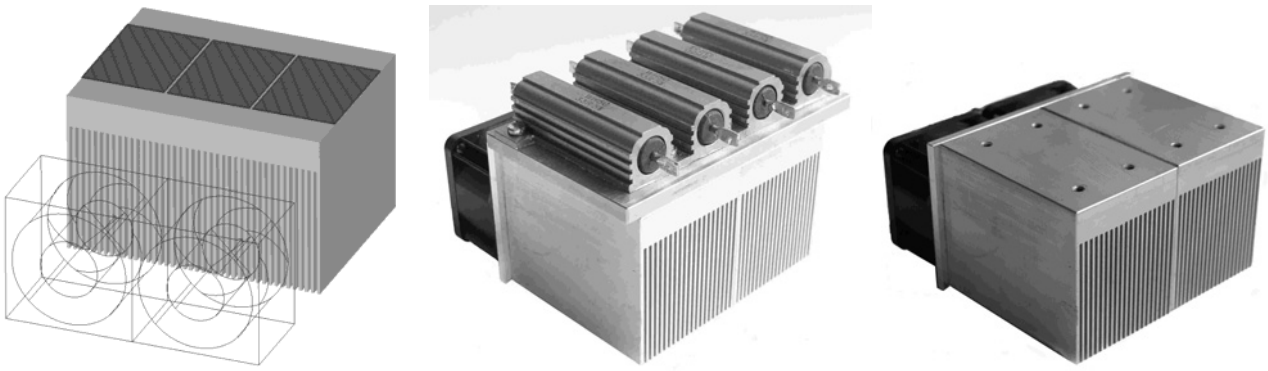


Fig.4: Heat sink "Type (A)" of aluminium (λ_{Al}=*210W/Km*) employing two fans San Ace 40/28mm [4] with dimensions *b=80mm*, *c=40mm*, *d=10mm*, *L=60mm*, *s=1.0mm*, *n=40*. The distance between fan and heat sink is *5mm* resulting in a total cooling system volume V_{CS}= *(28+5+60)×80×50mm*^{3}= *=0.372 liter*. The thermal resistance of the heat sink was measured as $R_{th,S\text{-}a}$ = *0.15K/W*. **(a)** 3D-CAD model of the numerical solver ICEPAK showing the three power modules on top of the heat sink (each module with area *25×34mm*^{2} emitting *150W* thermal power). **(b)** Experimental setup with heating resistors mounted onto heat spreader plates providing a total of *300W* thermal power. **(c)** Experimental setup without heating resistors. The eight holes in the base plate are for the screws fixing the heat spreader carrying the heating resistors.

Fig.5: Heat sink "Type (B)" of aluminium (λ_{Al}=*210W/Km*) employing one fan San Ace 40/28mm [4] with dimensions *b=40mm*, *c=40mm*, *d=10mm*, *L=80mm*, *s=1.5mm*, *n=16*. The distance between fan and heat sink is *5mm* resulting in a cooling system volume V_{CS} = *(28+5+80)×40×50mm*^{3} = *0.226 liter*. The thermal resistance of the heat sink was measured as $R_{th,S\text{-}a}$ = *0.25K/W*. **(a)** 3D-CAD model of the numerical solver ICEPAK showing the three power modules on top of the heat sink (each module with area *25×34mm*^{2} emitting *150W* thermal power). **(b)** Experimental setup with heating resistors mounted onto heat spreader plates providing a total of *300W* thermal power. **(c)** Experimental setup without heating resistors. The four holes in the base plate are for the screws fixing the heat spreader carrying the heating resistors.

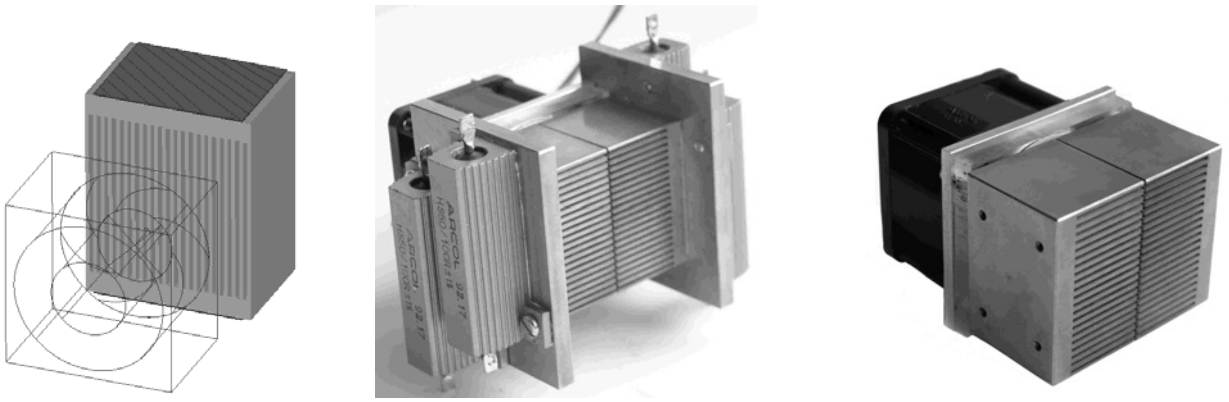


Fig.6: Heat sink "Type (C)" of copper (λ_{Cu} =*380W/Km*) employing one fan San Ace 40/28mm [4] with dimensions *b=40mm*, *c=40mm*, *L=27mm*, *s=1.0mm*, *n=21*. The heat sink has got two symmetrical base plates (each with *d=5mm*) where all power semiconductors of the converter system have to be placed. The distance between fan and heat sink is *5mm* resulting in a cooling system volume V_{CS}= *(28+5+27)×40×(40+2·5)mm*^{3}= *0.120 liter*. The thermal resistance of the heat sink was measured as $R_{th,S\text{-}a}$ = *0.27K/W*. **(a)** 3D-CAD model of the numerical solver ICEPAK showing one power module on top of the heat sink and one at the bottom (each module with area *27×40mm*^{2} emitting *225W* thermal power). **(b)** Experimental setup with four heating resistors mounted onto heat spreader plates providing a total of *300W* thermal power. The picture is rotated by *90°* compared to (a). **(c)** Experimental setup without heating resistors. The four holes in the visible base plate are for the screws fixing the heat spreader carrying the heating resistors.

Heat sink	channel number *n*	space between fins *s [mm]*	fin thickness *t [mm]*	spacing factor *k*	heat sink length *L [mm]*	Analytical $R_{th,S\text{-}a}$ *[K/W]*	Experiment $R_{th,S\text{-}a}$ *[K/W]*	ICEPAK $R_{th,S\text{-}a}$ *[K/W]*
"Type (A)" Al - 80×50, 2xSanAce	*40*	*1.0*	*0.93*	*0.53*	*60*	*0.17*	*0.15*	*0.12*
"Type (B) " Al - 40×50, 1xSanAce	*16*	*1.5*	*0.94*	*0.64*	*80*	*0.33*	*0.25*	*0.20*
"Type (C) " Cu - 40×50, 1xSanAce	*21*	*1.0*	*0.86*	*0.55*	*27*	*0.31*	*0.27*	*0.21*

Tab.1: Geometry and thermal resistance of the three different heat sink prototypes shown in Fig.4, Fig.5 and Fig.6.

Heat sink	spacing factor *k*	heat sink length *L [mm]*	Experiment $R_{th,S\text{-}a}$ *[K/W]*	Heat sink volume *[liter]*	Cooling system volume (heat sink plus fan) V_{CS} *[liter]*	Cooling system performance index $CSPI = (R_{th,S\text{-}a} \cdot V_{CS})^{-1}$
"Type (A)" Al - 80×50, 2xSanAce	*0.53*	*60*	***0.15***	*0.240*	*0.372*	***17.9***
"Type (B) " Al - 40×50, 1xSanAce	*0.64*	*80*	***0.25***	*0.160*	*0.226*	***17.7***
"Type (C) " Cu - 40×50, 1xSanAce	*0.55*	*27*	***0.27***	*0.054*	*0.120*	***31.2***

Tab.2: Geometry, measured thermal resistance, volume, and *CSPI* of the three different heat sink prototypes shown in Fig.4, Fig.5 and Fig.6.

For comparison of different heat sink designs concerning power density, we propose the "*cooling system performance index*" to be defined as

$$CSPI\left[\frac{W}{K\cdot liter}\right] = \frac{1}{R_{th,S-a}\left[\frac{K}{W}\right]\cdot V_{CS}[liter]}. \quad (22)$$

The cooling system power density d_{CS}*[W/liter]* can be expressed proportional to *CSPI* as

$$d_{CS}\left[\frac{W}{liter}\right] = \frac{P_{OUT,SYS}}{V_{CS}} = \frac{\eta_{SYS}}{1-\eta_{SYS}}\Delta T_{S-a}^{max}\cdot CSPI \quad > d_{SYS}. \quad (21)$$

The cooling system performance index *CSPI* of a cooling system (e.g., fan plus heat sink) tells what cooling system power density d_{CS} can be achieved. If, e.g., a cooling system shows three times the *CSPI* of a different one, the cooling system volume V_{CS} of the according converter can be made three times smaller. This is independent from system efficiency and temperature levels.

The cooling system power density d_{CS} defines an upper limit of the theoretically possible converter system power density d_{SYS} that can be reached theoretically only in case the combined volume of all other converter components (inductors, transformers, capacitors, power semiconductors, control electronic, EMI filter) can be neglected against the cooling system volume V_{CS}. Employing the *CSPI [W/(K·liter)]*, it is possible not only to quickly estimate the theoretical upper limit of the system power density (21), but also to directly compare different heat sinks as shown in **Tab.2** and **Tab.3**.

Table 3 shows values of the cooling system performance index *CSPI* for different cooling systems. The *CSPI* values of the heat sinks designed in section (2.3) are significantly larger than those of commercially available heat sinks ([6], [7], [8]) indicating a significant potential for further cooling system volume reduction. E.g., employing the copper heat sink "Type (C)" will reduce the whole cooling system volume (heat sink plus fan) of a converter by more than a factor *six* as compared to a hollow-fin cooling aggregate [6] that is typically employed in converter systems in

Heat sink	heat sink length *L [mm]*	$R_{th,S\text{-}a}$ *[K/W]*	Cooling system volume (heat sink plus fan) V_{CS} *[liter]*	Cooling system performance index $CSPI = (R_{th,S\text{-}a} \cdot V_{CS})^{-1}$
"Type (A)" Al - 80×50, 2xSanAce	*60*	*0.15*	*0.372*	***17.9***
"Type (B) " Al - 40×50, 1xSanAce	*80*	*0.25*	*0.226*	***17.7***
"Type (C) " Cu - 40×50, 1xSanAce	*27*	*0.267*	*0.120*	***31.2***
Fischer *LA V 9.*. Hollow-Fin Cooling Aggregate 80×80 (24Vdc) [6]	*100*	*0.20*	*1.043*	***4.8***
Fischer *LA V 9.*. Hollow-Fin Cooling Aggregate 80×80 (24Vac) [6]	*250*	*0.10*	*2.003*	***5.0***
CPU-Cooler "FCS-50" (Scythe), employing heat pipes [7]	-	*0.177*	*1.131*	***5.0***
CPU-Cooler "Freezer 64" (Artic Cooling), employing heat pipes [8]	-	*0.20*	*1.259*	***4.0***
Direct water cooling [1] - *excluding* pump, pipes, heat exch.	-	*0.10*	*0.037* *not the total volume!!*	*(270)*

Tab.3: Measured thermal resistance $R_{th,S\text{-}a}$, cooling system volume V_{CS} and cooling system performance index *CSPI* for different heat sinks.

the kW-range. If heat sink plus fan contribute, e.g., *40%* to the converter volume, employing "Type (C)" will reduce the total converter volume by about *33%*.

High-performance CPU-Coolers (e.g., [7], [8]) often employ heat pipes to improve the heat conduction inside the heat sink. They are designed will low noise operation in mind. Therefore, the cooling system power density is not much higher than for the hollow-fin cooling aggregate (characterized by approximately an equal *CSPI*). Employing water cooling (e.g., [1]) can significantly increase the potential cooling system power density, but if the necessary pump, heat exchanger and pipes are taken into account, the *CSPI* would be drastically reduced (from *CSPI= 270* to *CSPI ≈ 5.0* for [1]). Generally, the results in Tab.3 show that there is significant potential of performance improvement concerning power density for commercial applications.

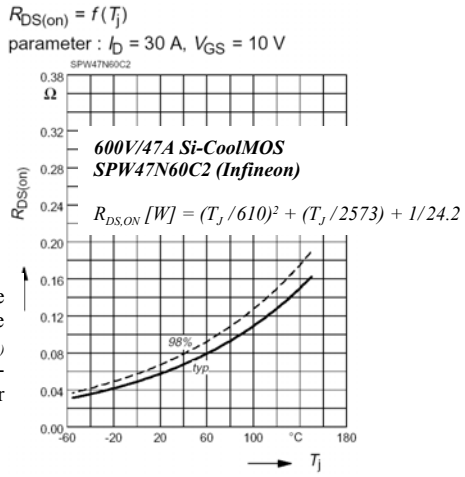


Fig.7: Temperature dependency of the on-resistance $R_{DS(on)}$ of a *600V/47A* Si-CoolMOS power transistor [9].

3 High-Temperature Semiconductor Characteristics

A *10kW/500kHz* Vienna Rectifier will be investigated operating at different heat sink and junction temperatures. In this section, semiconductor data is collected from literature and datasheets, which will be employed to calculate total losses and junction temperatures of a *10kW* Vienna Rectifier in section 4. Section 3.1 deals with Si-CoolMOS transistors and SiC-diodes operating at junction temperatures below *150°C*, while section 3.2 is dedicated to latest SiC-technology (diode and JFET) capable of operation up to *300°C* junction temperature.

3.1 Si/SiC-Power Semiconductors Operating Below 150°C

The data in **Table 4** summarizes all important parameters needed for calculating conduction- and switching losses for a CoolMOS power transistor [9], a free-wheeling SiC-diode [10] composed of three diode devices in parallel, and a fast-switching Si-diode [11]. The semiconductors presented in Tab.4 fit inside a power module [2], [5] that realizes one bridge-leg of the Vienna Rectifier. For the *10kW* Vienna Rectifier, currents in the range of about *20A* will be experienced and the power semiconductors have been selected accordingly.

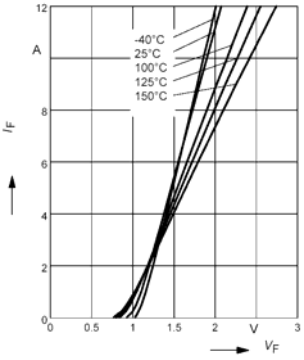
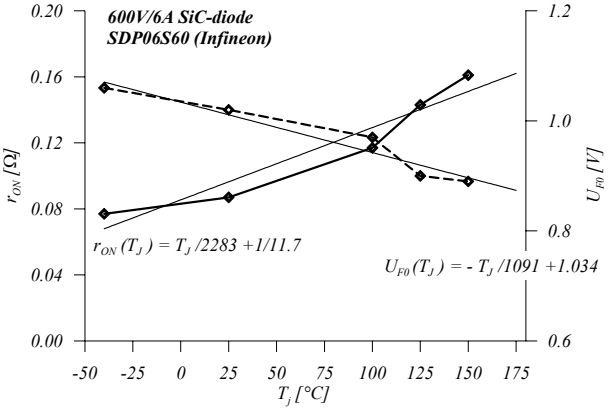


Fig.8: Temperature dependency of on-resistance r_{ON} (solid line) and voltage drop U_{F0} (dashed line) of a *600V/6A* SiC-diode SDP06S60 from Infineon derived from its datasheet [10]. Both curves can be approximated by linear functions with good accuracy as shown in the figure.



The temperature dependency of the on-resistance of the CoolMOS transistor is shown in **Fig.7**. A 2nd order approximation is given which is needed in the loss- and junction temperature calculations of section 4. The switching losses of the CoolMOS are given in Tab.4 in form of a factor *k [µWs/A]*, that has been experimentally derived [12], [13] at a junction temperature *125°C*. The switching losses are very small in case of employing a SiC-diode with negligible reverse recovery current. Furthermore, the switching losses can be assumed to be approximately temperature independent due to the characteristics of the SiC-diode involved in the switching process. Temperature dependent resistance and voltage drop of the diodes are given in **Fig.8** and **Fig.9**. All curves are approximated by functions that are useful for the calculations in section 4.

Si/SiC power semiconductors ***150°C***	Rating	Thermal resistance	Conduction losses	Switching losses
Si-CoolMOS SPW47N60C2 [9]	*600V / 47A*	$R_{th,JC}$ = *0.3 K/W*	See Fig.7	$k_{125°C@400V} \approx 11\mu Ws/A$ [12], [13] (in first approximation temperature independent due to combination with SiC-diode)
SiC-diode SDP06S60 [10] → D_F	*600V / 6A* (3 such diodes in parallel)	$R_{th,JC}$ = *2.6 K/W* 3 parallel devices: $R_{th,JC}$ = *0.87 K/W*	See Fig.8	-
Si-diode HFA15TB60 [11] → D_N, D_M	*600V / 15A*	$R_{th,JC}$ = *1.7 K/W*	See Fig.9	-

Tab.4: Si and SiC power semiconductors employed for a *10kW/500kHz* Vienna Rectifier for operation at junction temperatures below *150°C*.

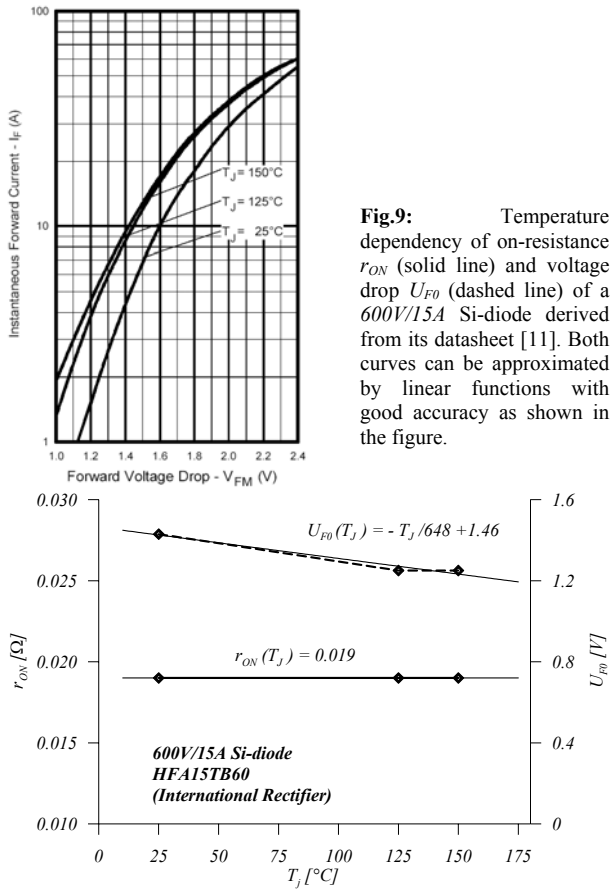


Fig.9: Temperature dependency of on-resistance r_{ON} (solid line) and voltage drop U_{F0} (dashed line) of a *600V/15A* Si-diode derived from its datasheet [11]. Both curves can be approximated by linear functions with good accuracy as shown in the figure.

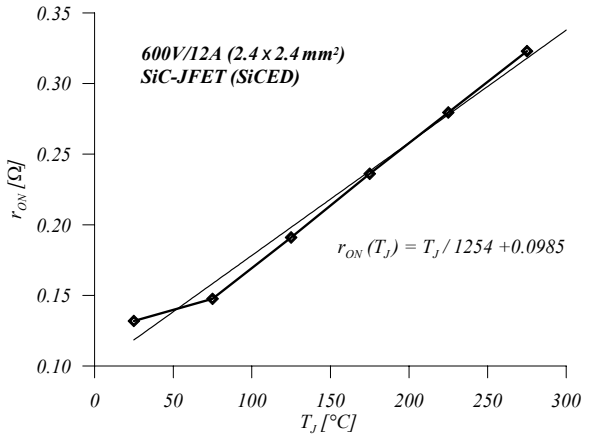


Fig.10: Temperature dependency of the on-resistance $R_{DS(on)}$ of the *600V/12A* SiC-JFET transistor (chip size $2.4 \times 2.4 mm^2$) from SiCED [15].

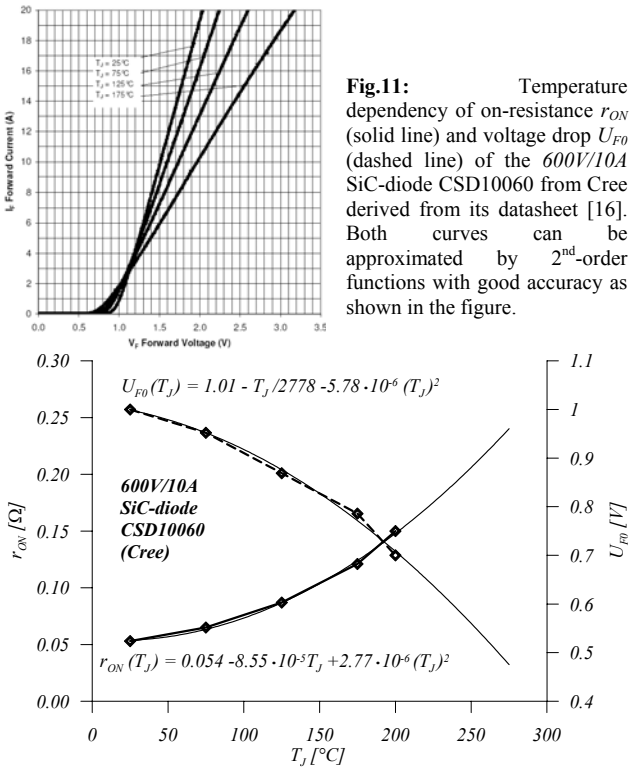


Fig.11: Temperature dependency of on-resistance r_{ON} (solid line) and voltage drop U_{F0} (dashed line) of the *600V/10A* SiC-diode CSD10060 from Cree derived from its datasheet [16]. Both curves can be approximated by 2nd-order functions with good accuracy as shown in the figure.

3.2 SiC-Power Semiconductors Operating Up to 300°C

For temperatures higher than *150°C* Si-devises cannot be employed. Therefore, the Si-semiconductors of section 3.1 have to be replaced by SiC-devices with parameters given in **Tab.5**. The devices are selected to be able to handle voltage stress (*600V*) and current stress (*20A*) of the converter system specified in detail in section 4, and to theoretically fit into a space provided by the power module introduced in the previous section ($26 \times 35 mm^2$, [2], [5]).

The switching losses characterized by *k [µWs/A]* in Tab.5 are in good approximation temperature-independent and small. For minimizing switching losses of SiC-JFETs it is essential to optimize the driver circuit as performed in [14]. Since the measured value of *k* (see [14]) is very close to the one given in Tab.4, we set *k* in Tab.5 equal to the value of the CoolMOS in Tab.4 to simplify comparison. The temperature-dependent on-resistance of a *600V/12A* SiC-JFET from SiCED [15] is given in **Fig.10**. One should keep in mind that the SiC-JFET power transistor is a result of latest research, and that performance improvements might be achieved in the near future which might change the parameters given in this section.

The SiC-diode given in Tab.5 is the same one [10] as given in Tab.4 with temperature-dependent parameters shown in Fig.8. Alternatively to three *600V/6A* SiC-diodes [10] from Infineon in parallel, two parallel *600V/10A* SiC-diodes CSD10060 from Cree [16] could be employed. The thermal resistance of these two paralleled devices would be $R_{th,JC} = 0.54 K/W$, and the temperature-dependent parameters necessary for loss-calculations are given in **Fig.11**. In section 4, we will employ the SiC-diodes from Infineon [10] for all calculations.

SiC power semiconductors ***300°C***	Rating	Thermal resistance	Conduction losses	Switching losses
SiC-JFET from SiCED [15]	*600V / 12A* (2 such transistors in parallel)	$R_{th,JC} = 2.2 K/W$ 2 parallel devices: $R_{th,JC} = 1.1 K/W$	See Fig.10	$k_{125°C@400V} \approx 11 \mu Ws/A$ [14] (in very good approximation temperature independent)
SiC-diode SDP06S60 [10] → D_F, D_N, D_M	*600V / 6A* (3 such diodes in parallel)	$R_{th,JC} = 2.6 K/W$ 3 parallel devices: $R_{th,JC} = 0.87 K/W$	See Fig.8	-

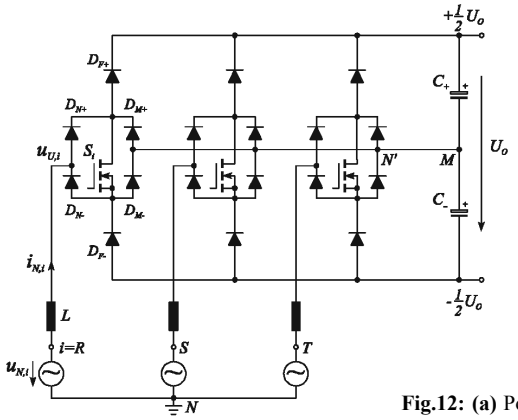
Tab.5: SiC power semiconductors employed for a *10kW/500kHz* Vienna Rectifier for operation at junction temperatures up to *300°C*.

4 THEORETICAL POWER DENSITY LIMIT FOR CONVERTER SYSTEMS

Generally, with higher heat sink temperatures (especially higher fin surface temperatures), proportionally more heat can be removed via forced convection. This means that the fin surface can be reduced resulting in a smaller heat sink volume and, therefore, higher power density. On the other hand, also losses increase with higher junction temperatures resulting in reduced system efficiency. Reduced system efficiency means higher losses for the same output power level resulting in the need for a lager cooling system, which will partly offset the beneficial effect of the higher heat sink temperature. In the following, for the example of a *10kW* three-phase Vienna Rectifier, we will discuss the impact of increased junction temperatures on the efficiency and power density which typically results in improved convection cooling but also higher semiconductor losses.

4.1 Thermal Modeling of a Converter System

The topology of the Vienna Rectifier is shown in **Fig.12**(a), the parameters are specified in the caption. A power module ([2], [5]) for realization of one of the three bridge legs is shown in Fig.12(b), where the internal power semiconductors listed in Tab.4 are shown.



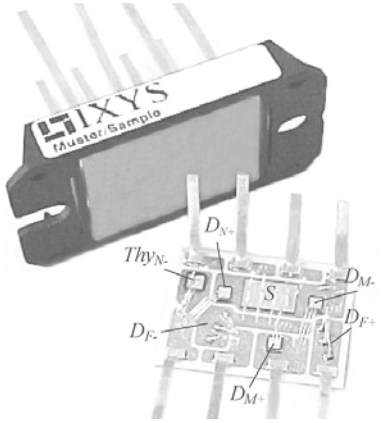


Fig.12: (a) Power circuit of the Vienna Rectifier with input voltage amplitude *327V*, DC output voltage *800V*, output power *10kW* and switching frequency *500kHz*. **(b)** Power module realizing one bridge-leg of the three-phase Vienna Rectifier employing SiC-freewheeling diodes (D_F), a CoolMOS power transistor (S), and Si-diodes (D_N, D_M).

The modulation index of the rectifier is defined as

$$M = \frac{\hat{U}_N}{\frac{1}{2}U_0} = \frac{327}{800/2} = 0.82 \cdot \tag{22}$$

The current stress of each power semiconductor of the Vienna Rectifier can be expressed in analytical form as summarized in **Tab. 6**. Switching and conduction losses can be calculated via equations (23) – (27) employing the semiconductor parameters given in section 3. The temperature-dependency of the semiconductor parameters is considered by setting the individual junction temperature of the according chip. If *n* semiconductors are connected in parallel to conduct the current, eg., three *600V/6A* SiC-diodes [10] in parallel to form one diode D_F (Fig.12(b) and/or Tab.4), the losses associated with the rms-current of the device are always reduced by a factor *1/n* (see (23) – (26)). The losses of one power module realizing one bridge leg of the Vienna Rectifier are calculated in (27). All losses are dependent on modulation index, input phase current amplitude and each chip's individual junction temperature.

$$\begin{aligned} P_{V,DN} &= U_{F,DN} \cdot I_{DN,avg} + \tfrac{1}{n} \cdot r_{DN} \cdot I_{DN,rms}^2 = \\ &= U_{F,DN}(T_{J,DN}) \cdot I_{DN,avg}(M, \hat{I}_N) \\ &\quad + \tfrac{1}{n} \cdot r_{DN}(T_{J,DN}) \cdot I_{DN,rms}^2(M, \hat{I}_N) \end{aligned} \tag{23}$$

$$\begin{aligned} P_{V,DM} &= U_{F,DM} \cdot I_{DM,avg} + \tfrac{1}{n} \cdot r_{DM} \cdot I_{DM,rms}^2 = \\ &= U_{F,DM}(T_{J,DM}) \cdot I_{DM,avg}(M, \hat{I}_N) \\ &\quad + \tfrac{1}{n} \cdot r_{DM}(T_{J,DN}) \cdot I_{DM,rms}^2(M, \hat{I}_N) \end{aligned} \tag{24}$$

$$\begin{aligned} P_{V,DF} &= U_{F,DF} \cdot I_{DF,avg} + \tfrac{1}{n} \cdot r_{DF} \cdot I_{DF,rms}^2 = \\ &= U_{F,DF}(T_{J,DF}) \cdot I_{DF,avg}(M, \hat{I}_N) \\ &\quad + \tfrac{1}{n} \cdot r_{DF}(T_{J,DF}) \cdot I_{DF,rms}^2(M, \hat{I}_N) \end{aligned} \tag{25}$$

$$\begin{aligned} P_{V,T} &= \tfrac{2}{\pi} k \cdot f_P \cdot \hat{I}_N + \tfrac{1}{n} \cdot r_{DS,ON} \cdot I_{T,rms}^2 \\ &= \tfrac{2}{\pi} k(T_{J,T}) \cdot f_P \cdot \hat{I}_N \\ &\quad + \tfrac{1}{n} \cdot r_{DS,ON}(T_{J,T}) \cdot I_{T,rms}^2(M, \hat{I}_N) \end{aligned} \tag{26}$$

$$\begin{aligned} P_{V,module} &= P_{V,T} + 2 \cdot (P_{V,DN} + P_{V,DM} + P_{V,DF}) = \\ &= P_{V,module}(T_{J,DN}, T_{J,DM}, T_{J,DF}, T_{J,T}; M, \hat{I}_N) \end{aligned} \tag{27}$$

A simple stationary thermal model of the converter system is set up under the assumption that the case of the power module shows a homogenous temperature distribution over the surface with no hot spots occurring. In reality there will be hot spots especially below chips with high losses because the chips inside the module are soldered onto a DBC plate with small heat spreading capability due to the thin copper layer (*0.3mm*). Such hot spots generally increase the junction temperature of chips located above, but will be neglected in the following to simplify the thermal model of the converter.

Each chip inside the power module shows an individual thermal junction-case (J-C) resistance (Tab.4, Tab.5, discussion in [2]). According to the chip's individual losses, individual junction temperatures occur. A stationary model is shown in **Fig.13** for one power module. The power losses of the individual chips are modeled as current sources, and the individual junction temperatures of the chips $T_{J,T}$, $T_{J,DF}$, $T_{J,DN}$ and $T_{J,DM}$ are represented by the voltages at the current source output.

$I_{DN,avg} = \hat{I}_N \cdot \frac{1}{\pi}$ $I_{DN,rms} = \hat{I}_N \cdot \frac{1}{2}$	$I_{DM,avg} = \hat{I}_N (\frac{1}{\pi} - \frac{1}{4} M)$ $I_{DM,rms} = \hat{I}_N \sqrt{\frac{1}{4} - \frac{2}{3\pi} M}$	$I_{DF,avg} = \hat{I}_N \cdot \frac{1}{4} M$ $I_{DF,rms} = \hat{I}_N \sqrt{\frac{2}{3\pi} M}$	$I_{T,avg} = \hat{I}_N (\frac{2}{\pi} - \frac{1}{2} M)$ $I_{T,rms} = \hat{I}_N \sqrt{\frac{1}{2} - \frac{4}{3\pi} M}$

Tab.6: Analytical equations of the current stress on the power semiconductors of the Vienna Rectifier dependent on modulation index defined in (22) and input phase current amplitude.

The model assumes a homogenous temperature T_C over the power module base plate (case). The thermal resistance of the heat sink as seen from one single power module $R_{th,C\text{-}a}^{module}$ includes the thermal resistance of the interface material (e.g., thermal grease) as defined in (28) for one power module with a base plate area $26\times35mm^2$. The thermal resistance of the heat sink as seen from one out of three power modules is three times larger than the total heat sink thermal resistance (29) for compact and optimized heat sinks as employed in this study.

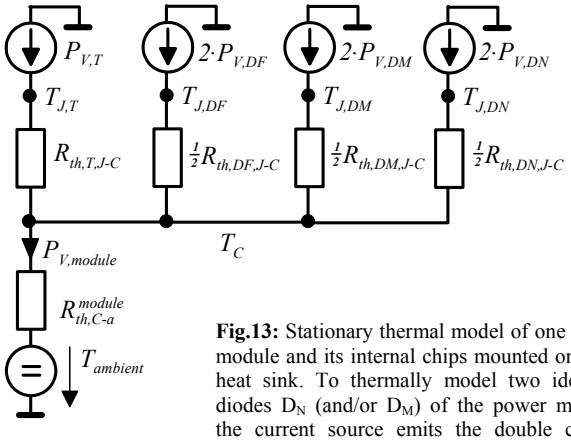


Fig.13: Stationary thermal model of one power module and its internal chips mounted onto the heat sink. To thermally model two identical diodes D_N (and/or D_M) of the power module, the current source emits the double current (power loss of two diodes) but assumes half of the thermal resistance to calculate correctly both the chip junction temperature and the total output power of the module.

$$R_{th,grease}=\frac{d_{grease}}{\lambda_{grease}\cdot A_{module}}=\frac{50\mu m}{1.0\,{}^{W}\!/_{mK}\cdot(26mm\cdot35mm)}=0.055\,{}^{K}\!/_{W} \tag{28}$$

$$R_{th,C-a}^{module}=3\cdot R_{th,C-a}^{(HS)}+R_{th,grease} \tag{29}$$

Based on the thermal model in Fig.13, the individual junction temperatures are expressed in terms of ambient temperature, temperature rise of the heat sink surface (including thermal grease) due to the total loss of the power module $P_{V,module}$, and individual temperature rise junction-case due to the losses of the individual chips. For ideally four different chips (T, D_N, D_M, D_F) there result four non-linear equations (30) – (33). With (23) – (27), the junction temperatures of the four different chips $T_{J,T}$, $T_{J,DF}$, $T_{J,DN}$ and $T_{J,DM}$ can be calculated numerically dependent on modulations index (assumed to be $M = 0.82 = constant$ (22) in the following) and amplitude of the input phase current.

$$T_{J,DN}=T_{ambient}+P_{V,module}(T_{J,DN},T_{J,DM},T_{J,DF},T_{J,T};M,\hat{I}_N)\cdot R_{th,C-a}^{module}+P_{V,DN}(T_{J,DN};M,\hat{I}_N)\cdot R_{th,DN,J-C} \tag{30}$$

$$T_{J,DM}=T_{ambient}+P_{V,module}(T_{J,DN},T_{J,DM},T_{J,DF},T_{J,T};M,\hat{I}_N)\cdot R_{th,C-a}^{module}+P_{V,DM}(T_{J,DM};M,\hat{I}_N)\cdot R_{th,DM,J-C} \tag{31}$$

$$T_{J,DF}=T_{ambient}+P_{V,module}(T_{J,DN},T_{J,DM},T_{J,DF},T_{J,T};M,\hat{I}_N)\cdot R_{th,C-a}^{module}+P_{V,DF}(T_{J,DF};M,\hat{I}_N)\cdot R_{th,DF,J-C} \tag{32}$$

$$T_{J,T}=T_{ambient}+P_{V,module}(T_{J,DN},T_{J,DM},T_{J,DF},T_{J,T};M,\hat{I}_N)\cdot R_{th,C-a}^{module}+P_{V,T}(T_{J,T};M,\hat{I}_N)\cdot R_{th,T,J-C} \tag{33}$$

$$P_{IN,VR1}=\tfrac{3}{2}\cdot\hat{U}_N\cdot\hat{I}_N \tag{34}$$

$$P_{OUT,VR1}=P_{IN,VR1}-3\cdot P_{V,module}=\eta_{VR1}\cdot P_{IN,VR1} \tag{35}$$

For a selected input phase current amplitude, conduction and switching losses and the individual junction temperatures of all power semiconductors inside the power module can be calculated from (23) – (33). Furthermore, for the selected current amplitude, the system input power, output power, and efficiency can be calculated directly from (34) and (35). From a (very time-consuming) numerical thermal 3D CFD-simulation it becomes obvious that the transistor is by far the hottest chip inside the power module (**Fig.14**). Therefore, the characteristic maximum junction temperature critical for the design of the converter system is defined as the transistor junction temperature $T_{J,T}$.

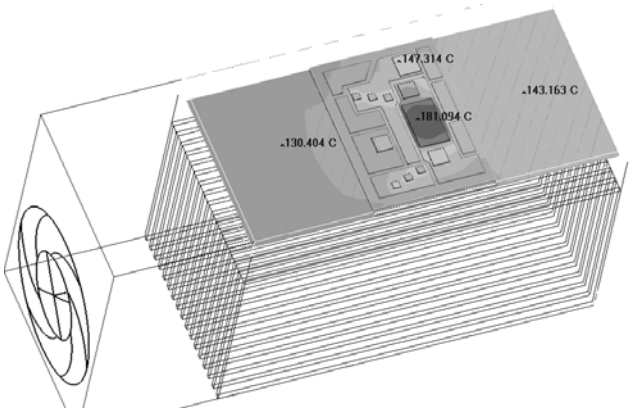


Fig.14: Details of the stationary temperature distribution inside one power module specified in Fig.12(b) employing the cooling system "Type (B)" (Fig.5) derived from a 3D-FEM CFD simulation (ICEPAK). The power switch realized by a CoolMOS is by far the hottest chip (*180°C*). Therefore, the critical junction temperature of the converter design is always that of the transistor.

4.2 Discussion of the Resulting Operating Temperatures, Power Densities and System Efficiency

As described in the previous section, for different phase current amplitudes, the chip temperatures including $T_{J,T}$, furthermore, system input power, output power and efficiency, can be calculated numerically employing (23) – (35). Therefore, for different junction temperatures $T_{J,T}$ all losses, temperatures and power levels of the converter system are available and can be presented graphically for a detailed discussion.

The system efficiency η_{VR1} as defined in (35) is shown in **Fig.15** dependent on the transistor junction temperature $T_{J,T}$ for the Si/SiC-combination *SiC-diode & Si-CoolMOS* (solid lines in Fig.15, Tab.4) and for the all-SiC-combination *SiC-diode & SiC-JFET* (dashed lines in Fig.15, Tab.5) employing the heat sinks of section 2.3. The heat sinks are characterized by their thermal resistance which makes "Type (B)" and "Type (C)" thermally equivalent but different in terms of cooling system power density. If, for example, the *SiC-diode & Si-CoolMOS* combination is employed with heat sink "Type (A)", the CoolMOS junction temperature has to be *135°C* to allow *10kW* output power at a system efficiency of η_{VR1} = *96.3%*. Employing heat sink "Type (A)" together with the *SiC-diode & SiC-JFET* combination, a SiC-JFET junction temperature of about *200°C* is needed to allow *10kW* output power at the same efficiency. However, such a direct comparison of the efficiency of the two different semiconductor combinations does not make much sense because

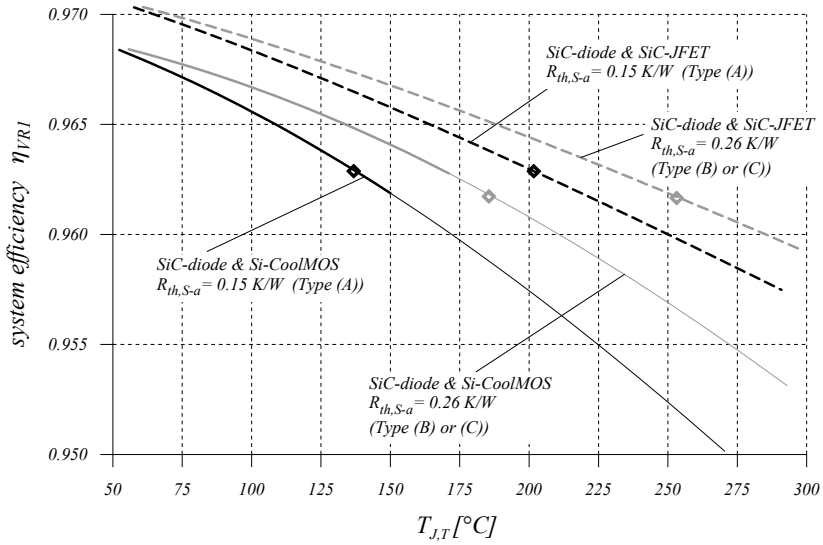


Fig.15: Converter system efficiency dependent on the transistor junction temperature for two different kind of heat sinks characterized by their thermal resistance $R_{th,S-a}$ (Tab.2) and two different kind of semiconductors (Tab.4 vs. Tab.5). With higher temperatures the system efficiency generally decreases. The four square symbols on the curves indicate operating points where P_{OUT} = *10kW* can be achieved.

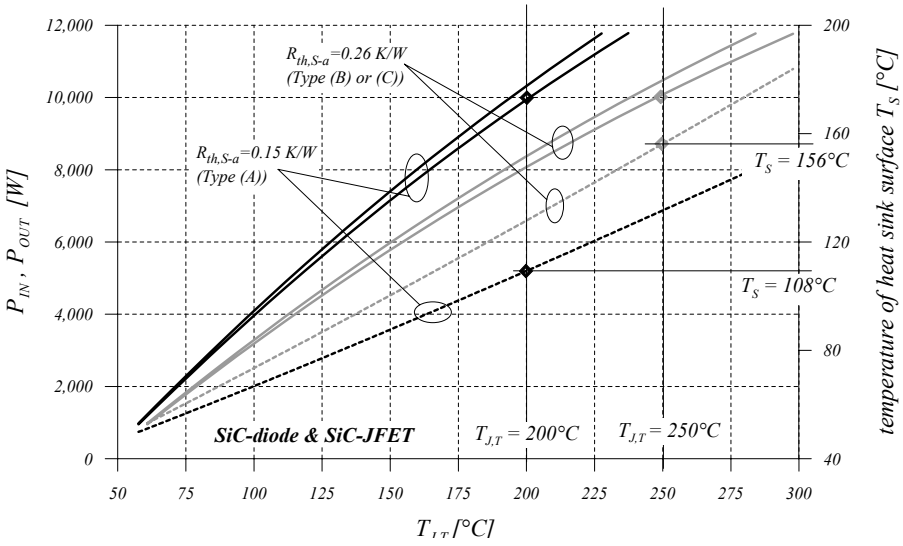


Fig.16: Input power and output power (solid lines) for the all-SiC combination (Tab.5) for two different heat sinks (Tab.2) dependent on the transistor junction temperature. The scale on the right-hand side shows the heat sink surface temperature dependent on the transistor junction temperature (dotted lines). The four square symbols on the curves indicate operating points where P_{OUT} = *10kW* can be achieved. To achieve rising output power, the junction temperature must be increased accordingly in case of a given heat sink. The heat sink surface temperature also rises as shown.

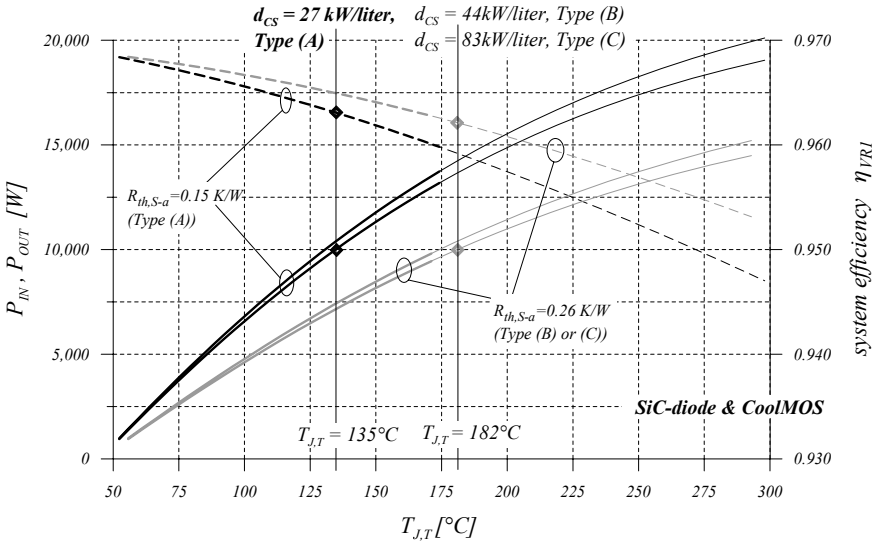


Fig.17: Input power and output power (solid lines) for the Si/SiC combination (Tab.4) for two different heat sinks (Tab.2) dependent on the transistor junction temperature. The scale on the right hand side shows the system efficiency (dashed lines) dependent on the transistor junction temperature. The four square symbols on the curves indicate operating points where P_{OUT} = *10kW* can be achieved. The operating temperature of the Si/SiC combination is limited with *150°C* (indicated by thin lines at higher temperatures). To increase the output power in case of a given heat sink, one has to increase the temperature, while the systems efficiency decreases.

the size of the CoolMOS chip is *65mm*^{2}, while the two parallel JFETs show together a total size of just *11.5mm*^{2}. Fig.15 shows that employing heat sink "Type (B)" or "Type (C)" for achieving *10kW* output power only works at a CoolMOS junction temperature of *185°C*, which exceeds the temperature limit of the CoolMOS. For such heat sinks only the all-SiC combination can deliver *10kW* output power with a SiC-JFET junction temperature of $T_{J,T}$ = *253°C*. The system efficiency is only slightly reduced in this case.

Input and output power of the converter dependent on the transistor junction temperature is shown in **Fig.16** (solid lines, left-hand side y-axis). The dotted lines show the temperature of the heat sink surface. The diagram shows only data of the all-SiC

combination (Tab.5) employing the heat sinks of section 2.3. To achieve a converter output power of *10kW* with heat sink "Type (A)", the SiC-JFET junction temperature has to be *200°C*. At this operating point, the heat sink surface temperature is T_S = *108°C*. For heat sinks "Type (B)" and "Type (C)" the heat sink surface approaches *156°C* in case of delivering *10kW* output power.

Figure 17 shows system input power, output power and efficiency for the Si/SiC combination (Tab.4) dependent on the CoolMOS junction temperature for the three heat sinks introduced in section 2.3. For heat sink "Type (B)" and "Type (C)" (grey colored lines), the CoolMOS junction temperature has to be *182°C* in order to allow *10kW* output power. This would mean cooling system power densities for forced air-cooling of *44kW/liter* employing "Type (B)" and *83kW/liter* employing "Type (C)". An operating temperature of *182°C* is exceeding the limits of the CooolMOS. Employing heat sink "Type (A)" gives a cooling system power density of ***27kW/liter*** with CoolMOS junction temperature *135°C* within the acceptable limits.

resulting optimized heat sinks have been built. The predicted performance of the optimized heat sink prototypes has been verified experimentally.

Input power, output power, efficiency and junction temperatures of a *10kW/500kHz* three-phase boost-type converter (Vienna Rectifier) are calculated for different heat sink temperatures on different optimized heat sinks. It is shown that employing a *600V/47A* Si-CoolMOS transistor and *600V/6A* SiC-diodes, a maximum power density of the cooling system of *27kW/liter* can be achieved at a transistor junction temperature of *135°C*. If the CoolMOS is replaced by *600V/12A* SiC-JFETs, the junction temperatures can be increased up to *250°C*. The accordingly higher heat sink temperature of *156°C* significantly improves the convective heat transfer and allows cooling system power densities of *83kW/liter*. If the junction temperatures are increased from *25°C* to *300°C*, the system efficiency only falls from *97%* to *95%*.

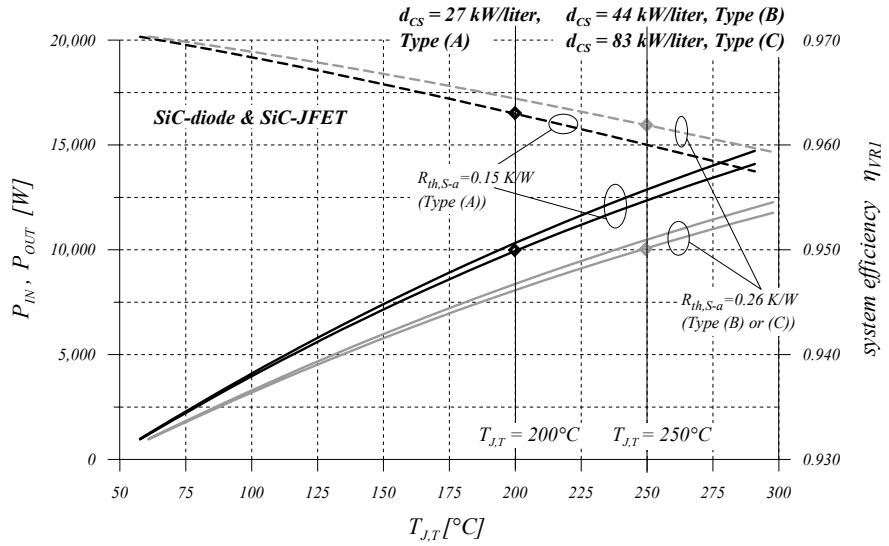


Fig.18: Input power and output power (solid lines) for the all-SiC combination (Tab.5) for two different heat sinks (Tab.2) dependent on the transistor junction temperature. The scale on the right hand side shows the system efficiency (dashed lines) dependent on the transistor junction temperature. The four square symbols on the curves indicate operating points where P_{OUT} = *10kW* can be achieved. The all-SiC combination can be operated over the full temperature range up to *300°C*.

If, instead, an all-SiC combination (Tab.5) is employed (**Fig.18**), the SiC-JFET junction temperature reaches *200°C* for heat sink "Type (A)" and *250°C* for heat sinks "Type (B)" and "Type (C)". This means that employing an all SiC-combination makes possible cooling system power densities up to ***83kW/liter*** for forced air-cooling.

Generally, the output power can be increased for a given heat sink by increasing the heat sink temperature and, therefore, the power semiconductor junction temperatures. This is generally limited by the thermal runaway of the system that occurs when the slope of the output power curves approaches zero (see output power curves in Fig.17 becoming increasingly flat at higher temperatures). At this point of temperature, it is not possible to increase the output power of the system any more because more power is lost due to the falling system efficiency than delivered from the input side.

5 CONCLUSION

To find the theoretical limit of the cooling system power density of a converter system employing forced air-cooling, first the heat sink has to be carefully optimized in terms of power density. A *cooling system performance index* has been defined that makes direct comparisons of different cooling systems (heat sink plus fan) concerning the possible power density. A mathematical procedure for heat sink optimization has been given, and the

REFERENCES

[1] **Drofenik, U., Laimer, G., and Kolar, J.W.:** *Pump Characteristic Based Optimization of a Direct Water Cooling System for a 10kW/500kHz Vienna Rectifier.* Proc. of the 35th IEEE Power Electronics Specialists Conference (PESC), Aachen, Germany, June 20 - 25, CD-ROM, ISBN: 07803-8400-8 (2004).

[2] **Drofenik, U., and Kolar, J.W.:** *Thermal Analysis of a Multi-Chip Si/SiC-Power Module for Realization of a Bridge Leg of a 10kW Vienna Rectifier.* Proceedings of the 25th IEEE International Telecommunications Energy Conference (INTELEC), Yokohama, Japan, Oct. 19 - 23, pp. 826 - 833 (2003).

[3] **Baehr, H.D. and Stephan, K.:** *Wärme- und Stoffübertragung (in German).* ISBN 3-540-64458-X, 3rd edition, Springer (1998).

[4] *Sanyo Denki*, Standard Fan SAN ACE 40 for 1U server, datasheet published at http://sanyodb.colle.co.jp/product_db_e/coolingfan/

[5] *IXYS Corporation*, Package of power module VUI 30-12 N1, datasheet published at http://www.ixys.com

[6] *Fischer Elektronik GmbH*, "Hollow-Fin Cooling Aggregates with Air-flow Chamber LA V 9..," datasheet published at http://www.fischerelektronik.de

[7] *Scythe*, CPU-Cooler "FCS-50", datasheet published at http://www.scythe.co.jp/de/

[8] *Artic Cooling*, CPU-Cooler "Freezer 64", datasheet publ. at www.arctic-cooling.com

[9] *Infineon*, CoolMOS Power Transistor (600V, TO-247, RDSon=0.07Ohm, 47.0A, Model Nr. SPW47N60C2), datasheet published at http://www.infineon.com

[10] *Infineon*, Silicon Carbide Schottky Diode (600V/6A SiC-diode in TO220-3 package, Model Nr. SDP06S60) , datasheet published at http://www.infineon.com

[11] *International Rectifier*, Ultrafast Soft Recovery Diode (600V, 15A, Model Nr. HFA15TB60), datasheet published at http://www.irf.com

[12] **Laimer, G., and Kolar, J.W.:** *Accurate Measurement of the Switching Losses of Ultra High Switching Speed CoolMOS Power Transistor / SiC Diode Combination Employed in Unity Power Factor PWM Rectifier Systems.* Proceedings of the 8th European Power Quality Conference (PCIM), Nuremberg, Germany, May 14 - 16, pp. 71 - 78 (2002).

[13] **Miniböck, J., and Kolar, J.W.:** *Experimental Analysis of the Application of Latest SiC Diode and CoolMOS Power Transistor Technology in a 10kW Three-Phase PWM (VIENNA) Rectifier.* Proc. of the 43rd International Power Electronics Conference (PCIM), Nuremberg, Germany, June 19 - 21, pp. 121 - 125 (2001).

[14] **Heldwein, M.L., and Kolar, J.W.:** *A Novel SiC J-FET Gate Drive Circuit for Sparse Matrix Converter Applications.* Proceedings of the 19th Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim (California), USA, February 22 - 26, Vol. 1, pp. 116 - 121 (2004).

[15] *SiCED*, http://www.siced.de/, 600V/12A SiC-JFET transistor.

[16] *Cree*, 600V/10A SiC-diode CSD10060, datasheet published at http://www.cree.com/ftp/pub/CSD10060.pdf