A General Scheme for Calculating Switching- and Conduction-Losses of Power Semiconductors in Numerical Circuit Simulations of Power Electronic Systems

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Abstract. Numerical simulation of junction temperature time behavior in a circuit simulation is performed by setting up thermal models of power semiconductors and cooling systems, and connecting these models, typically composed of thermal RC-networks, to the calculated power losses. Calculating or estimating accurately conduction losses and, especially, switching losses has been discussed in the literature but seems to be not well known among many engineers. Therefore, in this paper we will give an overview of this topic and propose improvements of the procedure of loss-estimation in power electronic circuit simulations. The proposed scheme calculates conduction losses and switching losses with minimum effort, high accuracy and does not slow down the numerical simulation. It can be embedded directly in any circuit simulator employing ideal switches. Loss calculations are based on datasheet values and/or experimental measurements. As an example, a 5kW-inverter connected to a drive is set up with each bridge leg realized by a power module, where the characteristic parameters for the loss calculation scheme are extracted from datasheet diagrams.

Keywords: switching losses, conduction losses, numerical circuit simulation

1 Introduction

System design guidelines in general and, increasingly, reliability issues put emphasis on the thermal analysis of power electronic systems. Numerical simulation of the junction temperature time behavior in a circuit simulation is possible by setting up a thermal model of power semiconductors and cooling systems, and connecting these thermal equivalent circuits, typically composed of RC-networks and/or analytical equations, to the calculated power losses of the semiconductors. Calculating or estimating accurately conduction losses and, especially, switching losses has been discussed in the literature but seems to be not well known among many engineers doing research and development in power electronics. Therefore, in this paper we will give an overview of this topic and propose some improvements in the procedure of loss-estimation in simulations.

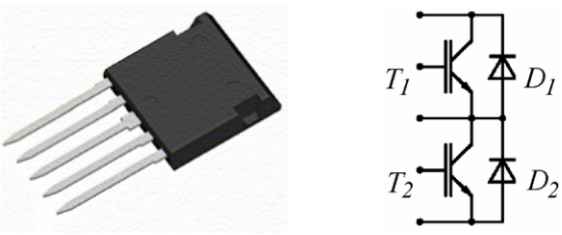

Fig.1: Power module IXYS FII50-12E under investigation.

In the following the time behavior of the total losses of the semiconductors of the power module IXYS FII50-12E [1] (**Fig.1**) will be discussed and calculated. The proposed simulation scheme calculates total losses with minimum effort, high accuracy and does not slow down the numerical simulation in a significant way. It can be embedded directly in any circuit simulator. Loss calculations are based on datasheet values [1] and/or experimental measurements.

2 Conduction Losses

Conduction losses of power semiconductors are often calculated by inserting a voltage U_F representing the voltage drop and a resistor r_{ON} representing the current-dependency in series with the ideal device. In this way, the non-linear characteristic of the current-voltage dependency is modeled in a simple way. One disadvantage of this approach is that ideal switches and diodes of the system are overloaded with additional parameters. Adding the ability to measure conduction losses this way means partly rebuilding a system in the circuit simulator. Often, the simulator provides the ability to set a switch model from "ideal" (no voltage drop, no resistance) to a U_F / r_{ON} -model or higher-order approximations of the current-voltage characteristics of the switch. Also, building temperature dependency of the characteristic into this model is only possible if the circuit simulator provides resistors with controllable resistance values.

The characteristic describing the relationship between voltage drop and U_{CE} and collector current I_C of the IGBTs as given in the datasheet is shown in **Fig.2**(a). This non-linear dependency is often modeled in a rough approximation as voltage source and resistor in series with an ideal switch. We propose to multiply the current I_C with the according voltage U_{CE} directly in the datasheet to get the conduction power loss $P_{V,COND}$ dependent on the current I_C as shown for two operating temperatures in Fig.2(b). The advantage of this procedure is that the curves in Fig.2(b) can be approximated very accurately with 2nd order polynomial fitting curves (dashed lines in Fig.2(b)) and generally be described in a form

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$$P_{V,COND} = c \cdot I_C + d \cdot I_C^2 \quad (1)$$

where the coefficients c and d are derived by curve fitting. A 2nd order approximation of the curves shown in Fig.2(b) gives the parameter values

$$P_{V,COND,TA=125} = c_{TA} \cdot I_C + d_{TA} \cdot I_C^2 = 1.103 \cdot I_C + 0.0401 \cdot I_C^2$$
$$P_{V,COND,TB=25} = c_{TB} \cdot I_C + d_{TB} \cdot I_C^2 = 0.855 \cdot I_C + 0.0336 \cdot I_C^2 \quad (2)$$

To describe the temperature dependency of the curve the coefficients can be made temperature-dependent. The more different operating temperatures have been recorded, the higher the order of this approximation can be set and the higher is the accuracy to be reached. In the example shown in Fig.2, only two operating temperatures are given (T_A=*125°C* and T_B=*25°C*) resulting in a first-order approximation as

$$c(T) = c_0 + c_1 \cdot T$$
$$d(T) = d_0 + d_1 \cdot T$$
$$P_{V,COND}(I_C, T) = (c_0 + c_1 \cdot T) \cdot I_C + (d_0 + d_1 \cdot T) \cdot I_C^2 \quad (3)$$

with the parameter values

$$c_0 = \frac{c_{TB} \cdot T_A - c_{TA} \cdot T_B}{T_A - T_B} = \frac{0.855 \cdot 125 - 1.103 \cdot 25}{125 - 25} = 0.793$$
$$c_1 = \frac{c_{TA} - c_{TB}}{T_A - T_B} = \frac{1.103 - 0.855}{125 - 25} = 0.00248 \quad (4)$$

in the example of Fig.2. Proceeding in analogy, we get for coefficients d_i

$$d_0 = \frac{d_{TB} \cdot T_A - d_{TA} \cdot T_B}{T_A - T_B} = \frac{0.0336 \cdot 125 - 0.0401 \cdot 25}{125 - 25} = 0.0320$$
$$d_1 = \frac{d_{TA} - d_{TB}}{T_A - T_B} = \frac{0.0401 - 0.0336}{125 - 25} = 65 \cdot 10^{-6} \quad (5)$$

If, as mentioned above, losses would be also known for, e.g., a third operating temperature T_C, a 3rd order model can be set up as

$$c(T) = c_0 + c_1 \cdot T + c_2 \cdot T^2$$
$$d(T) = d_0 + d_1 \cdot T + d_2 \cdot T^2 \quad (6)$$

with c_i and d_i to be defined. Three known temperatures T_A, T_B, T_C give two linear equation systems (three linear equations for c_i and three linear equations for d_i) which can be solved easily.

One can see from (4) and (5) that $c_1 \cdot T$ is very small against c_0 and that $d_1 \cdot T << d_0$. Therefore, alternatively, equation (1) can be set up temperature-independent for the highest acceptable junction temperature, e.g. *T=125°C*. If the junction temperature time behavior simulated under this assumption remains below *125°C*, the assumption is verified and there is even some thermal safety margin built into the design. This alternative concept will be employed in the following.

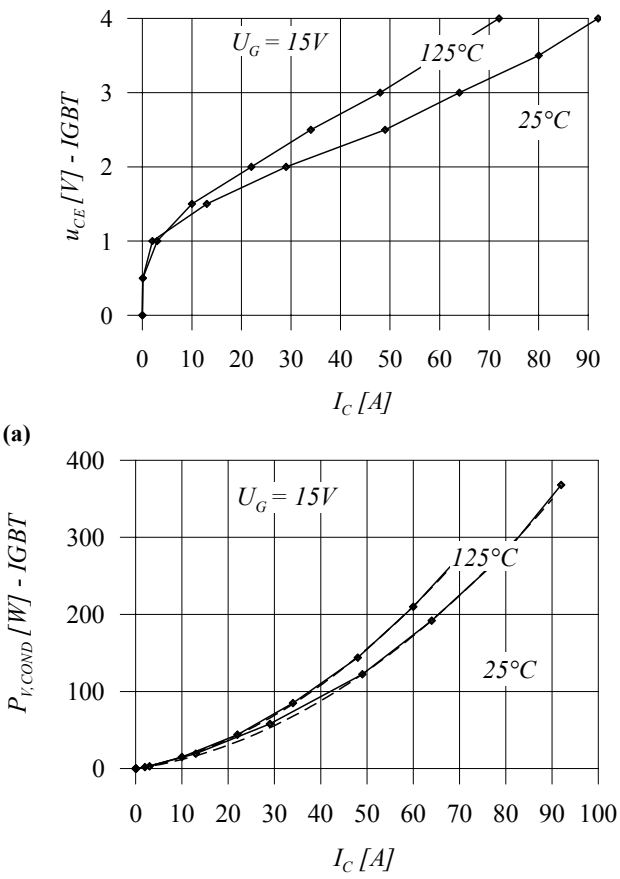


Fig.2: (a) Voltage-current characteristic of the IGBTs inside the module IXYS FII50-12E as given in the datasheet for two operating temperatures. **(b)** Conduction loss dependent on current derived by directly multiplying current with voltage in diagram (a). The dashed lines represent 2nd order polynomial fitting curves $P_{V,COND}[W] = c \cdot I_C + d \cdot I_C^2$.

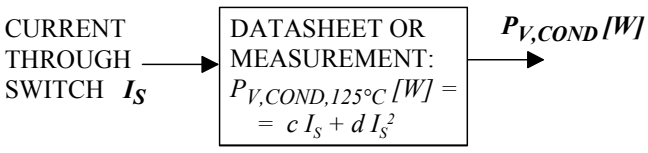


Fig.3: By applying the actual current through the IGBT to the 2nd order polynomial fitting curve (Fig.2(b)), the time behavior of the conduction loss $P_{V,COND}(t)$ of the IGBT can be directly calculated in a numerical circuit simulation.

Now, (1) can be embedded in the circuit simulation in form of an equation that uses the current through the ideal switch as input value and gives the time behavior of the conduction loss of the IGBT as output during the simulation. In **Fig.3** the temperature-independent implementation is shown in general form. The block in Fig.3 can be easily

added to any ideal circuit simulation with no need to rebuild the power circuit or change the switch models. **Figure 4** shows the characteristic curves for the free-wheeling diodes of the power module and (7) gives the 2nd order approximation of the conduction losses as shown with dashed lines in Fig.4(b).

$$P_{V,COND,TA=125} = c_{TA} \cdot I_C + d_{TA} \cdot I_C^2 = 1.277 \cdot I_C + 0.0150 \cdot I_C^2$$
$$P_{V,COND,TB=25} = c_{TB} \cdot I_C + d_{TB} \cdot I_C^2 = 2.065 \cdot I_C + 0.0136 \cdot I_C^2 \quad (7)$$

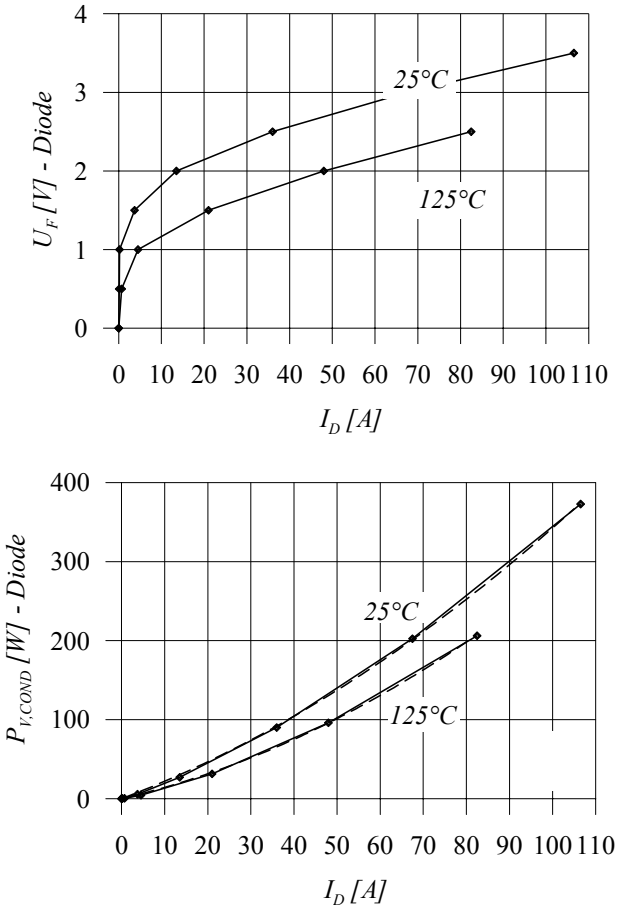


Fig.4: (a) Voltage-current characteristic of the anti-parallel diodes inside the module IXYS FII50-12E as given in the datasheet for two operating temperatures. **(b)** Conduction loss dependent on current derived by directly multiplying current with voltage in diagram (a). The dashed lines represent 2nd order polynomial fitting curves $P_{V,COND}[W] = c \cdot I_C + d \cdot I_C^2$.

3 Switching Losses

In power electronics switching losses typically contribute a significant amount to the total system losses. Therefore, omitting switching losses in the calculation or weighting the conduction losses with an estimated factor to take into account switching losses, might result in large errors concerning the total losses. If one plans to calculate the junction temperature time behavior to improve reliability of the design, it is necessary to accurately calculate the switching losses.

One way to do this is to build a very accurate model based on the physics of the semiconductor that provides voltage- and current-waveforms during switching-on and switching-off [2], [3]. Besides the high effort to set up, validate and tune these models, there is also the impact of the wiring stray inductance that strongly influences the switching events and, therefore, the switching losses. Here, coupling of electromagnetic FEM (finite element method) software with the circuit simulator would provide a computationally very expensive solution. Modeling the switching event in detail to get accurate switching losses results in extremely large simulation times since the time step width of the numerical simulation has to be adjusted to very small values.

Another method is to calculate conduction and switching losses analytically based on the on-times of the switches. This gives very good results for PWM systems where the modulation scheme is known (e.g. [4]). For systems employing hysteresis controllers that show chaotic switching behavior, such calculations cannot be performed. Generally, the necessary analytical calculations are often difficult perform.

In [5] the proposed strategy of finding the switching losses is to define a look-up table of the losses dependent on certain parameters like blocking voltage, current and/or junction temperature. The look-up table is filled with experimental data. The scope of that paper is not numerical simulation in a virtual design environment but on-line monitoring of chip-temperatures in form of a hardware implementation. The look-up table is consulted at each switching action to get the according power loss. In [6] the method of counting switching actions and weighting them with measured loss energy data stored in a look-up table is proposed for numerical circuit simulation. Emphasis of that paper is on the possibility to perform very fast numerical simulations with ideal switches, and calculate highly accurate semiconductor losses. In [7] a scheme based on a switching loss counter is introduced with measured switching loss data being described not by a look-up table but by an easy-to-handle equation assuming linear dependency of the switching loss energy on the current being switched. The same scheme is proposed in [8] in form of a "Loss Calculation Box" implemented in MATLAB. In this paper, the scheme introduced in [7] will be discussed and improved.

The current-dependency of switching losses for the IGBT module under investigation as given in the datasheet is shown in **Fig.5**(a). The losses are also dependent on the blocking voltage, the junction temperature, the gate resistor and the wiring stray inductance. Dividing the total energy losses through the current gives a switching-loss factor

$$k(I_C) = \frac{E_{TOTAL}}{I_C} \quad \left[\frac{\mu Ws}{A}\right] \quad (8)$$

which can be approximated by a second-order polynomial fitting curve as also shown in Fig.5(b) as

$$k(I_C) = a + b \cdot I_C + c \cdot I_C^2 = 256.0 - 2.160 \cdot I_C + 0.0466 \cdot I_C^2 \quad (9)$$

In many cases, if switching losses are in good approximation of linear dependency over the relevant current-range, k can set to be constant [4]. The total switching energy loss is then described as

$$E_{TOTAL} = k_{IGBT}(I_C) \cdot I_C = (a + b \cdot I_C + c \cdot I_C^2) \cdot I_C \quad (10)$$

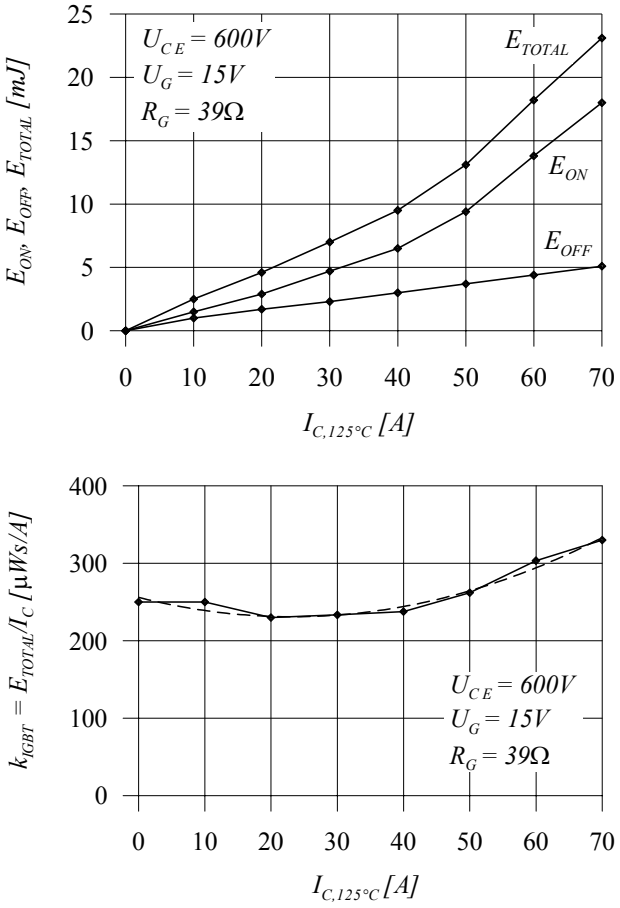


Fig.5: (a) Current-dependent switching energy loss of the IGBTs of the module IXYS FII50-12E as given in the datasheet for switching-on, switching-off and total loss $E_{TOTAL} = E_{ON} + E_{OFF}$ for $T_J = 125°C$. **(b)** The parameter k_{IGBT} describing the ratio of the total switching losses and the switched current for a given junction temperature ($T_J = 125°C$) shows a weak dependency on the switched current. The dashed line shows a 2nd order polynomial fitting curve $k_{IGBT,125°C}$ [µWs/A] as given in (9).

As already discussed with conduction losses, we will consider k for a given maximum junction temperature $T_J = 125°C$ and justify this assumption by making sure that the resulting T_J (t) will always remain below this value. Alternatively, if a minimum of two operating temperatures is given (which is not the case in the example of Fig.5), temperature-dependency could be considered in analogy to (3) as

$$a(T) = a_0 + a_1 \cdot T$$
$$b(T) = b_0 + b_1 \cdot T$$
$$c(T) = c_0 + c_1 \cdot T$$
$$k_{IGBT}(I_C, T) = (a_0 + a_1 \cdot T) + (b_0 + b_1 \cdot T) \cdot I_C + (c_0 + c_1 \cdot T) \cdot I_C^2 \quad (11)$$

This can be easily expanded to higher-order approximations if the necessary data (loss-measurements at three or more operating temperatures) is available (see (6)).

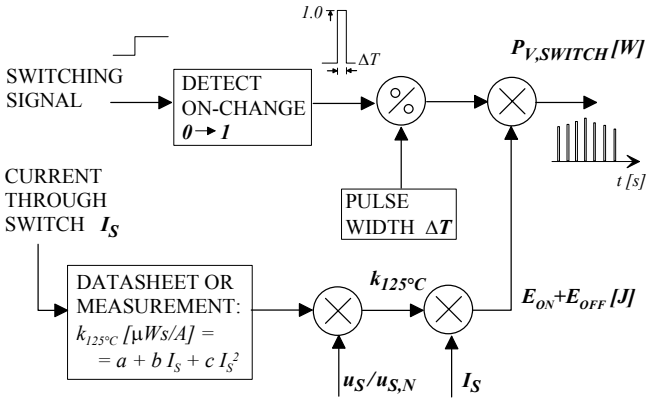


Fig.6: The general scheme employs the current through the switch, the switching signal and the approximation of ratio k_{IGBT} (equation (9)). It gives the time behavior of the switching power loss $P_{V,SWITCH}$ (t) during a numerical circuit simulation. The scheme acts as a simple counter detecting switching-actions.

A general implementation of the scheme calculating the switching losses is shown in **Fig.6**. Whenever the switching signal detects a change of the state of the ideal switch from *OFF* to *ON*, a pulse of height *1.0* is generated with a defined pulse width ΔT. Dividing this pulse through its width ΔT creates a pulse signal with unit $[s^{-1}]$ that, multiplied with energy, represents a power. This power is not dependent on the arbitrarily defined pulse width ΔT (this is obviously an absolute necessary condition for such a scheme).

Only if the pulse width ΔT is set to be in the order of the duration of a typical switching event, the resulting time behavior of the switching losses $P_{V,SWITCH}$ (t) will show pulses of physically correct magnitude and duration (as one might watch for an according experimental setup on an oscilloscope). Since the switching losses will be injected into the thermal model of the power semiconductor where the thermal time constant (~*10ms*) of the silicon chip is typically magnitudes larger than the duration of the switching event (~*100ns*), the shape of the switching loss pulse calculated by the scheme in Fig.6 does not influence the resulting time behavior of the junction temperature, and the definition of ΔT has no influence on the temperature calculation as long as $1/\Delta T$ is small compared to the switching frequency.

If the step width of the numerical simulation is known (e.g. constant step width simulation) the pulse width ΔT can be set equal to the numerical step width. This results in the smallest possible pulse implementation without having any negative impact on simulation time or numerical accuracy. A possible implementation of such a scheme employing a commercial circuit simulator is shown in a screenshot in [7].

As shown in Fig.6, the time-behavior of the current through the ideal switch is taken as an input value, and the switching loss factor k is then calculated based on the second-order approximation from the datasheet (and/or measurement). If the blocking voltage u_S is different from the one given in the datasheet ($u_{S,N}$), it can be adjusted by a linear approximation employing the factor $u_S/u_{S,N}$ (a higher-order approximation of the voltage dependency can be implemented easily if the necessary experimental data is available). Now, multiplying the actual value of k with the current I_S, the total energy loss $E_{TOTAL}=E_{ON}+E_{OFF}$ for the actual current I_S and the actual blocking voltage u_S is derived and used as weighting factor.

In the scheme as shown in Fig.6 only switching-off events are counted, but weighted with the total switching loss $E_{TOTAL}=E_{ON}+E_{OFF}$. This is justified as long as switching time constants are magnitudes smaller than the thermal time constants of the power semiconductors and, therefore, the time behavior of the junction temperature is not affected (which is typically the case). On the other hand, the loss calculation scheme is significantly simplified by counting on- and off-losses as a single event. If necessary, the scheme can easily be expanded by counting and weighting on- and off-losses separately.

Remark: Due to the programming of the underlying algorithms in a numerical circuit simulator, there might occur time delays of one (or even more) numerical time steps between power circuit and control circuit signals, and also between various signals within the control part of the simulator. Therefore, for an implementation of the proposed scheme in a specific circuit simulator, one has to make sure that the signal I_S that is multiplied with the pulse to create power losses, is not delayed against the pulse. If, e.g., the signal I_S (in the control part of the simulator) lags behind the pulse by even one numerical time step, the product of signal I_S and pulse might always be zero. A comparable problem arises with the implementation of the factor $u_S/u_{S,N}$ with u_S becoming zero when the switch goes into *ON*-state. Without an according short-term storage of the voltage value u_S the resulting switching losses might always be zero. These implementation details are dependent on specific circuit simulators and are, therefore, not discussed in further detail.

4 Implementation of the Loss-Calculation in a Numerical Circuit Simulation

4.1 Loss-Calculation in a Circuit Simulation

The implementation of the loss calculation scheme is shown in **Fig.7** for the example of an inverter connected to a drive. The power circuit is modeled employing ideal switches. The current I_S measured in the transistor T_1 provides an input of the loss calculation scheme. Furthermore, the switching signal of T_1, generated by the PWM control of the inverter, is used to calculate the switching losses. The total losses of T_1 are fed into the thermal model (see following section) of semiconductor T_1 to calculate the junction temperature time behavior of this transistor. The actual junction temperature $T_{J,T1}(t)$ can be fed back (dashed line in Fig.6) to the loss calculation box of switch T_1 if switching and conduction losses are defined to be temperature dependent as shown in (3) and/or (11).

Loss calculation schemes and thermal models of the other power semiconductors of this bridge leg D_1, T_2, D_2 are not shown in Fig.7. They are to be implemented in strict analogy.

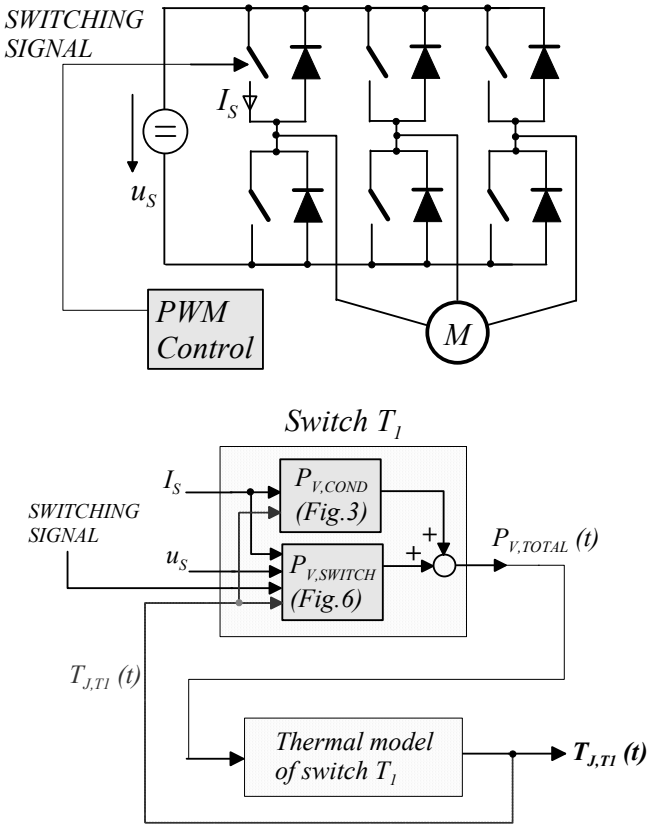
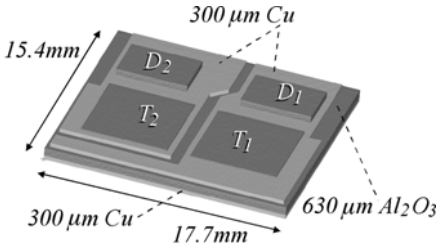


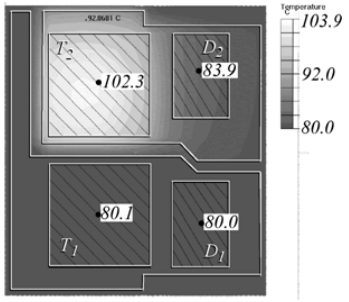
Fig.7: Implementation of the loss calculation scheme in a circuit simulator employing a circuit simulation with ideal switches. The box labeled "$P_{V,COND}$" corresponds with Fig.3 and the box labeled "$P_{V,SWITCH}$" is shown in detail in Fig.6.

4.2 Thermal Model of the Power Semiconductors

The thermal model of the power semiconductors is composed of a RC thermal equivalent network. This equivalent network is derived from the thermal step response of the power semiconductors which is calculated employing a 3D-FEM solver or measured experimentally. The mathematical background of the equivalent circuit model as employed in this example is the finite difference method. Since the thermal modeling theory is out of the scope of this paper only results will be shown. For details how to set up these models see [9] or [10].



(a)



(b)

Fig.8: (a) Internal geometry of the power module IXYS FII50-12E. (b) Stationary 3D-FEM simulation of the power module where only transistor T_2 is heated.

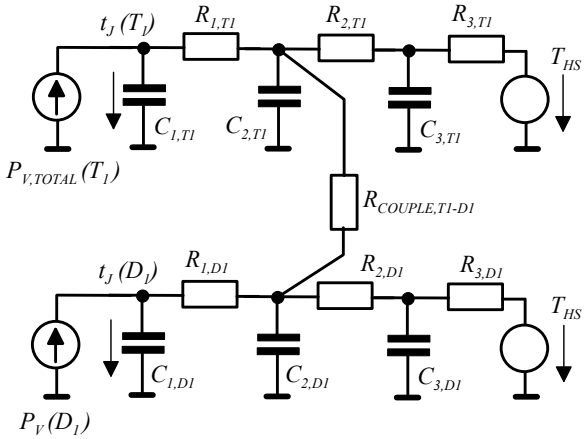


Fig.9: Thermal equivalent circuit of T_1 and D_1 of the power module IXYS FII50-12E as employed in Fig.7. Transistor T_1 is thermally coupled only with diode D_1 which is modeled by thermal resistance $R_{COUPLE,T1@D1}$. The heat sink temperature T_{HS} is given (e.g., assumed to be at a known constant value).

The internal layout of the power module of Fig.1 is shown in **Fig.8**(a). The temperature distribution calculated numerically by a 3D-FEM solver is shown in Fig.8(b). Here, only switch T_2 is heated up, showing that also diode D_2 is thermally affected but not the other two semiconductors T_1 and D_1. Since T_2 and D_2 are sitting on the same copper layer, they are thermally coupled which is considered by a thermal coupling resistor as shown in **Fig.9** for the two devices T_1 and D_1. In Fig.9 the power losses of transistor T_1 are modeled as electrical current from a controllable current source. The time-dependent voltage drop across thermal capacitor $C_{1,T1}$ represents the time-dependent junction temperature t_J *(T1)* of the switch T_1. Here, the heat sink temperature T_{HS} is assumed to be known and constant. In many practical cases also the heat sink has to be represented by a thermal model considering hot spots below the power modules and/or thermal coupling of modules being mounted onto the same heat sink. For details of thermal heat sinks modeling see [10]. The other two semiconductors T_2 and D_2 of the power module are represented by an analog thermal model with slightly different parameter values due to the asymmetric geometry of the internal module design (see Fig.8).

	R_1	R_2	R_3	C_1	C_2	C_3
T_1	0.0265	0.3844	0.3844	13m	42m	163m
D_1	0.0472	0.6845	0.6845	4m	27m	125m
	$R_{COUPING}$ = 7.400					

Tab.1: Parameter values of the thermal equivalent circuit of Fig.9. The heat sink temperature is assumed to be $T_{HS} = 80°C = const$.

4.3 Simulation Results

In **Fig.10** the time behavior of key waveforms of a *5kW*-inverter simulation is shown together with conduction losses, switching losses and total losses of all four semiconductor chips of the bridge leg realized by the power module IXYS FII50-12E. The conduction and switching loss characteristics are assumed for a constant junction temperature T_J *=125°C*. As shown in **Fig.11**, all temperature values remain below this value justifying the assumption of T_J *=125°C* plus providing some additional safety margin for the thermal design. In this example there is no implementation of a junction temperature feedback loop influencing the loss model (see Fig.7).

Simulation parameters:

u_S = *800V*
f_S = *16kHz*
u_M = *320V (phase amplitude of the motor)*
f_M = *50Hz*
L_M = *3.8mH*
R_M = *0.9Ω*

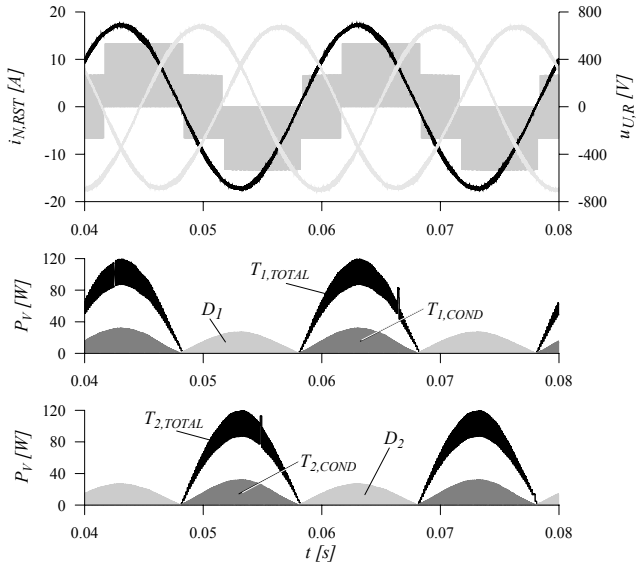


Fig.10: Numerical simulation of the time behavior of AC side current $i_{N,RST}$, AC side voltage $u_{U,R}$, and of the power losses of diodes (D_1 and D_2) and the IGBTs (T_1 and T_2) of the power module IXYS_FII50-12E. Switching losses of the diodes are neglected. For the transistors the conduction losses are shown in gray color and the total losses are shown in black. Time behavior of switching losses is smoothed by applying a running-average filter (not shown in Fig.6) to $P_{V,SWITCH}(t)$.

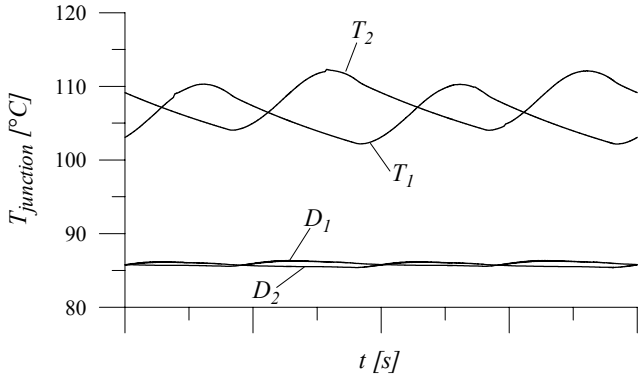


Fig.11: Numerical simulation of the time behavior of the junction temperatures of T_1, T_2, D_1, D_2. While the time behavior of the power losses of the IGBTs and/or diodes is of equal shape (see Fig.10), the asymmetry in the junction temperature time behavior is resulting from an small asymmetry of the internal geometry of the power module (Fig.8) and, therefore, different R_{th}- and C_{th}-values of the four chips inside the module.

The transistor and the diode conduction losses appear in Fig.10 as shaded areas because of the high PWM switching frequency. The transistor switching losses form a sequence of pulses of extremely high value as compared to the average value. For a better visualization of the waveforms in Fig.10, the switching loss pulses have been filtered employing a running-average filter (not shown in Fig.6 or Fig.7) which results in a smooth curve of the switching losses. Naturally, such a filtering effect always takes place when the losses are "injected" into the top silicon layer of the chip (represented by $C_{1,T1}$) that typically shows a large time constant compared to the duration of switching loss pulses. Therefore, the junction temperature time behavior as shown in Fig.11 does not show temperature variations with switching frequency.

5 Conclusion

The paper discusses loss estimation of power semiconductors in numerical circuit simulations. The proposed schemes are simple to implement, do not slow down the numerical simulation, and can be embedded by the user in most circuit simulators. The estimation of the losses, especially of the switching losses of the power semiconductors, is as accurate as the loss data provided by datasheets or experimental measurements. Therefore, the accuracy of the resulting total losses is principally not influenced by the proposed loss calculation scheme.

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