Analysis of a Multilevel Multicell Switch-Mode Power Amplifier Employing the "Flying-Battery" Concept

Hans Ertl, *Member, IEEE*, Johann W. Kolar, *Member, IEEE*, and Franz C. Zach, *Member, IEEE*

***Abstract*—This paper presents a novel switch-mode power amplifier based on a multicell multilevel circuit topology. The total output voltage of the system is formed by series connection of several switching cells having a low dc-link voltage. Therefore, the cells can be realized using modern low-voltage high-current power MOSFET devices and the dc link can easily be buffered by rechargeable batteries or "super" capacitors to achieve very high amplifier peak output power levels ("flying-battery" concept). The cells are operated in a phase-shifted interleaved pulsewidth-modulation mode, which, in connection with the low partial voltage of each cell, reduces the filtering effort at the output of the total amplifier to a large extent and, consequently, improves the dynamic system behavior. The paper describes the operating principle of the system, analyzes the fundamental relationships being relevant for the circuit design, and gives guidelines for the dimensioning of the control circuit. Furthermore, simulation results as well as results of measurements taken from a laboratory setup are presented.**

***Index Terms*—Class-D amplifier, interleaved pulsewidth modulation, multicell, switch-mode amplifier.**

I. Introduction

In THE AREA of industrial measurement, testing, and process technology there exist many applications of power amplifiers in order to generate current and voltage signals of special shape at high power levels. To give an example, the supply voltage simulation for testing reliability and electromagnetic interference (EMI) compliance of automotive power electronic systems should be mentioned. There, typically output voltages of ± 100 V and current levels of ± 100 A and more may be required. Until a few years ago, the power sources for the generation of such testing signals in most cases have been realized by application of linear power amplifiers. Carefully designed linear (class AB) power amplifiers in general show an excellent dynamic behavior and high bandwidth in connection with a good linearity. However, the dissipative losses are very high and the systems show a dramatically low efficiency, especially if nonresistive or nonlinear loads have to be supplied. Due to the high losses and the huge cooling effort the specific power density is comparatively low and the purchase and operating costs are high.

Manuscript received June 11, 2001; revised November 30, 2001. Abstract published on the Internet May 16, 2002. This work was supported by the Hochschuljubiläumsfonds der Stadt Wien.

H. Ertl and F. C. Zach are with the Power Electronics Section, Vienna University of Technology, A-1040 Vienna, Austria (email: j.ertl@tuwien.ac.at).

J. W. Kolar is with the Power Electronics Systems Laboratory, Swiss Federal Institute of Technology Zurich, CH-8092 Zurich, Switzerland.

Publisher Item Identifier 10.1109/TIE.2002.801056.

As a consequence of the innovations in the area of turn-off power semiconductors, linear power amplifiers today in many applications are replaced more and more by "digital" switch-mode (class D) amplifier systems. There, the output voltage is formed in theory without any losses by a pulse width modulated power stage with subsequent low-pass *LC* output filter. The most significant drawback of switch-mode amplifiers, however, is their low bandwidth caused by the fundamental compromise which has to be accepted between signal frequency, filter cutoff frequency and switching frequency. With the turn-off power semiconductor devices being presently available for the kVA-power region (insulated gate bipolar transistors (IGBTs) and MOSFETs), the switching frequency usually is limited to 20–100 kHz. The task of the *LC* filter at the output of the switching stage is the suppression of the switching frequency harmonics without significant influence on the signal components. For a practical realization, this results in the fact that the bandwidth of the signal to be amplified is limited to $\approx$1/10 of the switching frequency, i.e., to values of 2–10 kHz.

Several methods have been proposed for improving the output voltage quality and bandwidth of class-D amplifiers which are based on linear correction stages [1]–[5], on hybrid output filters [6] or on auxiliary switch-mode stages arranged in parallel and operated at very high switching frequencies [7]. However, also with these techniques the fundamental switching/signal frequency compromise of the switch-mode topology remains unaffected. To avoid this basic drawback, multistage topologies can be applied which result in switching frequency components being relevant for filtering which are a multiple of the switching frequency of a single stage. As an example, a multilevel switch-mode amplifier structure which is based on a *parallel* arrangement of several interleaved half-bridges should be mentioned [8]. However, in this case, an output inductor is required for each stage and the current flowing through the inductor shows a high ripple amplitude with basic switching frequency; only the total current of all stages (i.e., the current flowing into the output filter capacitor) is characterized by multiple switching frequency components. Furthermore, this concept requires specific control measures to balance the output currents of the individual stages.

Alternatively, the topology proposed here is based on a *series* connection of N full-bridge switching stages ("switching cells," see Fig. 1) being similar to the series arrangement of full-bridge stages as known from high-power converter systems, e.g., static var compensators [9], [10] or high-power drive systems [11]. By application of the concept of multicell topologies being op-

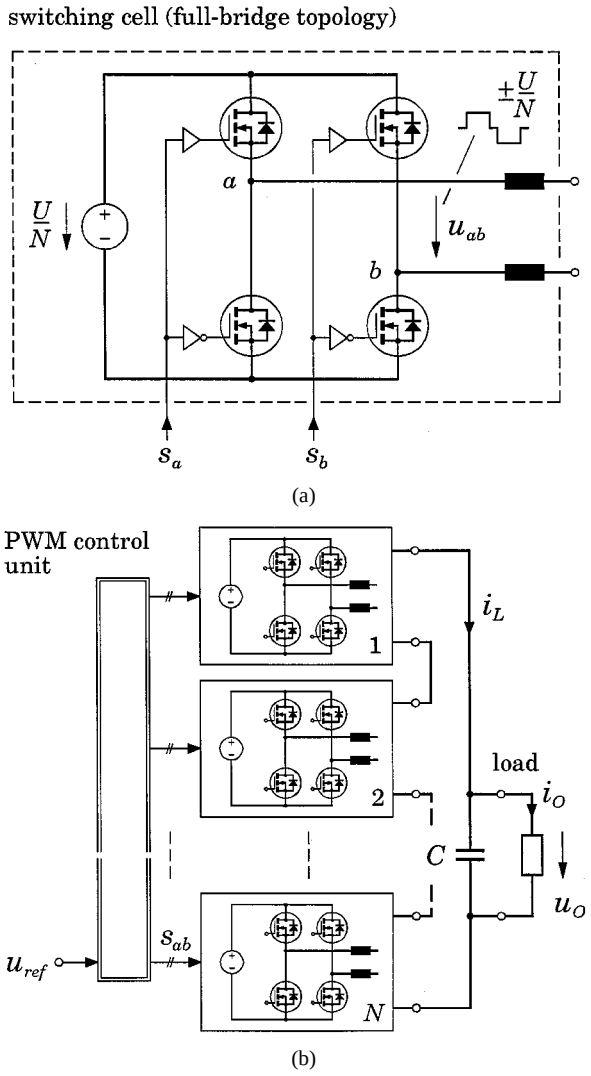


Fig. 1. Basic circuit topology of the proposed multicell multilevel switch-mode power amplifier. (a) Single switching cell (full-bridge topology) based on the application of low-voltage power MOSFETs. (b) Total multistage amplifier system formed by a series connection of N switching cells operated in interleaved (phase-shifted) PWM mode.

erated in an interleaved (phase-shifted) pulsewidth-modulation (PWM) mode to switch-mode amplifier systems, the effective switching frequency regarding the output *LC* filter results in N times the switching frequency of the single cell. Furthermore, simultaneously a significantly improved approximation of the voltage reference value is achieved due to the fact that a single switching instant contributes only a voltage step of $1/N$th of the total effective dc-link voltage U of the system. Therefore, the total voltage ripple appearing at the output of the multicell topology is significantly reduced as compared to a single-cell structure of equal switching frequency.

A further advantage of the proposed multicell class-D amplifier is given by the fact that for the realization of the switching cells power semiconductors with low blocking voltage capability can be considered. This allows the application of majority-carrier devices (low-voltage MOSFETs, Schottky diodes). In this area of semiconductor technology, major improvements have been achieved in recent years, primarily influenced by the requirements of battery-powered equipment (laptop computers, portable tools, etc.), automotive systems and supply units for high-speed CPUs. Contrary to conventional switch-mode amplifiers which have to be equipped frequently by minority carrier semiconductors (IGBTs, bipolar diodes) because of the high blocking voltage stress, the switching cells of the proposed system can be operated at higher switching frequencies at comparable switching losses. This leads to a further improvement of the output voltage quality. Furthermore, it should be mentioned that a significantly improved EMI behavior can be expected because only voltage transitions of amplitude U/N (instead of U as is the case for conventional switch-mode amplifiers) occur. Finally, the partial dc input voltage U/N (in general, generated by individual switch-mode power supply units) can easily be buffered by rechargeable batteries or double-layer ("super") capacitors. This results in amplifier systems which allow very high pulse currents and power levels for short-time operation as is required for testing applications in many cases ("flying-battery" amplifier concept).

II. Basic Operation

Fig. 2 demonstrates the basic stationary operation of the proposed multicell amplifier topology. The control signals $s_{a,i}$ and $s_{b,i}$ of the switching cell $i = 1 \ldots N$ are gained by comparison of the reference voltages $+u_{\rm ref}$ and $-u_{\rm ref}$ with a triangular carrier signal $u_{{\rm tri},i}$ of frequency f_S (switching frequency of the power MOSFETs). With this, the modulation index m (duty ratio) of the output voltage u_{ab} (period $T = 1/(2f_S)$) of a cell is defined by

$$m = \frac{u_{\rm ref}}{\hat{U}_{\rm tri}} \quad -1 \le m \le +1. \tag{1}$$

Remark: Due to the phase displacement of the control signals s_a, s_b of a switching cell, the cell itself already shows a fundamental frequency of $2f_S$. Due to the phase shift T/N of the N carrier signals $u_{{\rm tri},i}$ the effective switching frequency of the total output voltage $\sum u_{ab}$ of all cells (relevant for the dimensioning of the *LC* output filter) results in $2Nf_S$. The local average value $\overline{u}$ of the total output voltage follows as $\overline{u} = U/N \cdot mT \cdot N/T = mU$ ($U \ldots$ total DC link voltage). Neglecting the fundamental voltage components across the total smoothing inductor of the *LC* filter (i.e., $u_O = \overline{u}$) the ripple amplitude of the inductor current i_L can be calculated according to the basic relation $u = L di/dt$ considering the shaded rectangle of Fig. 2

$$\Delta i = \frac{1}{L}\left[\frac{U}{N} - \overline{u}\right]\Delta t = \frac{1}{L}\left[\frac{U}{N} - \overline{u}\right] mT \tag{2}$$

(valid for the interval $0 \le m \le 1/N$; L denotes the total value of the smoothing inductances $L = NL_i$). Using $\overline{u} = mU$ relation (2) leads to a quadratic dependency of the ripple on the modulation index (see Fig. 3)

$$\Delta i(m) = \frac{UT}{L}\left[\frac{m}{N} - m^2\right]. \tag{3}$$

For $m = 1/(2N)$, a maximum ripple amplitude of

$$\Delta i_{\max} = \frac{U}{8f_S L}\,\frac{1}{N^2} \tag{4}$$

appears. According to (4), the maximum current ripple amplitude is reduced by a the factor N^2 for multicell systems. As a consequence, a rather low value for L can be chosen which results in a low output impedance of the amplifier. Furthermore,

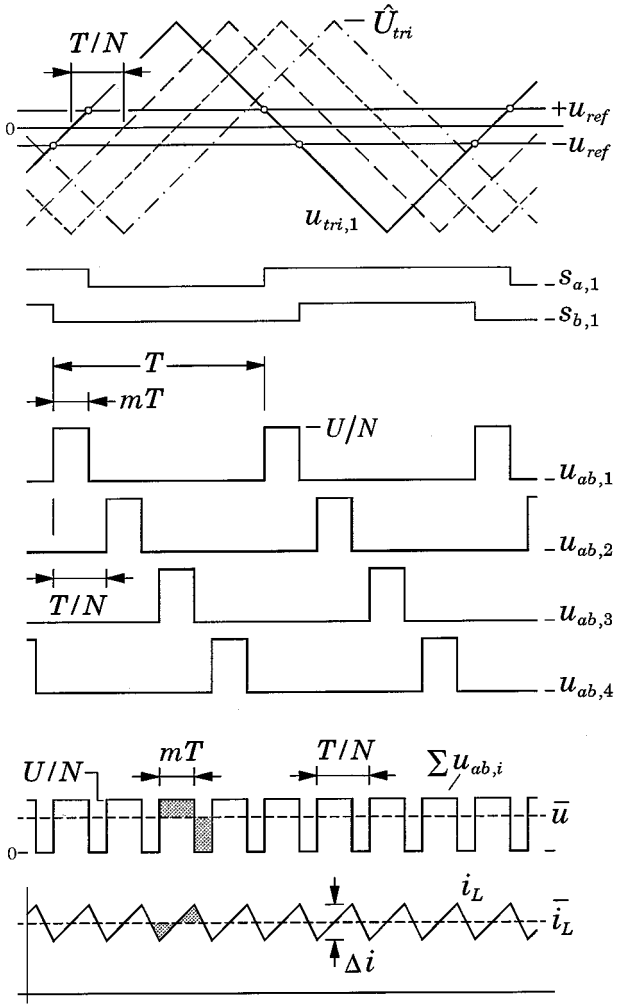


Fig. 2. Wave shapes of interleaved triangular carrier signals $u_{\mathrm{tri},i}$, partial voltages $u_{ab,i}$, total output voltage $\sum u_{ab,i}$, and output filter inductor current i_L for a multicell ($N = 4$) switch-mode amplifier (shown here for ($0 \leq m \leq 1/N$).

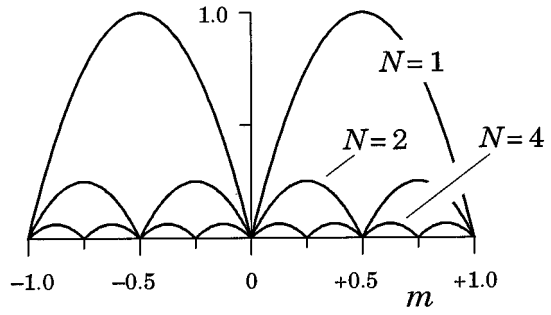


Fig. 3. Dependency of the output filter ripple current (normalized to $U/(8f_S L)$) on the normalized output voltage m given for different numbers N of switching cells.

the ripple amplitude Δu of the voltage appearing across the filtering capacitor C is improved even more. The integration of the ripple current component of i_L within one (half) period of a relevant switching cycle (see the shaded triangle in Fig. 2) according to $u = \int i dt/C$ and using (4) finally gives the maximum ripple of the total output voltage u_0

$$\Delta u_{\max} = \frac{T}{8C}\frac{1}{N}\Delta i_{\max} = \frac{U}{128 f_S^2 LC}\frac{1}{N^3}. \tag{5}$$

It should be noted that this equation shows a third-order dependency on the number of switching cells, i.e., doubling N will reduce the voltage ripple by a factor of 8. Rearranging (5) using $LC = 1/\omega_0^2$ and $\omega_0 = 2\pi f_0$ (cutoff frequency of the *LC* output filter) we receive for the output voltage ripple normalized to the total dc-link voltage U

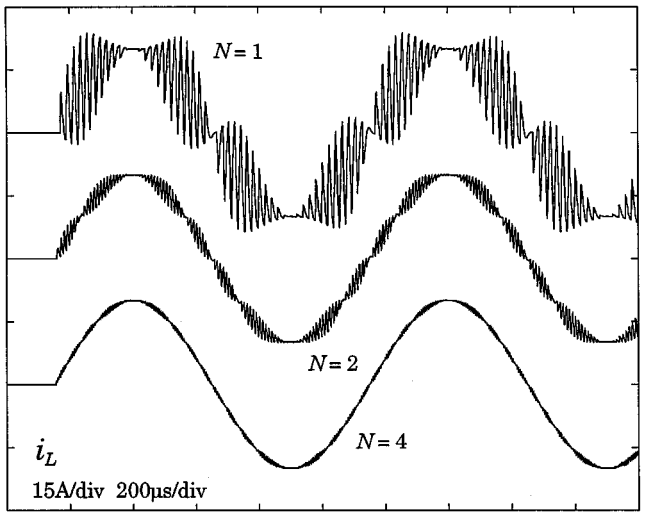
$$\frac{\Delta u_{\max}}{U} = \frac{\pi^2}{32}\left[\frac{f_0}{f_S}\right]^2 \frac{1}{N^3} \approx 0.3 \cdot \left[\frac{f_0}{f_S}\right]^2 \frac{1}{N^3}. \tag{6}$$

For example, for f_0 being approximately equal to the switching frequency f_S of the bridge leg of a single cell a voltage ripple of <0.5% will result for a system with $N = 4$ cells and 0.05% (≈65 dB) for eight cells, respectively. The simulated current/voltage wave shapes shown in Fig. 4 demonstrate the remarkable ripple reduction and performance of the proposed concept for increasing values of N.

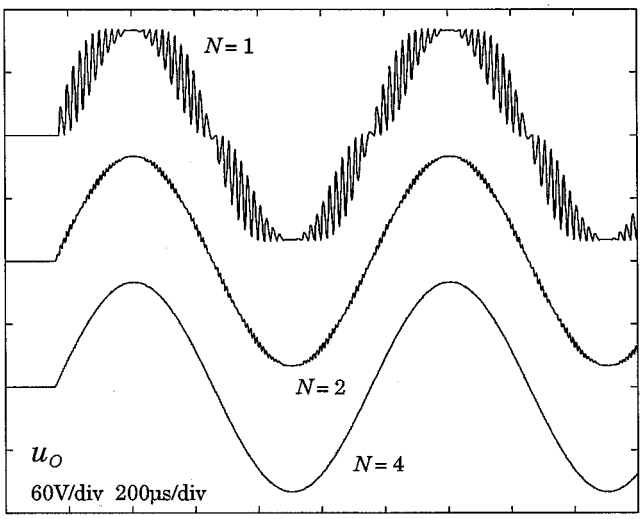
III. DC-Link Supply—Flying-Battery Concept

As a drawback of the proposed amplifier system one might see that N isolated supply units for feeding the individual dc links of the switching cells are required in general. However, amplifiers in the area of measuring and testing equipment often are applied for generating short-time testing signals (e.g., bursts, etc.) of high energy level. Here, the low dc-link voltage level of the multicell concept offers a possibility for easy energy storage by application of rechargeable batteries, double-layer ("super") capacitors, or conventional high-capacity electrolytic capacitors. With this, the dc-link supply units only have to be designed regarding the average power consumption whereas the application of modern low-voltage power MOSFET devices allows the generation of very high output current pulses. Furthermore, due to the comparatively low required inductance value of the output inductor L (see the values specified in Fig. 4) air core coils would be applicable, avoiding saturation in case of high current amplitudes. *Remark*: Contrary to the series topology proposed here which shows a "voltage-based" ripple reduction, interleaved PWM switch-mode amplifiers with cells arranged in parallel ("current-based reduction") are sensitive to saturation of the filtering inductors because the nonlinear shape of the inductor current in case of saturation impairs the ripple "cancellation".

The operation of all cells using a common modulation index m gives an equal dc input current of mi_L for each cell (ideal system assumed). Consequently, different dc input voltages of the cells are not "self-balanced" and have to be equalized by the dc-link supply. If this supply is realized by N individual switch-mode power supply (SMPS) units their output voltage control guarantees equal dc-link voltages. However, with this the energy storage capability using dc-link capacitors is not given and the SMPS units have to be chosen regarding the maximum output power of the amplifier. To overcome this drawback, it is necessary that the SMPS units emulate a defined output resistance by adequate control or inherently by the topology (e.g., using a series resonant converter as described



(a)



(b)

Fig. 4. Simulation of the 1-kHz sine-wave response of multicell switch-mode amplifiers for different numbers N of series-connected switching stages. (a) Output filter current; the ripple current minima are in close accordance with Fig. 3 (e.g., $m = \pm 0/\pm 0.5/\pm 1$ for $N = 2$). (b) Amplifier output voltage; parameters: $\hat{m} = 1, U = 100$ V, $f_S = 25$ kHz, $L = 25\ \mu$H, $C = 1\ \mu$F, ($f_0 = 31.8$ kHz), $R_{\text{load}} = 5\Omega$.

in [12]). This, in connection with equal modulation indexes m guarantees an effective and stable load sharing of all cells.

If the dc-link supply of the switching cells alternatively is performed by rechargeable batteries, the batteries of the individual switching cells can be charged successively using a single isolated SMPS charging unit connected to a "charging bus" (see Fig. 5). The required battery-charging strategy depends on the technology of the applied batteries. To achieve high output currents the realized prototype amplifier is equipped with pure lead-tin (PLT) batteries. According to [13], a modified intermittent charging scheme is implemented. The battery management system (realized using a small single-chip microcontroller) detects the switching cell showing the lowest dc-link voltage and connects it to the charging bus by a power relay (all other cells are disconnected). The SMPS unit shows a constant-current/limited-voltage characteristic with a relatively high charging current of, e.g., type C_1 (i.e., a charging current

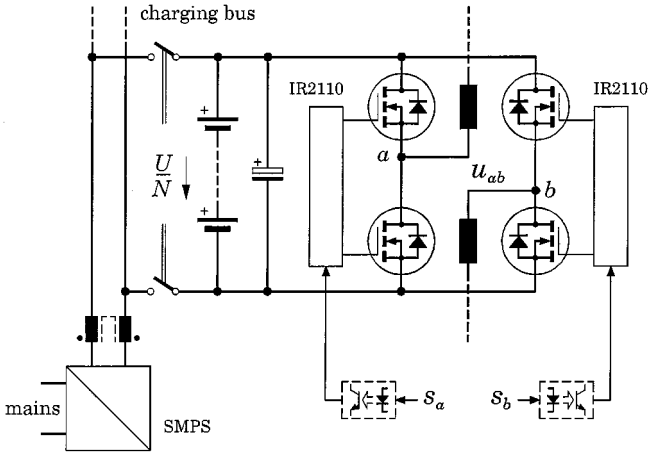


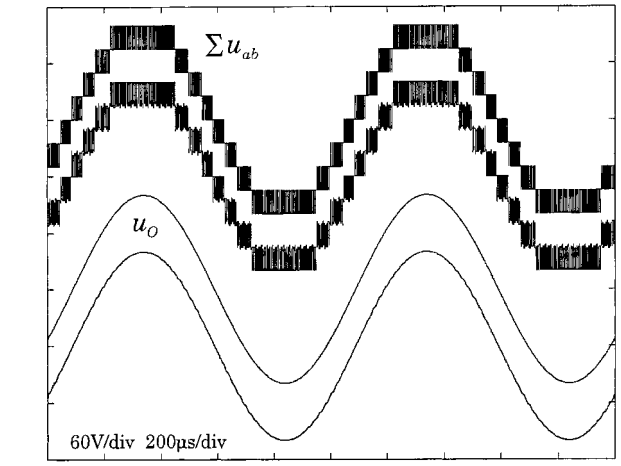
Fig. 5. Supply of the dc link of the switching cells by a rechargeable battery ("flying-battery" concept); sequential battery charging using a single SMPS charging unit.

equal to the nominal Ah rating of the battery is applied). After a specific time, or if the battery reaches the voltage limit for a specific time, or if the voltage difference of the charged cell as compared to the other cells exceeds a given threshold the charging of the specific cell will be terminated and the next cell for charging is chosen according to the dc-link voltage as described before. With this charging method, the dc-link voltages of the individual cells can be equalized to about 10% of the nominal voltage which is of significant importance because the ripple cancellation as described in Section II is not perfect in case of different dc-link voltages. The analyses presented by Fig. 6, however, show that the arising spectral components (i.e., for $f = 2f_s$) are of tolerable amplitude level (≈ 20 dB below the components of the ideal case at $f = 8f_s$).

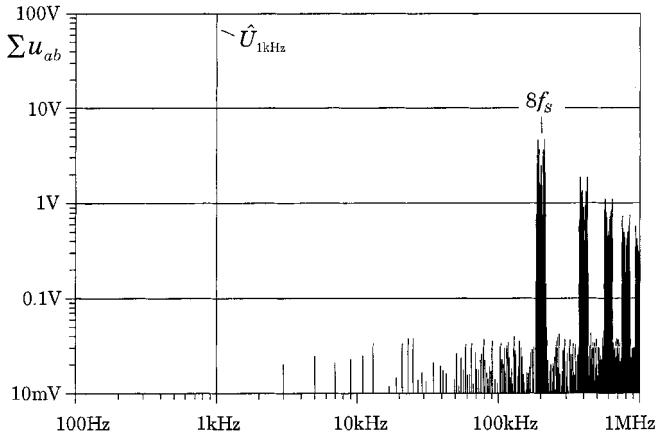
Besides the power MOSFETs and the battery with an additional low-impedance electrolytic capacitor connected in parallel to absorb the switching frequency current components, the power circuit of a single cell consists of two half-bridge gate drivers and two optocouplers which perform the required isolation of the driving signals. Using integrated half-bridge driver ICs limits the effort for the driver stages. Due to the low voltage level, the auxiliary power supply of the gate drivers can be drawn directly from the dc voltage link. It should be noted that according to the series connection each cell shows a common-mode voltage stress caused by the switching of all other cells. Therefore, care has to be taken to limit the resulting common-mode currents. This can be achieved if the charging power supply features a reduced capacitive input/output coupling and by insertion of a common-mode choke to the output of the SMPS.

IV. PWM Generation—Control Concept

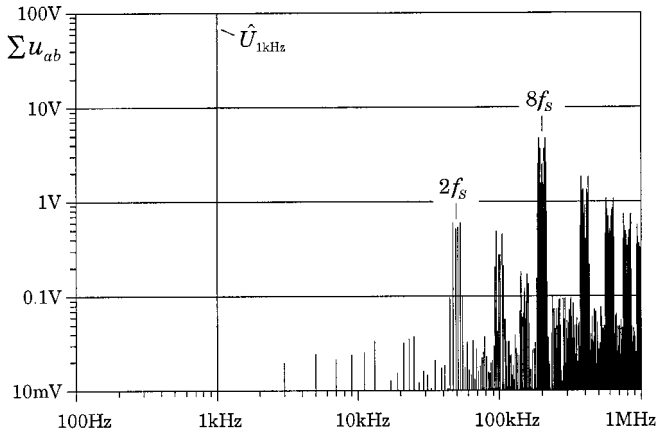
The generation of the phase-shifted control signals can be performed by a circuit according to Fig. 7. First, a chain of toggle flip-flops provides N square-wave signals of 50% duty ratio and corresponding phase shift to the input of analog integrators. At the output of these stages the required triangular carrier signals $u_{\text{tri},i}$ appear. Then, the control signals $s_{a,i}$ and $s_{b,i}$ are generated by simple voltage comparators (open collector



(a)



(b)



(c)

Fig. 6. Imperfect ripple "cancellation" due to unequal dc-link voltages. (a) Total cell voltage $\sum u_{ab}$ and output voltage u_O for the ideal case (upper traces, $U_i/N = 25$ V) and for $U_1/N = 23$ V, $U_2/N = 27$ V, $U_3/N = U_4/N = 25$ V, $N = 4$ (lower traces); frequency components for (b) balanced and for (c) nonbalanced dc-link voltages; parameters the same as for Fig. 4.

type) which directly drive the LEDs of the isolation optocouplers.

Switch-mode amplifiers often are equipped with a simple open-loop PWM control if there do not exist high requirements regarding the output voltage quality. However, in this case, the damping of the *LC* output filter has to be guaranteed by the load.

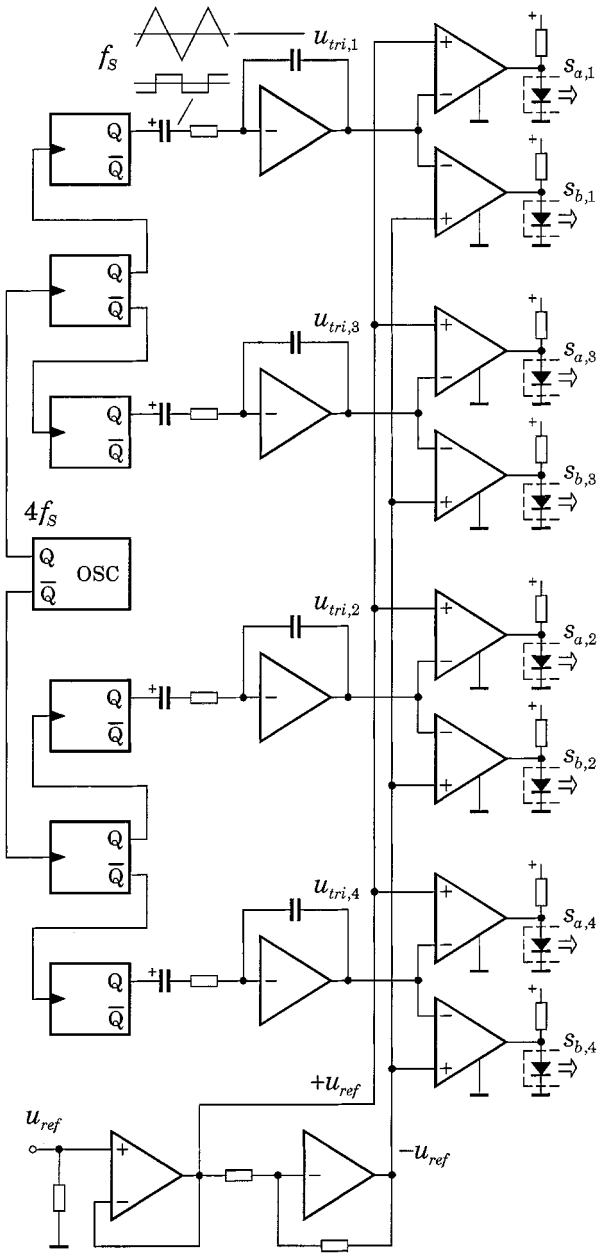


Fig. 7. Circuit diagram of the pulsewidth modulator for interleaved operating mode of four switching cells.

In the case of a pure resistive load R the characteristic impedance $Z_0 = \sqrt{L/C}$ of the filter has to be chosen correspondingly to get the desired transient response (e.g., $Z_0 = 2R$: critical damping, zero overshoot; $Z_0 = \sqrt{2}R$: Butterworth response, 4.3% overshoot; $Z_0 = R$: 16% overshoot). If, however, the load impedance is not well known and/or has no significant resistive component (e.g., an actuator for vibration testing systems) or is even of a nonlinear type (e.g., the input rectifier of a SMPS to be tested) this load-based damping of the *LC* filter may fail. Furthermore, in addition to the filter damping for no- or light-load operation it has also to be considered that real amplifier systems show nonlinear distortions due to the switching delays of the modulation and power circuitry (interlock delay) as well as due to time-varying dc-link voltages. These distortions can be reduced using closed-loop

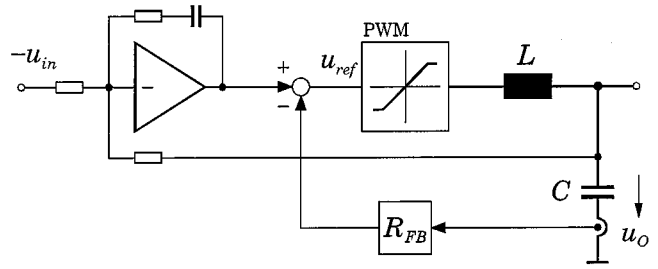


Fig. 8. Control-oriented circuit diagram of a switch-mode power amplifier with PI-type output voltage control and "pole splitting" using capacitor current feedback.

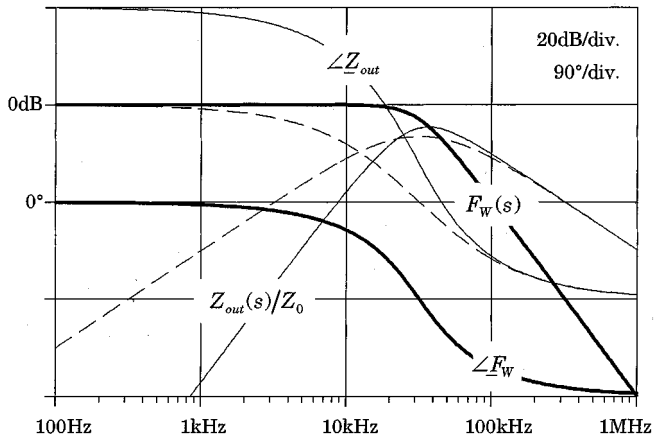


Fig. 9. Frequency response of transfer characteristic $F_W(s)$ and output impedance $Z_{\rm out}(s)$; the dashed curves indicate the output impedance without PI control.

control. The applied control concepts can be based on a direct measurement of the output voltage of the switch-mode unit (i.e., input voltage of the filter) to compensate for the interlock delay distortion. Alternatively, the filter itself can also be included into the feedback loop, which gives the possibility of an "active" damping of the *LC* filter.

Fig. 8 shows the control-oriented circuit diagram of a switch-mode power amplifier with direct output voltage control. To simplify the control of the second-order filter being inherently undamped, a feedback of the capacitor current is included first. Proper choice of the feedback coefficient R_{FB} leads to a pole split which consequently modifies the original −40 dB/decade transfer function

$$G_F(s) = \frac{U_O(s)}{U_{\rm ref}(s)} = \frac{1}{1 + s^2\,LC} \tag{7}$$

of the *LC* filter for $R_{FB} \geq 2Z_0$ to

$$G_F(s) = \frac{1}{1 + s\,kT} \cdot \frac{1}{1 + sT/k} \tag{8}$$

with $T = \sqrt{LC}$ and $R_{FB} = Z_0(1 + k^2)/k$ and, therefore, results in a region of first order roll-off for $1/(kT) \leq \omega \leq k/T$. The PI-type controller now is dimensioned such that it compensates the slower time constant of (8)

$$G_C(s) = \frac{1 + s\,kT}{s\,kT}. \tag{9}$$

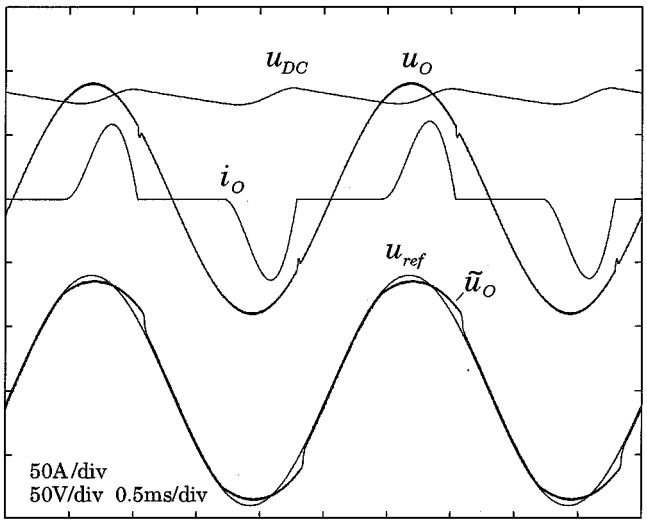


Fig. 10. Analysis of the control behavior (output voltage quality) for nonlinear amplifier load; load: full-bridge diode rectifier with capacitive smoothing and input inductor; $U_{\rm ref} = 90\ V_{pk}$, $f = 400$ Hz.

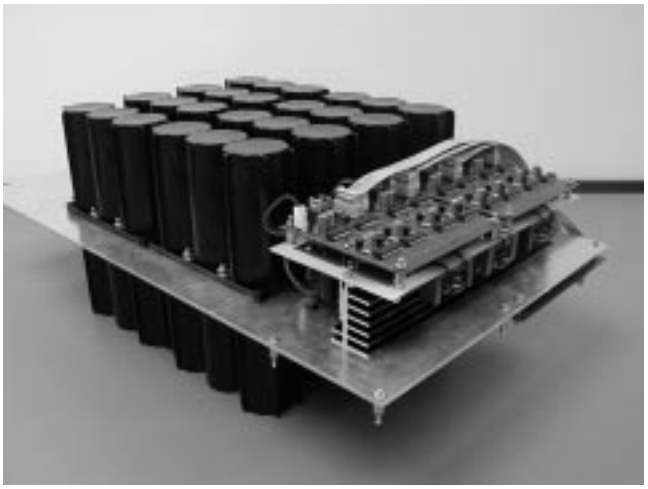


Fig. 11. "Flying-battery" amplifier laboratory setup.

With this, the total transfer function of the amplifier is calculated as

$$F_W(s) = \frac{U_{\rm in}(s)}{U_O(s)} = \frac{G_F(s)G_C(s)}{1 + G_F(s)G_C(s)} = \frac{1}{1 + s\,kT + s^2T^2}. \tag{10}$$

For $k = \sqrt{2}$, again, a Butterworth response is achieved (see Fig. 9) but now the distortions due to nonideal switching are reduced by the loop gain of the system. Furthermore, the PI controller also significantly improves the output impedance of the system which amounts to

$$Z_{\rm out}(s) = \frac{U_O(s)}{I_O(s)} = Z_0 \frac{s^2kT^2}{1 + s\,2kT + s^2(1 + k^2)T^2 + s^3kT^3}. \tag{11}$$

Especially for the lower signal frequency region $Z_{\rm out}$ results in considerably lower values than for open-loop operation or for the case that only R_{FB} feedback damping is applied (dashed curves of Fig. 9). In addition, the proposed control gives also a good output voltage quality for nonlinear loads, as indicated

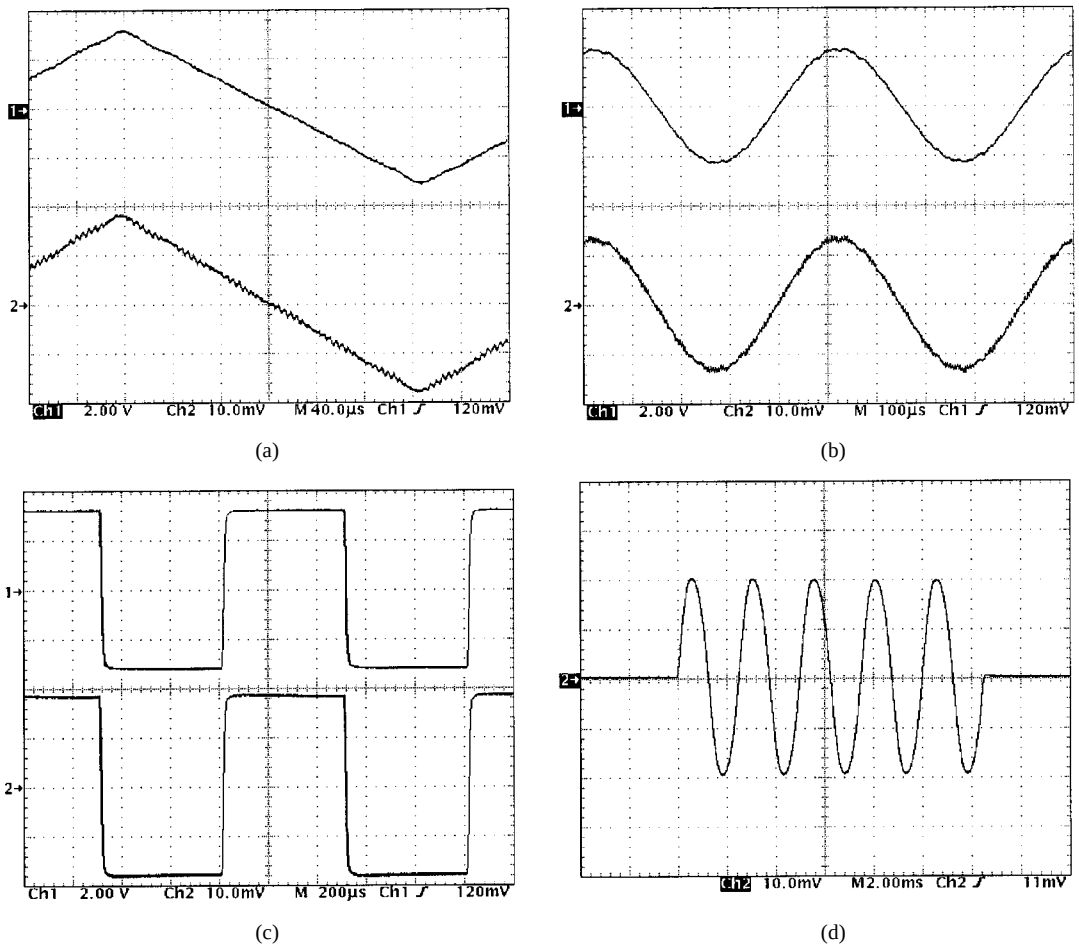


Fig. 12. Transient behavior of the proposed amplifier. (a)–(c) Upper traces: u_O (40 V/div); lower traces: i_L (10 A/div). (a) 2-kHz triangular response, 40 μs/div. (b) 2-kHz sine-wave response, 100 μs/div. (c) 1-kHz pulse response, 200 μs/div. (d) 400-Hz/100-A burst (i_O, 50 A/div, 2 ms/div).

by Fig. 10. Here, the output voltage u_O of the amplifier feeds a single-phase diode-bridge rectifier with capacitive smoothing (parameters: $C_{\rm DC} = 1000\ \mu$F, $R_{\rm DC} = 5\Omega$, $L_{\rm IN} = 50\ \mu$H). Without PI control, a much more distorted output voltage $\tilde{u}_O$ would result.

V. Laboratory Prototype

Based on the proposed concept, a laboratory setup of a "flying-battery" switch-mode power amplifier according to the following key specifications has been realized (see Fig. 11):

- output voltage—$u_O \approx \pm 100\ V_{\rm pk}$;
- nominal output current—$i_O = \pm 20$ A;
- nominal load—$R = 5\Omega$;
- switching frequency—$f_S = 25$ kHz;
- output filter—$L = 25\ \mu$H, $C = 1\ \mu$F;
- number of cells—$N = 4$;
- dc-link voltage—$U/N = 24$ V.

The system is equipped with 4×4 pieces 6-V/8-Ah Cyclon monoblock PLT batteries with 660-μF low-impedance electrolytic capacitors arranged in parallel to each battery block. For the power stage in total 16 pieces SiliconMAX PSMN005-55 trench MOSFET devices (nominal 55 V/75 A, $R_{DS,\rm on} < 6$ mΩ, TO220 case), eight IR2110 gate drive ICs, and eight optocouplers 6N137 for isolation are applied. The interleaved PWM generator consists of a CD4047 clock oscillator, three CD4013 dual flip-flops, a TL084 quad operational amplifier (integrator stages), and eight LM311 comparators according to Fig. 7. The control of the unit requires a second TL084 to implement the PI controller, the measurement of u_O (differential amplifier), and the sensing of the filter capacitor current according to Fig. 8 (R_{FB} feedback) using a small R10 ferrite-core current transformer. The whole PWM and control circuitry is realized using low-cost devices and fits on a single 160×100 mm printed circuit board.

The measured transient behavior of the amplifier system is given by Fig. 12. The detail of the filter inductor current of the triangle response shown in Fig. 12(a) demonstrates (in close accordance to the simulation results of Fig. 4 for $N = 4$) the several maxima/minima of the ripple amplitude within the full modulation range. As is indicated by Figs. 12(b) and (c), the amplifier shows a very good dynamic performance which primarily is defined by the Butterworth characteristic of the LC output filter in connection with the PI controller as described in Section IV. It has to be noted that, contrary to conventional class-D switch-mode amplifiers, the cutoff frequency f_0 of the applied LC filter is higher than the switching frequency of the power semiconductor devices ($f_0 = 31.8$ kHz, $f_S = 25$ kHz). Despite the fact that $f_S < f_0$ is valid, no output voltage ripple of significant amplitude occurs. Finally, probably the most essential advantage of the "flying-battery" amplifier concept, the generation of short-time output signals of a very high energy level shall be demonstrated. Fig. 12(d) shows a 400-Hz sine-wave load cur-

rent burst with an amplitude of $\approx 100\ A_{\mathrm{pk}}$. Here, the amplifier (connected to 12-A single-phase wall outlet) feeds a power burst output of 10-kW amplitude into the load.

VI. Conclusions

The proposed multicell multilevel topology allows the design of high-quality switch-mode power amplifiers. Due to the interleaved PWM control of the individual switching cells, the output voltage ripple of the total system is considerably small. Therefore, only a small output filter is required to suppress the switching frequency harmonics. Consequently, the system shows an excellent transient response and a good output impedance characteristic, especially if the output filter is included in the feedback control. Extending the basic multicell topology to the "flying-battery" concept, the peak current capability of modern low-voltage power MOSFETs in connection with the low inner impedance of rechargeable batteries gives a very interesting possibility for the generation of high-energy short-time testing signals. As compared to the achievable technical specifications the realization effort and cost are comparatively low. Using three amplifier units would allow short-time tests of three-phase equipment (e.g., active rectifier systems) at higher power levels operated from a single-phase supply mains for battery charging. However, the experiences gained from the prototype system also confirm that for a "flying-battery" amplifier system an effective battery management/charging system is required for equalizing the charging states of the single cells. Finally, it should be mentioned that the "flying-battery" multicell concept with its high peak current capability also would be well applicable to uninterruptable ac power supply systems (e.g., for short-time computer backup).

References

[1] G. B. Yundt, "Series- or parallel-connected composite amplifiers," *IEEE Trans. Power Electron.*, vol. 1, pp. 48–54, Jan. 1986.

[2] H. Ertl, J. W. Kolar, and F. C. Zach, "Basic considerations and topologies of switched-mode assisted linear power amplifiers," *IEEE Trans. Ind. Electron.*, vol. 44, pp. 116–122, Feb. 1997.

[3] N. S. Jung, N. I. Kim, and G. H. Cho, "A new high-efficiency and super-fidelity analog audio amplifier with the aid of digital switching amplifier: Class K amplifier," in *Proc. IEEE PESC'98*, vol. 1, 1998, pp. 457–463.

[4] A. Ginart, W. M. Leach, R. M. Bass, T. Habetler, and K. Gray, "Analysis of the class AD audio amplifier including hysteresis effects," in *Proc. IEEE APEC*, vol. 2, 2000, pp. 1095–1101.

[5] H. Ertl, J. W. Kolar, and F. C. Zach, "A new 1 kW Class-D supported linear power amplifier employing a self-adjusting ripple cancellation scheme," in *Proc. Power Electronics and Intelligent Motion Conf. (PCIM'96)*, Nürnberg, Germany, May 1996, pp. 265–274.

[6] ——, "A novel switch-mode power amplifier with high output voltage quality employing a hybrid output voltage filter," in *Proc. Power Electronics and Intelligent Motion Conf. (PCIM'97)*, Nürnberg, Germany, June 1997, pp. 419–428.

[7] J. Pforr, "Switch-mode current amplifier with high output current quality employing an active output filter," in *Proc. Power Electronics and Intelligent Motion Conf. (PCIM'99)*, Nürnberg, Germany, June 22–24, 1999, pp. 279–284.

[8] G. R. Stanley and K. M. Bradshaw, "Precision DC-to-AC power conversion by optimization of the output current waveform—The half-bridge revisited," in *Proc. IEEE PESC'97*, vol. 2, 1997, pp. 993–999.

[9] Y. Liang and C. O. Nwankpa, "A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 1118–1123, Sept. 1999.

[10] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static var generation," *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 1130–1138, Sept. 1996.

[11] A. Rufer, M. Veenstra, and K. Gopakumar, "Asymmetric multilevel converter for high resolution voltage phasor generation," in *Proc. 8th European Conf. on Power Elctronics and Applications (EPE)*, Lausanne, Switzerland, Sept. 7–9, 1999, CD-ROM.

[12] H. Ertl, J. W. Kolar, and F. C. Zach, "A novel multi-cell dc-ac converter for applications in renewable energy systems," *IEEE Trans. Ind. Electron.*, to be published.

[13] K. Jana, "Charging pure lead-tin batteries," Hawker Energy Products Inc, Warrensburg, MO, 1st ed., Mar. 1999.

Hans Ertl (M'93) was born in Mauerkirchen, Austria, in 1957. He received the Dipl.-Ing. (M.Sc.) and Ph.D. degrees in industrial electronics from the University of Technology Vienna, Vienna, Austria, in 1984 and 1991, respectively.

Since 1984, he has been with the University of Technology Vienna, where he is currently an Assistant Professor in the Power Electronics Section. He has performed various industrial research projects in the areas of field-oriented control of ac drive systems, switch-mode power supplies for welding and industrial plasma processes, and active rectifier systems. He is the author or coauthor of numerous scientific papers and patents. His current research activities are focused on switch-mode power amplifiers and multicell topologies, in particular, for the generation of testing signals, for active ripple current compensators, and for several applications in the area of renewable energy systems.

Johann W. Kolar (M'89) was born in Vöcklabruck, Austria, in 1959. He received the Ph.D. degree (*summa cum laude*) in industrial electronics from the University of Technology Vienna, Vienna, Austria, in 1998.

Since 1984, he has been with the University of Technology in Vienna, where he has been teaching and conducting research in close collaboration with the industry in the fields of high-performance drives, high-frequency inverter systems for process technology, and uninterruptible power supplies. He has proposed numerous novel converter topologies, e.g., the Vienna rectifier concept. He has authored more than 100 scientific papers published in international journals and conference proceedings and has filed 45 patents. He was appointed as a Professor at the Swiss Federal Institute of Technology (ETH) Zurich, Zurich Switzerland, in 2001. He is also currently the Head of the Power Electronics Systems Laboratory. The focus of his current research is on novel converter topologies with low effects on the mains, e.g., for power supply of telecommunication systems and distributed power systems in connection with fuel cells. A further main area of research is the realization of ultracompact intelligent converter modules employing the latest power semiconductor technology (SiC) and novel concepts for cooling and EMC filtering. He is a member of the technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion).

Dr. Kolar is a member of the Institute of Electrical Engineers of Japan. Since 1997, he has served as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

Franz C. Zach (M'83) was born in Vienna, Austria, in 1942. He received the Dipl.-Ing. (M.Sc.) degree in electrical engineering (telecommunications) and the Ph.D. degree (*cum laude*) in the area of automatic control optimization from the University of Technology Vienna, Vienna, Austria, in 1965 and 1968, respectively.

From 1965 to 1969, he was a Scientific Assistant with the University of Technology Vienna and, from 1969 to 1972, he was with the NASA Goddard Space Flight Center, Greenbelt, MD, where he developed new optimization methods for attitude control of earth-orbiting satellites. In 1972, he became an Associate Professor and then Professor of Power Electronics at the University of Technology Vienna, where he has headed the Power Electronics Section since 1974. He is the author of numerous technical and scientific papers and patents and of two books concerning automatic control and power electronics. His current activities are in the area of power electronics and associated controls, in particular, as used for power supplies and electrical drives.