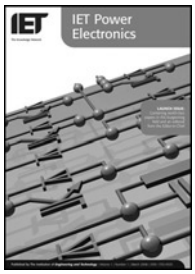
Published in IET Power Electronics
Received on 11th September 2007
Revised on 20th December 2007
doi: 10.1049/iet-pel:20070390



ISSN 1755-4535

Active voltage balancing of DC-link electrolytic capacitors

H. Ertl[1] *T. Wiesinger*[1] *J.W. Kolar*[2]

[1]*Institute of Electrical Drives and Machines, Power Electronics Section, Vienna University of Technology, Gusshausstrasse 27, Vienna A-1040, Austria*
[2]*Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, ETH Zentrum, ETL 22, Zurich CH-8092, Switzerland*
E-mail: j.ertl@tuwien.ac.at

Abstract: DC voltage links of three-phase power converters are frequently equipped with a series connection of two electrolytic capacitors because of high voltage level. For such a configuration, usually resistors have to be arranged in parallel to each capacitor in order to balance the partial voltages. These balancing resistors, however, have to be dimensioned regarding the worst-case scenario of capacitor's leakage currents; such leakage can lead to high permanent dissipative losses that also appear in case of low actual leakage currents. To avoid these losses to a very large extent, a novel low-cost and robust active unit for replacing the passive balancing resistors is introduced. The paper describes the operating principle of the circuit, analyses the fundamental relationships relevant for the balancing characteristic and gives guidelines concerning component selection. Furthermore, simulation results as well as measurements taken from a laboratory prototype are presented.

1 Introduction

DC voltage links of power electronic converters connected to the 400/500 V three-phase mains, for example, for AC drive systems (Fig. 1*a*), for welding converters or telecom switch-mode power supplies etc., are frequently equipped with a series arrangement of two electrolytic capacitors. The reason for the series connection is that electrolytic capacitors at present are available with maximum voltage ratings of only up to $\simeq$500 V. The DC-link voltage level of the converters mentioned (being typically $U_D \simeq 500\cdots800$ V) therefore precludes the application of a single capacitor device. Electrolytic capacitors unfortunately show a significant leakage current which may vary in a wide region dependent on the operating and ageing conditions of the device [1–3]. To guarantee a uniform distribution of U_D to both capacitors C_1 and C_2 (i.e. $U_{C1} \simeq U_{C2} \simeq U_D/2$), the manufacturers usually strictly recommend the application of balancing resistors R_B connected in parallel to each capacitor [4, 5]. As will be discussed in Section 2 these resistors cause high dissipative losses, especially if they are dimensioned to cover full-range capacitor worst-case leakage. If the converter is permanently connected to the mains (as often is the case in the industrial automation field), these balancing losses sum up to considerable additional energy costs during the operating life of the unit. Furthermore, it should be noted that simple low-cost balancing resistors often are located close to the capacitors and not mounted on the converter's main cooler. Hence the balancing losses will heat-up the capacitors and/or the surrounding electronic equipment (e.g. gate drive, control, current sensors etc.) inside the converter's cabinet.

To avoid the drawbacks of the passive voltage balancing mentioned before, alternative concepts have been reported in the literature. In [6], a circuit has been proposed consisting of a centre-tapped auto-transformer connected to the line-to-line mains voltage with an ohmic balancing resistor located between the centre tap of the transformer and the

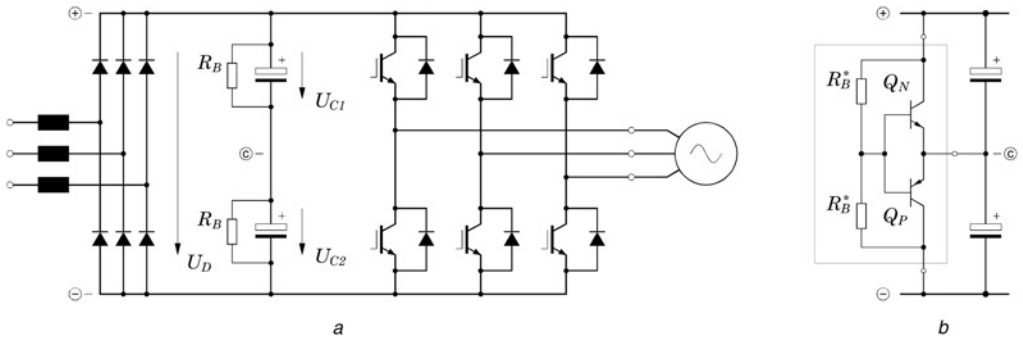


Figure 1 *Circuit topology of a three-phase power converter (e.g. AC drive system) using a series connection of two electrolytic capacitors to form the DC voltage link*

a Passive voltage balancing by two resistors R_B
b Basic circuit diagram of the proposed active voltage balancing consisting of a high-impedance voltage divider and a complementary emitter–follower

centre point of the DC-link capacitors. The transformer acts as a non-dissipative voltage divider; however, its output voltage not ideally matches the behaviour of the basic resistor voltage divider. Hence, a resulting AC current flow into the capacitors appears resulting in small permanent losses. Furthermore, the balancing feature is linked to an existing symmetric AC mains.

Also known by literature are systems where the capacitor balancing is based on a specific topology or arrangement of a switch-mode power supply (SMPS), for example, for providing the housekeeping power of the drive inverter. In [7–9], modified fly-back SPMS have been proposed which inherently balance their input voltage. However, fly-back converters, in general, are not optimal for higher input voltage levels and usually also show a rather low efficiency. The concept of a series arrangement of SMPS cells, however, can also be extended to forward converters [10–13] as well as to resonant concepts. In [14], an SMPS topology especially suited for high input voltages has been reported consisting of self-oscillating series-resonant converter cells. This structure – which is based on the input-serial/output-parallel converter concept [15, 16] – inherently equalises the voltages of the series-connected input capacitors. Furthermore, the capacitor voltage balancing problem is common to all multilevel (ML) inverter topologies. Numerous scientific papers on ML-inverters are, therefore, focused to active voltage balancing based on specific modulation strategies (e.g. [17–21] for diode-clamped ML topologies, [22–26] for capacitor-clamped ML topologies and [27–30] for cascaded H-bridge circuits). Additionally, active balancing has also been proposed for sinusoidal input current three-phase rectifiers [31, 32].

All modulation-based SMPS- or ML-converter balancing techniques mentioned before, however, may require large amount of load current or a specific load condition to guarantee the balancing property and may fail in case of stand-by operation or in case of a converter failure and hence do not fully give the robustness of a dedicated balancing unit. As a consequence, a novel simple, autonomous and robust active balancing scheme is introduced and discussed in Section 3. The basic idea of the novel method (cf. Fig. 1*b*) is that the connection point 'C' of the two DC-link capacitors is stabilised to $U_D/2$ using a high-impedance voltage divider (R_B^*) and a subsequent complementary emitter-follower stage (Q_N, Q_P). With this the losses can be lowered significantly, because the voltage divider quiescent current now can be reduced concerning the current gain of the transistors. Section 4 gives an advantageous realisation of an active balancing unit using a voltage-follower topology formed by a cascode array of low-cost small-signal low-voltage bipolar transistors. Section 5 presents measurements taken from a laboratory breadboard circuit and also gives a further realisation of the proposed basic concept relying on a cascode array of power MOSFETs.

2 Passive voltage balancing

For passive balancing, the two resistors R_B form a voltage divider and a perfect voltage distribution $U_{C1} = U_{C2}$ would be valid in case of zero output current $\Delta I = 0$ (Fig. 2). ΔI, however, is defined by the leakage current difference $I_{l,C1} - I_{l,C2}$ of the DC-link capacitors. This leads to the consequence that for practical applications, R_B has to be selected such

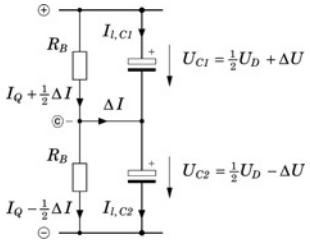


Figure 2 *Passive voltage balancing network*

doi: 10.1049/iet-pel:20070390

that the expected leakage current difference is small as compared with the voltage divider's quiescent current I_Q in order to achieve a good voltage equalisation $U_{C1} \simeq U_{C2} \simeq U_D/2$ (i.e. a voltage deviation $\Delta U \rightarrow 0$). Here, the most significant drawback of the passive voltage balancing becomes obvious: the quiescent current – which determines the dissipative losses – has to be a multiple of the worst-case leakage difference of the capacitors, and also if the actual value of ΔI is much smaller (or even $\Delta I \rightarrow 0$ is valid), considerable losses remain permanent.

Using the output resistance $R_B/2$ of the voltage divider, the capacitor voltage deviation calculates to $\Delta U = \Delta I \cdot R_B/2$; normalisation by the nominal voltage $U_D/2$ of the capacitors leads to

$$\Delta u = \frac{\Delta U}{(1/2)U_D} = \frac{\Delta I \cdot (1/2)R_B}{I_Q \cdot R_B} = \frac{1}{2}\frac{\Delta I}{I_Q} \qquad (1)$$

Consequently, if the capacitor voltages are balanced to, for example, typically $\Delta u \leq \pm 10\%$, a quiescent current of $I_Q \geq 5 \cdot \Delta I$ has to be chosen. Using (1), the total losses of the two balancing resistors ('balancing losses') sum up to

$$P_B = \underbrace{2R_B \cdot I_Q^2}_{P_Q} + \frac{R_B}{2} \cdot \Delta I^2 = P_Q \cdot [1 + \Delta u^2] \qquad (2)$$

For relevant values $\Delta u < 0.1$, the balancing losses therefore are dominated by the quiescent current losses $P_B \simeq P_Q$.

2.1 Capacitor leakage current

Causally related to the electro-chemical principle of electrolytic capacitors, the leakage current is largely dependent on operating, temperature and ageing conditions of the component. It should be noted, for example, that if the capacitor voltage is carefully increased to values higher than the specified surge voltage, the 'leakage' current increases rapidly because the reforming process (growing of the oxide layer) begins again [4]. Furthermore, at normal operation conditions (voltages below the surge level), the leakage current may be much higher than the specified data sheet value for the first minutes after the voltage is applied ('inrush current'). This is especially true after a longer period of voltage-free storage of the component (oxide layer deterioration). But also the regular operation leakage current approximately doubles its value for each 20 °C temperature increase. In Fig. 3, the specified typical operating leakage current $I_{l,op}$ and the guaranteed maximum leakage current $I_{l,max}$ (according to the 'acceptance test' of standard EN 1 30 300) are shown for a specific power electrolytic capacitor series (valid for 20 °C; for 35 °C this permissible limit has to be multiplied by a factor of 2.5!).

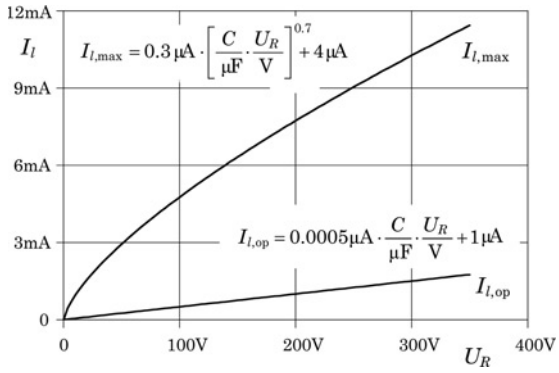


Figure 3 *Typical and maximum leakage currents of a LL-grade electrolytic capacitor series (according to [4]) in dependency on the rated capacitor voltage U_R, valid for 20°C*

2.2 Design example

To give an example for the dimensioning of a passive balancing network, it should be assumed that the 500 V DC voltage link of a 10 kVA AC drive system according to Fig. 1 is equipped with two 10 000 μF/350 V capacitors (e.g. EPCOS type B 43 564). The leakage current of this component for the relevant capacitor operating voltage (cf. Fig. 3, $U_R \simeq 250$ V) is in the range between $I_{l,op} \simeq 1.3$ mA (typical) and $I_{l,max} \simeq 9$ mA. Considering the fact that the output current ΔI of the balancing network is formed by the leakage current difference of the two capacitors, but on the other hand, the values given before are valid for 20 °C only, a worst-case value of $\Delta I = 5 \cdots 10$ mA will be assumed. Choosing $I_Q = 10 \cdots 5 \cdot \Delta I$ leads to a quiescent current of $I_Q = 50$ mA which will limit [using (1)] the centre point voltage deviation to $\Delta u \leq 5\%$. Now the resistance value of the balancing resistors can simply be calculated to $R_B = U_C/I_Q = 250\,V/50\,mA = 5\,k\Omega$.

The calculated dimensioning very closely coincides with a guideline frequently given by the manufacturers. In the data sheets or application recommendations (e.g. [4] or [5]), it is specified that the balancing resistors will be calculated using the relation $R_B \cdot C \simeq 50\,s = T_B$. For the case at hand, this again leads to $R_B = 5\,k\Omega$.

Remark: The relation used before also implies that the balancing process $\Delta U \rightarrow 0$ of the (first-order) system shows a time constant of T_B. If the capacitors are charged up to $\Delta u = \pm 20\%$ at the power-up of the converter (e.g. caused by ±20% different capacitance values), it will take ~3 min until $\Delta U \rightarrow 0$ is valid!

doi: 10.1049/iet-pel:20070390

A quiescent current of $I_Q = 50$ mA at $U_D \simeq 500$ V will result in balancing losses of $P_B = 25$ W. If the converter is permanently powered by the mains, these losses will sum up to a energy consumption of $\sim$220 kWh per year! Considering the product life cycle of the converter, the balancing energy costs are many times higher than the costs of the passive balancing network itself. This suggests the development of an advanced balancing method.

3 Active balancing: basic concept

The basic idea of the proposed active balancing is to separate the dimensioning of the voltage divider's quiescent current from the capacitor's leakage current. In an optimal case, the voltage divider only would define the potential of the centre point 'C' to $U_C = U_D/2$ acting as the input reference level of an idealised voltage follower stage (Fig. 4*a*). With this, $R_B^* \rightarrow \infty$, $I_Q^* \rightarrow 0$ would be possible and the balancing losses (appearing in the output stage of the amplifier) now are determined only by the actual leakage current difference and not by worst-case conditions as this is true for the passive balancing network.

Unfortunately, a realisation according to the operation principle shown in Fig. 4*a* is not adequate because a high-voltage operational amplifier would be required which is expensive and itself, in general, shows noticeable quiescent power losses. On the other hand, the excellent balancing accuracy that would be achievable with this circuit is not required for practical applications. Therefore the operational amplifier with direct voltage feedback can be replaced (as already anticipated in Fig. 1*b*) by a simple emitter–follower stage consisting of two complementary bipolar transistors (Fig. 4*b*). Although the ideal case $I_Q^* \rightarrow 0$ now is not valid any more, the losses can be considerably reduced because a much lower quiescent current as compared with the passive case is possible considering the current gain β of the transistors $\Delta I \rightarrow \Delta I/\beta$. Neglecting the losses of the voltage divider itself (i.e. $I_Q^* \rightarrow 0$, $\beta \rightarrow \infty$), the losses of the active balancing are calculated as

$$P_B^* = \frac{1}{2} U_D \Delta I \tag{3}$$

As demonstrated in Fig. 5, for the dimensioning example of Section 2, these losses are by far lower in comparison to the passive balancing method [cf. also (2) with (3)]. Furthermore, the active circuit also gives a much stiffer balancing characteristic ($U_{C1} = U_{C2} = U_D/2$ for the idealised case $\beta \rightarrow \infty$).

For realisation of the emitter–follower bipolar transistors with a rated collector–emitter voltage of at least $U_D/2$ are required. Considering DC-link overvoltages, unbalanced operating conditions and safety margins, at least 400...500 V semiconductor devices are required in practice for a DC link with 500 V nominal voltage. However, high-voltage bipolar transistors are characterised by a comparatively low β because of their wide effective base region. General-purpose 400 V NPN-/PNP-transistor pairs (e.g. MPSA44/MPSA94) show a current gain of being typically only $\beta \simeq 40$ and therefore are not well suited for the proposed concept. Although 'high-gain' high-voltage bipolar transistor pairs are available in the 400 V region (e.g. ZETEX ZTX458/ZTX558, $\beta \simeq 200$ [33]), it has to be considered that the transistor types mentioned before are 'low-power' devices limited to typ. $P \leq 1$ W. In the case of, for

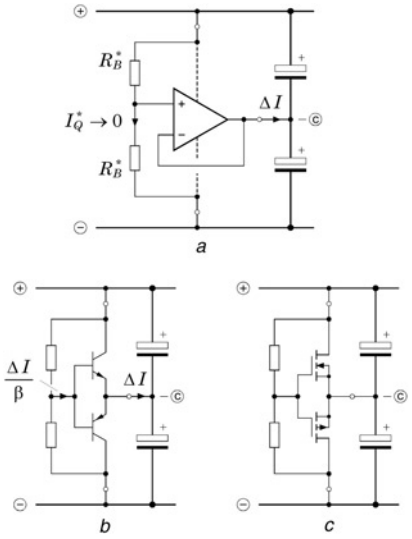


Figure 4 *Basic realisation of active voltage balancing using:*
a High-voltage operational amplifier
b Bipolar emitter–follower
c MOSFET source–follower

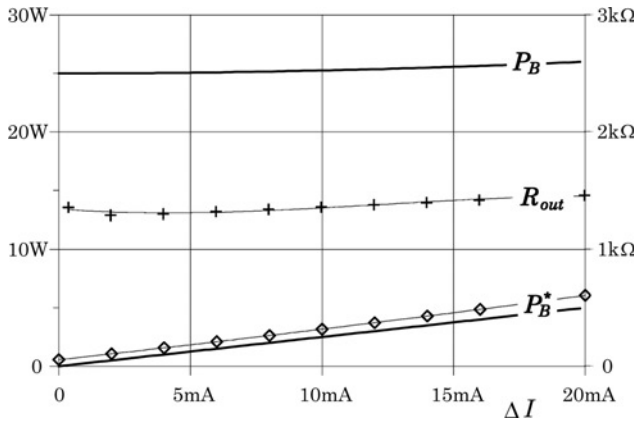


Figure 5 *Losses of the passive (P_B) and of the active (P_B^*) balancing; marked curves: simulation results: losses including quiescent losses and output resistance (cf. sections 4 and 5)*

doi: 10.1049/iet-pel:20070390

example $\Delta I > 4$ mA, these elements would be thermally overloaded. On the other hand, real high-voltage bipolar power transistors are hardly available as complementary pairs or show very low current gain.

4 Active balancing: cascode topology

To avoid the drawbacks mentioned before, an active balancing unit using a cascode circuit topology as shown in Fig. 6*a* is proposed. The splitting up of the voltage divider resistor $R_B{}^*$ into n equal partial resistors R makes possible to replace the high-voltage transistor by a 'chain' of general-purpose low-voltage small-signal transistors. This is of significant importance because these components are available as high-gain devices (e.g. the low-cost SMD transistors BC850C/BC860C are specified to $\beta \simeq 600 \cdots 800$), and therefore allow a high-impedance dimensioning of the voltage divider network resulting in low quiescent losses. Because of the limited voltage capability of the semiconductors (e.g. $U_{CEO} = 45$ V), typically $n = 10 \cdots 15$ transistors will be required for a 500 V DC link. With this, also the handling of the resulting power loss [e.g. in total $P_B \simeq 2.5$ W for $\Delta I = 10$ mA according to (3) or Fig. 5] does not cause serious problems, because the losses are distributed to several components and for each transistor only $\simeq$200 mW will appear, being well tolerable even for SMD components. Because of the large number of active and passive components, high costs might be expected. However, the transistors and also the resistors (0805 SMD chip type) are widely used ultra-low-cost components. The cost of the total circuit including the PCB therefore is very similar to the two power resistors of the passive balancing.

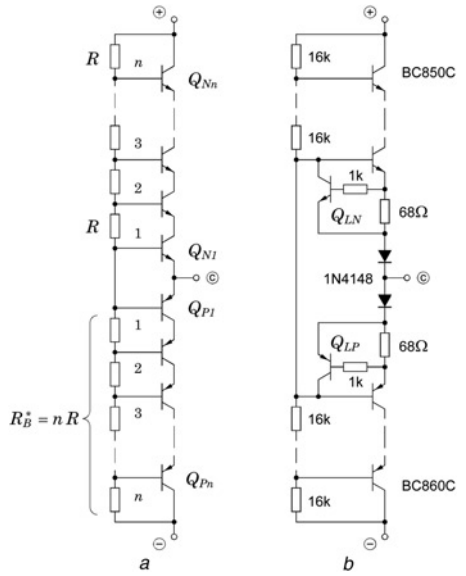


Figure 6 *Active balancing unit*

a Cascode arrangement of low-voltage small-signal transistors
b Extension of basic circuit for current limitation of ΔI

4.1 Output resistance

To minimise the quiescent losses, the resistance value of the voltage divider should be chosen as high as possible. However, this worsens the output resistance R_{out} of the total circuit which determines the balancing characteristic of the system. This characteristic should be better (i.e. a lower R_{out}-value) than the passive solution in order to achieve a stiffer centre point voltage. The output resistance of the passive balancing system is given by $R_{out} = R_B/2$, whereas for the simple active system (Fig. 4*b*), $R_{out}{}^* = R_B{}^*/(2\beta)$ would be valid. The calculation of the output resistance of the proposed cascode topology is more difficult and should be performed based on the equivalent circuit shown in Fig. 7. Starting at the output side (centre point 'C') with a given voltage U and a balancing current ΔI, the ith transistor stage contributes a collector-base voltage of $U/n + i \cdot R \cdot \Delta I/\beta$. With this, according to Fig. 7, the relation

$$U_D = U + \sum_{i=1}^{n}\left[\frac{U}{n} + i\frac{\Delta I}{\beta}R\right] = 2U + \frac{\Delta I}{\beta}R \cdot \sum_{i=1}^{n} i \tag{4}$$

is valid. (For the sake of brevity, the base-emitter voltage drop will be neglected and it will be assumed that all transistors show equal current gain β). Calculating Σi and rearranging (4) finally leads to the

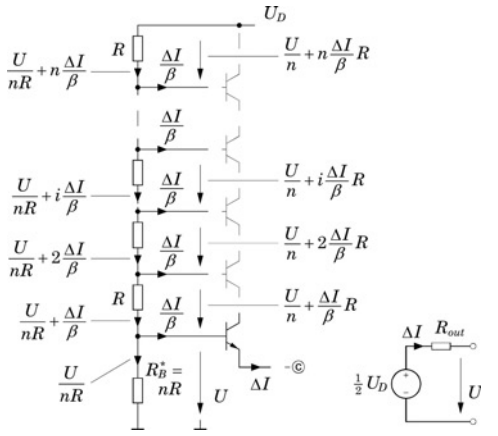


Figure 7 *Equivalent circuit diagram for calculating the output resistance R_{out} of the cascode topology (valid for $\Delta I > 0$)*

doi: 10.1049/iet-pel:20070390

output behaviour of the system

$$U = \frac{1}{2}U_D - \Delta I \cdot \underbrace{\frac{R}{\beta} \cdot \frac{n(n+1)}{4}}_{R_{out}} \tag{5}$$

and hence the output resistance results in

$$R_{out} = \frac{R}{\beta} \cdot \frac{n(n+1)}{4} = \frac{R_B^*}{\beta} \cdot \frac{n+1}{4} \tag{6}$$

It should be noted that according to (6) for a given value of R_B^* [which defines the quiescent losses $P_Q = U_D^2/(2R_B^*)$], the value of R_{out} worsens for increasing n. Therefore to give a good balancing performance, the number of cascode stages should be not too high considering the voltage and power limitations of the transistors.

5 Laboratory prototype

On the basis of the analyses described in the previous section, a prototype system has been realised to compete with the passive balancing method described in Section 2 using two 5 kΩ resistors. As mentioned, the assumed maximum balancing current of $\Delta I = 10$ mA leads to total balancing losses of $P_B = 25$ W for the passive solution. Considering the power limitations of BC850C/BC860C and guaranteeing a reliable operating voltage margin even in case of an output short circuit 2 × 15 cascode stages have been chosen ($n = 15$). Dimensioning the voltage divider resistors $R = 16$ kΩ (6) gives an output resistance of $R_{out} = 60 \cdot R/\beta = 1.37$ kΩ for $\beta \simeq 700$, which is significantly better in comparison to the 2.5 kΩ of the passive balancing resulting in a more precise voltage sharing. The selected voltage divider causes quiescent losses of $P_Q = U_D^2/(2nR) \simeq 0.5$ W (see also simulation results given in Fig. 5). In contrast to the 25 W losses of the passive solution, this value clearly demonstrates the advantage of the proposed method.

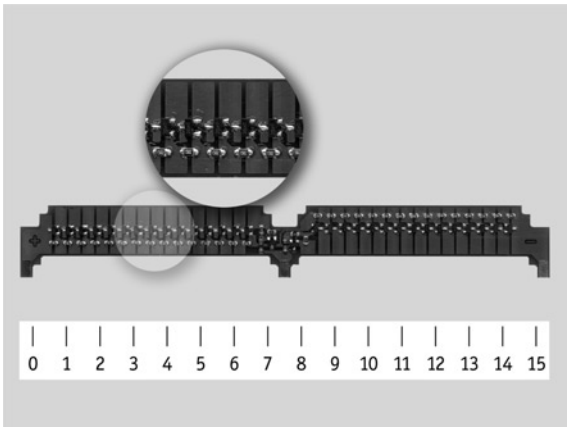


Figure 8 *Prototype of active balancing device (cm-scale)*

In order to reduce the heat dissipation of the transistors in case of a failure, the basic cascode circuit has been extended by a current limiter according to Fig. 6*b*. Using 68 Ω, current sensing resistors limit the output current to $\Delta I_{max} = U_{BE}/R_{sense} \simeq 700$ mV/68 Ω = 10 mA. As shown in Fig. 8, the whole system is realised on a small PCB stripe (size 155 × 20 mm, that is, the length is almost similar to the width of the two electrolytic capacitors 2 × 77 mmØ) using exclusively low-cost SMD components. The PCB stripe has three terminal fins (+/C/−) which can be soldered directly to the converter's main PCB board to replace the two passive balancing resistors.

In addition to the calculations presented in Section 4, the system has been checked further by a Spice simulation. As shown in Fig. 9, the output characteristic and the output resistance of the actual prototype system coincide very closely with the expected and simulated behaviour and with the output resistance calculated using (6) [cf. also the output resistance values gained by simulation (Fig. 5)]. The

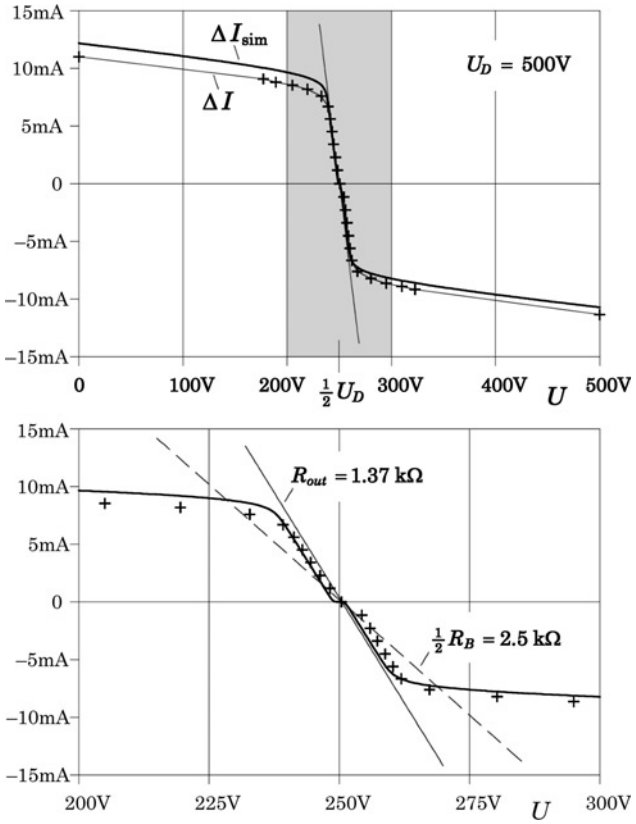


Figure 9 *Simulated and measured output characteristic ΔI(U) of the proposed system; the zoomed region (lower diagram) demonstrates the stiffer balancing behaviour of the active system (dashed line: passive resistor balancing)*

doi: 10.1049/iet-pel:20070390

transient behaviour of the proposed active concept in comparison to the passive resistor balancing is demonstrated in Fig. 10. At $t = t_0$, the respective balancing unit is activated pulling the capacitor voltage U_C to its stationary value $U_D/2$. The current consumption of the passive unit remains constant to $I_D = 50$ mA (25 W permanent losses), whereas I_D of the active unit almost disappears for $U_C \rightarrow U_D/2$.

During the measurements, a further advantage of the system became obvious: the cascode structure shows a remarkable balancing precision being by far better than the balancing precision of a passive solution. For a passive balancing unit few power resistors are available with precision ratings $> \pm 5 \cdots \pm 10\%$, resulting in a balancing accuracy of equal value. The resistors of the voltage divider network of the cascode balancing, however, usually are of $\pm 1\%$ precision, even in the case when low-cost components are used. Furthermore, due to the fact that the $2n$ components statistically cancel out their resistance errors, an even better balancing accuracy could be observed. For example, for $U_D = 500.0$ V, the no-load output voltage of the prototype has been measured to 249.7 V, that is, an error of only 0.12% is present. Nevertheless, the component costs of the active balancing unit assuming mass production are estimated to be 1...2€ and therefore in the region of a passive resistor solution.

5.1 MOSFET balancing unit

A second laboratory unit has been built for the balancing of the DC link of a high-power inverter. For this application, the balancing currents which can be achieved by small-signal bipolar transistors are not

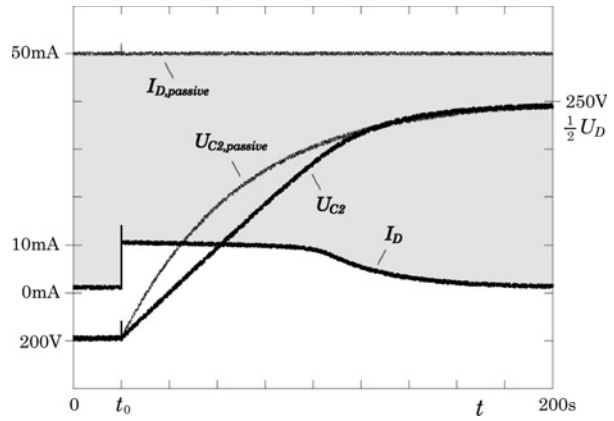


Figure 10 *Transient behaviour of the proposed active concept compared with passive resistor balancing*

Parameters: $C_1 = C_2 = 10$ mF, $U_D = 500$ V, $U_{C1,0} = 300$ V, $U_{C2,0} = 200$ V, $R_B = 5$ kΩ; balancing activated at $t_0 = 20$ s; the current I_D (which the balancing unit draws out of the DC link) represents the balancing losses, the shaded area depicts to the energy which can be saved by application of the proposed concept

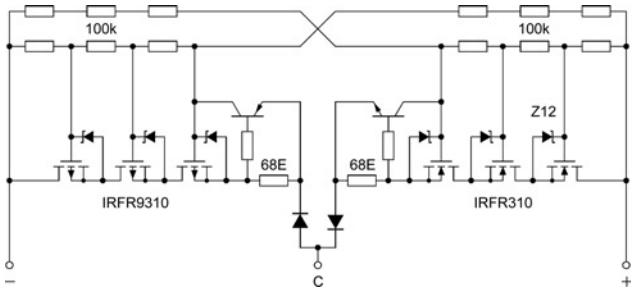


Figure 11 *Active balancing unit based on a cascode arrangement of power MOSFETs (here: 2 × 3 transistor unit)*

sufficient because of the limited maximum power dissipation of the SMD-transistor devices mounted on a simple FR4-board. To improve the thermal conditions, the basic cascode concept has been applied to MOSFETs (cf. Fig. 11). Because complementary power MOSFETs for linear operation are available up to typ. 400 V, a cascode arrangement of 3...4 transistor pairs is sufficient. The D-PAK transistor case gives a much better thermal behaviour as compared with small-signal transistors. To further improve the cooling, the MOSFETs are mounted on a ceramic hybrid module (Fig. 12). Owing to the limited manufacturing size of the ceramic carrier (limited here to 3 × 5 cm), the total balancing unit has been split up to two modules (each carrying four MOSFETS). The layout of the module has been drawn such that, the p- and n-channel transistors are 'shared', that is, each module contains two p-channel and two n-channel MOSFETs. With this, the dissipated power (actually appearing only in the n-channel or p-channel devices) can be distributed equally to both ceramic substrates. Furthermore, the layout has been done in a way that the total balancing unit can be built up using two identical ceramic

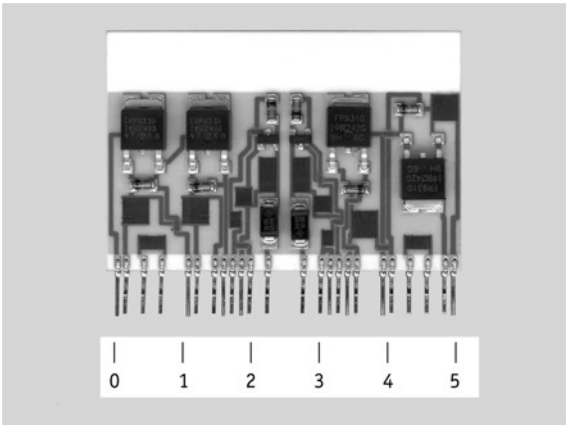


Figure 12 *Prototype of the MOSFET-based balancing module (cm-scale) shown: single module of a 2 × 4 transistor unit)*

doi: 10.1049/iet-pel:20070390

modules (showing different interconnections, however) which reduces the manufacturing costs.

6 Conclusion

The active concept introduced in this paper is a very attractive method for the voltage balancing of series-connected electrolytic capacitors. The proposed circuit advantageously substitutes the commonly used passive balancing resistors of DC voltage link converters. The active system that is preferably realised by the application of a cascode voltage-follower topology is characterised by the following features as compared with the passive resistor balancing.

- Significant reduction of balancing losses resulting in huge savings of energy cost considering the converter's life cycle.
- Stiffer balancing behaviour (reduced output resistance).
- Increased stationary balancing precision.
- Low cost (similar to passive solution).

Finally, the single property known so far that might be seen as a minor drawback should be mentioned. The proposed system is not very suited to safely discharge the DC voltage link after the power converter has been switched off. However, alternative discharge paths are often present: for example, the main load of the converter itself or its auxiliary power supply which, more and more, is realised using a small DC/DC converter fed by the main DC voltage link.

7 Acknowledgment

The authors are very much indebted to the Austrian Science Fund (FWF) for the support of this research project.

8 References

[1] ALWITT R.S., HILLS R.G.: 'The chemistry of failure of aluminum electrolytic capacitors'. Proc. 3rd Annual Symp. Physics of Failure in Electronics, Chicago, IL, September 1964, pp. 93–107

[2] GREASON W.D., CRITCHLEY J.: 'Shelf-life evaluation of aluminum electrolytic capacitors', *IEEE Trans. Compon. Hybrids Manuf. Technol.*, 1986, **9**, (3), pp. 293–299

[3] PERISSE F., VENET P., ROJAT G., RÉTIF J.M.: 'Simple model of an electrolytic capacitor taking into account the temperature and ageing time', *Electr. Eng. (Arch. Elektrotech.)*, 2006, **88**, (2), pp. 89–95

[4] EPCOS Corp: 'Electrolytic capacitors – general technical information', December 2006, available via www.epcos.com, included also in Aluminum Electrolytic Capacitors Data Book, ed. 12/2006

[5] EVOX-RIFA Corp: 'Electrolytic capacitors application guide', available at: http://www.evoxrifa.com/europe/technotes_electrolytics.htm, accessed on September 2007

[6] EDWARDS CH.W.: 'Low-dissipation capacitor voltage sharing circuit for a static AC/DC converter'. US Patent US 4 686 619, August 1986

[7] KOLAR J.W., ERTL H.: 'Gleichspannungs-Gleichspannungs-wandler mit selbsttätiger Symmetrierung der speisenden Eingangs-Teilspannungen'. Austrian Patent AT 406 432, 2000, (in German), May 2000

[8] ERTL H., KOLAR J.W., ZACH F.C.: 'Analysis of an extended DC-DC fly-back converter with inherent input voltage symmetrization'. Proc. 38th Int. Conf. Power Conversion (PCIM-PC), Nurenberg, Germany, May 1998, pp. 501–506

[9] LOUNILA M.: 'Balancing circuit for input voltage division between capacitors'. European Patent EP1107438A2, June 2001

[10] WEINMEIER H., KRANISTER A.: 'Switching transformer'. PCT Patent WO01/97368, December 2001

[11] GHODKE D.V., MURALIKRISHNAN K.: 'ZVZCS, dual, two-transistor forward DC–DC converter with peak voltage of $V_{in}/2$, high input and high power application'. Proc. 33rd Ann. Power Electron. Specialists Conf. (PESC), Cairns, Australia, June 2002, vol. 4, pp. 1853–1858

[12] CANALES F., BARBOSA P., LEE F.C.: 'A zero-voltage and zero-current switching three-level DC/DC converter', *IEEE Trans. Power Electron.*, 2002, **17**, (6), pp. 898–904

[13] BARBI I., GULES R., REDL R., SOKAL N.O.: 'DC–DC converter: four switches $V_{pk} = V_{in}/2$, capacitive turn-off snubbing, ZV turn-on', *IEEE Trans. Power Electron.*, 2004, **19**, (4), pp. 918–927

[14] EDELMOSER K., ERTL H., ZACH F.C.: 'A novel high-input voltage switch-mode power-supply concept', *WSEAS Trans. Power Syst.*, 2006, **6**, (1), pp. 1062–1069

[15] AYYANAR R., GIRI R., MOHAN N.: 'Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC–DC converters using dynamic input-voltage reference scheme', *IEEE Trans. Power Electron.*, 2004, **19**, (6), pp. 1462–1473

[16] GIRI R., CHOUDHARY V., AYYANAR R., MOHAN N.: 'Common-duty-ratio control of input-series connected modular DC–DC

converters with active input voltage and load-current sharing', *IEEE Trans. Ind. Appl.*, 2006, **42**, (4), pp. 1101–1111

[17] ROJAS R., OHNISHI T., SUZUKI T.: 'PWM control method for a four-level inverter', *IEE Proc. Elect. Power Appl.*, 1995, **142**, (6), pp. 390–396

[18] MARCHESONI M., TENCA P.: 'Diode-clamped multilevel converters: a practicable way to balance DC-link voltages', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 752–765

[19] LIU Y.H., ARRILLAGA J., WATSON N.R.: 'Multi-level voltage reinjection – a new concept in high voltage source conversion', *IEE Proc. Gener. Transm. Distrib.*, 2004, **151**, (3), pp. 290–298

[20] PAN Z., PENG F.Z., CORZINE K.A., STEFANOVIC V.R., LEUTHEN J.M., GATARIC S.: 'Voltage balancing control of diode-clamped multilevel rectifier/inverter systems', *IEEE Trans. Ind. Appl.*, 2005, **41**, (6), pp. 1698–1706

[21] SALAET J., GILABERT A., BORDONAU J., ALEPUZ S., CANO A., GIMENO L.M.: 'Non-linear control of neutral point in three-level single-phase converter by means of switching redundant states', *IEE Electron. Lett.*, 2006, **42**, (5), pp. 304–306

[22] PENG F.Z.: 'A generalized multilevel inverter topology with self voltage balancing', *IEEE Trans. Ind. Appl.*, 2001, **37**, (2), pp. 611–618

[23] CORZINE K.A., KOU X.: 'Capacitor voltage balancing in full binary combination schema flying capacitor multilevel inverters', *IEEE Power Electron. Lett.*, 2003, **1**, (1), pp. 2–5

[24] XU L., AGELIDIS V.G.: 'Active capacitor voltage control of flying capacitor multi-level converters', *IEE Proc. Electr. Power Appl.*, 2004, **151**, (3), pp. 313–320

[25] HUANG J., CORZINE K.A.: 'Extended operation of flying capacitor multilevel inverters', *IEEE Trans. Power Electron.*, 2006, **21**, (1), pp. 140–147

[26] ZHANG L., WATKINS S.J.: 'Capacitor voltage balancing in multilevel flying capacitor inverters by rule-based switching pattern selection', *IET – Electr. Power Appl.*, 2007, **1**, (3), pp. 339–347

[27] TOLBERT L.A., PENG F.Z., CUNNYNGHAM T., CHIASSON J.N.: 'Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles', *IEEE Trans. Ind. Electron.*, 2002, **49**, (5), pp. 1058–1064

[28] SONG Q., LIU W., YUAN Z., WEI W., CHEN Y.: 'DC voltage balancing technique using multi-pulse optimal PWM for cascade H-bridge inverters based STATCOM'. Proc. 35th Ann. Power Electron. Specialists Conf. (PESC), Aachen, Germany, June 2004, vol. 6, pp. 4768–4772

[29] BARRENA J.A., MARROYO L., RODRIGUEZ M.A., ALONSO O., TORREALDAY J.R.: 'DC voltage balancing for PWM cascaded H-bridge converter based STATCOM'. Proc. 32nd Ann. IEEE Conf. Industrial Electronics (IECON), Paris, France, November 2006, pp. 1840–1845

[30] WATSON A.J., WHEELER P.W., CLARE J.C.: 'A complete harmonic elimination approach to DC link voltage balancing for a cascaded multilevel rectifier', *IEEE Trans. Ind. Electron.*, 2007, **54**, (6), pp. 2946–2953

[31] KOLAR J.W., ZACH F.C.: 'A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules', *IEEE Trans. Ind. Electron.*, 1997, **44**, (6), pp. 456–467

[32] KOLAR J.W., DROFENIK U., ZACH F.C.: 'Current handling capability of the neutral point of a three-phase/switch/level boost-type PWM (VIENNA) rectifier'. Proc. 27th Ann. Power Electron. Specialists Conf. (PESC), Baveno, Italy, June 1996, vol. 2, pp. 1329–1336

[33] ZETEX CORP : 'Semiconductor data book – Book 1: through hole components' November 1995, 2nd Issue edn.