A Simple Active Method to Avoid the Balancing Losses of DC Link Capacitors

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Abstract – DC voltage links of three-phase power converters very often are equipped with a series connection of two electrolytic capacitors due to the high voltage level. In general, resistors arranged in parallel to each capacitor are necessary for balancing the capacitor partial voltages. The balancing resistors have to be dimensioned regarding the worst-case condition of the capacitor leakage currents, resulting in high permanent dissipative losses.

To avoid these losses to a large extent, a novel simple and low-cost active circuit to replace the passive balancing resistors by a cascode array of low-cost small-signal low-voltage bipolar transistors is presented. The paper describes the operating principle of the circuit, analyzes the fundamental relationships being relevant for the balancing characteristic and gives guidelines concerning component selection. Furthermore, simulation results as well as measurements taken from a laboratory prototype are presented.

1. INTRODUCTION

DC voltage links of power electronic converters connected to the 400V/500V three-phase mains, e.g., for AC drive systems (**Fig.1a**), for welding converters or telecom switch-mode power supplies etc., frequently are equipped with a series arrangement of two electrolytic capacitors. The reason for the series connection is that electrolytic capacitors at present are available with maximum voltage ratings of only up to ≈500V. The DC link voltage level of the converters mentioned (typically $U_D \approx 500 \ldots 800$ V) therefore permits the application of a single capacitor device. Electrolytic capacitors unfortunately show a significant leakage current which may vary in a wide region dependent on the operating and aging conditions of the device. To guarantee an about uniform distribution of U_D to both capacitors C_1, C_2 (i.e., $U_{C1} \approx U_{C2} \approx U_D/2$) in order to avoid voltage overloading, the manufacturers usually recommend the application of balancing resistors R_B connected in parallel to each capacitor [1, 2]. As will be discussed in **section 2** these resistors cause high dissipative losses, especially if they are dimensioned to cover the capacitor worst-case leakage. If the power electronic converter is permanently connected to the mains as often is the case in the industrial automation field, these "balancing losses" sum up to considerable additional energy costs during the operating life of the unit.

For avoiding this significant drawback of the passive voltage balancing, a simple active balancing method is proposed (**Fig.1b**) and discussed in **section 3**. The basic concept of this method is that the connection point "C" of the two capacitors is stabilized to $U_D/2$ using a high-impedance voltage divider (R_B^*) and a complementary emitter-follower stage (Q_N, Q_P). With this the losses can be reduced significantly, because the voltage divider quiescent current now can be reduced considering the current

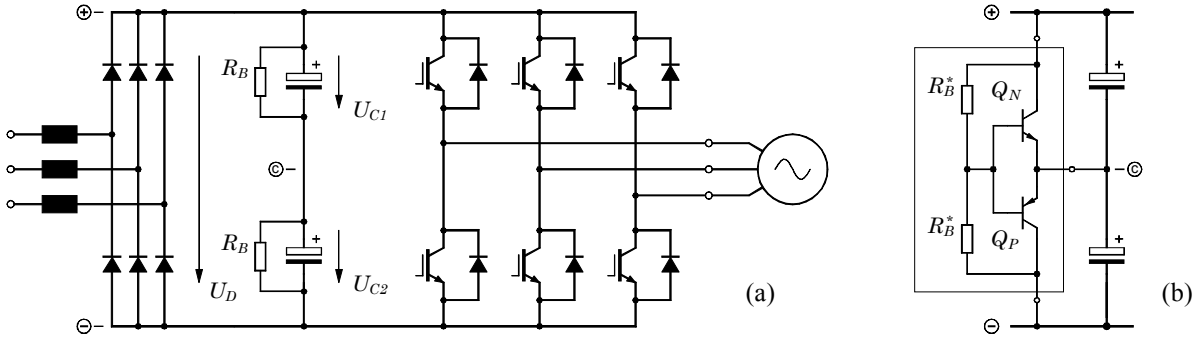

Fig.1: Circuit topology of a three-phase power converter (e.g., AC drive system) using a series connection of two electrolytic capacitors to form the DC voltage link; **(a)**: passive voltage balancing by two resistors R_B; **(b)**: basic circuit diagram of the proposed active voltage balancing consisting of a high-impedance voltage divider and a complementary emitter-follower.

gain of the transistors. Subsequently, **section 4** gives an advantageous realization of an active balancing unit using a voltage-follower topology formed by a cascode array of low-cost small-signal low-voltage bipolar transistors. Finally, **section 5** presents measurements taken from a laboratory breadboard circuit.

2. PASSIVE VOLTAGE BALANCING

For passive capacitor voltage balancing the two resistors R_B form a voltage divider and a perfect voltage distribution $U_{C1} = U_{C2}$ would be given in case of zero output current $\Delta I = 0$ (**Fig.2**). The output current, however, is defined by the leakage current difference $\Delta I = I_{l,C2} - I_{l,C1}$ of the DC link capacitors. This leads to the consequence that for practical applications R_B has to be selected such that the expected leakage current difference is small in comparison to the quiescent current I_Q of the voltage divider to achieve a good voltage distribution $U_{C1} \approx U_{C2} \approx U_D/2$, i.e. a voltage deviation $\Delta U \to 0$. Here, the most significant drawback of the passive voltage balancing becomes obvious: The quiescent current – which determines the dissipative losses – has to be a multiple of the worst-case leakage difference of the capacitors, and also if the actual value of ΔI is much smaller or even $\Delta I \to 0$ is valid, considerable losses remain permanently.

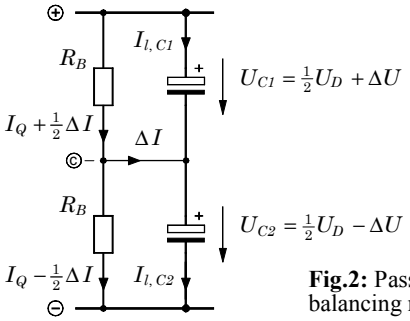

Fig.2: Passive voltage balancing network.

Using the output resistance $R_B/2$ of the voltage divider, the capacitor voltage deviation is calculated to $\Delta U = \Delta I \cdot R_B/2$; normalization by the nominal voltage $U_D/2$ of the capacitors leads to

$$\Delta u = \frac{\Delta U}{\frac{1}{2}U_D} = \frac{\Delta I \cdot \frac{1}{2}R_B}{I_Q \cdot R_B} = \frac{1}{2}\frac{\Delta I}{I_Q} \quad . \tag{1}$$

Consequently, if the capacitor voltages shall be balanced to, e.g., typically $\Delta u \le \pm 10\%$, a quiescent current of $I_Q \ge 5 \cdot \Delta I$ has to be chosen. Using Eq.(1), the total losses of the two balancing resistors ("balancing losses") sum up to

$$P_B = \underbrace{2R_B \cdot I_Q^2}_{P_Q} + \frac{R_B}{2} \cdot \Delta I^2 = P_Q\left[1 + \Delta u^2\right] \quad . \tag{2}$$

For relevant values $\Delta u < 0.1$ the balancing losses are dominated by the quiescent current losses $P_B \approx P_Q$.

Capacitor Leakage Current. Finally, as an effect of the "electro-chemical origin" of electrolytic capacitors, the leakage current is largely dependent on operating, temperature and aging conditions of the component. It should, e.g., be noted that if the capacitor voltage carefully is increased to values being higher than the specified surge voltage, the "leakage" current increases rapidly due to the re-starting of the reforming process (growing of the oxide layer) which will take place [1]. Furthermore, at normal operation conditions (voltages below the surge level) the leakage current may be much higher than the specified value for the first minutes after the voltage is applied ("inrush current"). This is especially true after a longer period of voltage-free storage of the component (oxide layer deterioration). But also the normal operation leakage current approximately doubles its value for each 20°C temperature increase. According to [1] the typical operating leakage current of power electrolytic capacitors can be calculated using

$$I_{l,\mathrm{op}} = 0.0005\mu\mathrm{A} \cdot \frac{C}{\mu F} \cdot \frac{U_R}{V} + 1\mu A \tag{3}$$

(U_R ... rated voltage) valid for long-life (LL) types at 20°C. The maximum leakage current ("acceptance test" according to standard EN 130 300), however, is only guaranteed to be limited to

$$I_{l,\max} = 0.3\mu\mathrm{A} \cdot \left[\frac{C}{\mu F} \cdot \frac{U_R}{V}\right]^{0.7} + 4\mu\mathrm{A} \quad , \tag{4}$$

valid also for 20°C (for, e.g., 35°C this permissible limit has to be multiplied by a factor of 2.5!).

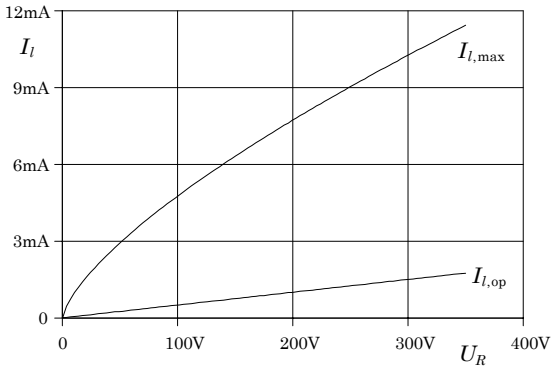

Fig.3: Typical and maximum leakage currents of a 10000µF LL-grade electrolytic capacitor according to Eqs.(3,4).

Design Example. To give an example for the dimensioning of a passive balancing network, it should be assumed that the 500V DC voltage link of a 10kVA AC drive system according to Fig.1 is equipped with two 10000µF/350V capacitors (e.g., EPCOS type B 43 564). The leakage current of this component according to Eqs.(3,4) for the relevant capacitor operating voltage (cf. **Fig.3**, $U_R \approx 250\,\mathrm{V}$) is in the

range between $I_{l,\mathrm{op}} \approx 1.3\,\mathrm{mA}$ (typical) and $I_{l,\max} \approx 9\,\mathrm{mA}$. Due to the fact that the output current ΔI of the balancing network is formed by the leakage current difference of the two capacitors, but on the other hand the values given before are valid for 20°C only, a maximum value of $\Delta I = 5\ldots10\,\mathrm{mA}$ shall be assumed. Choosing $I_Q = 10\ldots5 \cdot \Delta I$ leads to a quiescent current of $I_Q = 50\,\mathrm{mA}$ which limits (using Eq. (1)) the center point voltage deviation to $\Delta u \le 5\%$. Now the resistance value of the balancing resistors can simply be calculated to $R_B = U_C / I_Q = 250\,\mathrm{V}/50\,\mathrm{mA} = 5\,\mathrm{k\Omega}$.

The calculated dimensioning coincides very closely with a guideline given by the manufacturers. In the data sheets or application recommendations (e.g., [1] or [2]) it is frequently specified that the balancing resistors shall be calculated using the relation $R_B \cdot C \approx 50\,\mathrm{sec} = T_B$. For the case at hand this again leads to $R_B = 5\,\mathrm{k\Omega}$. Remark: The relation used before implies also that the balancing process $\Delta U \to 0$ of the (first-order) system has a time constant of T_B. If the capacitors are charged up to $\Delta u = \pm 20\%$ at the power-up of the converter (e.g., caused by $\pm 20\%$ different capacitance values), it will take approximately 3 minutes until $\Delta U \to 0$ is valid!

A quiescent current of $I_Q = 50\,\mathrm{mA}$ at $U_D \approx 500\,\mathrm{V}$ results in balancing losses of $P_B = 25\,\mathrm{W}$. If the converter is permanently powered by the mains (as often is the case for modern industrial automation systems), these losses will sum up to a considerable energy consumption of approximately 220kWh per year! Considering the product life cycle of the converter, the balancing energy costs are many times higher than the costs for the passive balancing network itself. This suggests the development of an advanced balancing method.

3. Active Balancing – Basic Concept

The basic idea of the proposed active balancing concept is to separate the dimensioning of the voltage divider's quiescent current from the leakage currents of the electrolytic capacitors. In an optimal case the voltage divider only would define the potential of the center point "C" to $U_C = U_D/2$ acting as the input reference level of an idealized voltage follower stage (**Fig.4a**). With this, $R_B^* \to \infty$, $I_Q^* \to 0$ would be possible and the balancing losses (appearing in the output stage of the amplifier) now are determined only by the actual leakage current difference and not by worst case conditions as this is true for the passive balancing network.

Unfortunately, a realization according to the operation principle shown in Fig.4a is not adequate because a high-voltage operational amplifier would be required which is expensive and itself in general shows noticeable quiescent power losses. On the other hand, the excellent balancing accuracy which is achievable with this circuit would not be required for practical applications. Therefore, the operational amplifier with direct voltage feedback can be realized (as already anticipated in Fig.1b) by a simple emitter-follower stage consisting of two complementary bipolar transistors (**Fig.4b**). Although the ideal case $I_Q^* \to 0$ now is not valid any more, the losses can be considerably reduced because a much lower quiescent current as compared to the passive case is possible considering the current gain β of the transistors $\Delta I \to \Delta I/\beta$. Neglecting the losses of the voltage divider itself (i.e., $I_Q^* \to 0$, $\beta \to \infty$) the losses of the active balancing are calculated to

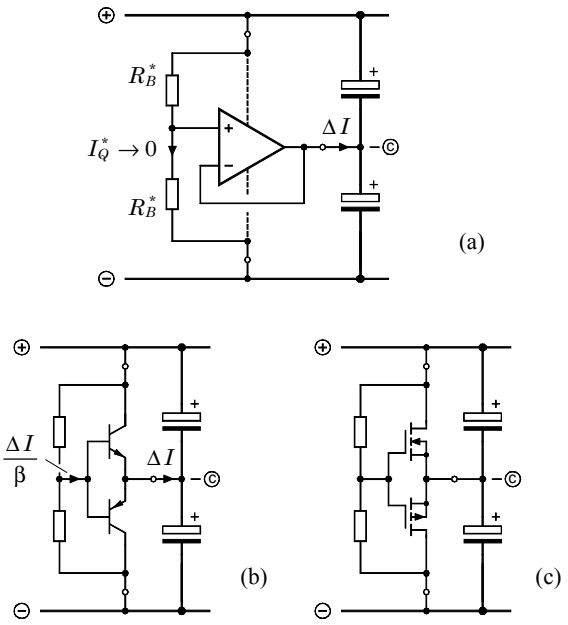

Fig.4: Basic realization of active voltage balancing using high-voltage operational amplifier **(a)**, bipolar emitter-follower **(b)** or MOSFET source-follower **(c)**.

$$P_B^* = \tfrac{1}{2} U_D \Delta I \quad . \tag{5}$$

As demonstrated by **Fig.5** for the dimensioning example given in section 2, these losses are by far lower in comparison to the passive balancing method (cf. also Eq.(2) with Eq.(5)). Furthermore, the active circuit also gives a stiffer balancing characteristic ($U_{C1} = U_{C2} = U_D/2$ for the idealized case $\beta \to \infty$).

For realization of the emitter-follower bipolar transistors which show a maximum collector-emitter voltage of at least $U_D/2$ are required. Considering DC link overvoltages, no-balanced operating conditions and safety margins to guarantee a robust and reliable operation of the active balancing, at least 400V... 500V semiconductor devices seem to be necessary in practice for a DC link with 500V nominal voltage. However, high-voltage bipolar transistors are characterized by a comparatively low β due to their wide effective base region. General-purpose 400V NPN-/PNP-transistor pairs, e.g., MPSA44/MPSA94 are characterized by a current gain of typically only $\beta \approx 40$ and, therefore, are not suited well for realizing

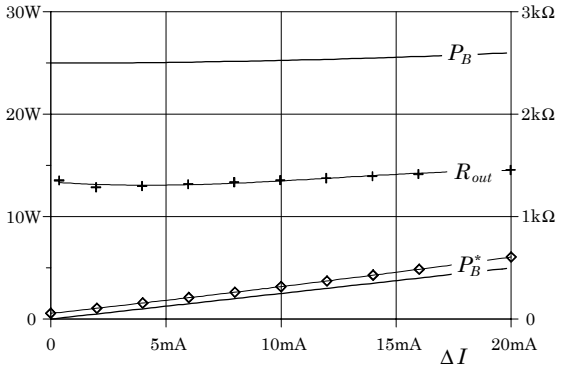

Fig.5: Losses of the passive (P_B) and of the active (P_B^*) balancing; marked curves: simulation results: losses including quiescent losses and output resistance (cf. section 5).

the proposed concept. Although "high-gain" high-voltage bipolar transistor pairs are available in the 400V region (e.g., ZETEX ZTX458/ZTX558, $\beta \approx 200$ [3]), it has to be considered that the transistor types mentioned before are "low-power" devices, i.e., limited to typ. $P \le 1\,\mathrm{W}$. In the case of, e.g., $\Delta I > 4\,\mathrm{mA}$ these elements would be thermally overloaded. On the other hand, real high-voltage bipolar power transistors are hardly available as complementary pairs and/or show very low current gain.

Consequently, an implementation using complementary power MOSFET transistors according to **Fig.4c** would be of advantage. But also here the availability of high-voltage p-channel devices is very limited (e.g., 500V transistor MTP2P50E by ON Semiconductor); furthermore, these semiconductor devices are rather expensive.

4. ACTIVE BALANCING – CASCODE TOPOLOGY

To avoid the drawbacks of the circuits of Fig.4b and Fig.4c mentioned before, an active balancing unit using a cascode circuit topology as shown in **Fig.6a** is proposed. The splitting-up of the voltage divider resistor R_B^* into n equal partial resistors R makes possible to replace the high-voltage transistor by a "chain" of general-purpose low-voltage small-signal transistors. This is of significant importance because these components are available as high-gain devices (e.g. the low-cost SMD transistors BC850C/BC860C are specified to $\beta \approx 600...800$) and, therefore, allow a high-impedance dimensioning of the voltage divider network resulting in low quiescent losses. Due to the limited voltage capability of the semiconductors (e.g., $U_{CEO} = 45\,\mathrm{V}$), typically $n = 10...15$ transistors will be necessary for a $500\,\mathrm{V}$ DC link. With this also the handling of the resulting power loss (e.g., in total $P_B \approx 2.5\,\mathrm{W}$ for $\Delta I = 10\,\mathrm{mA}$ according to Eq.(5) or Fig.5) does not cause serious problems, because the losses are distributed to many components and for each transistor only $\approx 200\,\mathrm{mW}$ will appear, being well tolerable even for SMD components. Due to the huge number of active and passive components high costs

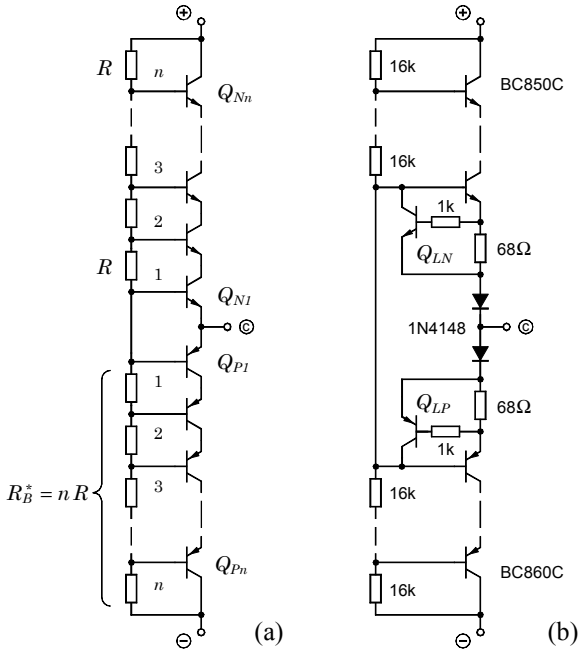

Fig.6: Active balancing unit using a cascode arrangement of low-voltage small-signal transistors **(a)**; extension of basic circuit (a) for current limitation of ΔI **(b)**.

might be expected. However, the transistors and also the resistors (0805 SMD chip type) are widely used ultra-low-cost components. The cost of the total circuit including the PCB therefore are very similar to the two power resistors of the passive balancing.

Output Resistance. To minimize the quiescent losses the resistance value of the voltage divider should be chosen as high as possible. However, this worsens the output resistance R_{out} of the total circuit which determines the balancing characteristic of the system. This characteristic should be better (i.e., lower R_{out}) or at least similar to the passive solution in order to achieve a "stiffer" center point voltage. The output resistance of the passive balancing system is given by $R_{out} = R_B/2$, whereas for the simple active system (Fig.4b) $R_{out}^* = R_B^*/(2\beta)$ is valid. The calculation of the output resistance of the proposed cascode system is more difficult and should be performed based on the equivalent circuit **Fig.7**. Starting at the output side (center point "C") with given voltage U and balancing current ΔI the i-th transistor stage contributes a collector-base voltage of $U/n + i \cdot R \cdot \Delta I/\beta$. With this, according to Fig.7 the relation

$$U_D = U + \sum_{i=1}^{n} \left[\frac{U}{n} + i \frac{\Delta I}{\beta} R \right] = 2U + \frac{\Delta I}{\beta} R \cdot \sum_{i=1}^{n} i \qquad (6)$$

is valid. (For the sake of brevity the base-emitter voltage drop shall be neglected and it shall be assumed that all transistors show equal current gain β .) Calculating $\Sigma\, i$ and rearranging of Eq.(6) finally leads to the output behavior of the system

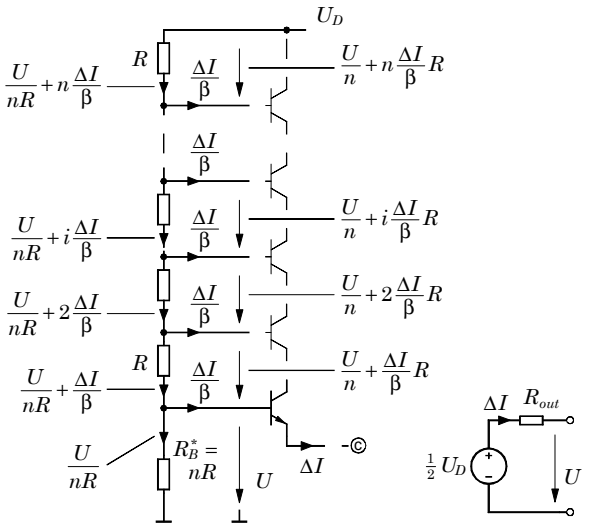

Fig.7: Circuit diagram for calculating the output resistance R_{out} of the cascode topology (valid for $\Delta I > 0$).

$$U = \tfrac{1}{2}U_D - \Delta I \cdot \underbrace{\frac{R}{\beta}\cdot\frac{n(n+1)}{4}}_{R_{out}} \tag{7}$$

and to the output resistance to be calculated:

$$\boxed{R_{out} = \frac{R}{\beta}\cdot\frac{n(n+1)}{4} = \frac{R_B^*}{\beta}\cdot\frac{n+1}{4}} \tag{8}$$

It should be noted that according to Eq.(8) for a given value of R_B^* (which defines the quiescent losses $P_Q = U_D^2/(2R_B^*)$) R_{out} worsens for increasing n. Therefore, to give a good balancing performance the number of cascode stages should be not to high considering the voltage and power limitations of the transistors.

5. Laboratory Prototype

Based on the analyses of the section before a prototype system of an active balancing unit has been realized to compete with the passive balancing method described in section 2 using two $5\,\text{k}\Omega$ resistors. As already mentioned before, the assumed maximum balancing current of $\Delta I = 10\,\text{mA}$ leads to a total balancing loss of $P_B \approx 2.5\,\text{W}$. Considering power limitations of BC850C/BC860C and guaranteeing a reliable operating voltage margin even in case of an output short circuit 2x15 cascode stages have been chosen ($n = 15$). Dimensioning the voltage divider resistors to $R = 16\,\text{k}\Omega$ Eq.(8) gives an output resistance of $R_{out} = 60 \cdot R/\beta = 1.37\,\text{k}\Omega$ for $\beta \approx 700$, which is significantly better in comparison to the $2.5\,\text{k}\Omega$ of the passive balancing resulting in a more precise voltage sharing. The selected voltage divider causes quiescent losses of $P_Q = U_D^2/(2nR) \approx 0.5\,\text{W}$ (see also simulation results given in Fig.5). In contrast to the $25\,\text{W}$ losses of the passive solution, this value clearly demonstrates the advantage of the proposed method.

In order to reduce the heat dissipation of the transistors in case of a failure, the basic cascode circuit has been extended by a current limiter according to Fig.6c. Using $68\,\Omega$ current sensing resistors limits the output current to $\Delta I_{\max} = U_{BE}/R_{sense} \approx$ $\approx 700\,\text{mV}/68\,\Omega = 10\,\text{mA}$. As shown in **Fig.8** the whole system is realized on a small PCB stripe (size 160x 20mm, i.e., the length is about similar to the width of the two electrolytic capacitors 2x77mm∅) using exclusively low-cost SMD components. The PCB stripe has three terminal fins (+/C/–) which can be soldered directly to the converters main PCB board replacing the two passive balancing resistors.

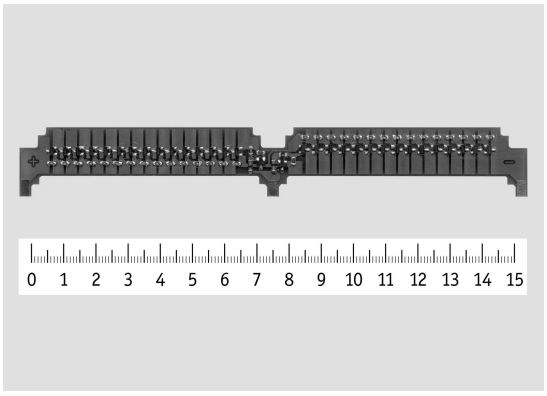

Fig.8: Prototype of active balancing device (cm-scale).

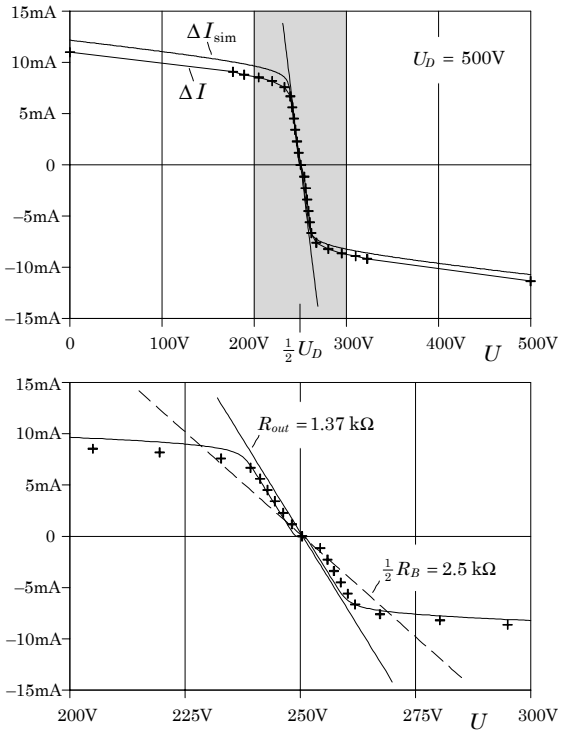

Fig.9: Simulated and measured output characteristic $\Delta I(U)$ of the proposed system; the zoomed region (lower diagram) demonstrates the stiffer balancing behavior of the active system (dashed line: passive balancing).

In addition to the calculations presented in section 4, the system has been checked further by a Spice-simulation. As shown in **Fig.9**, the output characteristic and the output resistance of the prototype system coincide very closely with the expected and simulated behavior and with the output resistance calculated using Eq.(8) (cf. also the output resistance values gained by simulation, Fig.5).

During the measurements a further advantage of the system became obvious. Although the circuit probably would not be characterized by the balancing precision of the system shown in Fig.4a, the cascode structure shows a remarkable accuracy which is by far better than the balancing precision of the passive solution. The power resistors being necessary for passive balancing hardly are available with precision ratings better ±5...±10%, resulting in a balancing accuracy of equal value. The resistors of the voltage divider network of the cascode balancing, however, usually are of ±1% precision, even if low-cost components are applied. Furthermore, due to the fact that the $2n$ components partially cancel out their resistance errors, an even better balancing accuracy could be observed. E.g., for $U_D = 500.0\ \mathrm{V}$ the no-load output voltage of the prototype has been measured to $249.7\ \mathrm{V}$, i.e., an error of only 0.12% results. The component cost of the active balancing unit assuming mass production is estimated to be 1...2€ and, therefore, in the region of the passive solution.

6. CONCLUSIONS

The proposed active voltage balancing is a very attractive alternative for balancing series connected electrolytic capacitors of power converters with DC voltage link to advantageously substitute the commonly used passive balancing resistors. The active system which preferably is realized by application of a cascode voltage-follower circuit topology is characterized by the following features in comparison to the resistor balancing:

- significant reduction of balancing losses resulting in huge savings of energy cost considering the converter life cycle
- stiffer balancing behavior (reduced output resistance)
- increased stationary balancing precision
- low cost (similar to passive solution)

Finally, also the only attribute known at present which might be seen as drawback should be mentioned: The proposed system is not very well suited to perform the safety discharge of the DC voltage link after the power converter has been switched off. However, frequently alternative discharge paths will be present, e.g., the main load of the converter itself or the auxiliary power supply of the converter which more and more is realized using a small DC/DC converter fed by the main voltage link. Future research in this area will focus on circuit extensions and topologies for balancing of series connections of more than two electrolytic capacitors.

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