A Novel Multi-Cell DC-AC Converter for Applications in Renewable Energy Systems

Hans Ertl, Johann W. Kolar*, Franz C. Zach

Technical University Vienna
Dept. of Electrical Drives and Machines
Power Electronics Section

Gusshausstrasse 27/372, A-1040 Vienna

phone: +43-1-58801-37235 fax: +43-1-58801-37297
email: j.ertl@tuwien.ac.at

* Swiss Federal Institute of Technology Zurich
Power Electronics and
Electrometrology Laboratory

ETH Zentrum, ETL 22 CH-8092 Zurich

phone: +41-1-632 28 34 fax: +41-1-6321212
email: kolar@lem.ee.ethz.ch

Abstract – The paper presents a novel DC-AC converter for applications especially in the area of distributed energy generation systems, e.g., solar power systems, fuel-cell power systems in combination with super-capacitor or battery energy storage. The proposed converter is realized using an isolated multi-cell topology where the total AC output of the system is formed by series connection of several H-bridge inverter stages. The DC links of the H-bridges are supplied by individual DC-DC isolation stages which are arranged in parallel concerning the DC input of the total system. Therefore, all switching cells of the proposed converter can be equipped with modern low-voltage high-current power MOSFETs which results in an improved efficiency as compared to conventional isolated DC-AC converters. Furthermore, the cells are operated in an interleaved PWM mode which in connection with the low voltage level of each cell significantly reduces the filtering effort on the AC output of the overall system. The paper describes the operating principle, analyzes the fundamental relationships being relevant for component selection and presents a specific circuit design. Finally, measurements taken from a 2kW laboratory model are presented.

1. INTRODUCTION

In connection with distributed energy generation (e.g., solar-cell or fuel-cell applications having battery or super-capacitor backup) in general unidirectional and/or bidirectional DC-AC converters are applied. To give an example, typical specific operating parameters and requirements of solar-power converters for home applications should be summarized: DC input voltage: 50...200V, rated power: 0.5...2kVA, AC output voltage (mains): $230V_{RMS}$, 4Q-operation of the DC-AC converter stage (generation of reactive power for stand alone applications), isolated topology (isolation between DC input and AC output due to safety requirements). Converter systems for the applications mentioned before have to be designed considering very high efficiency and reliability. Usually, full bridge circuit topologies feeding line-frequency transformers for isolation and voltage adaption (cf. **Fig.1 (a)**) are applied. Here, the DC-AC stage itself (H-bridge) shows high efficiency if it is equipped with modern power MOSFETs. However, the efficiency of the line frequency power transformer is rarely better than 95% and consequently the efficiency of the total system typically is only about 90%.

In order to avoid the bulky mains transformer and/or to increase power density and efficiency, alternatively, topologies with high frequency isolation based on a DC-DC system feeding the DC link of a full bridge DC-AC converter connected directly to the mains can be applied (cf. Fig.1 (b)). However, here the low losses of the high-frequency isolation transformer have to be seen considering the additional losses of the rectifier stage and, especially, the line side inverter. According to the required DC link voltage level (e.g., 400V) this power stage in general is equipped with IGBTs, which show a non-optimum

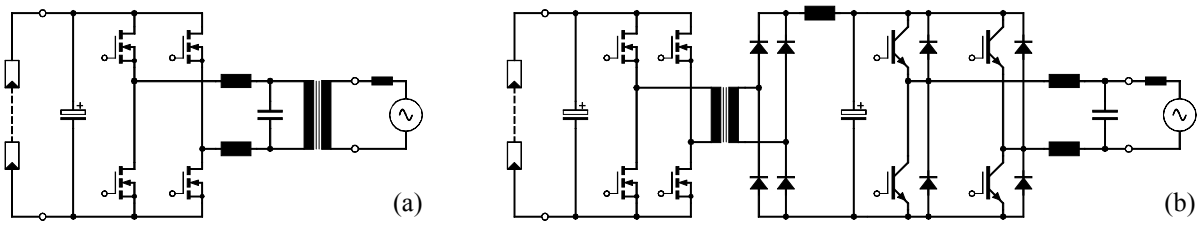


Fig.1: Basic circuit topology of a solar power converter with MOSFET-H-bridge and line-frequency isolation transformer **(a)** and, alternatively, topology with MOSFET DC-DC converter (high-frequency isolation transformer) with subsequent single-cell IGBT four quadrant DC-AC converter **(b)**.

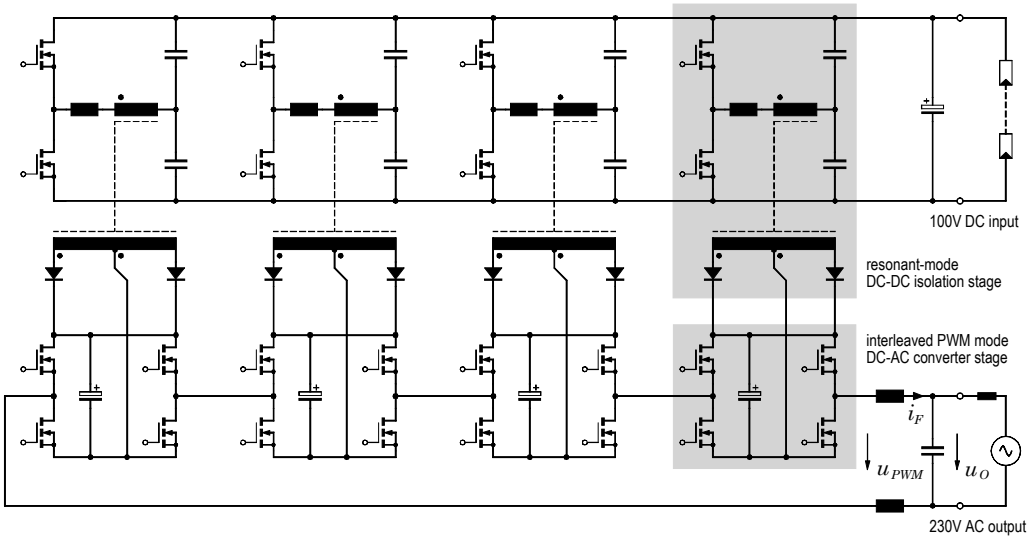


Fig.2: Basic circuit topology of the proposed DC-AC multi-cell converter based on high-frequency resonant-mode DC-DC isolation stages feeding interleaved PWM mode MOSFET DC-AC cells connected in series on the AC output (N=4 cells).

efficiency for operating in the partial load area. Remark: For equal losses at the rated operating point power MOSFETs showing resistive on-state behavior are more efficient as compared to IGBTs which show a more constant and/or current independent on-state voltage drop ($p_{on} \approx R_{DS,on} \cdot i_D{}^2$ for MOSFETs vs. $p_{on} \approx U_{CE,on} \cdot i_C$ for IGBTs).

Consequently, considering the efficiency the systems of Fig.1 are about comparable. The advantage of the topology of Fig.1 (b) is the increased power density due to the high-frequency transformer. Furthermore, both systems of Fig.1 are characterized by a single-stage AC voltage generation. This results in a poor mains current harmonic behavior, or, if the switching frequency is increased to lower the current harmonics, in a reduced efficiency.

2. MULTI-CELL CONVERTER – BASIC CONCEPT

Influenced by the recent developments in the area of low-voltage power MOSFETs a circuit topology known from high power converters [1] shall be proposed for the application in distributed energy generation systems. With this the drawbacks of the converter structures discussed in section 1 can be avoided resulting in a compact unit with high overall efficiency. There, the key specifications of the developed system are:

DC input voltage:	U_1	=	100V (80...120V)
AC output voltage:	U_{AC}	=	$230V_{rms}$
rated power:	P_N	=	2 kW
efficiency:	η	>	94% @ rated power

- high-frequency isolation stage
- low-voltage MOSFETs (majority carrier devices)

According to **Fig.2**, the whole circuit is formed by multiple converter cells which are arranged in parallel at the DC input side and are connected in series concerning the AC output voltage. Each cell consists of a high-frequency isolation stage feeding the DC voltage link of a full-bridge inverter. Because of the series arrangement also the inverter stages can be realized in the same semiconductor technology as the isolation stages (application of low voltage devices).

The isolation stage is implemented using a capacitively coupled half bridge converter operated in a constant frequency series resonant mode (no pulse width modulation), see section 3. This results in low on-state losses (no free-wheeling states) and low switching losses (zero-current and zero-voltage turn-on) for continuous conduction mode at switching frequencies being higher than the natural frequency of the resonant network. Therefore, the DC link voltage of each DC-AC stage varies directly according to the DC input voltage of the total system.

The control of the AC output voltage/current is achieved by pulse width modulation (PWM) of the DC-AC stages. Advantageously, this can be performed in an interleaved PWM mode of the individual cells in order to minimize the filtering effort due to fact that the resulting multi-level output voltage sum of all cells then very closely approximates the sinusoidal voltage reference value. Therefore, the PWM switching frequency of each DC-AC cell can be chosen comparatively low; this results in low switching losses. Furthermore, it is of advantage to operate also the isolation stages in an interleaved mode in order to minimize the ripple current stress of the DC input smoothing capacitor.

3. SERIES-RESONANT ISOLATION STAGE

As already mentioned, the series-resonant topology has been chosen for the isolation stage due to the expected good efficiency based on the zero-current and zero-voltage turn-on of the power transistors. Furthermore, the blocking voltage stress on all semiconductors is well defined and the leakage of the transformer contributes to the effective inductance of the resonant network. Therefore, different to, e.g., transformers for flyback converters a certain amount of leakage is desirable here. This is also of importance because the coupling capacitance between primary and secondary should be minimized because the proposed topology is characterized by a common mode voltage stress between the individual PWM DC-AC cells; a low coupling capacitance helps to limit the resulting common mode current. A circuit topology which is not sensitive to transformer leakage is furthermore of advantage because the primary winding of the transformer shall be realized by application of the ″bow winding principle″, i.e., copper wire bows are connected via the printed circuit board (PCB) to form the primary winding, whereas the secondary windings are of conventional type. Such a transformer usually shows significant leakage (but low coupling capacitance) and, therefore, is well suited for the series mode resonant topology.

A. Analysis of the Stationary Operating Behavior

In the following, the characteristics of the stationary operation shall be calculated analytically. It should be mentioned that a center-tapped secondary is used for the designed converter, which results in an only single diode forward voltage drop as compared to bridge rectification (**Fig.3 (a)**). Remark: For the desired output voltage range of up to 120V usually 400V diodes would be suitable for center-tapped rectification whereas for bridge rectification 200V diodes would be sufficient. Although 400V devices show a higher on-state voltage than 200V diodes, the two 200V devices acting in series for bridge rectification cannot compete with the single 400V diode of a center tapped system.

Here, the bridge rectifier is given only to develop the equivalent circuit diagram of Fig.3 (b, c). The system is characterized by four different states defined by the polarities of the input voltage u_1 and of the reflected secondary voltage u_2. Whereas the polarity of u_1 is defined by the control circuit, the polarity of u_2 is given by the direction of the resonant current i_L. The four possible states (A→B→C→D) are listed in Tab.1. For state A, voltages u_1 and u_2 show equal direction and the (small) difference $\Delta U = U_1 - U_2$ is

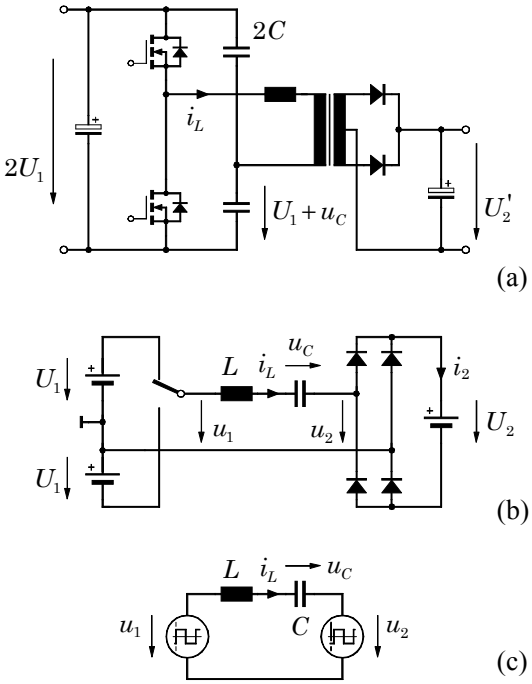
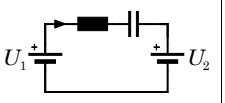
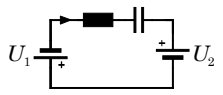
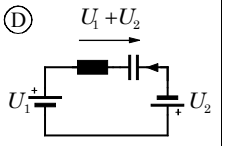
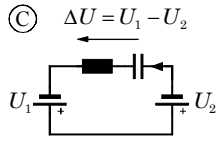


Fig.3: Circuit diagram of the series resonant converter **(a)** and corresponding equivalent circuits **(b,c)**.

	$u_1 > 0$	$u_1 < 0$
$i_L > 0$	Ⓐ $\Delta U = U_1 - U_2$ 	Ⓑ $U_1 + U_2$ 
$i_L < 0$	Ⓓ $U_1 + U_2$ 	Ⓒ $\Delta U = U_1 - U_2$ 

Tab.1: Operating states of the series resonant converter.

applied to the LC series circuit. This results in a circular shaped system trajectory around the center point $[+\Delta U, 0]$ (cf. $u_C Z_0 i_L$ – diagram of **Fig.4 (a)**, $Z_0 = \sqrt{L/C}$ defines the characteristic impedance of the resonant network). Because the system operates with a switching frequency f_S above the natural frequency $f_0 = 1/(2\pi\sqrt{LC})$, the input voltage u_1 changes its polarity at instant 1 due to the turn-off of the high-side transistor before i_L becomes zero. Consequently, the system transits to state B where the sum $U_1 + U_2$ causes a steep current reduction (cf. Fig.4 (b)) according to the circular trajectory with the center

point $[-(U_1+U_2),0]$. At instant 2, the current i_L becomes negative, the current in the rectifier diodes commutates and u_2 again shows equal (i.e., negative) polarity as u_1 (state C); now $[-\Delta U,0]$ is the new center of the trajectory valid until the lower power transistor turns off at instant 3 and the system passes over to state D (center $[+(U_1+U_2),0]$) which completes a full cycle in instant 4.

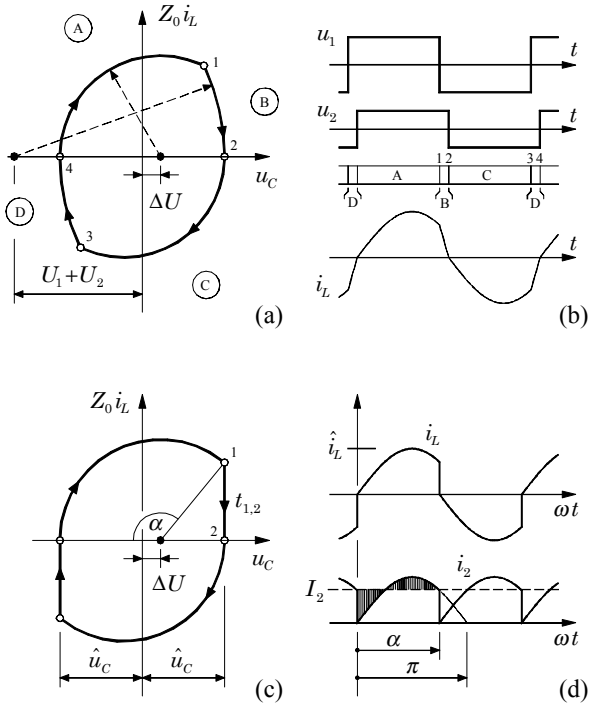


Fig.4: System trajectory **(a)** and time behavior **(b)** of the series resonant converter; **(c), (d)**: simplification valid for $\Delta U \ll U_1$; i_2 : output current of rectifier (cf. Fig.3 (b)).

For the practical realization of the series resonant converter stage of the proposed system it is of importance that, in general, $\Delta U \ll U_1$ is valid; this is caused by the fact that the characteristic impedance $Z_0 = \sqrt{L/C}$ is defined by the small inductance L given to a significant extent by the transformer leakage. With this assumption the system trajectory in good approximation shows the shape of Fig.4 (c), i.e., the current contribution of states B and D to i_2 can be neglected ($t_{1,2} \to 0$, Fig.4 (c)). With this and using the conduction angle

$$\alpha = \frac{\pi}{f_S/f_0} \qquad (1)$$

the equations

$$(\hat{u}_C + \Delta U)\cos(\pi - \alpha) = \hat{u}_C - \Delta U \qquad (2)$$

and

$$Z_0 I_2 = (\hat{u}_C + \Delta U)\frac{1}{\alpha}\int_0^{\alpha} \sin(\omega t)\, d\omega t \qquad (3)$$

can be written according to the geometrical relations given by Fig.4 (c) and according to the fact that the average value of i_2 (i.e., the rectified inductor current i_L) in the stationary case is defined by the load current I_2. Evaluation of Eq.(3) and rearranging using Eq.(2) finally leads to

$$\Delta U = I_2 \cdot R_{out} \quad \text{with} \quad R_{out} = Z_0 \frac{\frac{\alpha}{2}}{\tan^2\frac{\alpha}{2}} \qquad (4)$$

and

$$\hat{u}_C = \tfrac{\alpha}{2} Z_0 I_2 = \frac{I_2}{4 f_S C} \quad . \qquad (5)$$

These equations state that for a given switching frequency (fixed conduction interval α) the output voltage U_2 decreases proportional to the load current I_2, i.e., the converter shows a quasi-ohmic output impedance (current-independent output resistance R_{out}, cf. equivalent circuit given in **Fig.5**). Remark: This system behavior is very similar to the commutation voltage drop of line commutated converters where the commutation inductances finally cause a current-proportional output voltage reduction. An exact calculation as given in [3] results in an output characteristic described by ellipses (cf. thin curves in

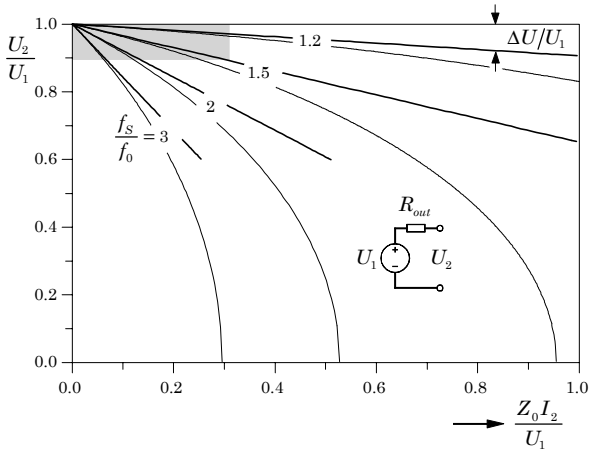


Fig.5: Output characteristic of the series resonant converter for fixed frequency operation above the natural frequency.

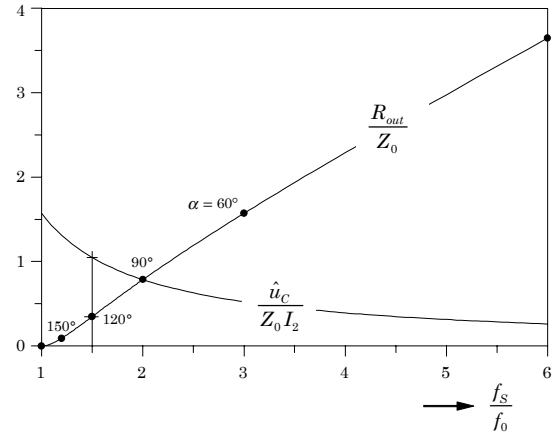


Fig.6: Dependency of the output impedance R_{out} and of the capacitor peak voltage value on the switching frequency.

Fig.5). However, as is also indicated by the shaded area of Fig.5, for the operating region being relevant for the proposed system ($\Delta U < 10\%$), the simplified calculation given here shows excellent accuracy. **Figure 6** demonstrates that the output impedance R_{out} is approximately linearly dependent on the switching frequency and $R_{out} \to 0$ for $f_S \to f_0$ is valid. Therefore, the desired stiff output characteristic suggests $f_S = f_0$. However, this would lead to a worse transient response (voltage overshoot) because R_{out} also acts as damping resistor for the resonant circuit given by the output inductance (not shown in equivalent diagram of Fig.5) and the output smoothing capacitor. Furthermore, it has to be taken into account that the turn-off of the power transistors has to be performed at $i_L > 0$; only in this case there exists a remaining current which charges the drain-source capacitance of the transistors in order to get zero-voltage turn-on. For a practical realization the resonant network usually is dimensioned to achieve $\alpha \approx 120°$ (i.e., $f_S = 1.5 f_0$).

B. Practical Design and Realization

Concerning the design of the multi-cell converter with the key specifications as given at the beginning of section 2 (rated power 2kW in a four cell arrangement) the specifications of the DC-DC isolation stage are defined by:

DC input voltage:	U_1	=	100V (80...120V)
DC output voltage:	U_2	≈	U_1 (1:1 transf. ratio)
rated power:	P_N	=	500 W
switching frequency:	f_S	≈	100 ... 125 kHz.

For the two power MOSFETs the SiliconMAX®-devices PSMN035-150P (TO220 type package, 150V, 35mΩ) have been chosen. The gate drive is performed using an IR2113 driver circuit with additional turn-off speed-up using two PNP transistors BC327 to enhance the discharge of the MOSFET gate. The center tapped rectifier on the secondary side of the transformer is equipped with a MUR1640 (2x8A, 400V) diode.

The power transformer is, as already mentioned at the beginning of section 3, realized by application of the ″bow winding principle″, i.e., the primary winding is formed by $N_1 = 5$ copper bows (∅2.5mm) on the selected E42/21/20 ferrite core (material: N87). The secondary windings ($N_2 = 2$ x 10 turns to get a 1:1 voltage transfer ratio of the converter, ∅1mm) are implemented using conventional winding techniques. A coil former of specific shape (cf. **Fig.7**) is applied to get a compact transformer design and to guarantee the required creepage and clearance distances.

The dimensioning data given before causes a peak flux density of $\hat{B} \approx 100$mT resulting in core losses of

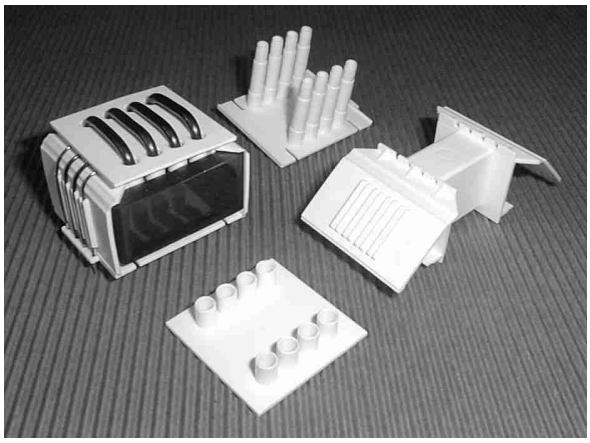


Fig.7: Transformer of the resonant 500W DC-DC converter using ″bow winding″ technique (shown here for N_1=4) for direct PCB mounting and components of the coil former.

$P_{Fe} \le 3\text{W}$ @ ($U_1 = 120\text{V}$, $f_S = 125\text{kHz}$, $T = 100°\text{C}$) as specified by the data sheet. Although the proposed winding technique does not show very tight coupling, the stray inductance of the transformer is too low and a small additional choke (5 turns of litz wire on a single ETD29 leg (half core set)) has to be used for adjusting the natural frequency of the resonant circuit to $f_0 \approx 80$ kHz. With the applied resonance capacitors (2x5x0.1µF polyester foil type components in parallel, $C = 1$ µF) for $f_S = 125$ kHz this results in

$L \approx 4$ µH	$Z_0 = \sqrt{L/C} = 2\ \Omega$
$\frac{f_S}{f_0} \approx 1.5$	$\alpha \approx 120°$
$R_{out} \approx 0.7\ \Omega$	$\hat{u}_C \approx 16$ V @ $I_2' = 4$ A

using the relations of section 3. Concerning R_{out} it has to be noted, that R_{out} specifies the output impedance related to the primary side of the transformer; this value has to be multiplied by $(N_2/N_1)^2 = (10/5)^2 = 4$ for characterizing the output (load-side) behavior of the converter.

C. Laboratory Prototype System – Measurements

The measurements (cf. **Fig.8**) taken from the laboratory model show a close correspondence to the theoretical wave shapes as given in Fig.4 with the exception that the real system shows a significant reverse recovery current $I_{RR} \approx 3.5$A of the rectifier diodes; this matches also with the datasheet specifications of MUR1640 for $di/dt \approx 40$A/µs.

The loss measurements demonstrate an efficiency of 96.3% at rated power (500W) for 110kHz switching frequency (**Fig.9**). The partial load region is characterized by efficiency values up to 97%. It has to be noted that the rectifier diodes contribute to about up to 50% of the total losses. This suggests the application

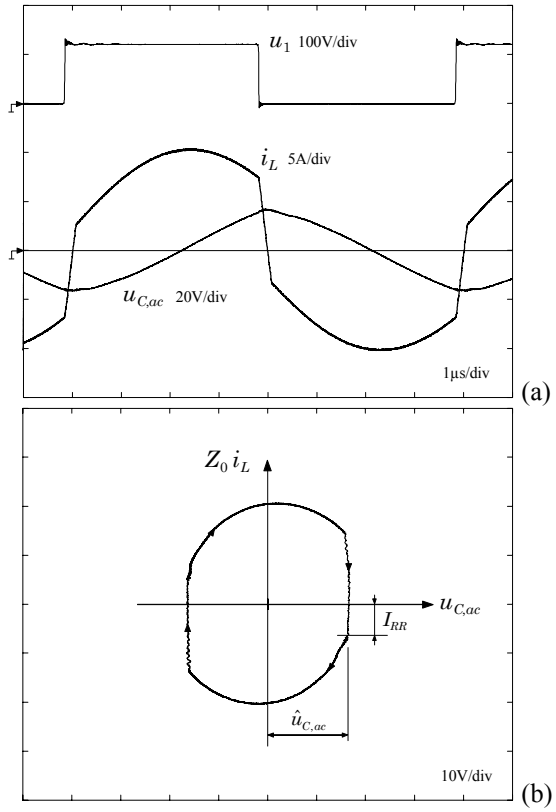


Fig.8: Measured voltage and current wave shapes **(a)** and measured system trajectory **(b)** of the laboratory prototype of the series resonant DC-DC converter; parameters: $U_1 = 120\text{V}$, $f_S = 125\text{kHz}$, $P \approx 440\text{W}$.

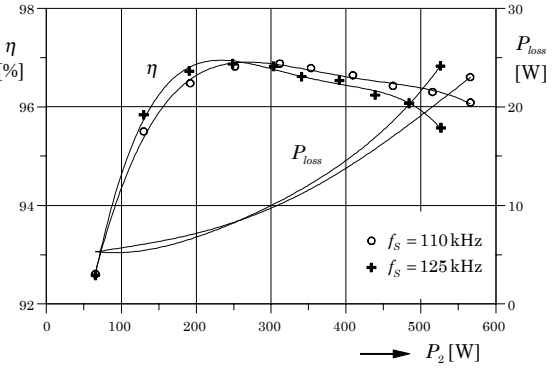


Fig.9: Measured losses and efficiency of the prototype DC-DC isolation stage; parameters: $U_1 = 120\text{V}$.

of synchronous rectification circuit extensions as will be proposed in section 5. Furthermore, the switching losses could be optimized by implementation of a load-dependent interlock delay time of the driver stage or, alternatively, by application of a driver stage with inherent $u_{DS} = 0$-turn-on capability (according to the dual-thyristor principle as described in [3]) to achieve true zero-voltage switching within the total load region.

4. MULTI-CELL DC-AC CONVERTER

For the description of the DC-AC converter for generating the 230V_{rms} AC output of the system it should be referred to a large extent to the analyses of the multi-cell class-D switch-mode amplifier presented in [2]. To give a short summary, it has to be pointed out that the essential benefit of this multi-cell topology is that if the switching cells are operated in an interleaved PWM mode the output current ripple is reduced by a factor of N^2 (N ... number of cells). By application of a second-order LC output filter, the output voltage ripple across the filtering capacitor is reduced by N^3 according to Eqs.(4,5) in [2], i.e., for $N = 4$ the ripple is reduced by a factor of 64! This makes possible to operate the system at a comparatively low PWM switching frequency. For the realized prototype system a single-cell switching frequency of f_{PWM} = 1kHz has been chosen. The interleaved pulse width modulation is performed by a circuit similar to the circuit shown in Fig.6 of [2]. There, flip-flops generate 4 interleaved rectangular signals feeding the inputs of 4 analog integrator stages. At the integrator outputs 4 phase-shifted triangular signals appear which act as carrier signals for the PWM comparators.

Simple low-cost optocouplers (SFH606) are used to provide the required isolation between the PWM generator and the (floating) driver stages of the switching cells. The auxiliary supply of the gate drive circuits (IR2111) is by small 0.5W standard DC-DC converters. The power consumption of the total control board (incl. driver stages) for the multi-cell converter has been measured to be ≤1.8W.

Due to the 1:1 voltage transfer ratio of the DC-DC converter the power stages of the DC-AC converter can be equipped with the same type of MOSFET (4x4=16 pcs. of PSMN035-150P devices). The measurement results of the prototype system illustrate the multi-level voltage generation of this multi-cell topology (cf. converter output voltage u_{PWM} in **Fig.10 (a)**). The ripple of the current i_F through the output filter inductor (L≈2mH) shows nodes being typical for a multi-level approach (Fig.10 (b)). Across the filter capacitor (C=3µF) there appears the very smooth AC output voltage u_O of the system. As indicated by the Fourier-analysis of the unfiltered output voltage u_{PWM} (**Fig.11**) significant harmonic components exist only in the vicinity of multiples of $2Nf_S$, i.e., here for f_S = 1 kHz, in the vicinity of 8 kHz, 16 kHz,... due to the cancellation of all lower frequency components according to the interleaved PWM mode.

As indicated by **Fig.12**, the DC-AC converter shows the expected excellent efficiency due to the low $R_{DS,on}$ of the power transistors in connection with the almost negligible switching losses. However, it has to

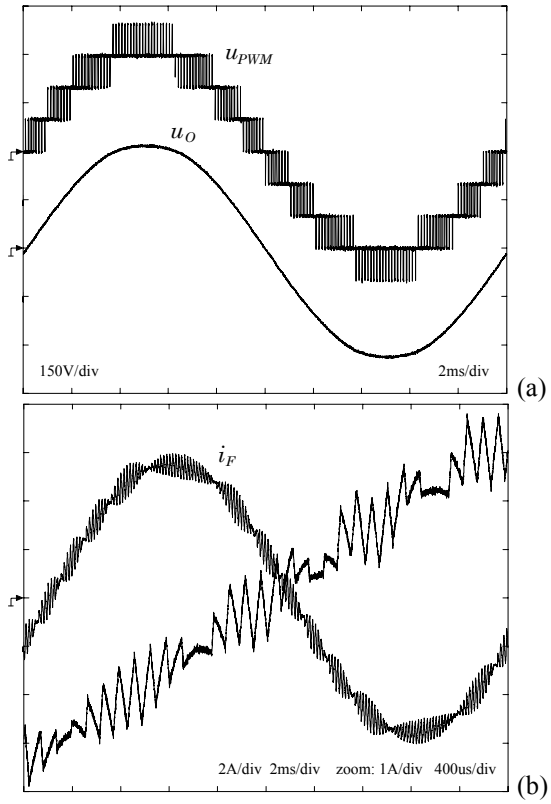


Fig.10: AC output voltage (u_{PWM} : before filtering, u_O : after LC-output filter having ≈2kHz roll-off frequency **(a)** and output filter inductor current **(b)** of the DC-AC converter laboratory prototype; parameter: f_S = 1kHz.

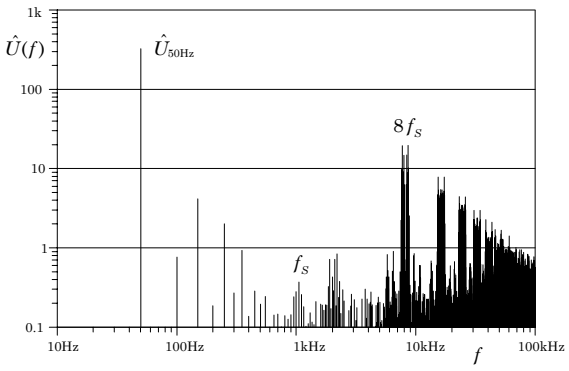


Fig.11: Frequency components of the unfiltered converter output voltage u_{PWM} . The harmonics in the frequency range 100...700Hz are due to an non-ideal behavior of the duty-cycle limiting stage which is required to guarantee the operation of the charge-pump of the IR2111 driver).

be noted that the accurate measurement of the losses of ultra-efficient converters requires a very precise testing equipment; even very low measurement errors show serious impact on the resulting efficiency/loss characteristic of the tested converter. Especially for the case that prototypes of different systems are tested using different measurement equipment, the measurements and the comparison of the results should be performed very carefully.

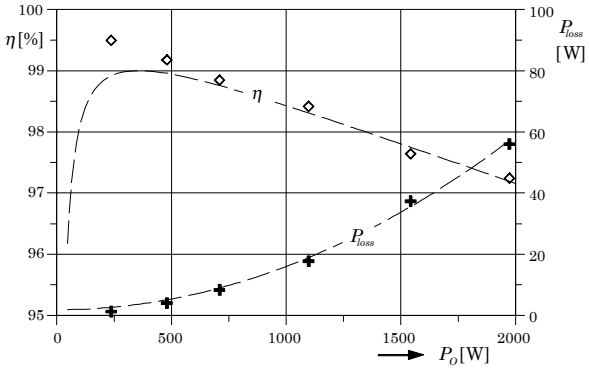


Fig.12: Efficiency and losses of the DC-AC converter. The characteristics shown by the dashed curves give an approximation based on an ideal 230V voltage source with 0.75Ω output resistance and 1.8W permanent no-load losses. Furthermore, the diagram demonstrates the sensitivity to measurement errors especially for very high efficiency values because the dashed curve in any case defines an upper limit for the efficiency.

5. CONCLUSIONS – FUTURE DEVELOPMENTS

With the proposed multi-cell multi-level converter topology energy conversion to the mains voltage level ($230V_{RMS}$) is possible using exclusively MOSFETs with comparatively low rated voltage. These devices are characterized by a very low on-state voltage drop which results in low conduction losses. Due to the interleaved switching of the individual cells the output voltage ripple of the total system is small and therefore, good mains behavior (i.e., low mains current harmonics) can be achieved although the pulse width modulation of a single cell is based on a low switching frequency (low switching losses). Consequently, there result very low total losses and the converter shows very high efficiency.

Because the voltage control of the system is performed by PWM of the DC-AC converter, the DC-DC converter being required for feeding the floating DC-AC stages can be realized by application of an uncontrolled fixed frequency series-resonant topology using equal MOSFET devices as for the DC-AC converter.

The high quantity of required power semiconductor devices (e.g., 24 transistors plus 12 half bridge driver circuits for the designed 2kW prototype) might be seen as a drawback of the proposed topology. However, on the other hand this does allow the application of low-cost standard power semiconductors; the low total losses distributed to a high number of power transistors (i.e., the more uniform heat distribution) significantly simplifies the system cooling. To demonstrate this circumstances it should be mentioned that the prototype DC-AC converter can be operated at 50% of the rated power (1kW) without any heat sink!

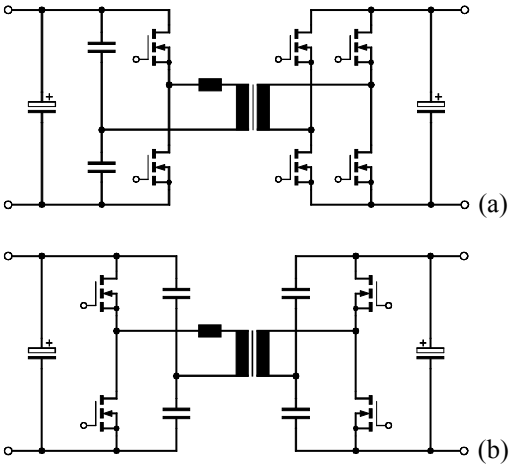


Fig.13: Extension of the resonance-mode DC-DC converter to synchronous rectification **(a)** and to bidirectional operation **(b).**

As already mentioned in section 3, concerning future developments it would be of interest to apply synchronous rectification to the DC-DC isolation stages because the on-state losses of the diodes contribute considerably to the total system losses. In this case, however, it would be preferable to change to a full bridge circuit as shown in **Fig.13 (a)** due to the higher efficiency caused by the basic physical characteristic of majority-carrier based semiconductors (in theory $R_{DS,on} \infty U_{DS,\max}^{2.6}$) and to allow the application of transistors of same type for the input and output sections of the converter.

In principle, the converter of Fig.13 (a) also permits a bidirectional power flow. This operation mode would be of interest if the system is utilized for super-capacitor or battery based systems (e.g., uninterruptable power supplies, power flow equalizer systems etc.) to re-charge the energy storage device on the DC input. It should be mentioned, that the DC-AC converter using the proposed multi-cell arrangement itself intrinsically permits a full four-quadrant operation. (This is of special importance also for reactive power generation if the system is used for stand alone applications being not connected to the mains.)

However, the converter of Fig.13 (a) does provide a DC current path on the secondary which might result in a saturation of the core. This can be avoided by application of a secondary side blocking capacitor or, alternatively, by splitting up the resonance capacitor to both transformer windings as shown in Fig.13 (b).

In this connection, finally the multi-cell converter topology also should be proposed for non-isolated solar power systems as shown in principle in **Fig.14**. Despite the fact that the solar panels show significant common mode voltages (which, however, may be lowered by current compensated input chokes) and

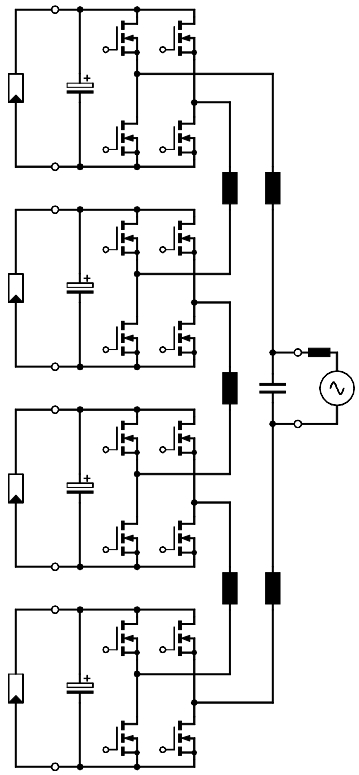


Fig.14: Application of the multi-cell topology to non-isolated solar converter systems.

that a relatively complex control is required to achieve low AC harmonics also for different DC input voltages, this topology could gain attention due to its ultra-high efficiency. Furthermore, this system might be also of interest for realizing as distributed power converter in photo-voltaic applications.

ACKNOWLEDGEMENT

The authors are very much indebted to the "*Hochschuljubiläumsfonds der Stadt Wien*" for the generous support of this research activity.

REFERENCES

[1] **A. C. Rufer, N. Schibli, Ch. Briguet,** "A Direct Coupled 4-Quadrant Multilevel Converter for $16^2/_3$Hz Traction Systems", *Proc. of the 6th Int. Conf. on Power Electronics and Variable Speed Drives*, Nottingham, UK, 23–25 Sept., pp. 448–453, 1996.

[2] **H. Ertl, J. W. Kolar and F. C. Zach**, "Analysis of a Multi-Level Multi-Cell Switch-Mode Power Amplifier", *Proc. of the 41st Int. Conf. on Power Electronics and Intelligent Motion*, Nürnberg, Germany, June 6–8, pp. 491–497, 2000.

[3] **Y. Cheron, T. Meynard and C. Goodman**, "Soft Commutation", *Chapman & Hall (Kluwer Academic Publishers),* Dordrecht, 1992.