Dimensioning and Control of a Switch-Mode Power Amplifier Employing a Capacitive Coupled Linear-Mode Ripple Suppression Stage

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Abstract – A new power amplifier system focused mainly on EMC testing applications is analyzed. The proposed topology consists of a three-level switching power amplifier connected in parallel with a capacitive coupled linear stage which absorbs the output current ripple of the switch-mode stage resulting in an almost ripple-free output voltage of the total amplifier.

This concept alternatively can also be interpreted as a switch-mode power amplifier with a hybrid output filter consisting of a passive LC-circuit and of a linear amplifier which compensates the voltage ripple appearing across the filter capacitor (resulting from the ripple current of the switch-mode stage).

The design of the linear amplifier has to be performed only regarding the ripple voltage and the ripple current of the passive filter part. Consequently, the rated power of the amplifier and the appearing losses become low as compared to the output power of the total system. A further advantage of the concept is that the output impedance of the total system will be determined mainly by the linear stage. Therefore, contrary to conventional switch-mode amplifiers where the output filter significantly worsens the output impedance, the presented system concerning this property (which especially is important for EMC testing applications) almost is equivalent to a pure linear power amplifier which, however, would show a much lower efficiency. The paper describes the operating principle of the system, specifies the fundamental relationships being relevant to the circuit design and analyzes the control behavior of the switch-mode stage as well as of the linear circuit part.

1. INTRODUCTION

Linear power amplifiers today are still in the market for various scientific and measuring applications also at higher (kVA) power levels. These amplifiers are characterized by a very high output voltage quality (low distortion, large bandwidth) as well as by a very low output impedance. Unlike switch-mode systems, the output voltage of linear power amplifiers is not impaired by switching frequency ripple, subharmonic frequency components, blanking distortion and increased output impedance. The advantages mentioned before, however, are of importance especially for the generation of artificial mains voltages for the EMC test according to, e.g., IEC 1000-3-2.

A substantial drawback of the linear power amplifier, however, is that its efficiency is limited to $\pi/4 = 78\%$ even for the ideal case (i.e., maximum output voltage amplitude and pure ohmic load, which hardly ever can be obtained in practical applications) caused by high dissipative losses. These losses are a direct consequence of the "linear regulator" operating principle and, therefore, cannot be reduced, e.g., using "better" output power transistors.

In order to improve the efficiency of linear power amplifiers, therefore, switch-mode circuit enhancements have been proposed for the first time in the early 1980ies [1-3]. The basic idea of such Switch-Mode Assisted Linear (SMAL) amplifier systems (which in the meantime have been reported in many variants especially in realizing the switching stage in literature [4-11] and which sometimes also are denoted as "composite" or "hybrid" amplifier) is that a switch-mode stage is arranged in parallel to the linear power amplifier (**Fig.1a**) and controlled in a way, that

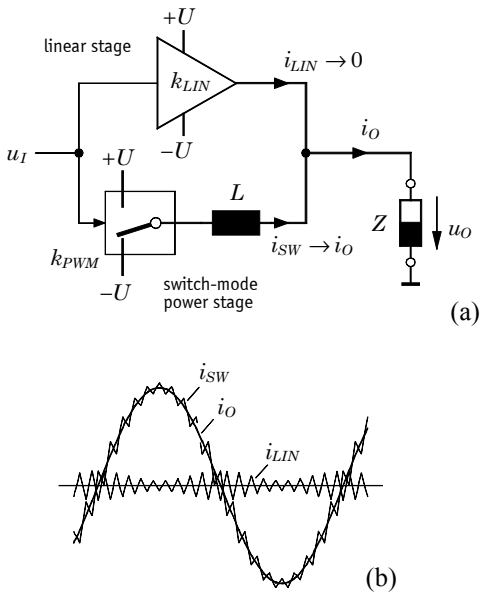

Fig.1: Switch-mode assisted linear power amplifier consisting of a switching stage arranged in parallel to the linear amplifier **(a)** which is controlled such that its output current i_{SW} closely follows the load current i_O **(b)**.

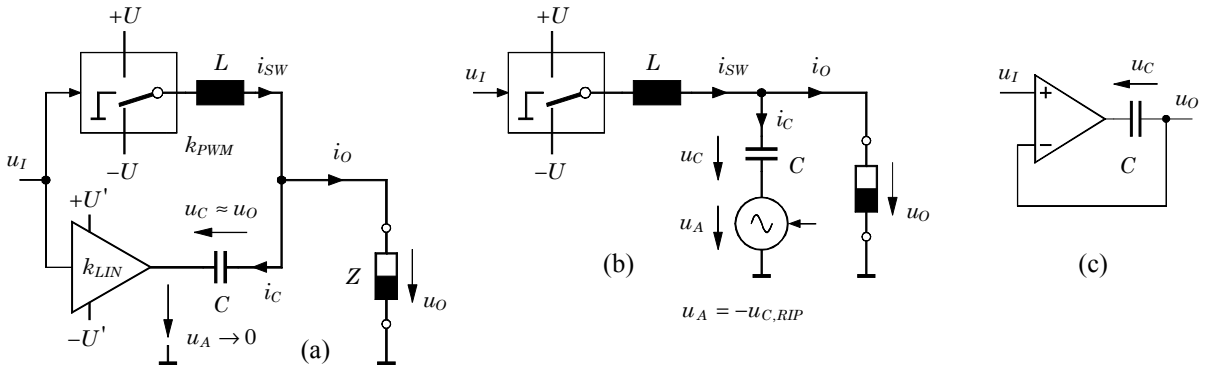

Fig.2: (a): Extension of the basic SMAL principle (insertion of a coupling capacitor C); **(b)**: alternative view of the concept: auxiliary correction voltage u_A compensates the switching frequency ripple of the filter capacitor of a conventional switch-mode power amplifier; **(c)**: extension of the feed-back loop of the linear stage to include the coupling capacitor C.

its output current i_{SW} closely follows the load current i_O (Fig.1b). Hence, the linear stage output current i_{LIN} is minimized to the ripple and to the control error of the switch-mode stage which considerably reduces the losses of the linear amplifier as calculated in [5,6]. Regarding the output voltage behavior the linear stage acts as the guiding master because u_O is defined by its very low inner impedance. On the other hand, concerning the power flow the switching stage can be seen as master which has to be dimensioned to the total system output power whereas the linear stage acts as a kind of active filter compensating the switching frequency ripple. In the stationary case, therefore, the linear amplifier only has to be designed with respect to the ripple current of the switching stage, being typically in the range of 10...20% of the maximum load current for practical realizations. Due to the fact that the linear amplifier generates the entire output voltage of the system, its rated power results to about 10...20% of the total output power.

A major advantage of the basic SMAL concept is, that the transient behavior of the total amplifier unit is given by the linear stage. Assuming proper design of the linear part, very high du/dt -rates can be achieved at the output. This is true for the small-signal behavior but also for large output voltage swings because the linear and switch-mode parts are fed by the same DC supply voltages $\pm U$. (In case of large transients the control error simply dynamically leaves the tolerance band of the current control due to the limited slew-rate of the switching part which, however, has no impact on u_O , cf. Section III of [6]).

2. Capacitive Coupled Linear Stage Basic Concept

For the amplifier used in EMC testing applications as mentioned in the introduction usually output voltage levels of up to 400...500V and a bandwidth of typically 5...10kHz would be required. This leads to DC supply voltages in the range of $U = \pm 500...600$V. The property of the basic SMAL concept which gives the excellent large-signal behavior as described in the previous paragraph now shows up in a realization drawback. As the high operation voltages in generally are no significant problem for the implementation of the switching stage (especially if three-level topologies are used), this causes a serious difficulty for realizing the linear amplifier originated primary by the lack of proper high-voltage complementary power transistors.

To further reduce the rated power of the linear stage and to avoid its specific high-voltage design, therefore, a switch-mode assisted amplifier topology shall be proposed where the linear stage is connected to the load employing a coupling capacitor C as shown in **Fig.2a**. The task of this capacitor is to block off the fundamental load voltage u_O from the output of the linear stage but to act as a by-pass to absorb the ripple current from the switching stage such that the load current becomes almost free of ripple. The switch-mode stage is controlled in a manner that the (fundamental) capacitor voltage u_C closely follows u_O , i.e., that the output voltage u_A of the linear stage is minimized. Actually, the linear stage takes on the output ripple current of the switch-mode part and compensates the switching frequency voltage ripple appearing across C . Remark: The system can also be interpreted as a switch-mode power amplifier with a hybrid output filter consisting of the passive LC filter circuit where the voltage of the lower capacitor terminal is regulated by an auxiliary voltage source u_A in such a manner, that the capacitor voltage ripple is compensated (Fig.2b).

With the proposed concept it is not required to design the linear amplifier for the high supply voltage $\pm U$ of the switch-mode stage. Because the linear amplifier only has to generate output signals with the magnitude of the switching frequency component of u_C , its supply voltage $\pm U'$ can be chosen much lower as compared to the basic SMAL concept. For a practical application a supply voltage of typ. 10...20% of $\pm U$ would be sufficient. Considering that the linear stage also has to be designed only with respect to the ripple current of the switching stage (i.e., typically

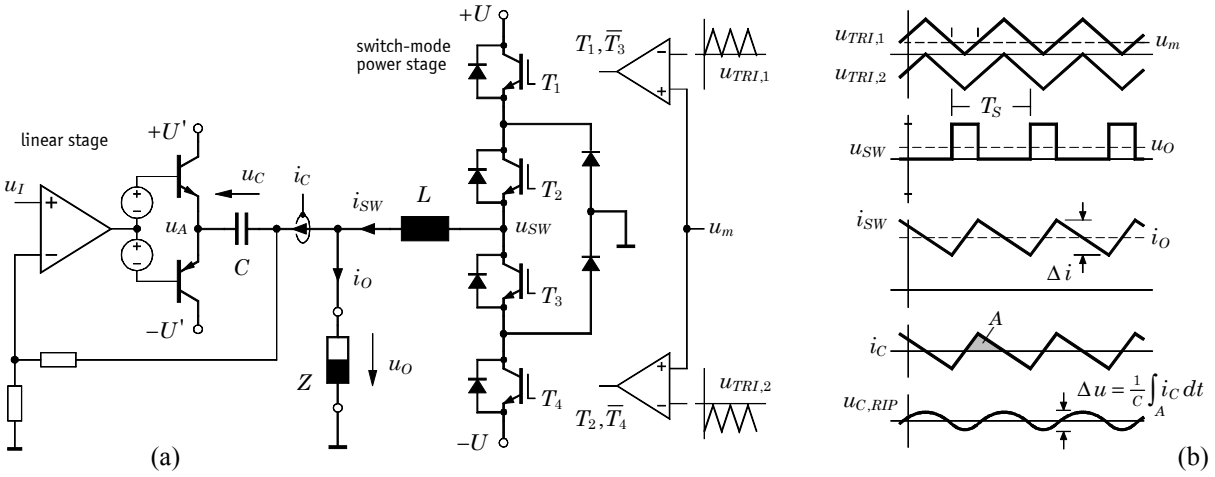

Fig.3: Circuit diagram **(a)** and characteristic voltage and current signals **(b)** of the proposed power amplifier (switching stage realized by a center point clamped three-level branch).

10...20% of the load current, as mentioned in section 1) it finally shows a rated power in the amount of only 1...4% of the output power of the total system.

In order to achieve the desired low output impedance of the complete system it is of substantial importance that the coupling capacitor C is included into the feed-back loop of the linear stage as indicated by Fig.2c. With this the impedance of the capacitor is reduced by the loop gain of the amplifier as will be described in depth in section 5.

3. THREE-LEVEL SWITCH-MODE STAGE STATIONARY OPERATION

As already mentioned in the previous section, a DC link voltage level of ≈ ±500V is required for generating AC output signals of 400V amplitude. If, therefore, the switch-mode stage is realized employing a two-level converter topology, power semiconductors of ≈1200V blocking capability would be necessary. Unfortunately, such high-voltage devices today in general are focused mainly to drive applications where switching frequencies of 10...20kHz are sufficient. For the realization of a switch-mode power amplifier with a projected bandwidth of up to 10kHz, however, a switching frequency of up to 100kHz is required which leads to very high switching losses if 1200V devices are applied. For the switching stage of the proposed amplifier, therefore, a three-level topology shall be utilized (**Fig.3**). This allows the application of 600V transistors and diodes being available as high-speed devices mainly driven by requirements for power factor control (PFC) and switch-mode power supply (SMPS) applications.

In addition to the higher basic switching frequency the three-level technique also halves the voltage ripple at the output of the switching branch which further reduces the ripple of i_{SW}. Although this ripple has no direct influence on the output voltage u_O because it is "absorbed" by the linear stage, a low ripple still is of importance because its amplitude Δi determines the required supply voltage $\pm U'$ of the linear stage and influences also its losses.

Within the scope of this paper a power amplifier system according to the following key specifications shall be dimensioned briefly:

output voltage:	$u_{O,\max}$	= ±400V
output current:	$i_{O,\max}$	= ± 20A
average output power:	P_O	= 4kW
bandwidth:	f_G	≈ 10kHz
switching frequency:	f_S	= 100kHz
DC supply voltage:	U	= ± 500V

Using the modulation index $m = u_O / U$ (output voltage related to the DC link supply voltage) the ripple current amplitude is calculated as

$$\Delta i = \Delta i_{\max} 4\left[|m| - m^2\right] \quad \text{with} \quad \Delta i_{\max} = \frac{U}{4 f_S L} \,, \quad (1)$$

valid for $m = -1...+1$. Choosing $L = 250\mu\text{H}$, the maximum ripple current amplitude results in $\Delta i_{\max}$ = 5A appearing at $m = \pm 1/2$ (cf. **Fig.4**). The ripple amplitude of the capacitor voltage is determined by integrating the shaded area "A" of Fig.3b

$$\Delta u = \frac{\Delta i}{8 f_S C} = \frac{U}{8 f_S L C}\left[|m| - m^2\right] \,. \quad (2)$$

With $C = 0.25\mu\text{F}$ the maximum ripple voltage results in $\Delta u_{\max} = 25\text{V}$ which has to be compensated by the

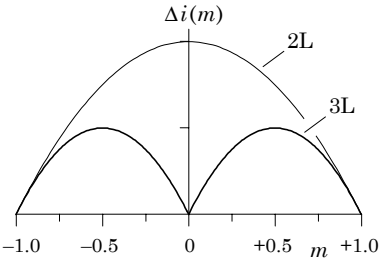

Fig.4: Ripple current amplitude in dependency of the modulation index for two-level and three-level mode.

linear stage in the stationary case. As opposed to two-level topologies here the ripple quantities approach zero for small output voltages $u_O \to 0$ ($m \to 0$) which giving an additional advantage of the three-level structure. The selected elements define an LC filter with a cut-off frequency of $f_0 = 20\text{kHz}$ and a characteristic impedance of $Z_0 \approx 32\Omega$.

4. CONTROL OF SWITCH-MODE STAGE

Basic Control. The output voltage of the total amplifier is, as already mentioned, defined by the linear stage and its feedback loop. The task of the switch-mode stage control is to achieve $u_C = u_O$ as close as possible to minimize the output voltage $u_A = u_O - u_C$. In the simplest way this can be performed by a control structure according to **Fig.5**. The control signal u_m of the pulse width modulator (PWM) there is mainly formed by the amplifier input voltage u_I in combination with the output voltage u_A of the linear stage. Due to the applied regular sampling PWM using $\hat{u}_{TRI} = \pm U$, the modulator functionally can be replaced by a pure unity-gain zero-delay stage and the fundamental component of u_{SW} directly follows the control signal u_m [12,13]. For achieving an adequate damping, a feed-back path of the capacitor current is implemented where the feed-back coefficient R emulates the behavior of an ohmic damping resistor (without, however, any additional losses). To eliminate the load current dependency moreover a feed-forward path $L\, di_O/dt$ is added. Furthermore, it shall be assumed that the output voltage u_O follows its reference value u_I in an idealized manner (i.e., idealized linear stage control $u_O = u_I$). With this, and using the relations $U_A = U_O - U_C$ and $I_C = sC \cdot U_C$ the capacitor voltage transfer function follows to

$$U_C = U_O \frac{1}{s^2LC + sRC + 1} \quad . \tag{3}$$

Choosing $R = \sqrt{L/C} = Z_0$ this 2nd-order low-pass filter with a cut-off frequency of $\omega_0 = 1/\sqrt{LC}$ shows Butterworth-response, i.e., U_C follows U_O in a maximum flat manner. Using $U_A = U_O - U_C$ the frequency of the linear stage output voltage shows a 2nd-order high-pass characteristic

$$U_A = U_O \frac{s^2LC + sRC}{s^2LC + sRC + 1} \quad . \tag{4}$$

Equations (3) and (4) indicate a kind of transition between the two amplifier stages. For higher frequencies the linear stage increasingly takes over the generation of the total output voltage u_O. There, however the output voltage level is limited to the reduced supply voltage $\pm U'$ of the linear stage.

Remark: As far as the linear stage does not run into clipping mode (i.e., limitation of u_A due to the low supply voltage $\pm U'$) its bandwidth exclusively defines the frequency limitations of the whole amplifier system although the switch-mode part (with its lower bandwidth given by the LC filter components)

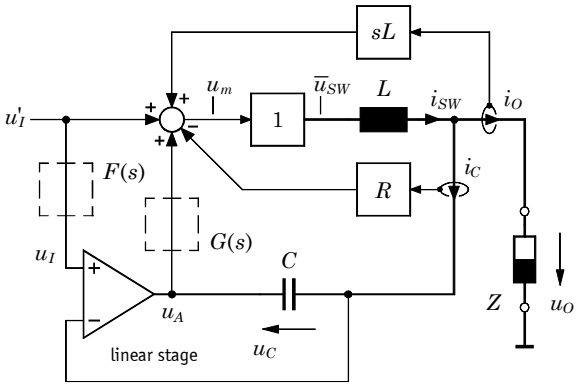

Fig.5: Equivalent schematic diagram of the amplifier's control structure.

operates as an efficient power supporting unit. In fact the linear stage compensates the voltage drop of the LC filter which becomes higher and higher for increasing frequencies. Hence, the small-signal bandwidth of the concept is defined by the linear part, the large-signal (power) bandwidth, however, is given by the cut-off frequency of the LC filter of the switching part. It should be noted that the proposed system actually is a switch-mode power amplifier enhanced by a low-power linear-mode *correction* stage.

Auxiliary Signal Filter Path. The nonlinear behavior if the linear stage runs into clipping mode as described before may not be acceptable for several applications. These clipping distortions, however, can only be avoided in a way that the bandwidth of the whole system is limited to the value specified by the LC filter. This can be achieved simply by insertion of an auxiliary filter $F(s)$ into the linear stage signal path (Fig.5). If the frequency response of $F(s)$ is fixed to

$$F(s) = \frac{U_I'}{U_I} = \frac{1}{s^2LC + sRC + 1} \quad , \tag{5}$$

the linear stage shows a frequency behavior equal to the switch-mode part. With this additional filter the equations (3) and (4) are modified to

$$U_C = U_O \quad \text{and} \quad U_A = U_O - U_C = 0, \tag{6}$$

i.e., the actual linear amplifier voltage u_A in this case shows only the switching frequency component Δu calculated by eq. (2). The total amplifier system now is characterized by a low-pass filter response with cut-off frequency ω_0 and a 2nd-order roll-off (of Butterworth-type if $R = Z_0$ is valid) as given by eq. (5).

PI-Type Control. The control structure as discussed so far is based on an idealized pulse width modulator and switching part to guarantee that the fundamental output voltage of the switching branch follows the control voltage in a perfect manner. Due to variations of the DC link voltage $\pm U$, voltage drops across the semiconductor devices and pulse width distortions as

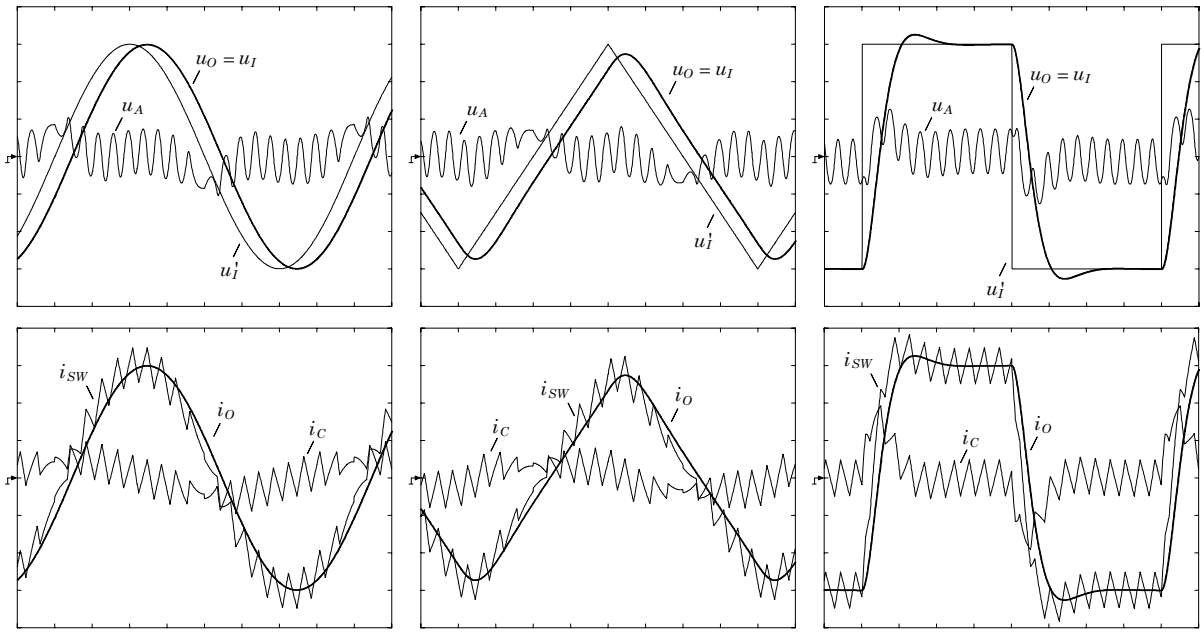

Fig.6: Voltage (top) and current (bottom) wave shapes of the proposed amplifier system (5kHz sinusoidal, triangular and square wave response, amplitude: ±300V); due to the implemented auxiliary signal path filter (see text) any clipping of the linear stage is avoided and u_O precisely follows the reference signal u_I'; scales: 100V/div (u_A:20V/div), 5A/div, 50µs/div.

a consequence of the blanking time delay (required to prevent cross-conduction of the power transistors), $\overline{u}_{SW} = u_m$ can be achieved for practical systems only with an accuracy of typ. 2...5%. At a first glance this does not seem to be a major problem since the voltage generation error of the switching stage is compensated by the linear stage. The amount of u_A required to correct this stationary error, however, reduces the operating range for the intended ripple voltage compensation. To avoid that there appear undesired static or low-frequency components of u_A as a result of the non-ideal switch-mode stage behavior, the basic control structure is extended by an additional PI-type control path $G(s) = (1+sT)/sT$ as indicated in Fig.5. With this, the low-frequency components of u_A are reduced by the additional gain of the $1/sT$ branch. Considering $G(s)$, the disturbance transfer function now shows a 3rd-order response. For the dimensioning of T this dynamic response can be optimized, e.g., for flat-top response. A more detailed analysis shall be omitted here, however, for the sake of brevity.

As indicated by the simulations presented in **Fig.6**, the proposed control gives a good dynamic response of the considered system (dimensioning as specified in section 3) avoiding any clipping of the linear stage. In order to optimize the square wave response the damping has been chosen to $R = \sqrt{2}\,Z_0 = 45\Omega$ here, the integration acting time of the PI-type controller $G(s)$ has been adjusted to $T = 50\mu s$ (cf. $T_0 = \sqrt{LC} = 7.9\mu s$ which gives $f_0 = 1/(2\pi T_0) = 20kHz$ as filter cut-off frequency). The presented wave shapes are given for different output signals of $\hat{u}_O = 300V$ amplitude fed into a pure ohmic load of $Z = 20\Omega$ (4.5kVA peak power level). The u_A-traces demonstrate that the output voltage of the linear part is limited to ≈ ±30V at which maximum peak current levels up to ±10A appear. Consequently, a supply voltage level of U'= ±50...±80V is sufficient for realizing the linear power amplifier. Therefore, a concept basically known from audio power amplifiers of approximately 200...300W output level would be adequate. However, the dynamic behavior has to be improved as compared to audio systems because for the principle proposed here it is of significant importance that the linear stage shows a very low output impedance not only in the frequency region of u_O but also for the switching components in order to guarantee a low noise level which shall be discussed in the following section.

5. LINEAR POWER STAGE DESIGN

Output Impedance – Basic Approach. According to the basic operating principle of the proposed amplifier the linear stage has to show a very low output impedance Z_{OUT} because it determines the remaining noise voltage at the load $U_{noise} \approx \Delta I \cdot Z_{OUT}$. In fact, $Z_{OUT} << Z$ must be valid to guarantee that the linear part efficiently shunts the ripple component of i_{SW}. Different to the basic SMAL concept as described in [4-6] Z_{OUT} is formed here not only by the linear amplifier stage itself but includes also the coupling capacitor's reactance $X_C = 1/(\omega C)$, which in general is dominant also in the switching frequency region. To get a sufficiently low output impedance, therefore the feedback loop of the linear stage includes also the capacitor C as mentioned (cf. **Fig.7a**). With this, X_C

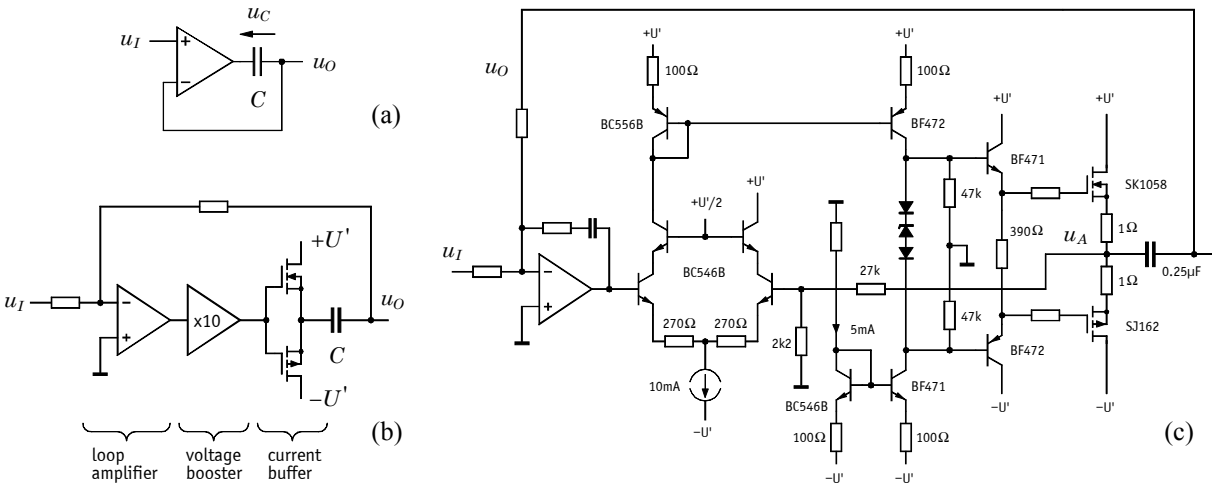

Fig.7: Linear power stage design. **(a)**: Basic circuit structure (feedback loop includes coupling capacitor C); **(b)**: Realization principle consisting of loop amplifier, voltage booster and current buffer; **(c)**: Schematic circuit diagram.

is lowered by the loop gain. If – for a first approximation – the frequency characteristic of the amplifier is interpreted to have a gain-bandwidth-product of ω_T and shows a –20dB/dec. roll-off (e.g., typical for "common use" operational amplifiers) the output impedance is calculated to $Z_{OUT} = 1/(\omega_T C)$ being ohmic ($Z_{OUT} = R_{OUT}$ = const.!) as a result of the amplifier's 1st-order roll-off. To give a numerical example: For $C =$ 0.25µF ($X_C = 6.4\Omega$ at $f_S = 100$kHz) as chosen in section 3 an amplifier with $f_T = 4$MHz would lead to $R_{OUT} = 0.16\Omega$ resulting in a peak-to-peak noise voltage of 0.8V for $\Delta I = 5$A. However, this simple calculation only gives a first estimate of the expected noise amount. A more detailed consideration (as will be presented at the end of this section) also has to include the amplifier's output impedance and the more complex frequency roll-off of the linear power stage.

Linear Power Stage. According to Fig.7b the actual linear power stage is formed by the parts (i) loop-amplifier, (ii) voltage booster and (iii) current buffer. Due to the required high-frequency gain the loop amplifier shall be implemented utilizing a modern operational amplifier, e.g., AD811. The output voltage of such devices, however, is limited to ≈ ±5...10V. Hence, a voltage booster stage is necessary to achieve the mentioned voltage levels ($\hat{u}_A = 40...70$V). As shown in Fig.7c this booster is realized using discrete semiconductors starting with a differential amplifier stage. To achieve a good frequency response a cascode circuit has been implemented which allows the application of low-voltage transistors with high transit frequency. The output current of this stage controls the positive branch of a complementary-type current mirror with the output transistors BF471 and BF472, respectively. These devices – which originally have be intended for video output stages in television sets and monitors – permit high output voltages and give a comparatively good frequency response.

To maximize the bandwidth of the voltage booster the intended gain of 10 (allowing ±50V output voltage for the ±5V control voltage performed by the loop amplifier) is defined "locally" by the 270Ω emitter resistors of the differential amplifier in connection with the 47kΩ collector resistors of the complementary pair and by the 27kΩ/2.2kΩ voltage divider (internal feedback loop). The output stage of the booster is formed by a second pair of BF471/472, however not for voltage amplification but for lowering the driving impedance for the power MOSFETs.

The real output signals of the linear stage, however, are generated by the unity-gain current buffer built up with the complementary power MOSFETs SK1058 and SJ162. These semiconductors have been designed especially for linear amplifier applications. It has to be noted that most state-of-the-art power MOSFETs aim for switching applications and may not be used for linear amplifiers due to hot spot effects [14]. The current buffer is operated in AB-mode. The quiescent current (≈10% of the output current) is adjusted by an appropriate bias voltage in connection with the source resistors of the MOSFETs. The bias voltage is generated by a chain of Zener diodes which are inserted between the collectors of the first BF471/472 pair. The diodes are thermally coupled closely to the MOSFETs and selected carefully regarding their thermal coefficients to give a sufficient thermal stability of the quiescent current.

Output Impedance – Loop Response. Based on the equivalent circuit diagram shown in **Fig.8a** the output impedance of the source follower (which contributes to the intrinsic total output impedance especially in the MHz-region) is calculated to

$$Z_{OUT,SF} = \frac{1}{g_m} \cdot \frac{1 + s R_G C_{GS}}{1 + s \frac{C_{GS}}{g_m}} \qquad (7)$$

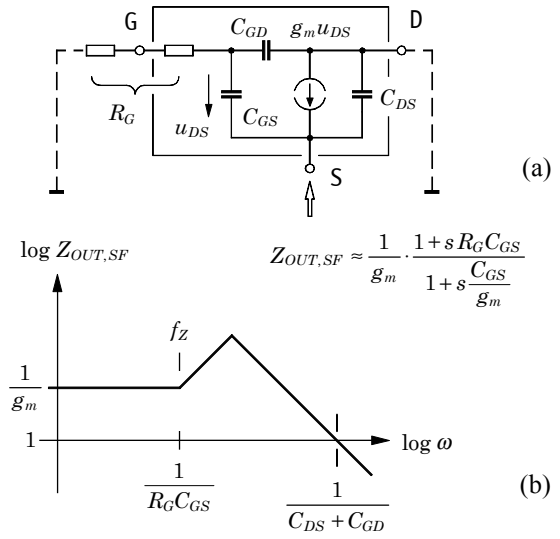

Fig.8: Source follower output impedance. **(a)**: Equivalent circuit diagram; **(b)**: Frequency response.

being valid for low and medium frequencies. For low frequencies $Z_{OUT,SF}$ is defined by the transfer conductance g_m of the MOSFET. The effective gate resistor R_G in connection with C_{GS} of the transistor gives a zero in the frequency response and a +20dB/dec. slope for $f > f_Z = 1/(2\pi R_G C_{GS})$ (Fig.8b). With typical values $R_G \approx 100\Omega$, $C_{GS} \approx 1$ nF this transition frequency is calculated to $f_Z = 1.6$ MHz. To achieve the desired low output impedance in the MHz-region, therefore a low R_G-value in connection with a low inner impedance of the driver seems to be preferable. However, it has to be noted that with very low values (e.g. $R_G = 1...10\Omega$) improper ringing and even permanent oscillations of the current buffer may appear, because R_G also acts as a damping resistor for the parasitic inductances. Beyond the validity of eq. (7) for very high frequencies (e.g., $f > 10...50$MHz), however, the output impedance of the source follower is defined mainly by the capacitances $C_{DS} \approx 300$pF and $C_{GD} \approx 50$pF: $Z_{OUT,SF,HF} = 1/s(C_{DS}+C_{GD})$ (–20dB/dec. roll-off, cf. Fig.8b).

As indicated by **Fig.9** for the components at hand $Z_{OUT,SF}$ shows a value of ≈1.5Ω ($g_m \approx 2$A/V, $1/g_m$ = 0.5Ω + 1Ω source resistor) in the switching frequency region and, therefore, almost can be neglected as compared to the impedance X_C of the coupling capacitor C. The total effective output impedance $Z_{OUT,SF} + X_C$ now is reduced by the loop gain which, therefore, should be as high as possible. This possibility, however, is limited mainly by the frequency characteristic of the voltage buffer stage. As a closer analysis shows, the control performance of this stage can be approximated by a well damped 2nd-order low-pass filter with a cut-off frequency of ≈8MHz, resulting in an effective time constant of ≈20ns. The loop amplifier then has been adjusted to a PI-response with an integration acting time of 40ns which gives an actual open-loop transfer function $F_O(s)$ with a unity

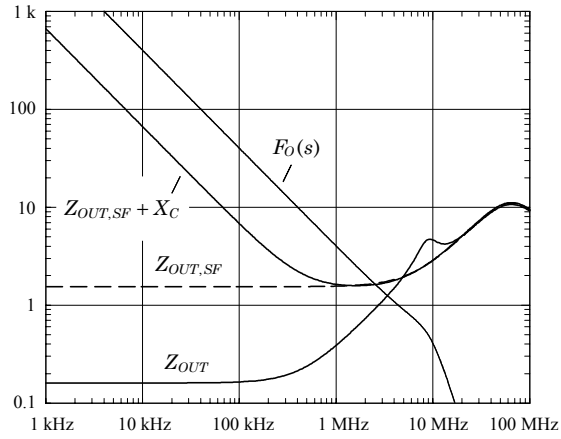

Fig.9: Output impedance of the linear stage; $Z_{OUT,SF}$: open loop, amplifier exclusively; $Z_{OUT,SF}+X_C$: as before, but including coupling capacitor C; Z_{OUT}: total closed loop impedance; $F_O(s)$: open loop gain of control.

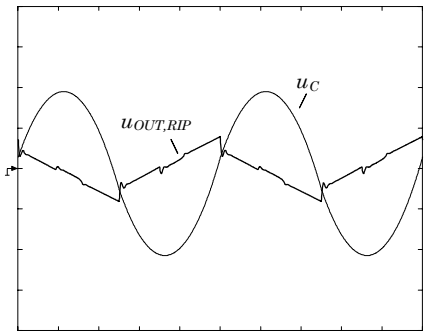

Fig.10: Residual noise voltage ripple $u_{OUT,RIP}$ (0.5V/div) as compared to the voltage ripple u_C across the coupling capacitor C (5V/div); time scale: 2µs/div (f_S = 100kHz).

gain transition of ≈ 4MHz (–20dB/dec. roll-off). With this, the loop gain results in a value of ≈ 40 at 100kHz lowering $X_C = 6.4\Omega$ to an effective output impedance of $Z_{OUT} \approx 0.16\Omega$. This finally leads to a peak-to-peak output noise voltage ripple of 0.8V for $\Delta i = 5$A (cf. **Fig.10**) as derived already from the simplified consideration presented at the beginning of this section.

6. CONCLUSIONS

A novel concept to enhance the output voltage quality of switch-mode power amplifiers especially suited for EMC testing applications has been presented. The proposed topology consists of a three-level switch-mode power stage connected in parallel with an additional capacitive coupled linear amplifier. This auxiliary stage in connection with a proper control forms a low-impedance path in parallel to the load which shunts the ripple current of the switch-mode stage. Consequently, the load current and voltage become almost free of ripple components. By application of the specified control scheme and using an additional signal filter path as well as a feed-forward of the load current the switching stage can be

controlled in a manner that the residual output voltage of the linear stage is minimized to the switching frequency voltage ripple of the filter (coupling) capacitor.

The design of the linear amplifier only has to be performed regarding the ripple voltage and current values of the passive filter part. Consequently, the rated power of the linear amplifier only amounts to about 1...4% of the output power of the total system. Due to the reduced current ripple as a result of the three-level switch-mode stage the maximum losses appearing in the output transistors of the linear stage (which can be determined as a first estimate easily using $P_T = U' \cdot \Delta I / 4$, according to eq. 3 of [6]) for the given dimensioning example are calculated to be only ≈2% of the total output power.

The advantage of the proposed concept is that the output voltage quality and also the output impedance of the total system mainly are determined by the linear stage. Therefore – contrary to conventional switch-mode amplifiers where this impedance is worsened by the output filter – the presented topology concerning this property (which is important especially for EMC testing applications) practically is equivalent to pure linear power amplifiers which, however, show a much lower efficiency. To achieve a low output impedance and a good output voltage quality, however, a high loop gain of the linear stage is required. Because this has to be true also in the switching frequency range, a careful design of the linear stage up to the MHz frequency region has to be performed.

Finally, it has to be noted, however, that the large signal response of the total amplifier is limited to the specifications of the switch-mode part, i.e., the large-signal bandwidth of the system is given by the cut-off frequency of the LC filter components. Due to the reduced supply voltage the linear stage is able to maintain very high dynamics only for the small-signal range. This is different from the basic switch-mode assisted linear amplifier approach where the linear stage provides excellent dynamic output behavior for the full supply voltage range, but at the cost of significantly higher losses.

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