A Novel Method for On-Line Monitoring and Managing of Electrolytic Capacitors of DC Voltage Link PWM Converters

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Abstract – The paper presents a novel concept for monitoring and managing the DC link electrolytic capacitors of PWM converters, especially for drive applications. The unit performs on-line identification of the equivalent series resistance (ESR) of the capacitor in order to detect the end-of-life cycle to permit a preventive maintenance of the converter prior to a capacitor failure. The ESR detection scheme is based on the determination of the capacitor AC losses calculated from voltage/current measurements using a simple single-chip microcontroller. The unit is designed as a small printed circuit board located between the capacitors screw terminals and the converter busbars. This also opens the possibility to easily detect the capacitor's operating temperature which is important for the evaluation of the identified ESR values. The intention is, furthermore, that the monitoring unit operates without a separate power supply and draws its supply current out of the power capacitor. The measurement results of the individual converter capacitors are gathered by an opto-isolated three-wire bus. Finally, besides the ESR detection the monitoring unit further allows an energy efficient capacitor voltage balancing in case a series array of capacitors is used. As opposed to conventional resistor voltage divider networks this method reduces the balancing losses to a very large extent by avoiding high quiescent currents.

The paper gives a short introduction into the life cycle problems of electrolytic capacitors, presents a survey of known monitoring concepts and describes a novel concept based on capacitor power loss determination. Subsequently, a laboratory prototype of the proposed monitoring and managing system based on a single chip microprocessor is demonstrated.

1. INTRODUCTION

Electrolytic power capacitors today form essential components for virtually any power electronic system. Especially modern PWM converters for AC drive applications (cf. **Fig.1**) utilize these components in the DC voltage link for energy storage and to absorb the switching frequency current ripple of the inverter transistors. Unfortunately, due to their electrochemical operating principle, the aging of electrolytic capacitors much more depends on operating and ambient conditions than this is true for the power transistors of the converter. Many capacitor datasheets, e.g. [1], specify that the lifetime approximately is cut into half if the capacitor core temperature is increased by 10°C (this often is denoted somewhat sloppy as *Arrhenius rule*). The capacitor temperature, however, may vary in a wide region during the life cycle of the converter. Consequently, a reliable but on the other hand also cost-efficient lifetime matching of capacitors and semiconductors hardly is achievable. Frequently, electrolytic capacitors are the key components which determine the life cycle of the whole unit and often are responsible for converter breakdown failures. In this connection especially the MIL handbook 217F [2] sometimes is referenced which specifies the failure rate for electrolytic capacitors being approximately twice as high as for power transistors, even at low temperature levels (see Fig.3 in [3] or Fig.1 in [4]).

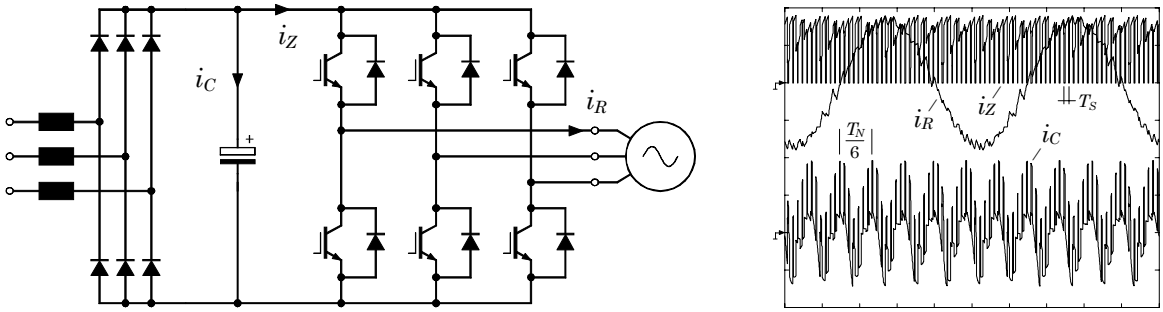

Fig.1: Three-phase AC drive converter with DC voltage link; the DC link capacitor current consists of the switching frequency ripple of the inverter input current i_Z and of a low frequency AC component originating from the diode mains rectifier.

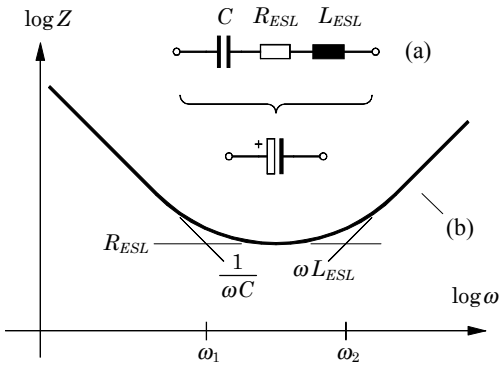

Fig.2: Equivalent circuit diagram (a) and impedance characteristic (b) of electrolytic capacitors.

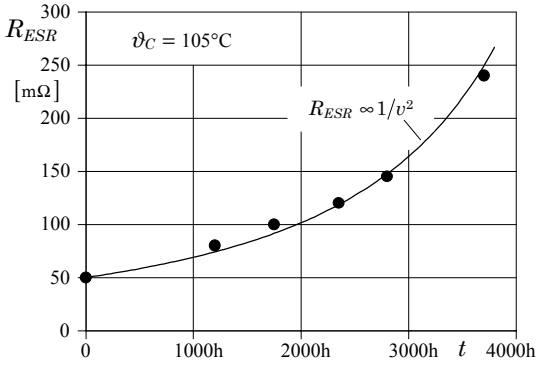

Fig.3: Increase of the equivalent series resistance (ESR) due to electrolyte loss according to Fig.7 of [10].

To avoid these serious failures – which can also cause high consequential costs if, e.g., the converter drive is part of a complex manufacturing process (paper machine etc.) – on-line monitoring units have been proposed which detect the end-of-life status of the capacitor to allow a timely replacement (preventive maintenance). It is well known from literature that the impedance of electrolytic capacitors rises with operating time (e.g, [5, 6]). In [7] a very simple monitoring unit has been proposed, where the AC voltage across the capacitor caused by the ripple current is sensed. If this voltage exceeds a fixed limit, the output comparator of the monitoring circuit signalizes a capacitor "error" condition. The drawback of this simple concept is that the error signal might appear misleadingly also in case of low capacitor temperatures and/or transient current peaks. In fact, no real detection of the aging status can be performed.

A more accurate monitoring requires the identification of the equivalent series resistance (ESR) of the capacitor considering the operating temperature of the component. The increase of the ESR is very pronounced as compared to the capacitance value which is reduced only slightly for increasing operating time (cf. Figs.4a/b in [3]).

2. Electrolytic Capacitor Impedance and Aging Procedure

In the simplest case the impedance $Z(s)$ of an electrolytic capacitor usually is modeled by an equivalent circuit diagram according to **Fig.2a** consisting of a series connection of the pure capacitance C, an ohmic resistor R_{ESR} representing all AC losses (ESR) and a stray inductance L_{ESL} depending on the winding design of the capacitor foils and how the foils are connected to the capacitor terminals (equivalent series inductance ESL): $Z_C(s) = 1/(sC) + R_{ESR} + sL_{ESL}$. The impedance is dominated by a −20dB/dek. capacitor response for low frequencies $\omega \le \omega_1 = 1/(R_{ESR}C)$, by a +20dB/dek. inductance response for high frequencies $\omega \ge \omega_2 = R_{ESR}/L_{ESL}$), and by the ohmic value R_{ESR} for the medium frequency region $\omega_1 < \omega < \omega_2$ (cf. Fig.2b). It shall be noted that the time constant $T_1 = R_{ESR} \cdot C$ varies only in a comparatively narrow region for electrolytic capacitors of highly different capacity and/or voltage ratings. Typically $T_1 = 50...150\mu s$ is valid in practice for almost any capacitor at room temperature. Hence, in practice for frequencies above $f_1 = 1...3kHz$ the impedance is determined by R_{ESR}. Remark: The reason for the approximately constant $R_{ESR} \cdot C$-product is given by the fact that the capacity C is proportional to the area of the capacitor foils whereas the loss resistor R_{ESR} is inversely affected by this area. Similarily, typical upper cut-off frequencies of $f_2 \approx 100...500kHz$ can be calculated from the R_{ESR}/L_{ESL}-values of common electrolytic capacitors for power applications.

Capacitor Aging. The total equivalent series resistance substantially is determined by the electrolyte; the aluminum foils and tabs contribute to it only by a small fraction [8]. During the operating life cycle of the capacitor the electrolyte volume is reduced by vaporization (diffusion through the end seal). The electrolyte loss causes a continuous rise of R_{ESR} according to $R_{ESR} = R_{ESR,0}/v^2$ [9], where $v = V/V_0$ denotes the electrolyte volume related to its initial value. As a rule-of-thumb and specified by many capacitor manufacturers the capacitor will be at the end of its life time if it has lost 30...40% of its electrolyte, i.e., if R_{ESR} has increased by a factor 2...3 [8, 9]. In **Fig.3**, e.g., the ESR rise of a 2200µF low-voltage capacitor is shown; after ≈2000 hours @ 105°C the capacitor already has doubled its initial ESR. Unfortunately, the vaporization/diffusion process of the electrolyte heavily depends on the actual component temperature. This complicates the life cycle dimensioning of the converter to a large extent and reflects the need for on-line monitoring.

ESR Temperature Dependency. In addition to the temperature dependency of the electrolyte loss further also the actual R_{ESR} significantly depends on the temperature. According to [9] an ESR reduction to about 40% can be expected if the component temperature ϑ_C rises from 20°C to 80°C following the relation $R_{ESR,hot} = R_{ESR} \cdot [\, D + Y \cdot \exp(-\vartheta_C / F)\,]$, where the parameters D, Y and F depend on the capacitor type. The reason for the ESR reduction is an increase of the

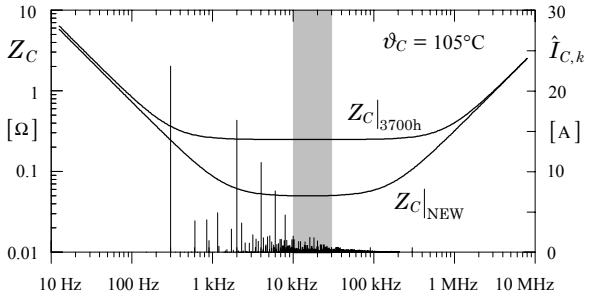

Fig.4: Impedance characteristic of a new electrolytic capacitor according to Fig.3 and at the end of its life cycle; also shown are spectral components of the DC link capacitor current of a 15kW drive converter; shaded area: see text.

electrolytes ion mobility for rising temperatures. As a consequence, a capacitor monitoring unit in any case has to have an accurate temperature sensing device to allow a temperature weighting of the identified R_{ESR} and/or a correction of the R_{ESR} - "reference-value" defining the warning threshold level of the monitoring unit.

3. MONITORING UNIT – BASIC CONCEPTS

All concepts for on-line detection of R_{ESR} described so far utilize the operating current ripple stress of the capacitor as the "testing" signal. In **Fig.4** the harmonic components of i_C are depicted for a 15kW AC drive according to Fig.1. The DC link capacitor shows a pronounced 300Hz ripple originating from the diode rectifier as well as ripple components grouped around multiples of the effective switching frequency (here 2kHz). In the case at hand, especially for ripple components in the range 10...30kHz (indicated by the shaded area of Fig.4) the capacitor impedance Z is defined to a very large extent by R_{ESR}. In [10] therefore a monitoring method has been proposed which consists of capacitor AC voltage and current sensing with subsequent bandpass filtering to extract the signal components of the ohmic impedance region ("frequency window"). Afterwards the value of R_{ESR} is calculated using an analog divider (cf. **Fig.5a**). The drawback of this concept is, however, that on one hand the bandwidth of the filter has to be sufficiently large to avoid the effect that only a few frequency components are evaluated, because this would lead to a large dependency on the actual converter duty cycle. On the other hand the components below and near ω_1 shall be rejected sufficiently in order minimize the influence of the capacitive impedance portion $1/(sC)$. To achieve a good measurement precision a higher order bandpass filter would be required which leads to an analog solution of considerable effort.

Furthermore, drive systems of medium and higher power level usually are operated at switching frequencies in the range of typically 1...5kHz. Hence the signals $i_{C,F}$, $u_{C,F}$ at the output of steep 10...30kHz bandpass filters (where Z is dominated by R_{ESR}) would show comparatively low amplitudes which may cause problems of the following analog RMS-to-DC converter (utilization of the dynamic range). But also a pure digital realization using a signal processor for filtering similar to the system described in [4] is a rather expensive solution mainly due to the fast A/D converters of high dynamic resolution which would be required for the direct real-time sampling of i_C and u_C.

Alternatively, the bandpass filters can be designed much simpler (or can be even avoided) if the influence of the pure capacitive term of the voltage u_C is compensated by an additional network with transfer function $G_C(s) = sT_1/(1+sT_1)\cdot 1/(1+sT_2)$. However, the parameters T_1, T_2 of $G_C(s)$ would have to be trimmed exactly to the capacitor characteristic (similar as the frequency compensation of an oscilloscope probe) and for increased aging a more and more prominent error in the calculated value of R_{ESR} will appear.

Proposed Monitoring Method. To avoid the drawbacks mentioned before, a novel monitoring concept based on a power measurement approach shall be proposed (Fig.5b). According to the equivalent circuit diagram of Fig.2a the total averaged real power drawn by the capacitor is represented by R_{ESR} (the DC losses caused by the capacitor leakage current can be neglected due to the assumed AC coupling of

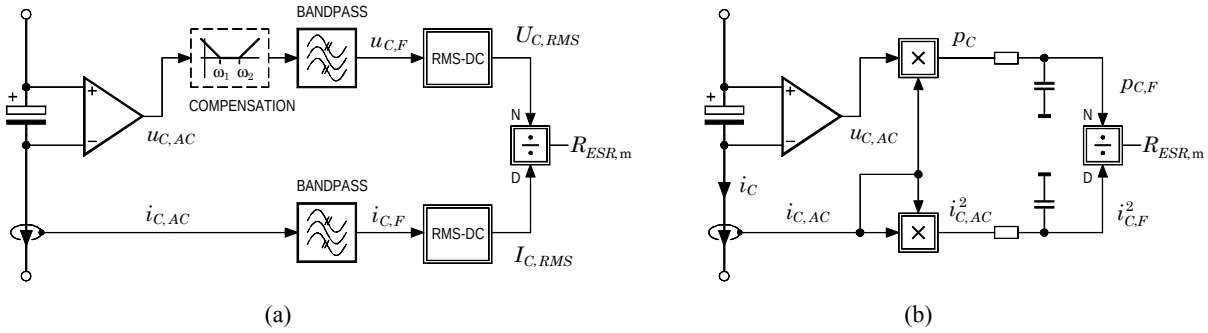

Fig.5: On-Line monitoring of R_{ESR} – basic concepts. (a): Determination utilizing voltage/current signals of the ohmic frequency range of the capacitor [10]. (b): Novel concept which avoids extensive filtering by calculation of the AC power losses of the capacitor.

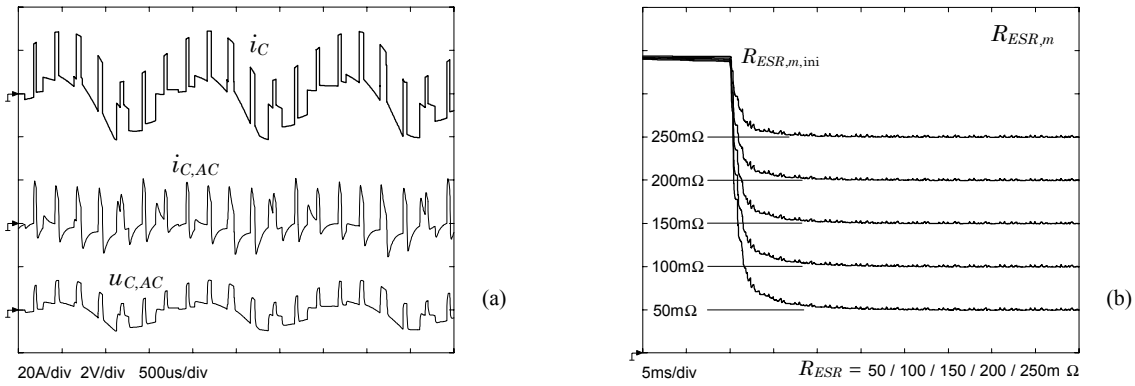

Fig.6: On-Line monitoring of R_{ESR} based on the proposed power measurement approach of Fig.5b. (a): Capacitor current and measurement signals gained by AC coupling and moderate low-pass filtering; (b): output signal of the divider circuit demonstrating the fast and accurate identification of the ESR value (simulation).

the sensing path). The determination of R_{ESR} now is performed in that way that in a first step the instantaneous power p_C as well as the quantity $(i_C)^2$ are derived via multipliers using the measurement signals $u_{C,AC}$ and $i_{C,AC}$ representing the capacitor voltage and current AC components. Finally, after averaging of p_C and $(i_C)^2$ using a simple low-pass filter the desired ESR value of the capacitor is determined by division of the filtered quantities according to $R_{ESR,m} = p_{C,F} / (i_{C,F})^2$.

It shall be noted that utilizing the power measurement approach the gained value of R_{ESR} does not depend on any filtering time constants. Although the signal paths show AC coupling (i.e., a high-pass behavior, cf. **Fig.6a**) and also some kind of low-pass filtering to limit the bandwidth for the signal processing, this filtering does not take influence on the result of $R_{ESR,\mathrm{m}}$. This essentially is different from alternative monitoring concepts, e.g., the direct measurement of Fig.5a using the RMS current/voltage quantities.

As demonstrated by Fig.6b, starting from an initial guess, e.g., its assumed worst-case value at the end of the life cycle (in the case at hand 340mΩ, realized by appropriate preload values of the averaging filter capacitor), the correct magnitude of R_{ESR} is achieved within a 10...15ms interval, despite the time constant of the averaging filter has been set to ≈30ms.

4. REALIZATION ASPECTS

Although the proposed concept could be also realized using analog circuitry technology in a similar way as described in [10] for the system of Fig.5a, the new concept is especially suited for digital implementation. Because the required basic operations (summations and multiplications) are quite simple and due to the fact that the final division operation has to be performed at low repetition rates, no high-performance digital signal processor as, e.g., proposed in [4] would be required. Instead a rather low-cost single-chip microprocessor is sufficient. Modern components of this type (e.g., the series ADUC84x by Analog Devices Corp. or comparable mixed signal microcontrollers by Microchip, Atmel or Silicon Labs. Inc.) usually are characterized by features which ideally fit the requirements of the proposed monitoring system: (i) integrated A/D converter with high sampling rate, good resolution and internal reference, (ii) serial bus interface, (iii) effective arithmetic unit, (iv) low-power operation and power management unit, (v) on-chip temperature sensor etc. Despite these advantages the controllers are available at price levels which are only a fraction of the costs of the electrolytic power capacitor to be monitored (usually the DC voltage link of medium and high power drive systems is equipped with large-can capacitors of size, e.g., Ø77x220mm).

As shown in **Fig.7**, using a modern single-chip microcontroller permits the implementation of the monitoring unit as an electrically autonomous system connected directly to the electrolytic capacitor. The negative capacitor terminal forms a local reference ground GND. So the capacitor voltage can be taken simply from the positive terminal, whereas the capacitor current is sensed by a low resistance shunt R_{SH} inserted in the negative current path. A simple passive high-pass/low-pass network serves for band-

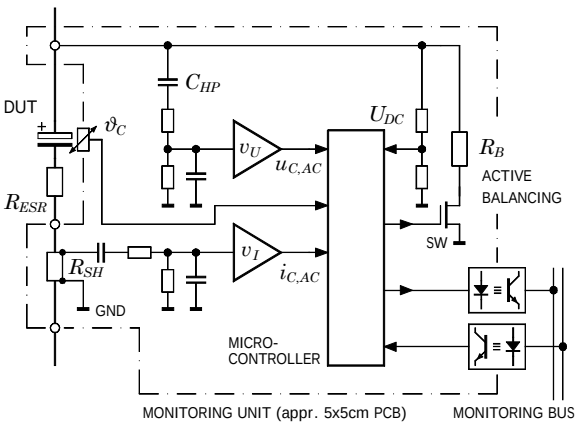

Fig.7: Basic schematic of the proposed monitoring unit utilizing a single-chip microcontroller for signal processing.

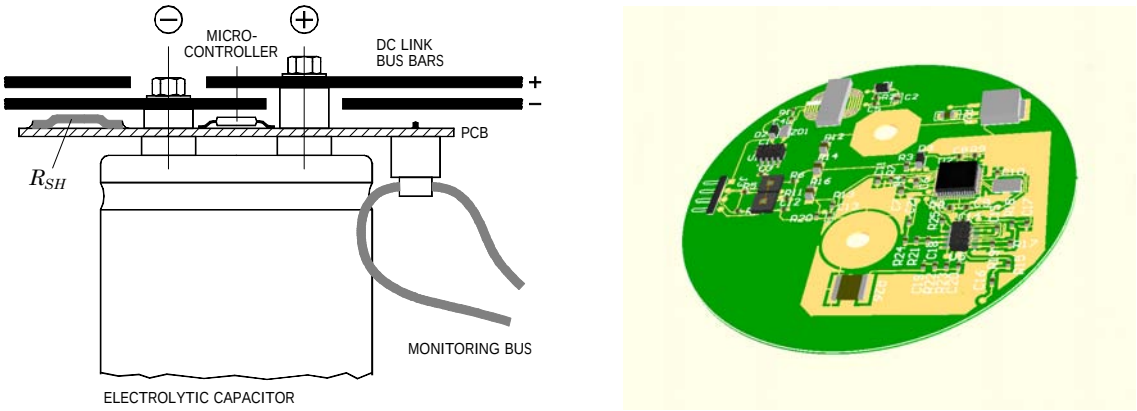

Fig.8: Physical design (to be realized) of the monitoring unit mounted directly on the terminals of the electrolytic capacitor.

width limitation and DC decoupling as described in the previous section. Here, filter time constants of $T_{HP} = 100\mu s$, $T_{LP} = 10\mu s$ are used for generating the AC signals shown in Fig.6a. As already mentioned, the exact values of these filtering constants do not influence the result provided that the filtering characteristics are equal for both signal paths. The highpass characteristic of the voltage path is also essential for blocking-off the high DC voltage from the power capacitor (C_{HP}, therefore, has to have a rated voltage of typically 400...600V), while for the current sensing path the AC coupling is substantial for offset minimization. To avoid additional losses, the shunt resistance shall be very low, e.g., $R_{SH} = 1m\Omega$. With this a gain of typically $v_I \approx 50...200$ has to be chosen for the current path amplifier. Without AC coupling of the amplifier, however, the amplifier offset would be increased by the factor v_I.

The output information of the monitoring unit, i.e., the determined ESR value (or, alternatively, of the average signals $p_{C,F}$ and $(i_{C,F})^2$ if the evaluation of $R_{ESR,m}$ shall be performed by the superimposed system) is transmitted in a purely digital form via a serial bus to the drive controller (which finally issues an error signal to the operator in case of a "weak" capacitor). The serial 2- or 3-wire bus (common for all monitoring units of the converter) also gives an easy possibility for realizing the required isolation using some kind of digital couplers (opto- or magnetic couplers). The isolation is of importance due to the local GND of each unit, due to safety reasons and implicitly permits the monitoring of series connected capacitor groups. Furthermore, the unit is also equipped with an "up-link" channel for addressing of individual units and to transmit parameters and reference values (e.g., the nominal capacitor voltage for the "active balancing" described in section 5) from the central drive processor to the monitoring units.

Physical Design. As shown in **Fig.8**, the whole circuit is realized on a small double-sided printed circuit board (PCB) located immediately between the capacitor screw terminals and the busbars of the DC link. The bottom layer of the PCB (where also u_C is sensed) directly contacts the positive capacitor terminal. Afterwards, a power through-connection carries the current to the top layer which finally attaches the positive busbar using a conductive bolt spacer. A second spacer connects the negative busbar with the PCB top layer where the current is fed to the bottom layer (and hereafter to the negative capacitor terminal) via insertion of the shunt R_{SH}.

This physical layout minimizes the wiring effort of the system and avoids extra sensing cables which would be problematic due to the high noise level in close vicinity of the main power transistors and/or due to the low signal level, especially appearing in the current sensing path. Furthermore, the direct mounting of the monitor board gives a simple possibility for measuring the capacitor temperature which is required by all means to evaluate the identified ESR values. In the case at hand the selected microcontroller features an on-chip temperature sensor. Hence, the controller is placed very closely to the capacitor terminals.

Data Acquisition – Sampling Techniques. The basic circuit of the proposed method (Fig.5b) is suited very well for digital implementation. No extensive data storing is necessary, only simple multiplying and averaging operations have to be executed in real time. For drive converters with switching frequencies up to 5kHz (medium and higher power level), the dominant current components of i_C are well below 50kHz (cf. Fig.4). These frequencies usually can be handled with good precision by the A/D channel sampling rates of modern advanced microcontrollers. In the case at hand, the chosen controller allows sampling rates of up to 400ks/sec. However, if the system should be applied to converters with higher operating frequencies (e.g., small-size IGBT or MOSFET inverters or even high-power switch-mode supplies with switching frequencies of 100kHz and above), aliasing effects have to be taken into account. These effects also may appear at low converter switching frequencies if ultra-low-cost microcontrollers with very slow A/D channels are used for capacitor monitoring.

The proposed concept, however, offers an excellent opportunity to cope with such circumstances. It is well known from literature that specific parameters of periodic and semi-periodic signals are not affected by undersampling, i.e., if the signal is acquired at random time instants using an averaged sampling frequency being far below the signal components (cf., e.g., [12], pp. 104–107, or [13], pp. 69–71). Random based techniques have been used for many years for rms measurement of high-frequency signals even without any digital or computing background [14, 15]. Also true rms voltmeters with high bandwidth using slow A/D converters and first generation microprocessors have been reported since the early 1980ies [16]. Furthermore, digital wattmeters employing "asynchronous" sampling have been described at that time [17]. Here it is interesting to note that applying specific random sampling strategies a single sampling stage with a single A/D converter channel is sufficient for power measurement [18]. A sampling of voltage and current signals at equal time instants is not necessary, which ideally fits to the structure of today's microcontrollers which usually show only a single sampling stage (channel multiplexer in front of sampling stage).

Power Supply. Concerning the power supply of the monitoring unit the final aim is that its power consumption is minimized to a level that the supply current can be drawn directly from the power capacitor to be tested. Modern microcontrollers show low operating currents of typically a few mA and can be set into power-down mode with a quiescent current of a few µA. The intent is that a series resistor R_S, which is connected from the supply voltage pin VDD of controller to the positive power capacitor terminal is dimensioned such, that a "bias" current say I_B = 1mA results (e.g., R_S = 250V / 1mA = 250kΩ assuming a capacitor nominal voltage of 250V). With this a power loss of ≈250mW appears which can be handled easily by SMD resistors.

If the controller is in power-down mode I_B charges up the controller's buffer capacitor C_B (connected from VDD to GND) and after a certain charging time this capacitor stores adequate energy that the controller can be operated for a measurement interval (e.g. 50...100ms). The capacitance value of C_B has to be dimensioned such that the voltage droop of VDD within the measurement interval can be tolerated (e.g., 4 → 3V). The measurement interval ends with setting the controller into power-down mode. Due to the fact that the ESR detection is performed only once per second or even per minute, there is ample time that I_B recharges C_B again. The maximum value of VDD is guaranteed by a zener diode arranged in parallel to C_B. Alternatively, also an "active" regulation of VDD by the controller itself would be possible where the controller periodically checks VDD within the power-down interval by a short active cycle and remains in active mode for a several time if VDD has reached its upper threshold. It shall be noted, however, that both concepts are based on the fact that VDD varies between two thresholds which can only be tolerated because the internal reference voltage of the applied controller is fixed to 2.5V and not relative to VDD.

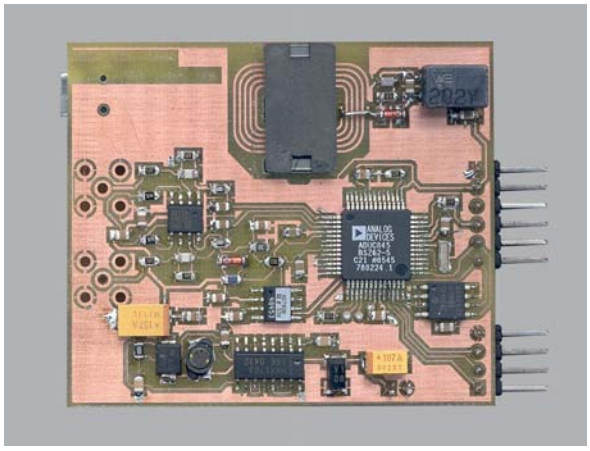

Fig.9: Laboratory prototype of the monitoring unit.

Because a first version of the monitoring unit also includes a USB interface to ease software development and testing (interface to a personal computer), the laboratory prototype as shown in **Fig.9** does not yet include the power supply concept as described before, but uses a dedicated DC/DC converter with flat-core transformer. Furthermore, the module layout still does not allow direct mounting to the power capacitor terminals as depicted by Fig.8, however, features an interface for a small LCD panel to display parameters and results (upper connector strip on right edge; lower connector strip: monitoring bus).

5. Active Capacitor Voltage Balancing

The unit described so far exclusively serves to monitor the aging of the power capacitor. However, the system can be extended at very low cost to cover further functions. With the exception of low power systems drive converters usually are operated from a three-phase mains. For the widely used 400V mains DC link voltage levels of ≈500V appear which may rise to typically 600...700V with active rectifier systems or in case of motor braking. Due to technology limitations electrolytic capacitors mainly are available only in the voltage range < 500V. Consequently, the DC voltage link of such converters in general is equipped with a series connection of two or more capacitors. To achieve a homogenous voltage distribution the capacitor manufacturers usually demand balancing resistors R_B connected in parallel to each capacitor to form a resistor voltage divider (cf. F**ig.10a**). These resistors have to be dimensioned such that the appearing quiescent current I_Q is substantially higher than the leakage currents of the capacitors. Unfortunately, however, the leakage current of electrolytic capacitors may vary in a wide region, dependent on aging status and temperature. As a rule of

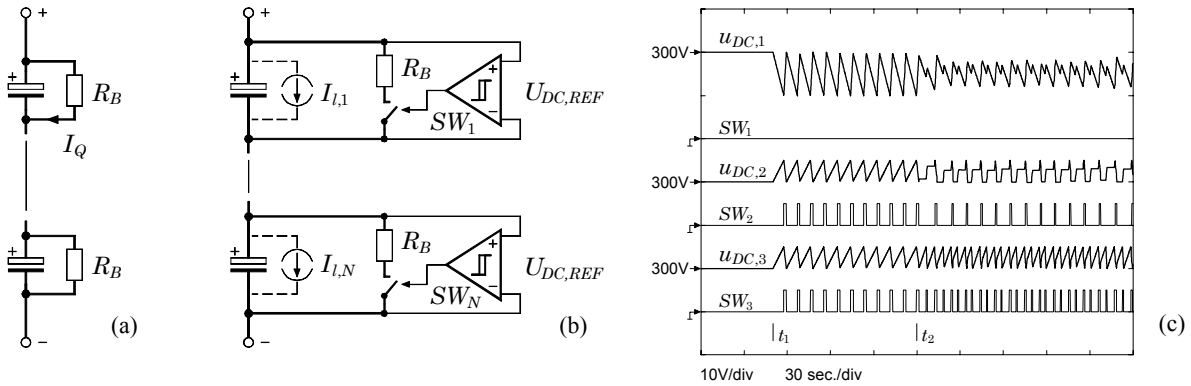

Fig.10: Voltage balancing of capacitor strings. (a): Conventional resistor divider; (b): functional circuit of proposed active concept (hysteresis comparator with programmable reference value $U_{DC,REF}$); (c): capacitor voltages $u_{DC,i}$ and switching signals of the balancing switches SW_i; parameters: $U_{DC,REF}$ =300V, hysteresis width 5V, C=1mF, R_B=30kΩ, initial values: $u_{DC,i,0}$ =300V, $I_{l,i,0}$ =1mA; at t_1 leakage current $I_{l,1}$ →3mA, SW_2 and SW_2 start to operate to keep $u_{DC,2}$ and $u_{DC,3}$ within defined limits; at t_2 leakage current $I_{l,2}$ →2mA, SW_2 and SW_2 now show different duty cycles.

thumb, it is usually recommended to choose R_B such that $R_B \cdot C \approx 50$ sec. is valid [19, 20]. For a 5000µF capacitor this, e.g., gives a balancing resistor of R_B = 10kΩ leading to a quiescent current of 25mA (@250V capacitor voltage) and resulting in additional losses of 2 x 250V x 25mA = 12.5W for the total converter. If the converter is permanently operated or at least powered by the mains, this losses sum up to a substantially energy consumption of ≈110kWh/year! The problem of this balancing method is that R_B has to be selected regarding an absolute worst-case condition of the capacitors but high additional losses also exist even if the capacitors show much smaller actual leakage currents.

To avoid this unattractive drawback active balancing has been proposed based on cascode-type linear-mode voltage follower circuits [21, 22]. Furthermore, concepts have been described where an extended auxiliary power supply of the drive converter also takes on the voltage balancing of the DC link capacitors [23, 24]. Both concepts mentioned, however, show the drawback that they are not applicable for a series connection of more than two capacitors.

Because the monitoring unit described in this paper operates in direct connection with the capacitor and can be fully controlled via the serial bus, a very simple energy saving balancing concept can be implemented with low additional costs: As shown in Fig.7, for measuring the voltage U_{DC} of the DC link first the circuit is extended by a voltage divider connected to an additional A/D channel of the controller. Furthermore, a balancing resistor R_B is added which, however, is not active permanently but can be switched on/off by a small high-voltage MOSFET switch SW. Now the control software of the unit is extended to turn SW on if U_{DC} exceeds a predefined upper limit and to turn off SW if U_{DC} falls below a lower limit (hysteresis type on/off control). The reference value of this hysteresis controller is programmed via the monitoring bus by the central drive controller such that the total DC link voltage is partitioned equally to the individual capacitors $U_{DC,REF} = \Sigma U_{DC}/N$ (N... number of capacitors in series). With this, a functional circuit diagram as shown in Fig.10b can be given. (Remark: The central drive processor in general has knowledge about ΣU_{DC} because this quantity is required for PWM calculation; alternatively, ΣU_{DC} can also easily be detected by summing up the $U_{DC,i}$ of the individual stages.)

The DC current through the whole capacitor chain now will be determined by the capacitor with highest leakage current $I_{l,\max}$. The SW of the corresponding balancing stage will be permanently off. All other stages will turn on their SW periodically with a duty cycle δ_i such that the relation $I_{l,\max} - I_{l,i} = \delta_i \cdot U_{DC,i} / R_B$ is valid. As depicted by Fig.10b, this balancing concept works well and further offers an additional capacitor monitoring principle. Considering the individual δ_i the central drives processor may perform a statistical evaluation or even calculate the leakage current distribution of the capacitor chain if also the $U_{DC,i}$ values are taken into account. With this a "weak" capacitor (i.e., a capacitor whose leakage current is abnormal or rises abnormally) can be detected in time in addition to the ESR monitoring concept proposed before.

6. CONCLUSIONS

A novel system for on-line monitoring and managing of DC voltage link power electrolytic capacitors has been presented. The circuit allows the on-line detection of the capacitor's equivalent series resistance (ESR) utilizing the current ripple of the converter as testing signal. The new basic operating principle of the proposed concept is based on the calculation of the capacitor losses. After measurement of the AC ripple components of the capacitor voltage and current the power loss is calculated which directly corresponds to the ESR value. With this the specific frequency compensation filters required for alternative concepts can be avoided.

The unit is realized using a modern single chip microcontroller mounted on a small printed circuit board located directly between the capacitor's screw terminals and the converter busbars. This also allows a simple detection of the capacitor's operating temperature which is important for the evaluation of the measured ESR values. The unit operates as a "self powered" system which draws its supply current out of the monitored capacitor. The measurement results of all individual capacitors of the converter are gathered by a simple opto-isolated three-wire bus.

The unit can be produced at low cost and is ideally suited for IGBT converters in the medium and higher power range (starting from several kVA) with typical switching frequencies 1-10kHz being very common for, e.g., modern AC drive systems. However, using specific random sampling techniques, also converters operated at considerably higher switching frequencies can be covered.

Finally, besides the ESR detection the monitoring unit further allows an energy efficient capacitor voltage balancing in case a series array of capacitors is used. As opposed to conventional resistor voltage divider networks this method reduces the balancing losses to a very significant extent by avoiding high quiescent currents.

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