Applied Power Electronics at APEC

The Applied Power Electronics Conference and Exposition (APEC) celebrated its 25th anniversary from February 21 - 25 in Palm Springs (California/USA). About 1200 attendants registered for the event, along with some 150 exhibitors, making it one of the most important power electronic events in 2010. APEC 2011 will be held from March 6 - 10 in Fort Worth, Texas.

The plenary session on February 22 gave an introduction to some of the main topics, starting with a look back on APEC history by John Kassakian, one of the four key contributors to the origin of APEC. The demise of the Power Concepts, Inc. International Power Electronics Conference (1975-1984), left the power electronics industry without a conference focused on the working engineer. The IEEE Power Electronics Council, the predecessor to the IEEE Power Electronics Society (PELS), acted to fill this void and created the Applied Power Electronics Conference and Exposition. The first APEC was held in April of 1986, only about nine months after the concept was first proposed. APEC has been held every year since.

Robert V. White, Chief Engineer at Embedded Power Labs, covered "Digital Power: After the Hype". Not so long ago it seemed every power electronic publication had an article on the wonders of digital power. Digital power was going to reduce cost, increase functionality, increase efficiency, have units send out messages they were failing, and with adaptive controls, put power electronics engineers out of work. Cycle by cycle loop compensation in new ICs coming to market offer eliminates instability problems once and for all. In the server world, PMBus is being use to enable energy saving system management functions. So while digital power has not yet, and probably never will, live up to the hype, it is becoming a powerful tool in the power electronics designer's toolbox. His conclusion - best tools but not best chips are going to win market share in the future.

According to Ron Van Dell, CEO SolarBridge Technologies, DC/AC inverters are key to overall photovoltaics system function yet only represent about 10% of total system cost. Distributed generation of solar power, particularly on residential and light commercial roof-tops, is major new segment to be developed, but poses some unique challenges, and has not been well served with current technologies based on high voltage DC feeds into centralised inverters. Recently, major strides are being made in micro-inverters by a number of companies with the objective of doing roof-top power conversion on a per-panel basis. This approach can yield significant gains in how many sites can qualify for PV, and increase energy harvest, while also decreasing installation cost. There are, however, some tough technical challenges that must be overcome if ACPV is to realise its full potential and accelerate the timing to grid parity. His conclusion - Micro inverters are the best approach for distributed PV generation, and grid parity can be reached already in the year 2012, not in 2015!

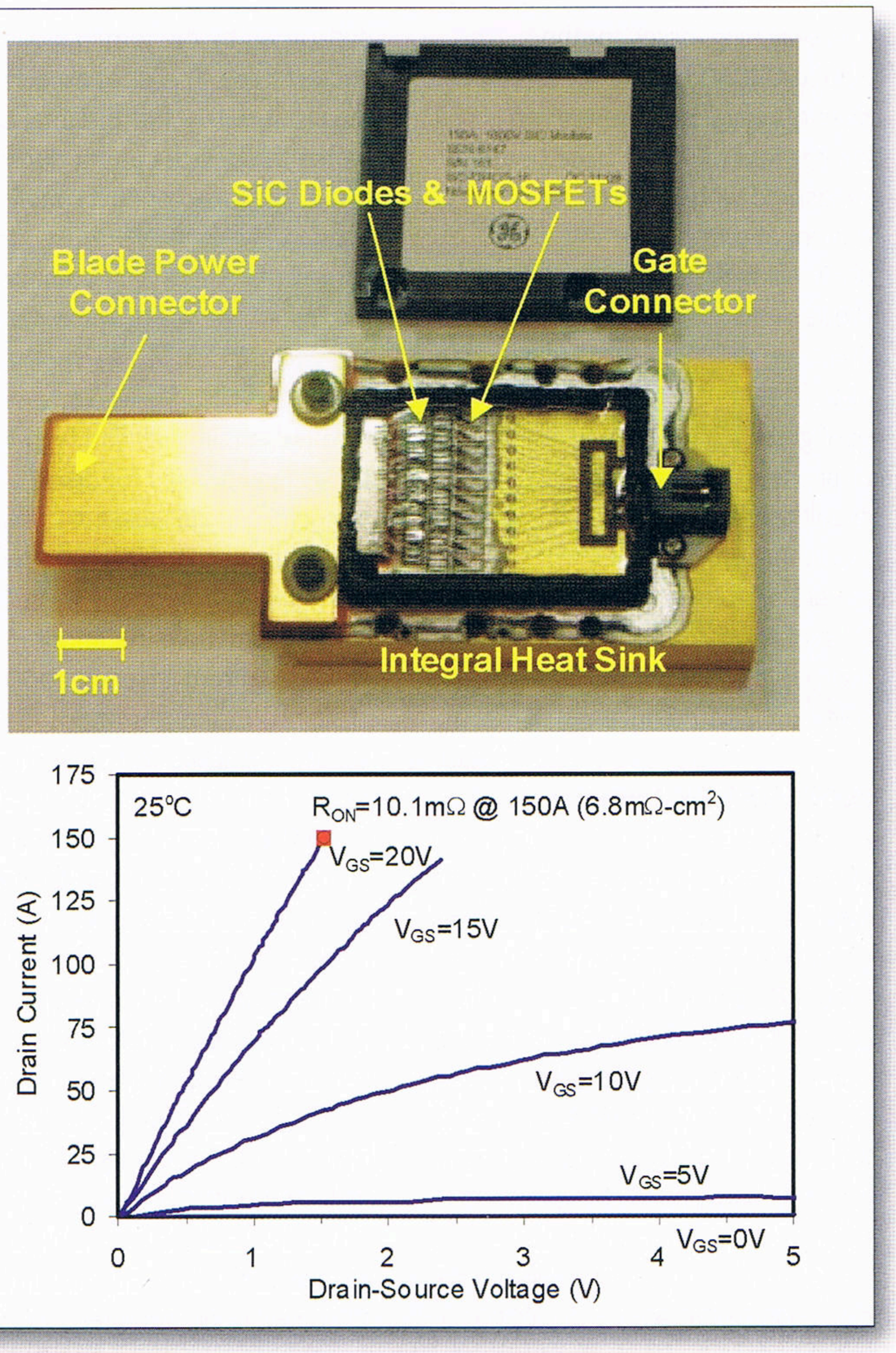
JB Straubel, CTO of Tesla Motors, gave a keynote on "Power Electronics and continued improvements in Electric Vehicle performance, efficiency and drivability". Batteries are usually the first topic of discussion for electric vehicles and with good reason due to their dominance over vehicle range but the power electronics that manage the flow of all electricity between the battery, motor and power grid have been improving quickly and offering dramatic improvements in overall vehicle acceleration, charging times, reliability and cost. Tesla Motors have moved through four generations of power electronics in the Roadster sports car (priced at $100,000) and each time increased current density and motor torque substantially while decreasing cost. The latest generation of 900A inverters allow for acceleration to 100km/h (60miles/h) in just 3.6 seconds. In just the last few years it has become possible to build an electric power-train with better overall performance than any internal combustion engine and these desirable driving characteristics will only accelerate EV adoption beyond the environmental benefits. Power electronics improvements and cost reductions are also allowing for faster charging rates and more sophisticated vehicle interfaces with the power grid. Though Tesla focuses on high-efficiency inverters, Silicon Carbide technology is not applicable today due to lack of appropriate devices. Instead massive paralleled TO247 IGBTs are used so far.

APEC 2010 opening by John Kassakian, one of the founders of this event celebrating its 25th anniversary

Silicon Carbide Power FETs to come

Silicon IGBTs are used in majority of today's power electronics applications with device voltage ratings between 1.2kV and 6.5kV. Developed almost thirty years ago and continually refined ever since, the IGBTs have reached performance entitlement of both material and device structure. A quantum leap in device performance requires either a better material or a better device structure. One such possibility are wide-bandgap (WBG) semiconductor materials, such as Silicon Carbide (SiC) or Gallium Nitride (GaN).

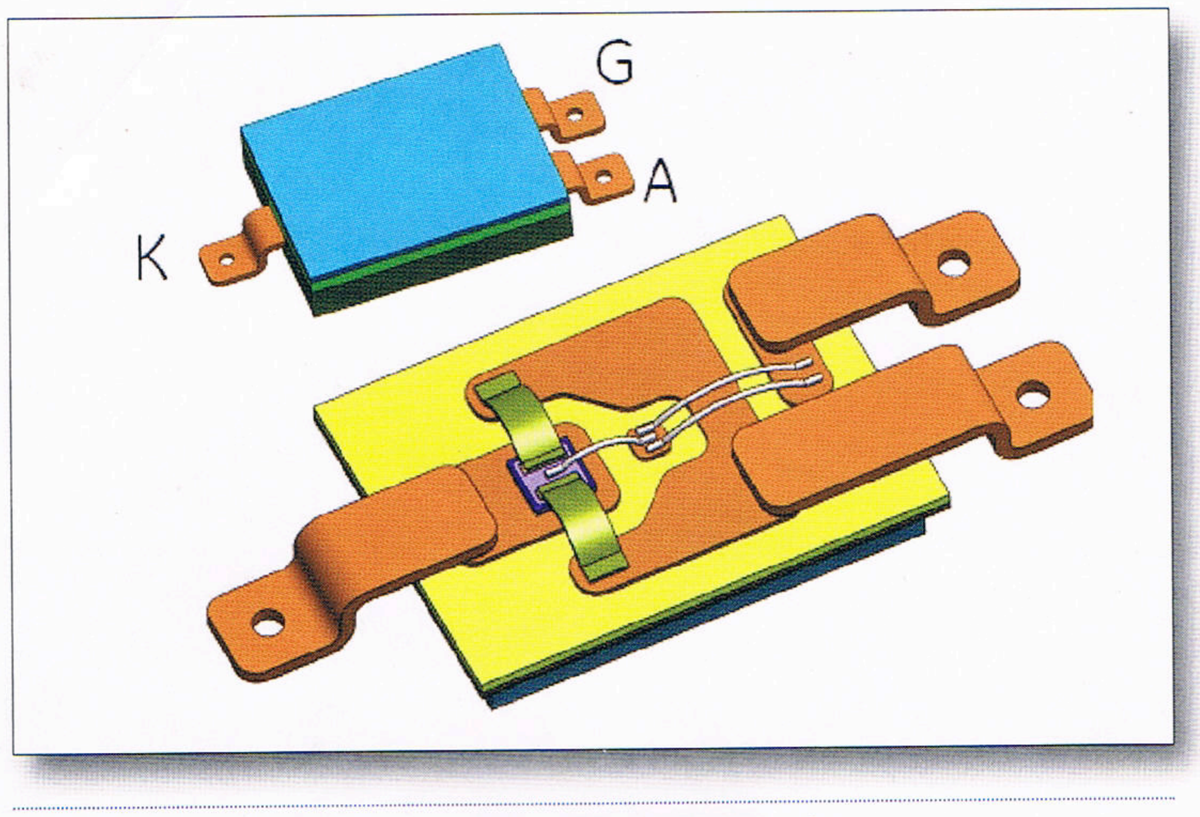
Emerging SiC MOSFET power



GE's all-SiC power module with low inductance blade power connector. The 150A, 1000V module has ten SiC MOSFETs and fifteen SiC diodes. Shown below are on-state characteristics at Tj = 25°C. At the rated current of 150A, the module's on-resistance is 10mΩ

devices promise to displace silicon IGBTs from the majority of challenging power electronics applications by enabling superiour efficiency and power density, as well as capability to operate at higher temperatures. A paper presented by Ljubisa D. Stevanovic (stevanov@ge.com) from General Electric's Global Research Center reported on the recent progress in development of 1200V SiC power MOSFETs. Two different chip sizes were fabricated and tested: 15A (2.25mm x 4.5mm) and 30A (4.5mm x 4.5mm) devices. First, the 30A MOSFETs were packaged as discrete components and static and switching measurements were performed. The device blocking voltage was 1200V and typical on-resistance was less than 50mΩ with gate/source voltages of 0V and 20V, respectively. The total switching losses were 0.6mJ, over five times lower than the competing Si devices. Next, a buck converter was built for evaluating long-term stability of the MOSFETs and typical switching waveforms. Finally, the 15A MOSFETs were used for fabrication of 150A SiC modules. The module's on-resistance values were in the range of 10 m_, resulting in the best-in-class on-state voltage values of 1.5V at nominal current. The module switching losses were 2.3mJ during turn-on and 1mJ during turn-off. The results validate performance advantages of the SiC MOSFETs, moving them a step closer to power electronics applications.

According to Stevanovic the key roadblock to SiC MOSFETs has been the reliability of its gate oxide. As in Silicon, availability of the native SiO2 oxide makes SiC uniquely suitable for implementation of MOS-gated devices. However, the MOSFET gate oxide growth and subsequent device fabrication steps are significantly different between Silicon and SiC MOSFETs. One obvious difference is the presence of carbon atoms in the



3000V/25A high temperature surface mount SiC thyristor package

SiC crystal lattice and their detrimental impact at the SiC-SiO2 interface. The other differences are higher processing temperatures during the gate oxide growth and subsequent fabrication steps. It was, therefore, not surprising that direct application of previously developed Silicon gate oxidation processes gave very poor SiC MOSFET results. Because the early results were so discouraging, the gate oxide was perceived as a showstopper to commercialisation of SiC MOSFETs. However, more recent research activities demonstrated reliable gate oxides. The focus can now be shifted to optimising device structure to reach its performance entitlement.

Zheng Chen from Virginia Tech (CPES) characterised Cree's 1.2kV SiC MOSFET, including its static and dynamic characteristics, and its high-frequency (1MHz), high-power (1.2kW) zero voltage switching (ZVS) operation in a half-bridge parallel resonant converter. The result: For high switching frequency operation, thermal constraint is the practical issue. Although the SiC MOSFET suffers relatively large switching loss partly due to larger capacitance density (capacitance per die size), it has a lower total power loss with its superiour on-resistance. In addition, SiC MOSFET has a higher power loss handling capability due to its high thermal conductivity and high junction temperature which is limited by the current package technology. When ZVS is desired in high switching frequency applications, the fast reverse recovery time of SiC MOSFET body diode makes it an unbeatable alternative to Si counterpart for high switching frequency ZVS operation.

Cree's head of development John Palmour looks in SiC MOSFET pricing at a system level where significant savings can be realised through elimination of snubbers and higher switching frequencies up to 20 times compared to Silicon devices. And 10kV SiC DMOS FETs could replace 6.5kV IGBTs, switching frequencies in the range of 200Hz will be possible. Additionally 12kV SiC IGBTs are in development at Cree.

The first commercially available pure enhancement-mode SiC power VJFET (EM SiC VJFET), introduced one year ago by Semisouth, has been gaining significant interest among power electronic designers. This new normally-off EM SiC VJFET has a low specific on-resistance of 2.8mΩ-cm^2 resulting in a die size of 9mm^2 for a 50mΩ device rated at 1.2kV. This design enables very low parasitic charges of 70nC gate charge. The EM SiC VJFET is in single die form, without any cascode and does not contain body diode or gate oxide.

Prior work has demonstrated the use of the EM SiC VJFET as a drop-in replacement for existing Si-MOSFETs and Si-IGBTs in high-side and low-side switch mode applications. With only a direct replacement of the semiconductor power switches in both a commercial solar inverter and commercial PFC demo board and addition of the RC gate driver with no other circuit optimisation performed, incremental efficiency improvements were realised. These socket replacement demonstrated a first step toward device acceptance; however, further system efficiency improvements could be realised from power circuits and gate drivers.

A newly optimised two-stage, DC coupled gate driver introduced by Robin Kelley demonstrated record low switching losses for the SJEP120R050 EM SiC VJFET. Fall time of only 25ns and turn-on energy loss of 137µJ have been measured with no resulting tail current at turn-off like that of an IGBT. Also the absence of a body diode, like that of a MOSFET, means there are no problems operating the EM SiC JFETs in a bridge configuration. The resulting optimised two-stage gate driver circuit presented here has overcome the limitations of the AC coupled RC driver and further optimisation led to a list of application recommendations that aid in achieving the best possible switching performance.

3000V/25A SiC thyristor

A 3000V/25A asymmetrical SiC thyristor for pulse power applications was presented by Ahmed Elasser (Ahmed.elasser@ge.com) from GE Global Research. The devices' chip area is 4mmx4mm. It was fabricated on ultra low micropipe density 4H-SiC wafers, the yield after screening for blocking voltage, leakage current, forward drop, and latching is over 80%, a very high yield by the standards of SiC power devices. The chips are packaged in a 200°C capable, low profile, surface mount package with a low junction to case thermal resistance. Pulse testing results show that the device is capable of very high current densities, and high peak currents. It also exhibits very low forward voltage at high pulse currents due to the thinner drift layer thickness.

The devices are asymmetrical, blocking high voltage only in the forward direction, and their reverse blocking voltage is on the order of 50V. For many pulse applications, only forward blocking is required. Although the total chip area is 16mm^2, most of the area is consumed by the terminations and contact pads. The device's active area is about 1/3 of the total area, hence the device current density is quite high. Interconnect metal and interlayer dielectrics are used to connect the interdigitated fingers together while keeping the gate and anode isolated from each other. Thick pad metal is used to enable high pulse currents, and high-voltage passivation is used for device protection. The P-contact anode resistance was optimised to reduce the forward drop during pulse conditions, where the anode-cathode current exceeds 1000A.

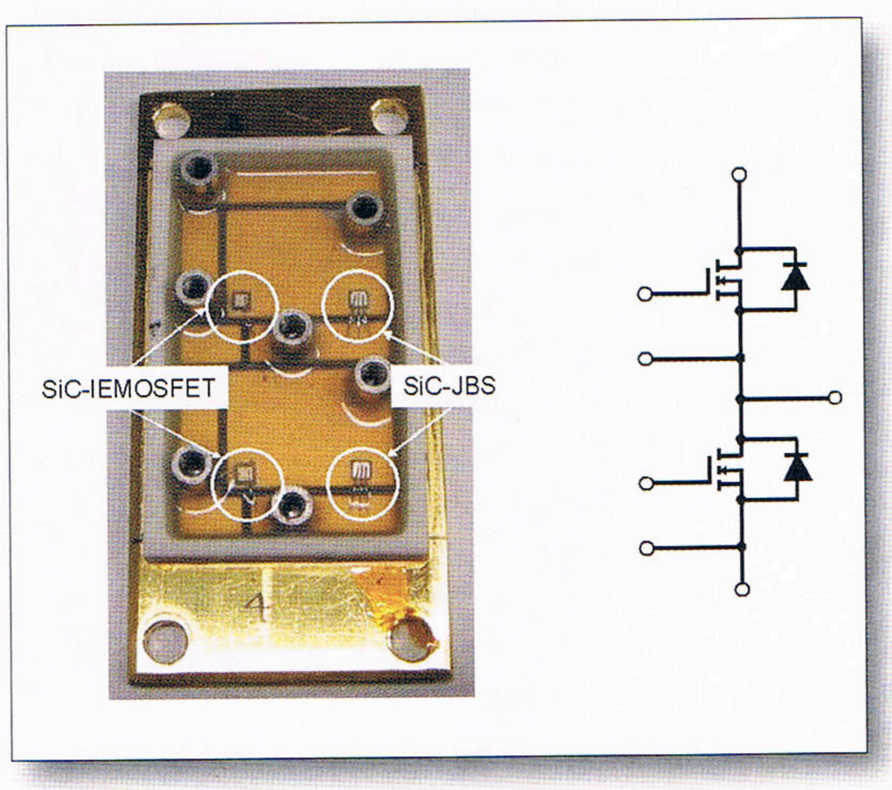
At 150°C, the maximum leakage current increases to 10µA. The high temperature (150°C) SiC leakage current is at least two to three orders of magnitude lower than the leakage current of an equivalent 3kV Silicon thyristor at 125°C junction temperature. At temperatures above 150°C, the SiC thyristors still exhibit very low leakage currents.

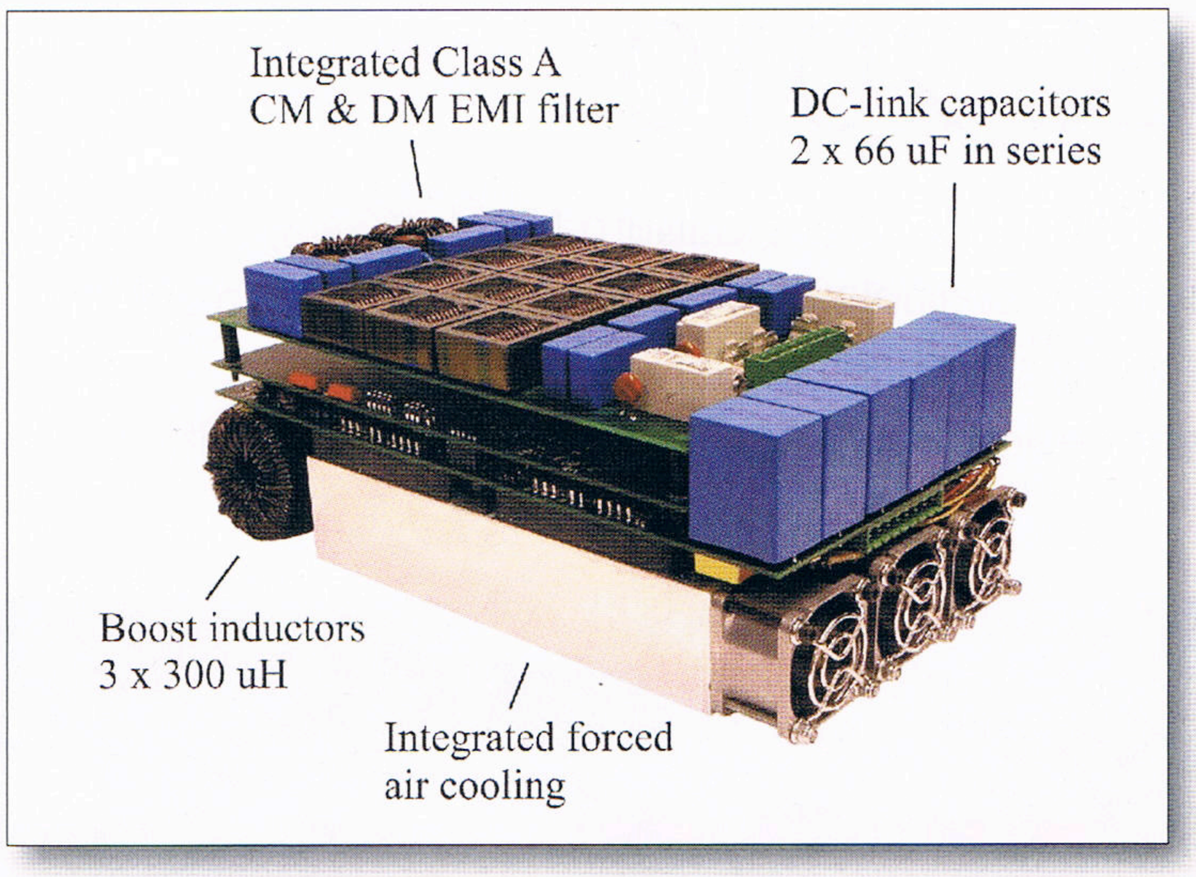
The devices were packaged in a high voltage, high temperature surface mount package.

For applications where high voltage, high pulse current, and high temperature are required, the SiC thyristor simplifies the circuit design, and enables reduced size and weight, hence compact power converters. The SiC parts significantly reduce conduction, leakage, and switching losses, thereby dramatically reducing cooling requirements and improving converter efficiency. The high current density under pulse conditions will lead to very high pulse current once large area SiC defect free substrate and material become a reality.

This progress is made possible by recent improvements in the quality of the SiC substrates (ultra low micropipe density), excellent epitaxial

SiC power module outline and equivalent circuit of the module





Compact 10kVA, 3LNPC-VLBBC prototype with 48kHz switching frequency

material (highly uniform with low defects and reduced internal stresses), great advances in device fabrication, packaging, and testing. With the continuous improvement in SiC substrates and material, and with the availability of SiC wafers from multiple suppliers, the cost of SiC devices will continue to decrease and will ultimately become competitive in the power device marketplace, Elasser concluded.

Silicon Carbide power modules

The power loss reductions attributable to the use of SiC power modules are influenced by operation conditions (switching frequency, junction temperature, and current density). In the case of Si-IGBTs with a voltage rating of 600V - 1200V, the future current density and junction temperature will approach 300A/cm^2 and 200°C. This means SiC MOSFETs are also required to have at least the same current densities and junction temperatures as Si IGBTs. According to Kazuto Takao (kazuta.takao@toshiba.co.jp) and Takashi Shinohe from Toshiba's Corporative Research & Development Center one should also consider the advantage of the SiC power modules compared with Si IGBT and SiC SBD hybrid pairs because of Si IGBTs' potential for performance improvements based on a nanometer-scale trench gate structure.

The presented paper evaluated power loss performances of a 1200V class SiC power module based on parameters of the junction temperature, current density, and switching frequency. The evaluated SiC power module comprises SiC IEMOSFETs and low on-voltage SiC JBSs. The SiC IEMOSFET has low on-resistance characteristics compared to those of SiC DIMOSFETs having conventional structure. The active areas of SiC IEMOSFETs and SiC JBS are 1.7mm x 1.7mm and 2.0mm x 2.0mm, respectively. The SiC IEMOSFET keeps the normally-off characteristic up to a junction temperature of 250°C. The switching characteristics of the SiC IEMOSFET depend on the temperature dependence of the threshold voltage.

As a result, in a three-phase PWM inverter, significant power loss reduction with the SiC power module can be realised in the case that the chip area of the SiC IEMOSFET is more than 1/2 that of the Si-IGBT. In the case of switching frequency of 5kHz and output power of 6800W, the power loss of the SiC IEMOSFETs is 54% compared to that of the hybrid-pair module. In the case of 20kHz switching, the power loss of the SiC module at 250°C is 52% of that of the hybrid pair module at 150°C and 6800W. This result indicates that the SiC module is advantageous in high-frequency switching operations compared with the hybrid pair module.

A high efficiency 10 kVA high frequency input and output Si IGBT and SiC Schottky diode 3-level neutral point clamped voltage DC-link back-to-back converter (3LNPC-VLBBC) was presented by Mario Schweizer (schweizer@lem.ee.ethz.ch) from Swiss Federal Institute of Technology (ETH Zurich). A switching frequency of 48kHz makes the converter suitable for driving high-speed and low-inductive machines. A detailed loss analysis reveals that only four of the six diodes in a 3-level bridge-leg have to be replaced by SiC diodes to enable high efficiency operation if an appropriate modulation scheme is used.

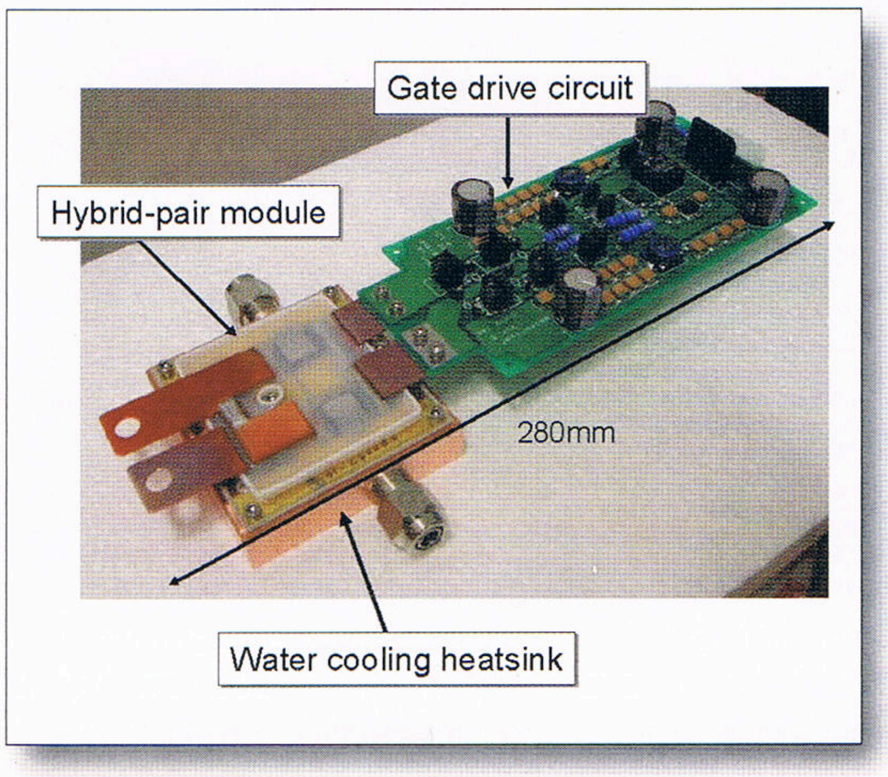
At the nominal switching frequency of 48kHz and at nominal output power of 10kVA the losses could be reduced by 10%. The converter built with the SiC module reaches a pure semiconductor efficiency of 97.0% compared to 96.6% of the standard Si version.

Compared to an equivalent 2-level converter with 1200V IGBTs of the same generation, the reduction of the losses is 42%. Interesting is also the very flat dependency of the efficiency on the switching frequency. This opens an additional degree of freedom for optimising the converter. A very compact system with small filtering components because of the higher switching frequency and a low volume cooling system due to the low losses could be realised.

It should be noted that in the real implementation additional loss sources as forced-air cooling fans (15W), digital control and gate drive power (15W) and also losses in the boost inductors (30W) are present. These will sum up to additional 60W and reduce the efficiency of the SiC 3LNPC-VLBBC to approximately 96.4%.

Considering the costs for the two modules, the custom SiC module is roughly 6.5 times more expensive than the conventional module. The converter costs accordingly will increase by roughly 300$. With a loss reduction of 10% = 32 W the energy payback time with an energy price of 0.1$/kWh will be equivalent to 10.5 years of uninterrupted operation at nominal power. At a switching frequency of 120 kHz the payback time reduces to 3.2 years of uninterrupted operation. This is quite a long operating time and restricts the application of the SiC 3-level converter to niche areas where exceptional high switching frequencies and efficiencies is required. This is the case e.g. in aircraft applications where weight and efficiency are of major interest.

A 3-level Power Converter with high-voltage SiC PiN diode and hard-gate driving of IEGT for future high-voltage power conversion systems has been presented again by Kazuto Takao from Toshiba's Corporative Research & Development Center. High-switching frequency operation is essential for reducing the volume of magnetic components. Hybrid pairs of 6kV SiC PiN diodes and 4.5kV Si IEGTs have been applied to realise the high switching frequency operation of medium voltage power converters. For low switching losses and series operation of power devices, a gate driving technique with an extremely low gate resistance (hard gate driving) is employed. Switching characteristics of the hybrid pair are measured experimentally. It has been demonstrated that the total switching loss can be reduced up to 50% with the hybrid pair. In order to demonstrate a 2kHz switching frequency of the hybrid pair, which is about 4 times higher than that of conventional medium voltage power converters, a 378kVA prototype 3-level inverter has been designed and constructed. **AS**



100A hybrid-pair switching unit

www.apec-conf.org
www.ge.com
www.cpes.vt.edu
www.cree.com
www.semisouth.com
www.toshiba.co.jp
www.lem.ee.ethz.ch