CIPS 2016 - Power Electronics in Challenging Little Boxes and More

More than 300 engineers and scientists attended the conference. Attendees came from 21 countries in Europe, America and Asia with 22 participants alone from Japan. The 9th International Conference on Integrated Power Electronics Systems (CIPS 2016) was held on March 8-10, 2016, in Nuremberg as part of the ECPE Annual Event. The Conference was organized by ETG, the Power Engineering Society within VDE, and by ECPE, the European Center of Power Electronics. IEEE PELS and ZVEI were technical co-sponsors.

By Prof. Eckhard Wolfgang, ECPE, Prof. Andreas Lindemann, Univ. Magdeburg and Prof. Dieter Silber, Univ. Bremen, Technical Program Chairs CIPS 2016, and Prof. Johann Kolar/ ETH Zurich

The program of this year's conference included 100 papers (80 in 2014): Four keynotes, 9 invited, 54 oral and 33 poster papers. A good balance of contributions was achieved between industry and academia.

Prof. Johann Kolar/ETH Zurich and Prof. Eckart Hoene/Fraunhofer IZM explained in the 1st keynote speech "The Google/IEEE PELS Little-Box Challenge". Here is a brief summary:

The intention of Google was to start an open competition to build the worldwide smallest single-phase power inverter, with a $1,000,000 prize. This would make power electronics systems more compact, and cheaper. The prize was given on February 28, 2016, to the team "Red Electrical Devils" of the Belgian company CE+T. The use of GaN technology and soft-switching enabled a power density of 143 W/in³ of the 2 kVA inverter which had to be realized in this project. The dimensions are 2.5 x 1.615 x 3.41 in³ resulting in a volume of 13.77 in³. This volume is significantly smaller than the smallest existing inverter on the market. However, the lower efficiency also has to be considered. Besides the GaN devices, MLC capacitors and ferrite magnetic components were used; for details see https://www.littleboxchallenge.com/. Furthermore, instead of electrolytic capacitors a low-volume active DC-side power pulsation buffer was used for buffering the power fluctuation with twice the AC output frequency intrinsic to single-phase DC/AC converter systems.

Prof. Kolar analyzed the concepts of the 15 finalists – the presented power densities were mainly in the range of 120…220 W/ in³ (10 out of 15 teams) – and showed details of the approach used by the team of ETH Zurich, Fraunhofer IZM and Fraza d.o.o. (cf. Fig.1 and https://www.pes.ee.ethz.ch–Publications–Conferences). As a main conclusion, power densities of 200 W/in^3 could be achieved even with moderately high switching frequencies and SiC instead of GaN power devices, and advanced high-frequency magnetics, careful thermal management and 3D-packaging/integration are key enablers for a further power density improvement.

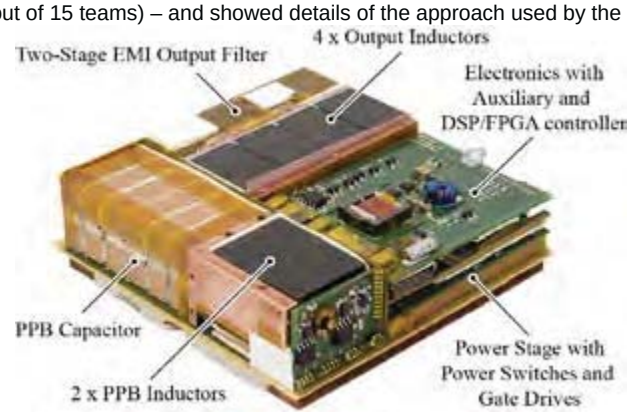

Figure 1: Converter system of ETH Zurich/FhG-IZM/Fraza (135 W/in^3) presented at the finals of the Google/IEEE Little-Box Challenge

Schneider Electric achieved the 2nd place and presented their concept (100 W/in^3) and results in the CIPS 2016 special Little-Box dialog session together with the team of ETH Zurich, Fraunhofer IZM, and Fraza (135 W/in^3).

Figure 1 shows a Converter system of ETH Zurich/FH-IZM/Fraza (135 W/in^3) presented at the finals of the Google/IEEE Little-Box Challenge. The system employs two interleaved bridge legs per phase which are operated in triangular current mode to achieve ZVS of the GaN GIT power switches (CoolGaN, Infineon, 200 kHz….1 MHz). Moreover, a new gate drive with 500 kV/µs dv/dt-immunity and only 20 ns delay time, innovative foil winding inductors with multiple airgaps and low high-frequency losses (Fraza d.o.o.), as well as an active buck-type power pulsation buffer (PPB) equipped with high energy density ceramic capacitors (CeraLink), and advanced air cooling, i.e. a top- and bottom-side heat sink (top-side heatsink not shown in Fig.1) are used.

Dr. Engel/ CeraCap Technology & Innovation Consulting presented an invited paper "Design and Materials of Antiferroelectric Capacitors for High Density Power Electronic Applications". Based on the specific solutions for power electronics and high temperature environment, the MLCCs based on anti-ferroelectric ceramics and copper inner electrodes are recommended for use in power electronics. They combine small size, low ESR, low ESL, high current handling capability, high isolation resistance at elevated temperatures, and potentially low cost, even comparable to film caps. CeraLink MLCCs can be used at high frequencies too which is necessary for GaN based circuits.

In the Keynote "Prospects for advances in power magnetics" given by Prof. Charles Sullivan/ Thayer School of Engineering at Dartmouth, Hanover NH, USA, the use and limitations for magnetic components in high frequency circuits were discussed. Inductors and transformers are critical for advances in power conversion. Increased frequency can, in principle, reduce their size and power losses, but high-frequency losses make this hard to realize in practice. In windings, proximity effect is the most severe challenge. It can be addressed either by using many winding layers sufficiently thin compared to δ

or by using a single layer. Design errors can result in large increases in loss relative to lower-cost designs, so design calculations are essential. Other strategies and considerations include interleaving, positioning of the winding relative to the gap, parallel windings, and aluminum conductors. Research in windings includes effective utilization parallel thin foil layers, as well as current balancing in very large litz-wire bundles. Evaluation of magnetic materials using performance factor assumes ideal windings, but can be modified to account for high-frequency winding loss. Results show opportunities for continued miniaturization of power converters using frequencies above 2 MHz. The introduction of GaN devices has encouraged power electronics designers to develop advanced power device integration concepts towards monolithic integration. The respective Keynote paper was "100 MHz GaN Power Conversion" presented by Dr. Dragan Maksimovich. He demonstrated this technology for VHF D – mode converters using a GaN-on-Si Process. The presented application was a radio frequency transmitter with much improved efficiency by tracking the signal envelope. Such types of amplifiers are well-known from audio frequency amplifiers, and their basic approach is the principle of pulse width modulated dc-dc-converters. Previous developments had been based on Silicon LDMOS devices but GaN devices enable much higher frequencies. In the presented example the AC envelope frequency is >20 MHz. PWM switching frequency can be as high as 200 MHz. A half bridge including gate drivers is monolithically integrated. Output Power is 7 W at 91% peak power efficiency. The developments of GaN devices encourages the author to scale the principle to much higher power in future. Therefore in the outlook a 3 MHz ZVS switching at 380 V, 500W was shown using a recently developed monolithic 600 V GaN-on-Si half bridge (from IAF, Freiburg) with integrated Schottky diodes. It described the potential of post-silicon power electronics.

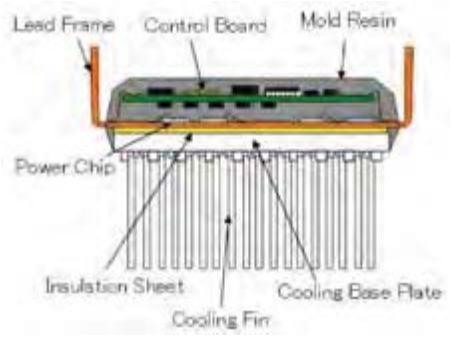

Figure 2: Cross-section of highly-integrated inverter module

Dr. Reinhard Herzer/ Semikron had been invited to give an overview on "New Gate Driver Solutions for Modern Power Devices and Topologies". More and more SiC switches (MOSFET, JFET) with voltage classes between 600V and 1700V are coming on the market with decreasing RDSon and costs as well as sufficient reliability. To use the outstanding performance of SiC devices it is extremely important to improve their application and system environment. From the package side low inductivities and thermal resistances, high temperature operation (≥ 175°C) and higher reliability are demanded. On the driver side fully integrated gate drivers with complex driving and protection functions for higher frequencies (40...200kHz), higher operation temperatures and close and low inductive connections to the switches are necessary.

In the Keynote "Review of Integration Trends in Power Electronics Systems and Devices", Dr. Gourab Majumdar/ Semiconductor & Device Group, Mitsubishi Electric Corporation, Japan showed the path to a highly integrated power module (Figure 2).

Various technological advancements in the areas power chip, circuit concepts and packaging structures made so far have immensely improved power modules' capability leading to realization of a nearly full inverter solution integrated within a smart modular housing. This trend is considered to progress sustainably in the future as well bringing in advanced solutions for power conversion systems and, thus, contributing in global efforts on energy saving.

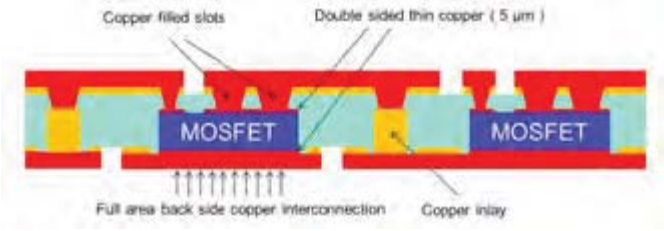

Figure 3: Power Core Half Bridge Packaging Concept

DI Hannes Stahr/ AT&S Austria, presented an "Investigation of a power module with double sided cooling using a new concept for chip embedding" in his invited paper. The embedding technology shows promising potential for power modules in many applications, e. g. in automotive, and due to its advancements with respect to electrical, thermal, reliability performance and space requirements in comparison to conventional SMT solutions. This is demonstrated by an embedded power module for driving a Pedelec, Figure 3. It has been shown that by applying embedding technology the shortest possible interconnections and, therewith, significantly reduced switching losses could be realized.

It can be concluded that 2016 CIPS conference showcased cutting-edge integrated power electronics. Contemporary systems - such as for electromobility, renewable energy and energy efficiency - will benefit from the reported results of intense research and development.

As in the previous CIPS conference there were two awards:

The VDE best poster award of 1000 € in recognition of an outstanding paper presented in the dialogue session. The award committee selected: Sebastian Kremp, Oliver Schilling, Verena Müller, Infineon Technologies AG, Germany – "Empirical study on humidity conditions inside of power modules under varying external conditions"

The ECPE Young Engineers Award promoting young engineers to present papers at CIPS. The award of 1000 € was given to: Daniel Kearney, Slavo Kicin, Enea Bianda, Andrej Krivda and David Bauman ABB Corporate Research Centre, Baden-Dättwil, Switzerland – "PCB Embedded Power Electronics for Low Voltage Applications

Figure 4 shows the members of the organizing/technical program committee.

Figure 4: From left to right: Thomas Harder/ ECPE, Prof. Dieter Silber/ University of Bremen, Prof. Eckhard Wolfgang/ ECPE, Prof. Andreas Lindemann/ University of Magdeburg, Prof. Leo Lorenz/ ECPE.

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Fig. 2:Gourab Majumdar, Takeshi Oi, Tomohide Terashima, Shiori Idaka, Dai Nakajima, Yoichi Goto: Review of Integration Trends in Power Electronics Systems and Devices; CIPS 2016
Fig. 3: H.Stahr, m. Morianz, S. Gross, M. Unger, J. Nicolics, L. Böttcher: Investigation of a power module with double sided cooling using a new concept for chip embedding; CIPS 2016
Fig. 4: Tilman Weishart Photography