ETH zürich

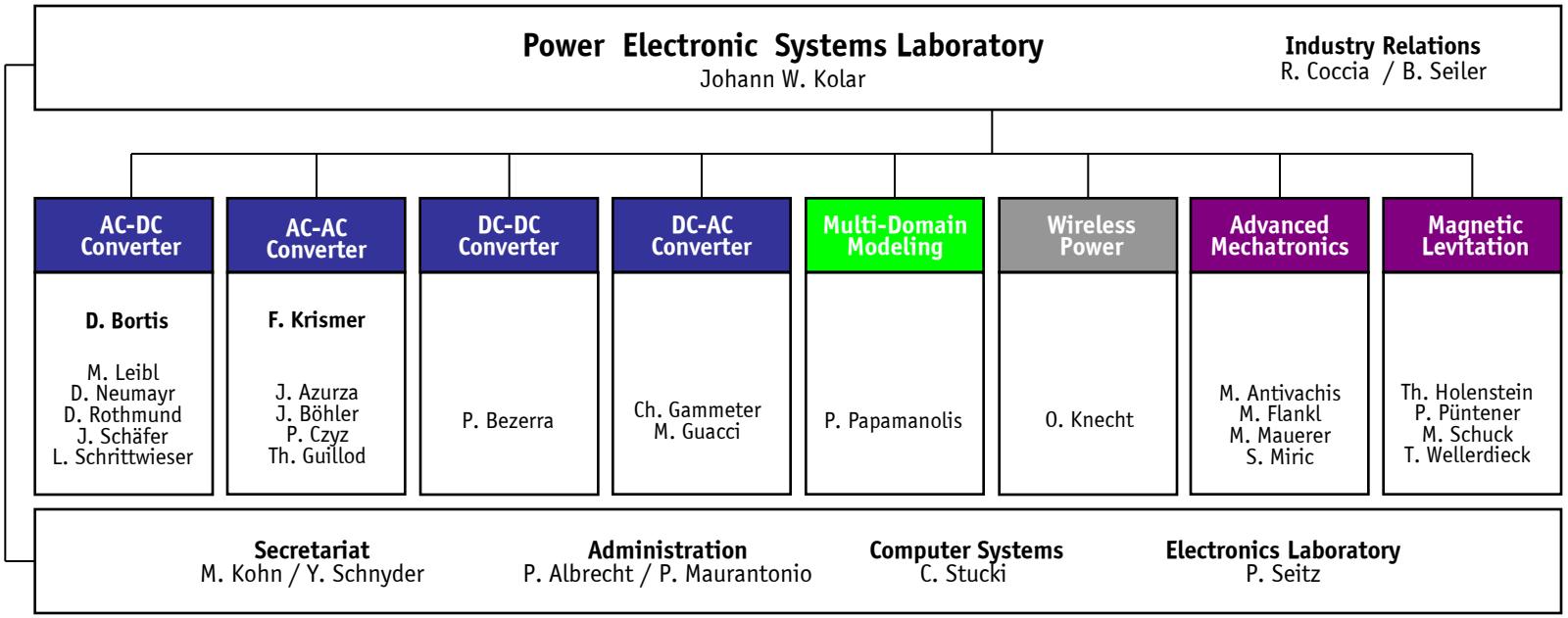
The Google Little Box Challenge

Ultra-Compact GaN- or SiC-Based Single-Phase DC/AC Power Conversion

Johann W. Kolar

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

ETH Zurich - Power Electronic Systems Laboratory



22 Ph.D. Students
2 Post Docs

ECPE Competence Centre

EPSMA

Leading Univ. in Europe

Outline

- The Google Little Box Challenge
- *Little Box 1.0*
- *Concepts & Performances of Other Finalists*
- *Little Box 2.0*
- Conclusions

Acknowledgement
D. Bortis
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L. Camurca
M. Kasper
E. Hatipoglu

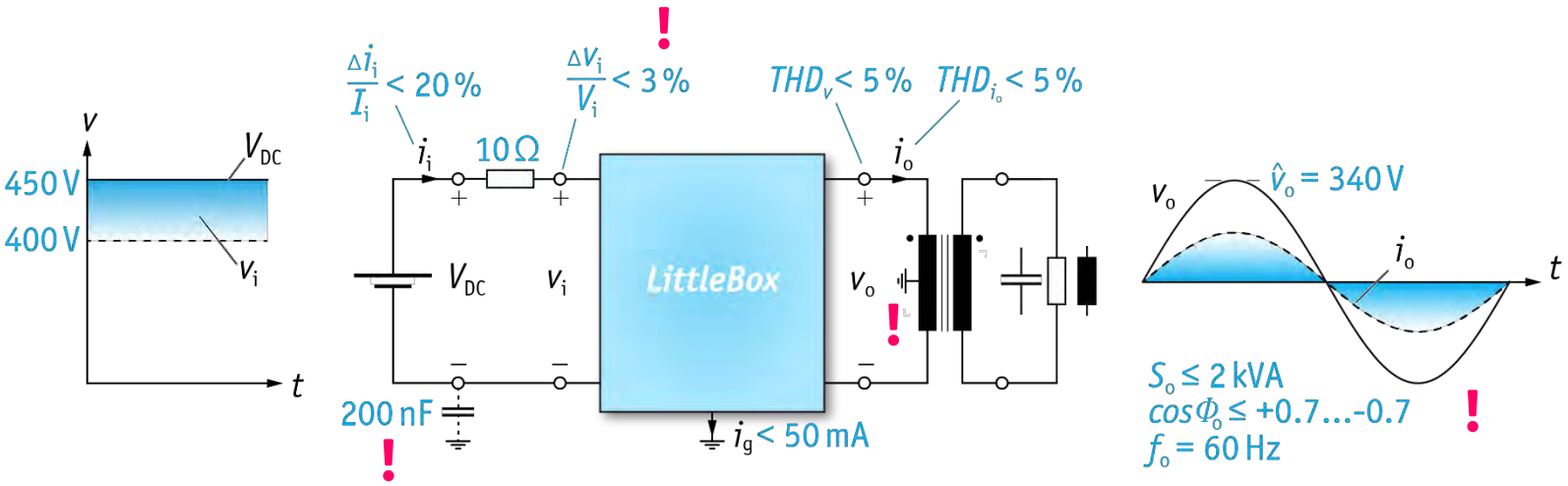
Google Little Box Challenge

Requirements
The Grand Prize
Finalists & Finals

LiTTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-ΦSolar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (> 50W/in³, multiply kW/dm³ by Factor 16)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B



■ Push the Forefront of New Technologies in R&D of High Power Density Inverters

The Grand Prize

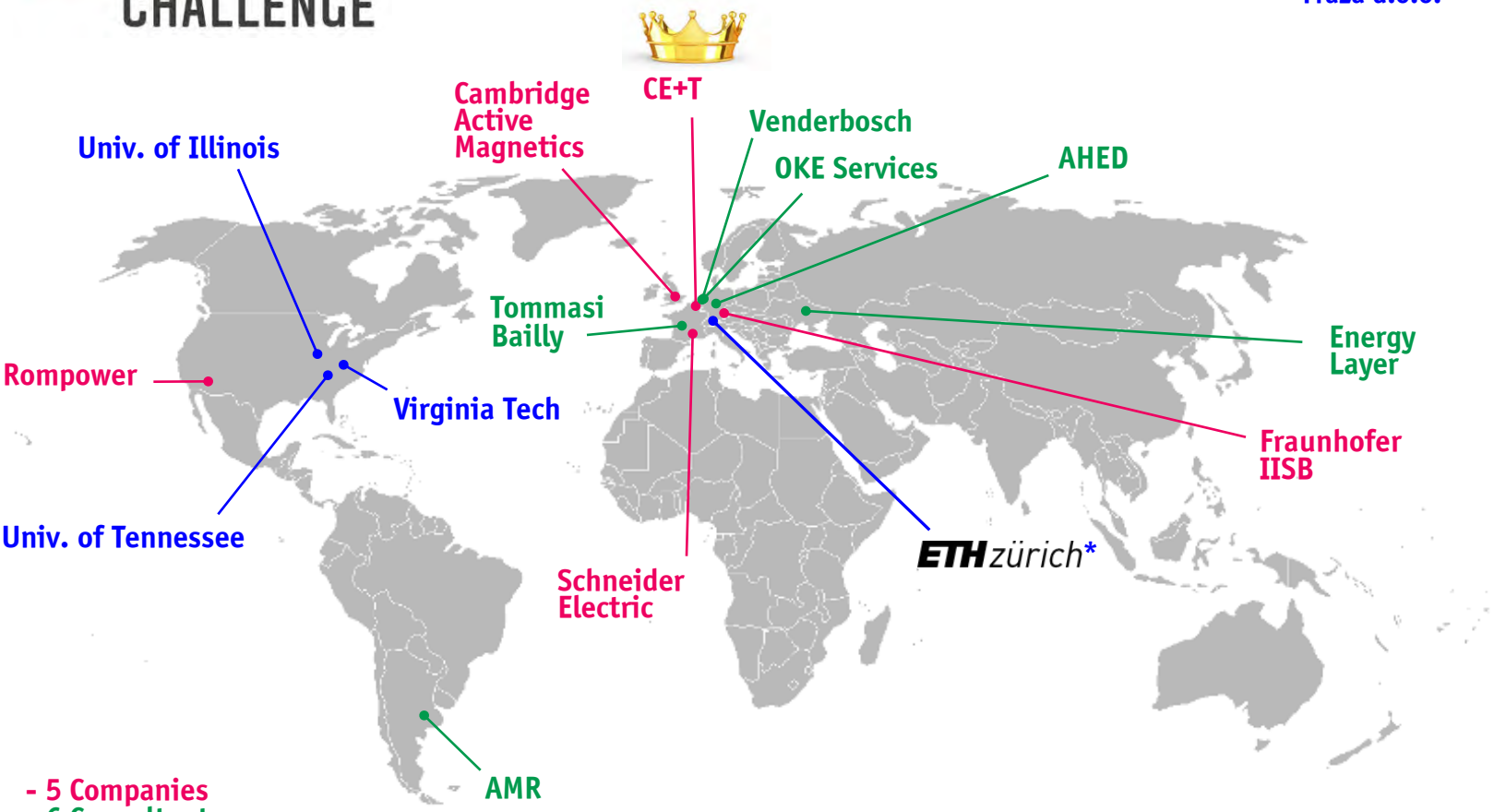
- **Highest Power Density (> 50W/in^3)**
- **Highest Level of Innovation**

$1,000,000

- Timeline
  - Challenge Announced in Summer 2014
  - **2000+ Teams Registered** Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - **18 Finalists (3 No-Shows)**

LiTTLE BOX CHALLENGE Finalists

* and FH IZM / Fraza d.o.o.

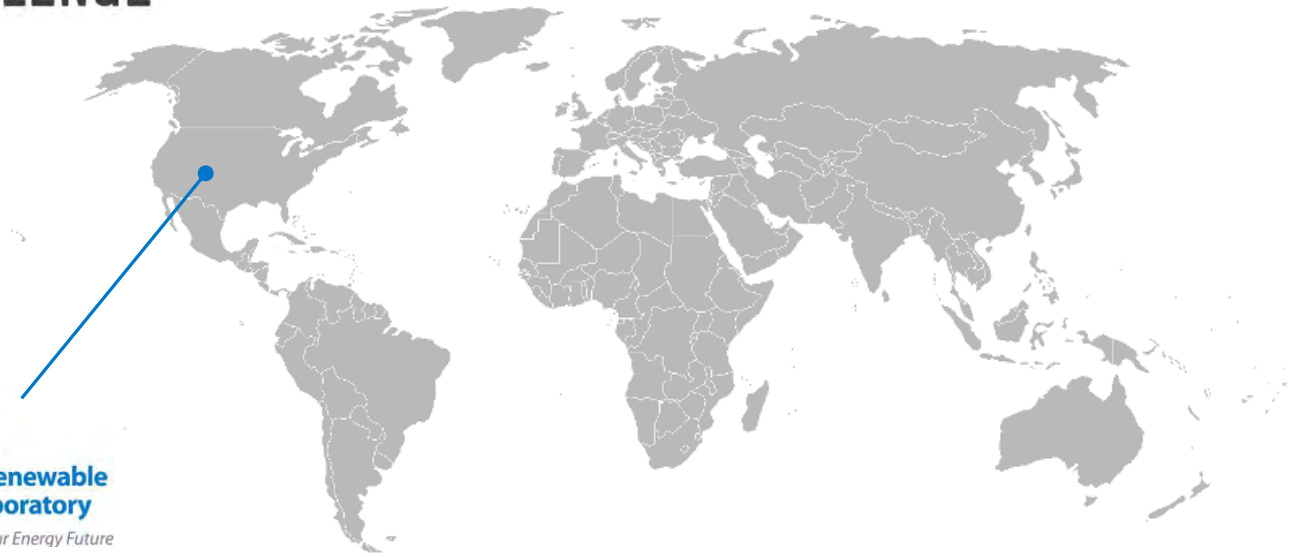


- 5 Companies
- 6 Consultants
- 4 Universities

15 Teams/Participants in the Final @ NREL

LiTTLE BOX CHALLENGE

Final Presentations



NREL
National Renewable Energy Laboratory
Innovation for Our Energy Future

- Finalists Invited to NREL / USA
- Presentations on Oct. 21, 2015
- Subsequent Testing by NREL

City of Golden

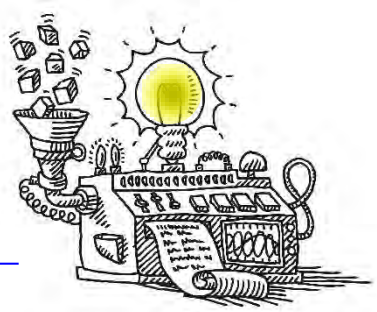
Little Box 1.0

Converter Topology
Modulation & Control
Technologies /Components
Mechanical Concept
Exp. Analysis

Acknowledgement

Infineon
Google
ECPE
EPCOS
TDK

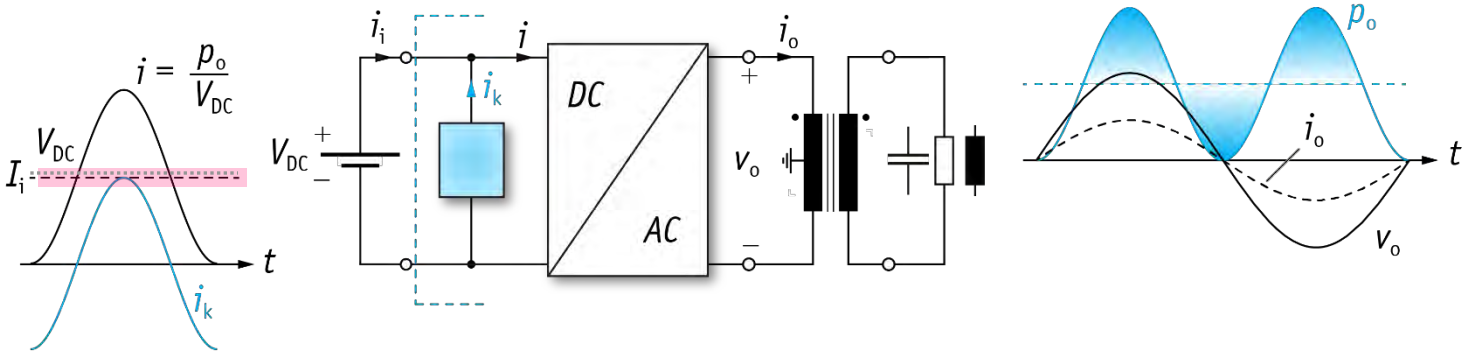
Derivation of Converter Concept



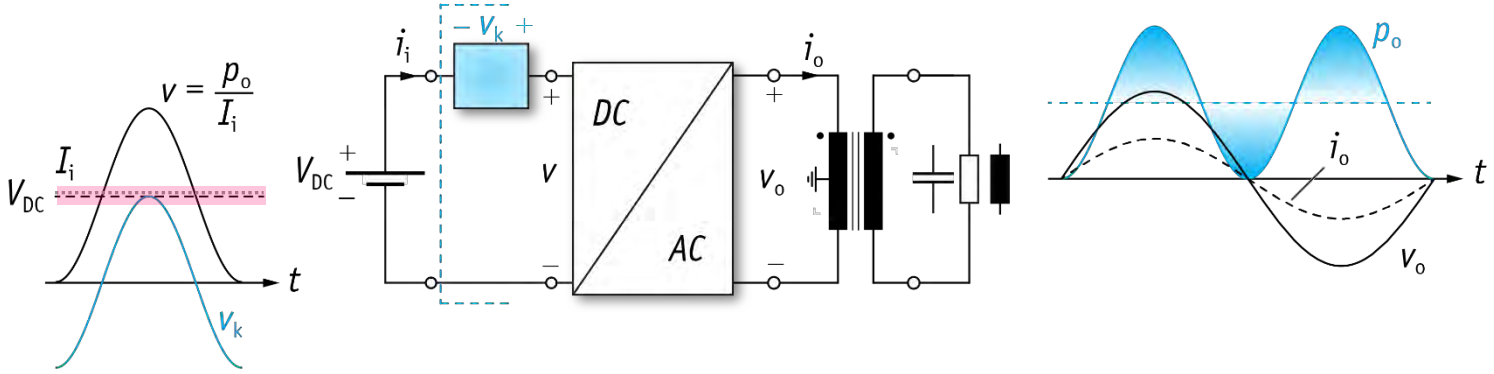
1-Φ Output Power Pulsation Buffer

Power Pulsation Buffer

- Parallel Buffer @ DC Input



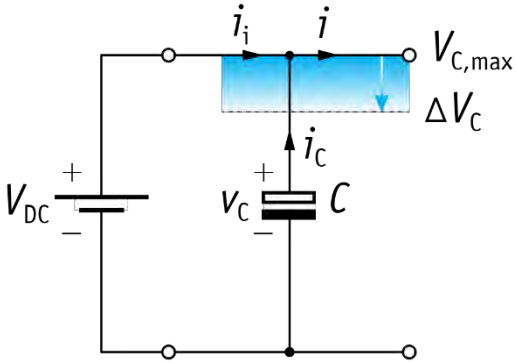
- Series Buffer @ DC Input

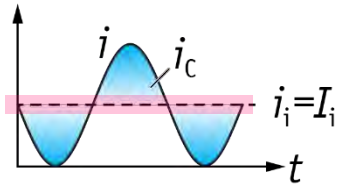


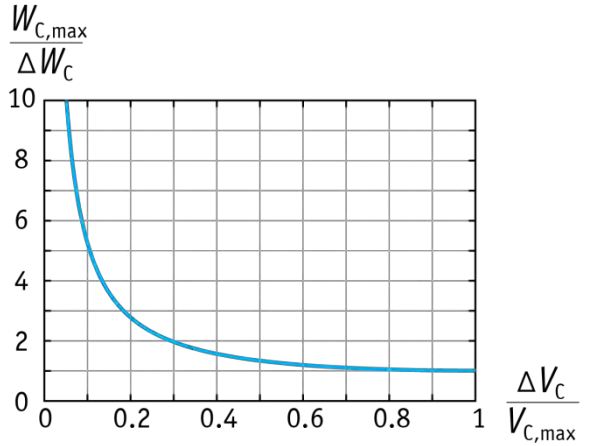
- Parallel Approach for Limiting Voltage Stress on Converter Stage Semiconductors

Passive Power Pulsation Buffer (1)

- Electrolytic Capacitor







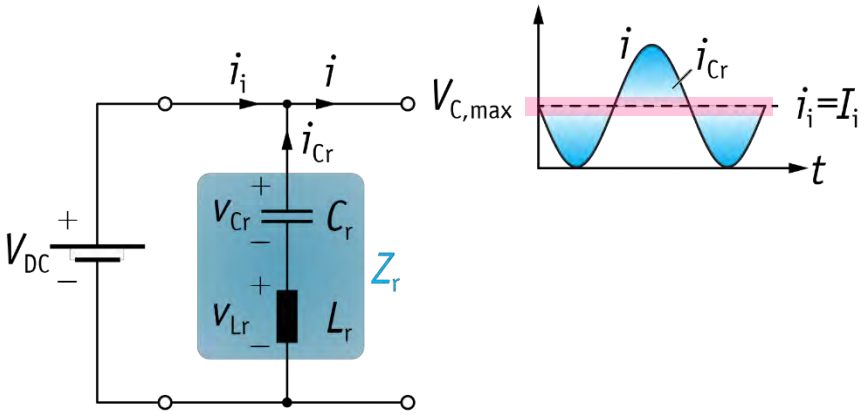
S_0 = 2.0 kVA
cos Φ_0 = 0.7
$V_{C,max}$ = 450 V
$\Delta V_C / V_{C,max}$=3 %

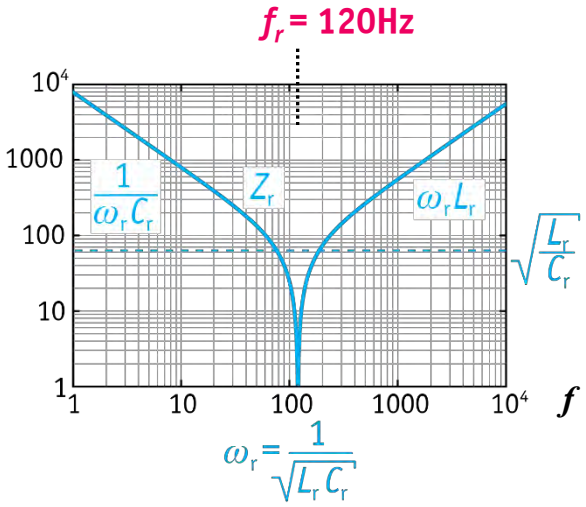
EPCOS
5 x 493µF/450 V
C= 2.46 mF

- C > 2.2mF / 166 cm^3 → Consumes 1/4 of Allowed Total Volume !

Passive Power Pulsation Buffer (2)

- Series Resonant Circuit / Used in Rectifier Input Stage of Locomotives



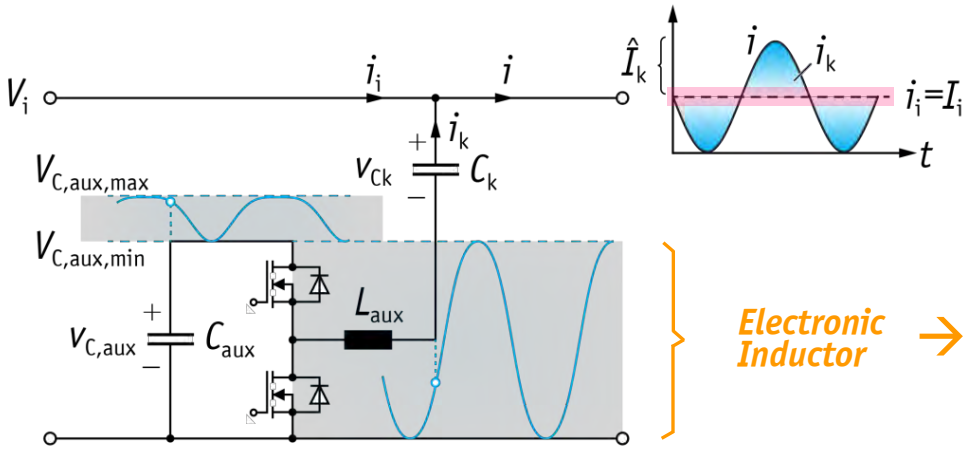


* C_r = 20 µF
* L_r = 127 mH @ v_{Lr} = 400 V

■ Unacceptably Large Inductor Volume !  → Electronic Inductor

Partial Active Power Pulsation Buffer

- Coupling Capacitor & "*Electronic Inductor*" Processing Only *Partial Power*



Electronic Inductor →

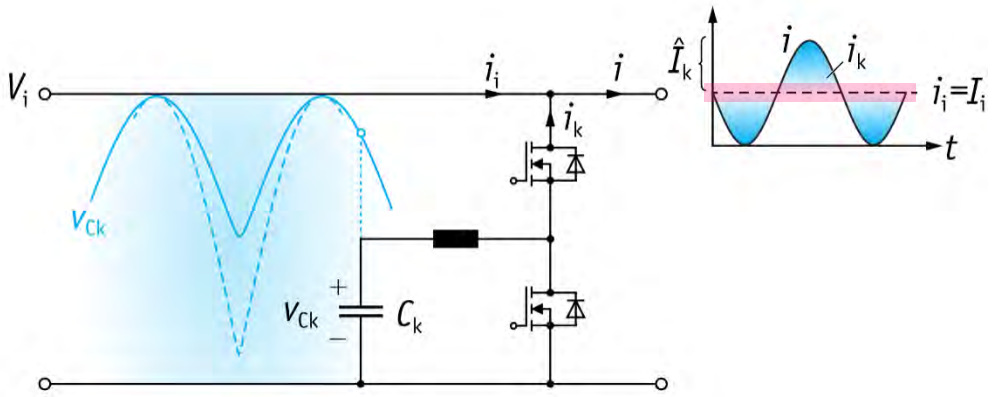
* Ertl (1999)
* Enslin (1991)
* Pilawa (2015)

- Low $U_{C,aux}$ → Low Converter Losses
- High Values of C_K, C_{aux} Required for Low $U_{C,aux}$
- Full-Bridge Aux. Converter Allows Lower $U_{C,aux}$

Full Active Power Pulsation Buffer

* Kyritsis (2007)

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck- or Boost-Type DC/DC Interface Converter
- Buck-Type allows Utilizing 600V Technology



CeraLink TDK

108 x 1.2 µF /400 V
$C_k \approx 140$ µF
$V_{Ck} = 23.7\text{cm}^3$

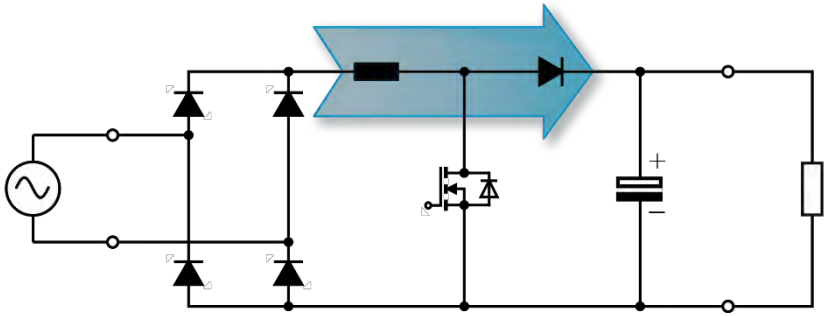
- Significantly Lower Overall Volume Compared to Electrolytic Capacitor

Output Stage Topology / Modulation

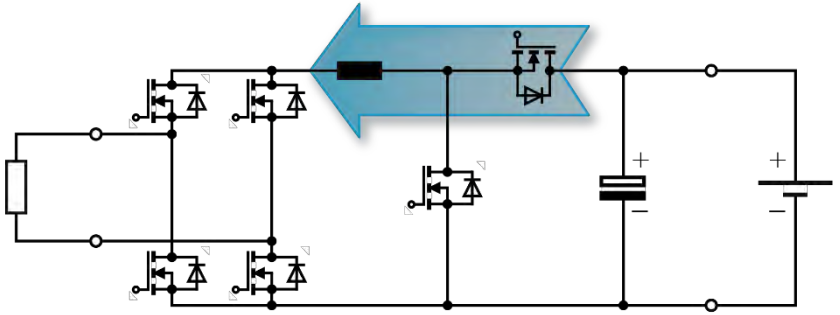
Derivation of Output Stage Topology (1)

- Inversion of Basic 1-Φ PFC Rectifier Topology

– Boost-Type
1-Φ PFC Rectifier



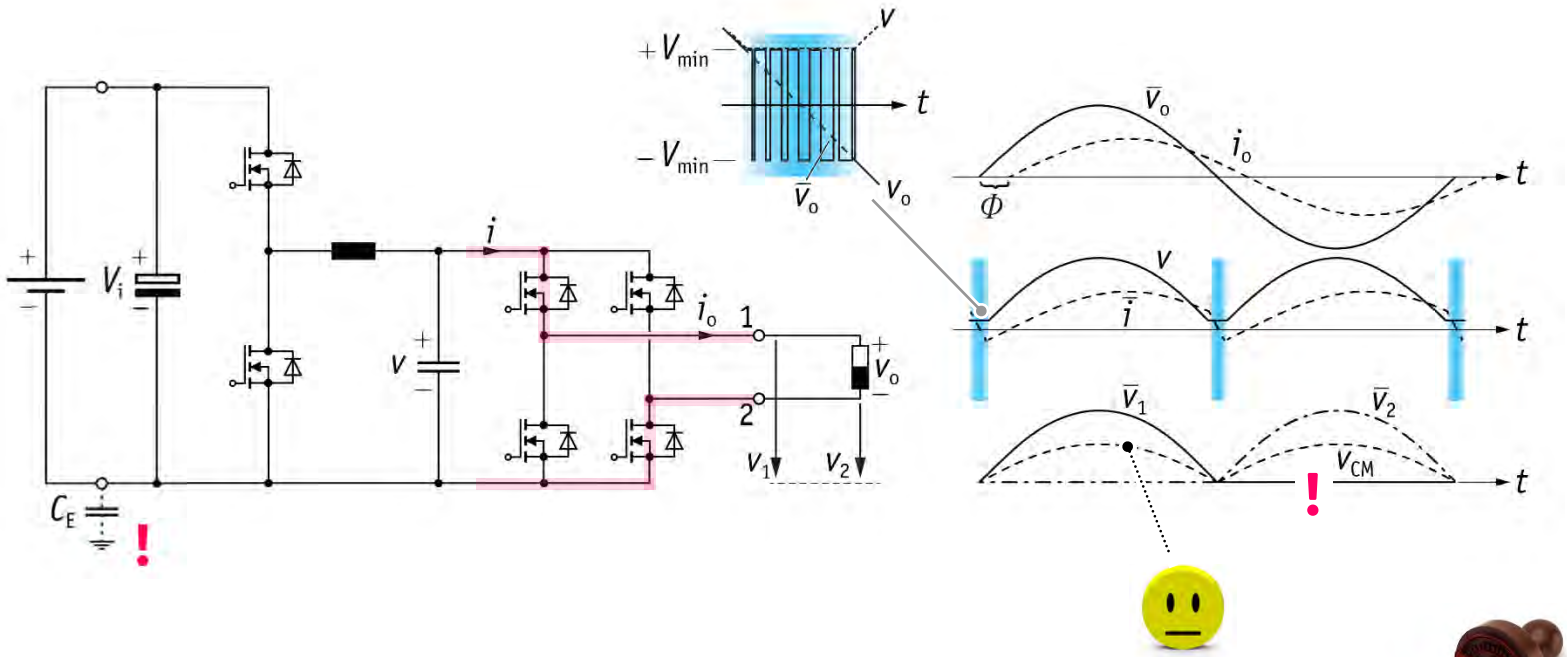
– DC/|AC| Buck Converter &
Mains Frequency "Unfolder"



* Erickson (2009) → Analysis Only for cos Φ = -1

Advanced DC/|AC|-Buck Conv. & Unfolder

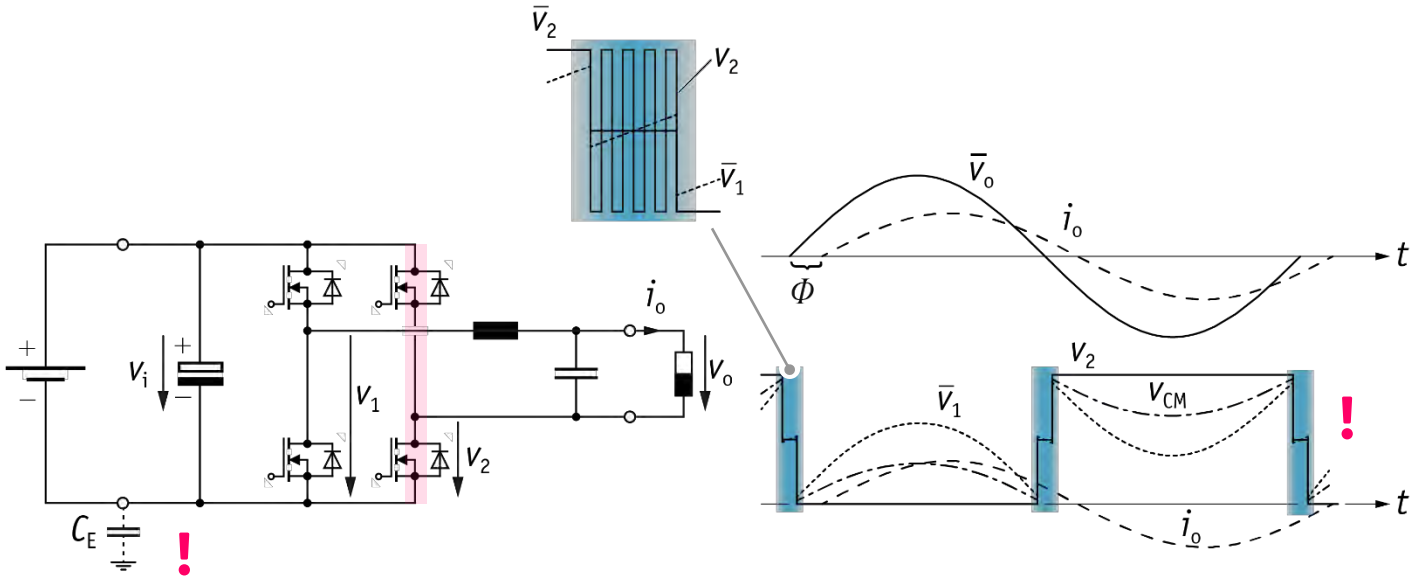
- Temporary PWM Operation of Unfolder @ $U < U_{min}$ to Avoid AC Current Distortion



- CM Component of Output Voltage v_0
- Larger EMI Filtering Requirement Due to Temporary High-Frequ. Switching of Unfolder

Advanced Full-Bridge DC/AC Conv. Topology

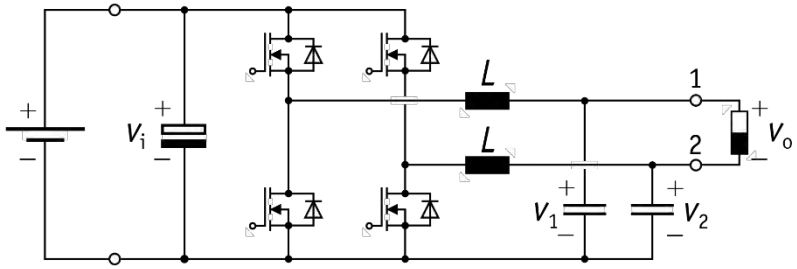
- New Control Concept - PWM Operation of Mains Freq. Unfolder Bridge Leg @ $|u| < u_{0,min}$

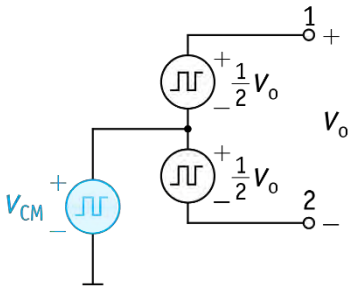


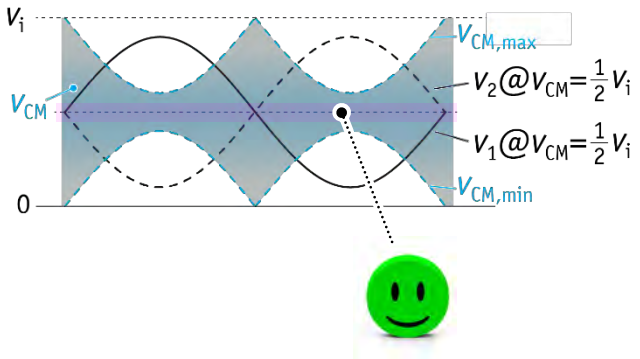
- CM Component u_{CM} of Generated Output Voltage
- Potentially Larger EMI Filtering Requirement

Symmetric PWM Full-Bridge AC/DC Conv. Topology

- Symmetric PWM Operation of Both Bridge Legs
- No Low-Frequency CM Output Voltage Component





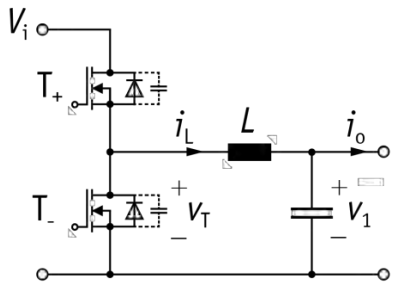


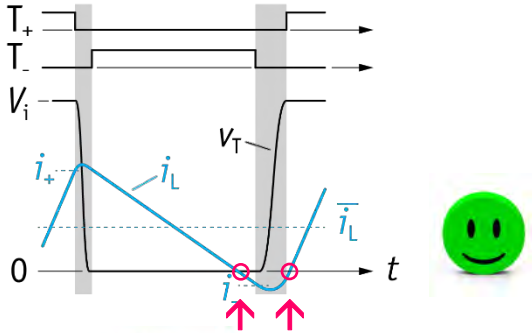
- DM Component of u_1 and u_2 Defines Output u_0
- CM Component of u_1 and u_2 Represents Degree of Freedom of the Modulation (!)

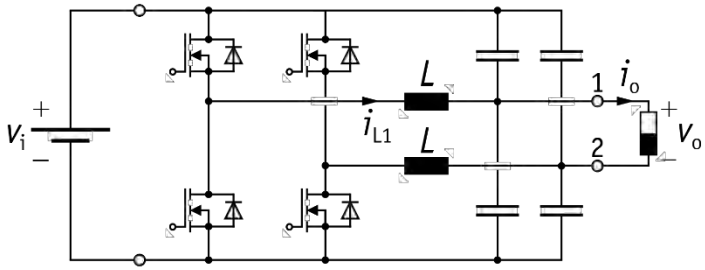
ZVS of Output Stage / TCM Operation

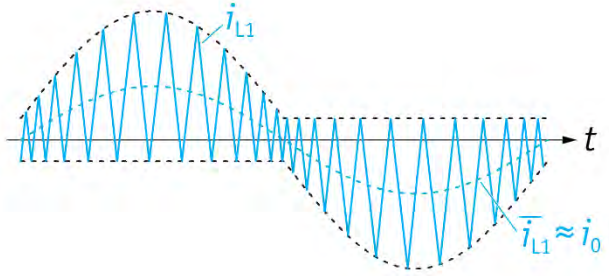
* Henze (1988)

- TCM Operation for Resonant Voltage Transition @ Turn-On/Turn-Off





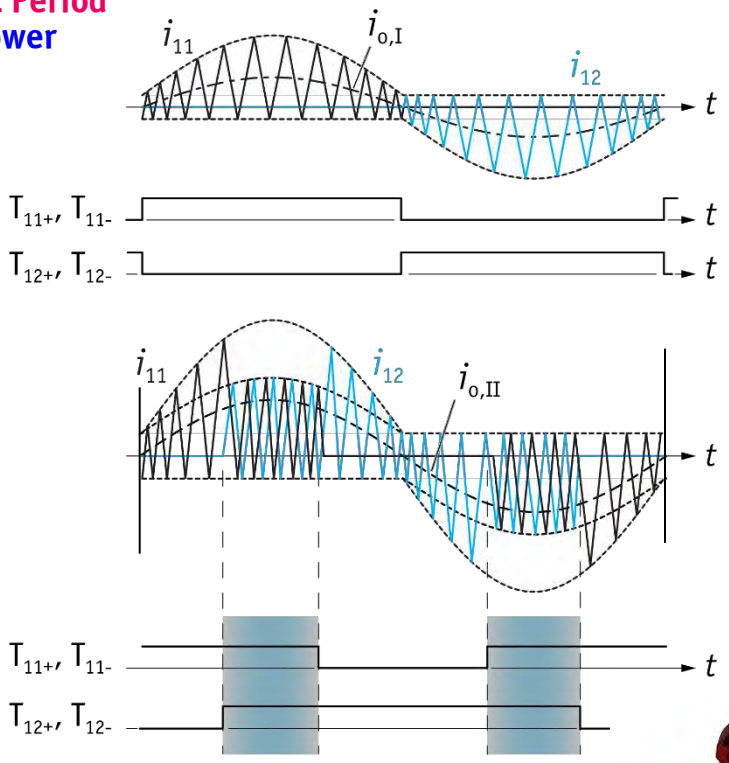


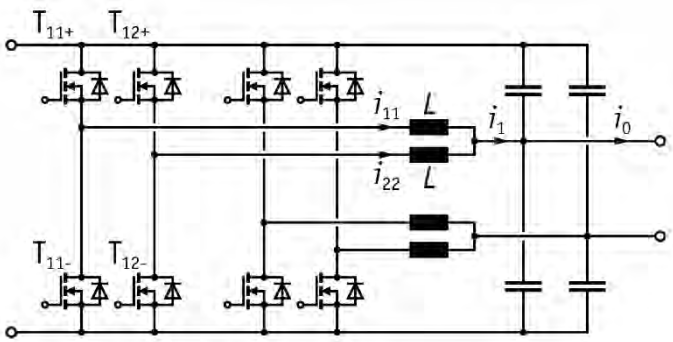


- Requires Only Measurement of Current Zero Crossings, i = 0
- Variable Switching Frequency Lowers EMI

4D-Interleaving

- Interleaving of 2 Bridge Legs per Phase - Volume / Filtering / Efficiency Optimum
- Interleaving in Space & Time – Within Output Period
- Alternate Operation of Bridge Legs @ Low Power
- Overlapping Operation @ High Power



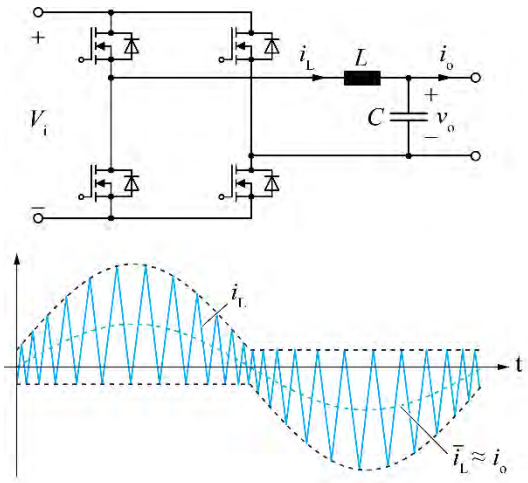


- Opt. Trade-Off of Conduction & Switching Losses / Opt. Distribution of Losses

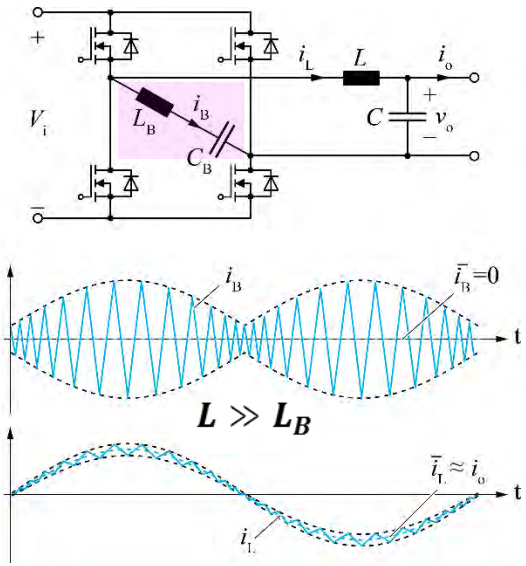
Remark: iTCM Inverter Topology

- TCM : Challenging Inductor Design → Superposition of HF & LF Currents
- iTCM: Adding LC-Circuit between Bridge Legs → Separation of LF & HF Currents → $L >> L_B$

– TCM



– iTCM

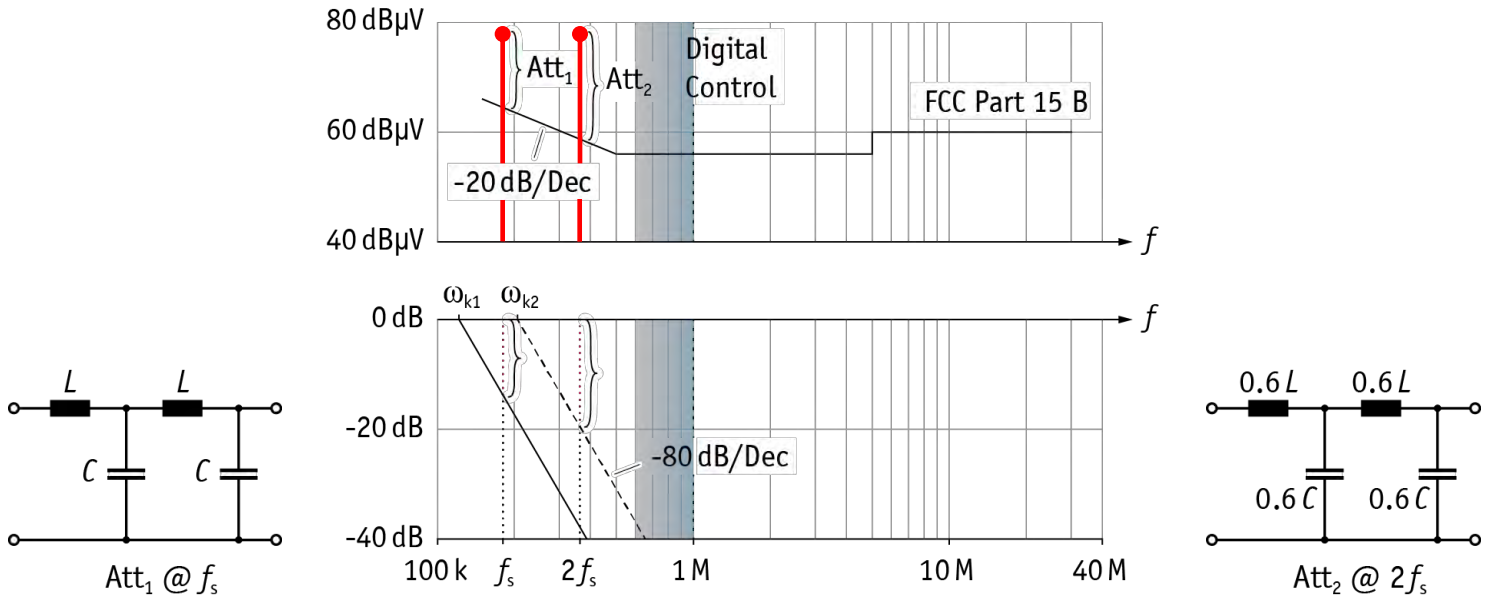


- Low Output Current Ripple → Reduced Filtering Effort
- PWM Modulation Applicable → Simple Control Strategy
- Dedicated LF and HF Inductor Designs Possible → Improved Converter Efficiency

* P. Jain (2015)

Selection of Switching Frequency

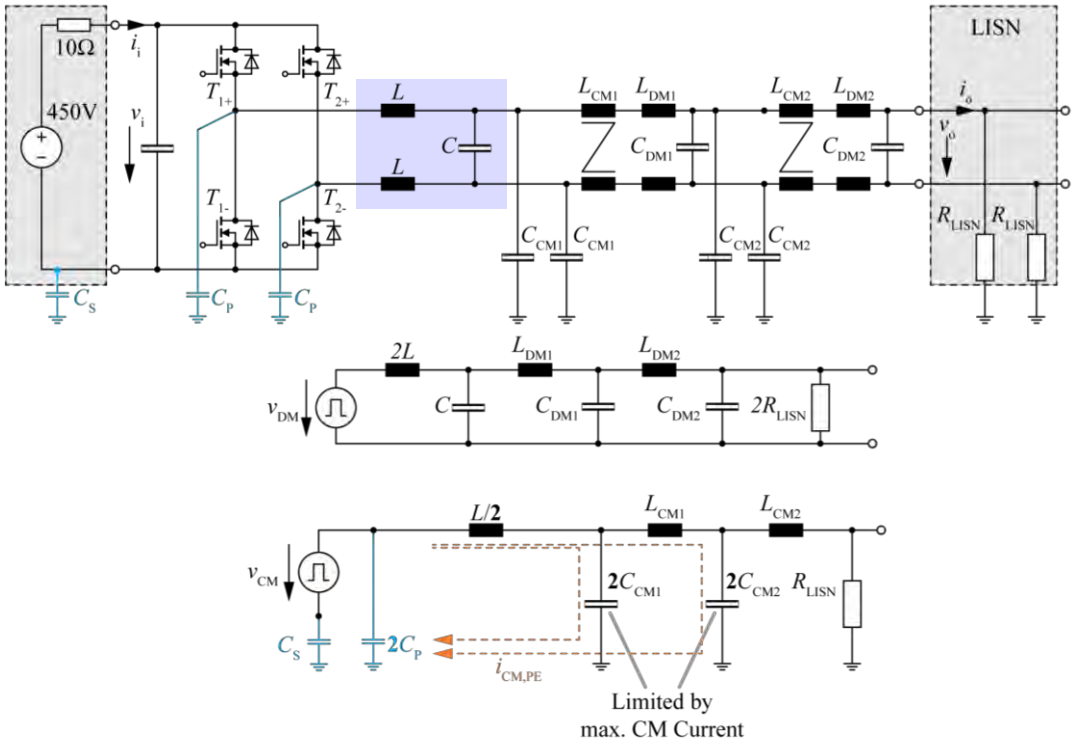
- Significant Reduction in EMI Filter Volume for Increasing Sw. Frequency



- Doubling Sw. Fequ. f_S Cuts Filter Volume in Half
- Upper Limit due to Digital Signal Processing Delays / Inductor & Sw. Losses – Heatsink Volume

EMI Filter Topology (1)

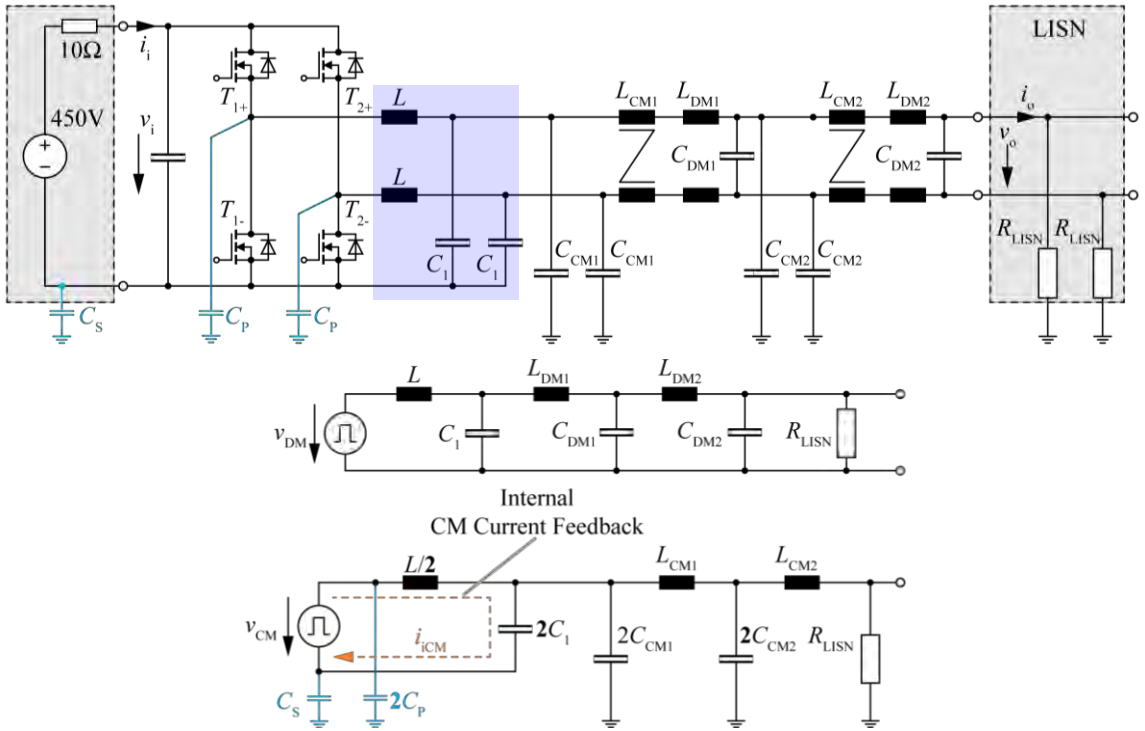
- Conventional Filter Structure
  - DM Filtering Between the Phases
  - CM Filtering Between Phases and PE



- CM Cap. Limited by Earth Current Limit – Typ. 3.5mA for PFC Rectifiers (GLBC: 5mA then 50mA !)
- Large CM Inductor Needed – Filter Volume Mainly Defined by CM Inductors

EMI Filter Topology (2)

- Filter Structure with Internal CM Capacitor Feedback
- Filtering to DC- (and optional to DC+)

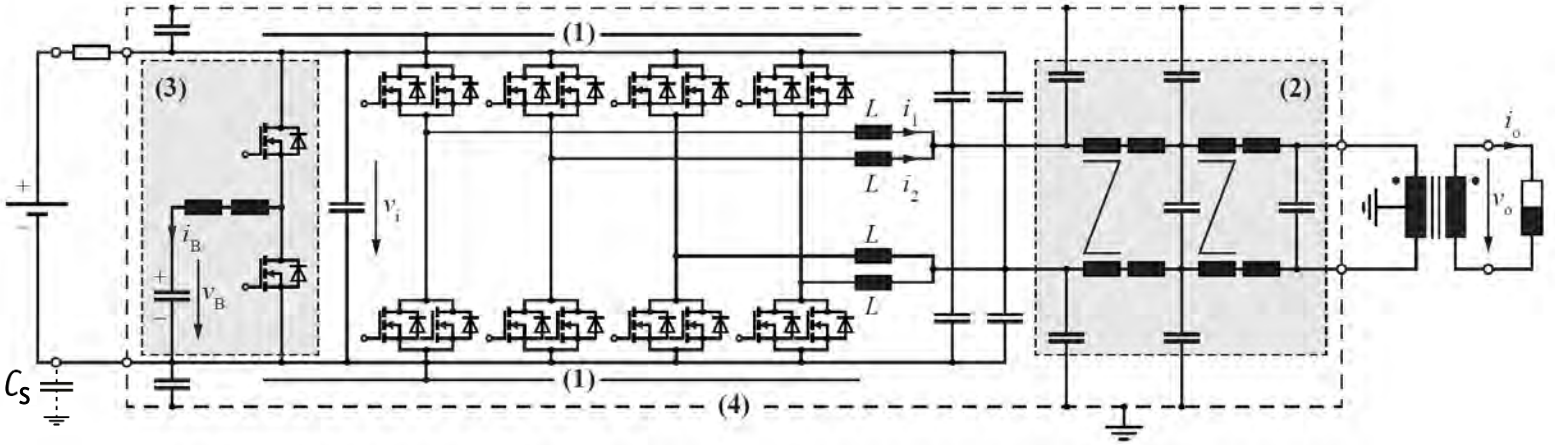


- No Limitation of CM Capacitor C_1 Due to Earth Current Limit → µF Instead of nF Can be Employed
- Allows Downsizing of CM Inductor and/or Total Filter Volume

Final Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

(1) Heat Sink
(2) EMI Filter
(3) Power Pulsation Buffer
(4) Enclosure



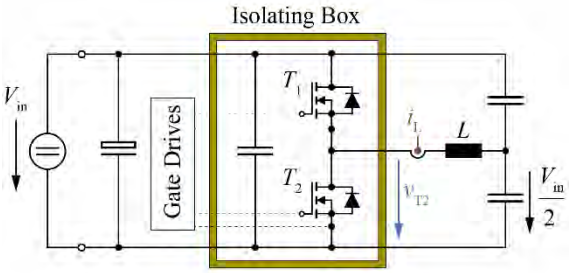
- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

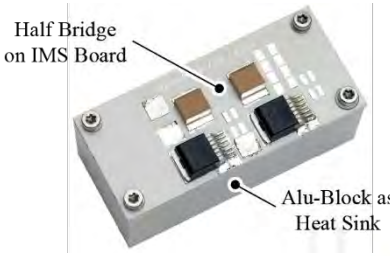
Technologies

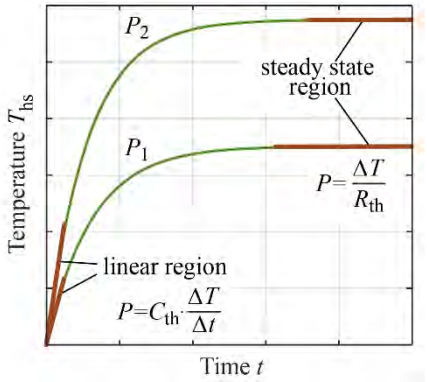
- *Power Semiconductors*
- *HF Inductors*
- *Cooling*
- *Etc.* 

Evaluation of Power Semiconductors (1)

- Accurate Measurement of ZVS Losses Using Calorimetric Approach
- High Sw. Frequency for Large Ratio of Sw. and Conduction Losses



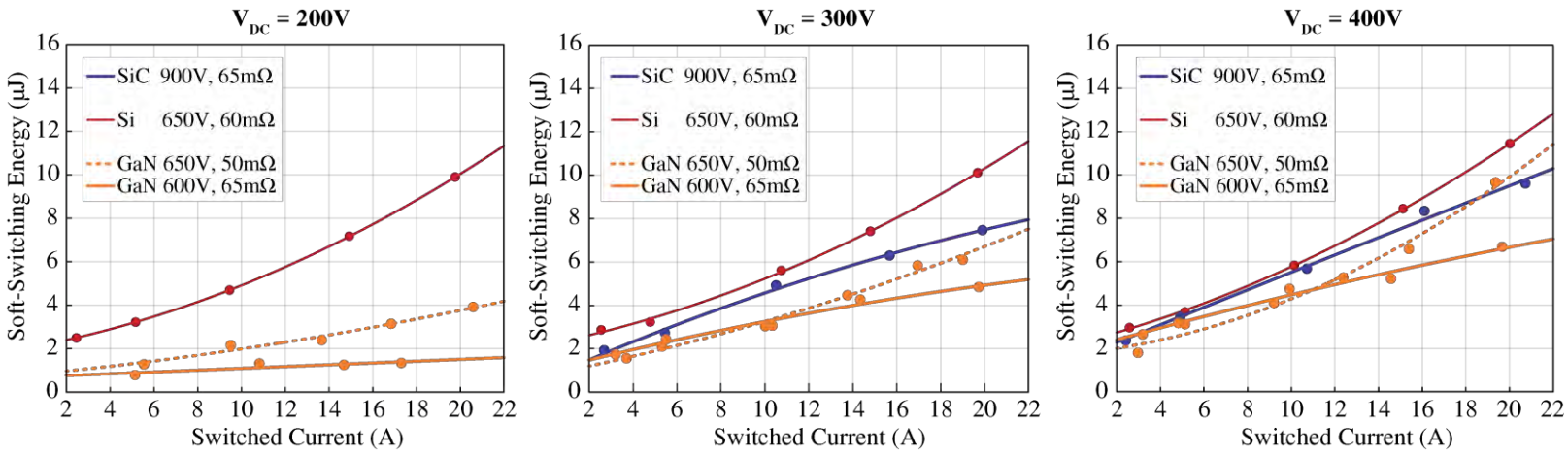




- Direct Measurement of the Sum of Sw. and Conduction Losses
- Subtraction of the Conduction Losses Known from Calibration
- Fast Measurement by $C_{th}.\Delta T/\Delta t$ Evaluation

Evaluation of Power Semiconductors (2)

- Comparison of Soft-Switching Performance of ~60mΩ, 600V/650V/900V GaN, SiC, Si MOSFETs
- Measurement of Energy Loss per Switch and Switching Period

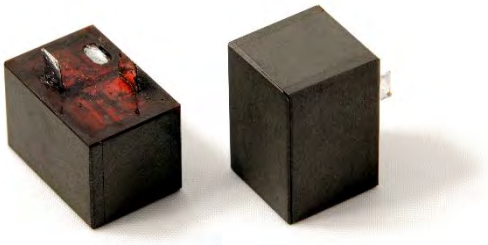


- GaN MOSFETs Feature Highest Soft-Switching Performance
- Similar Soft-Switching Performance Achieved with Si and SiC
- Almost No Voltage-Dependency of Soft-Switching Losses for Si-MOSFET

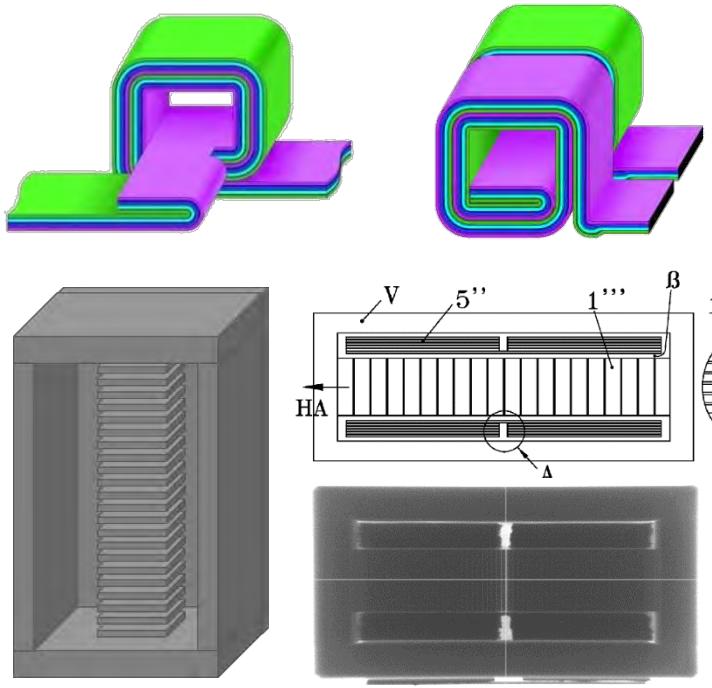
High Frequency Inductors (1)

- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- L= 10.5µH
- 2 x 8 Turns
- 24 x 80µm Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 µm Copper Foil / 4 in Parallel
- 7 µm Kapton Layer Isolation
- 20mΩ Winding Resistance / Q≈600
- Terminals in No-Leakage Flux Area

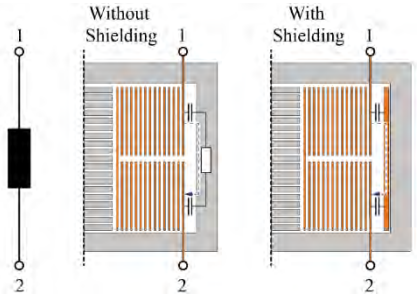


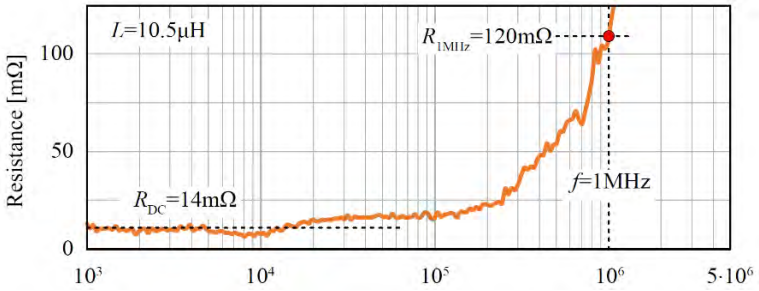
■ Dimensions - 14.5 x 14.5 x 22mm³

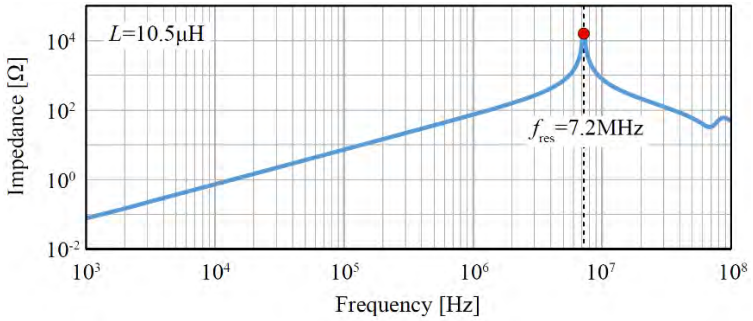


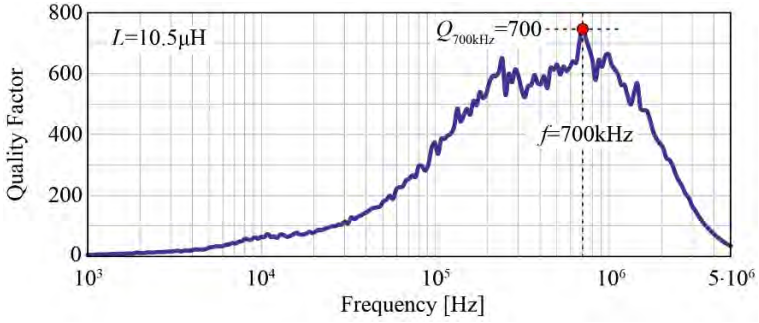
High Frequency Inductors (2)

- High Resonance Frequency → Inductive Behavior up to High Frequencies
- Extremely Low AC-Resistance → Low Conduction Losses up to High Frequencies
- High Quality Factor







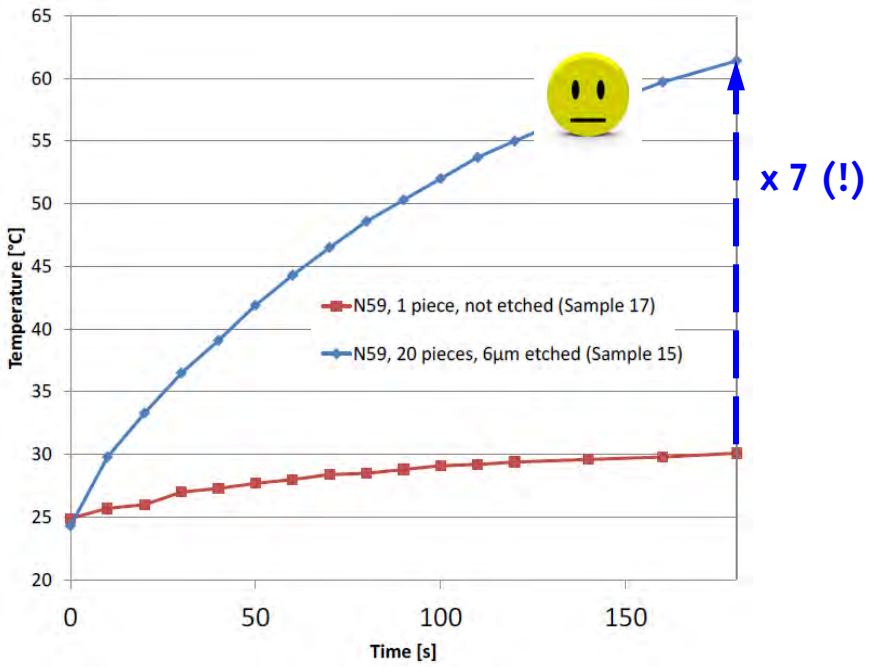


- Shielding Eliminates HF Current through the Ferrite → Avoids High Core Losses
- Shielding Increases the Parasitic Capacitance

High Frequency Inductors (3)

* Knowles (1975!)

- Cutting of Ferrite Introduces Mech. Stress
- Significant Increase of the Loss Factor
- Reduction by Polishing / Etching (5 µm)

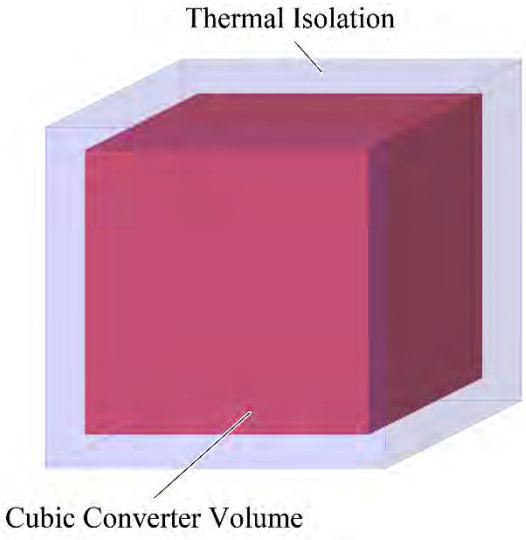


- Comparison of Temp. Increase of a Bulk and a Sliced Sample @ 70mT / 800kHz

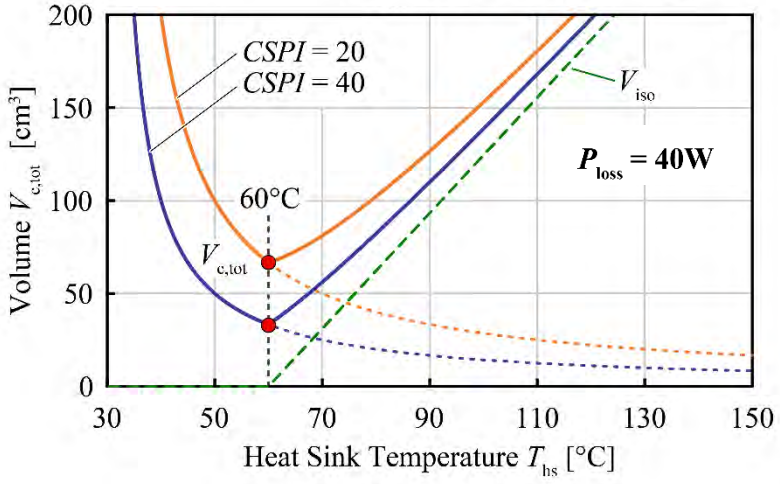
Thermal Management

- 30°C max. Ambient Temperature
- 60°C max. Allowed Surface and Air Outlet Temperature

- Evaluation of Optimum Heatsink Temperature for Thermal Isolation of Converter



$$CSPI\left[\frac{W}{K\cdot liter}\right]=\frac{G_{th,S-a}^{(HS)}\left[\frac{W}{K}\right]}{Vol_{CS}\left[liter\right]}=\frac{1}{R_{th,S-a}^{(HS)}\left[\frac{K}{W}\right]\cdot Vol_{CS}\left[liter\right]}$$



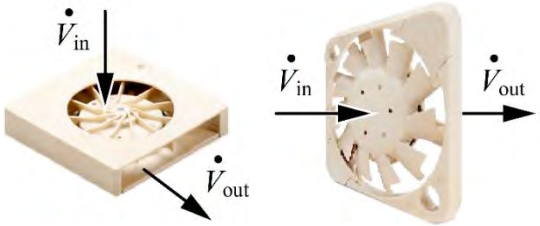
- Minimum Volume Achieved w/o Thermal Isolation with Heatsink @ max. Allowed Surface Temp.

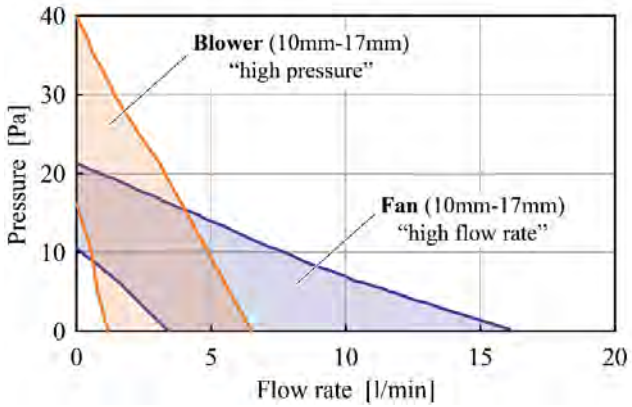
Thermal Management

- Overall Cooling Performance Defined by Selected Fan Type and Heatsink

– Radial Blower

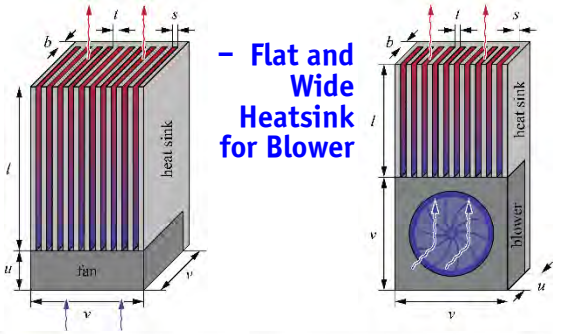
– Axial Fan

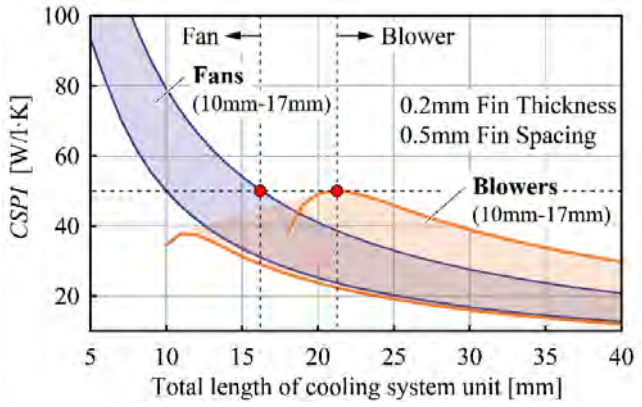




– Square Cross Section of Heatsink for Using a Fan

– Flat and Wide Heatsink for Blower



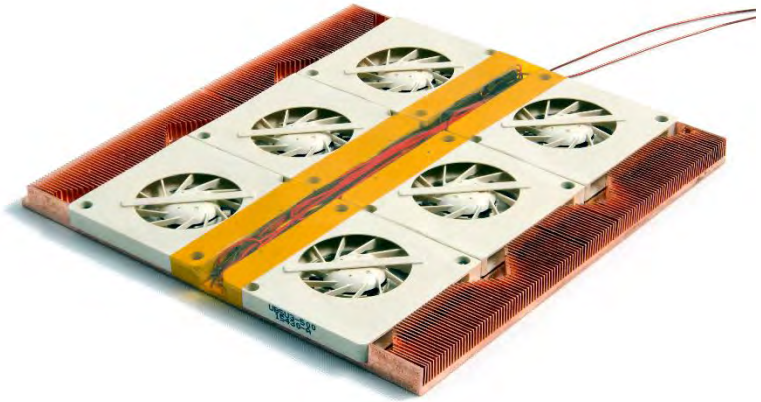


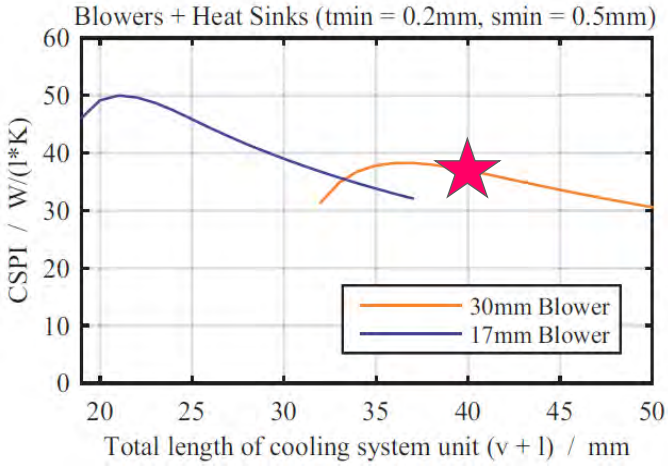
- Optimal Fan and Heat Sink Configuration Defined by Total Cooling System Length
- Cooling Concept with Blower Selected → Higher *CSPI* for Larger Mounting Surface

Final Thermal Management Concept (1)

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters

- 200um Fin Thickness
- 500um Fin Spacing
- 3mm Fin Height
- 10mm Fin Length
- CSPI = 37 W/(dm³.K)
- 1.5mm Baseplate

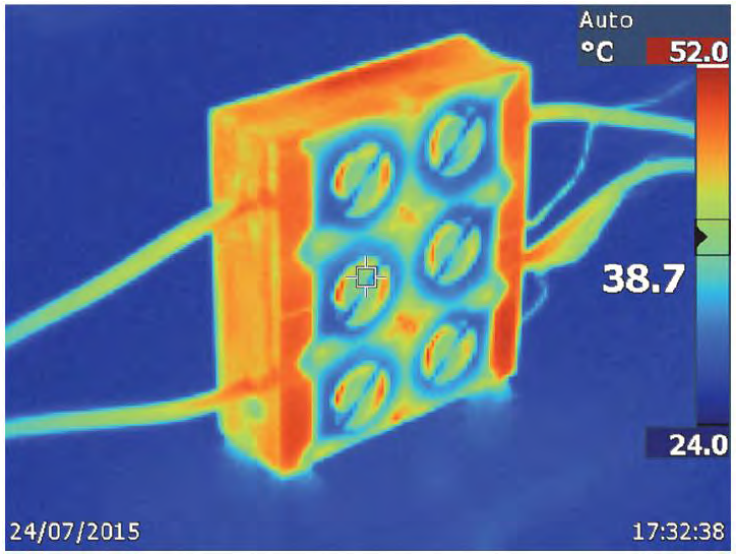




- $CSPI_{eff}$= 25 W/(dm³.K) Considering Heat Distribution Elements
- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)

Final Thermal Management Concept (2)

- CSPI = 37 W/(dm^3.K)
- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters
- CSPI$_{eff}$=25 W/(dm^3.K) incl. Heat Cond. Layers



- CSPI$_{eff}$= 25 W/(dm^3.K) Considering Heat Distribution Elements
- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)

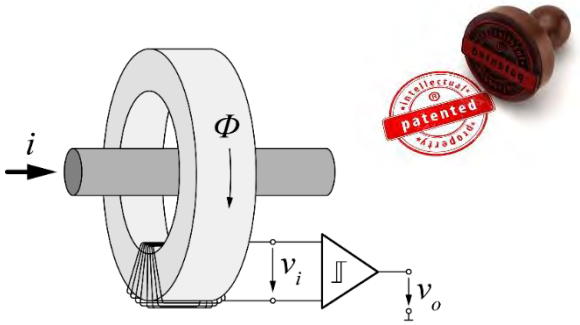
i=0 Detection

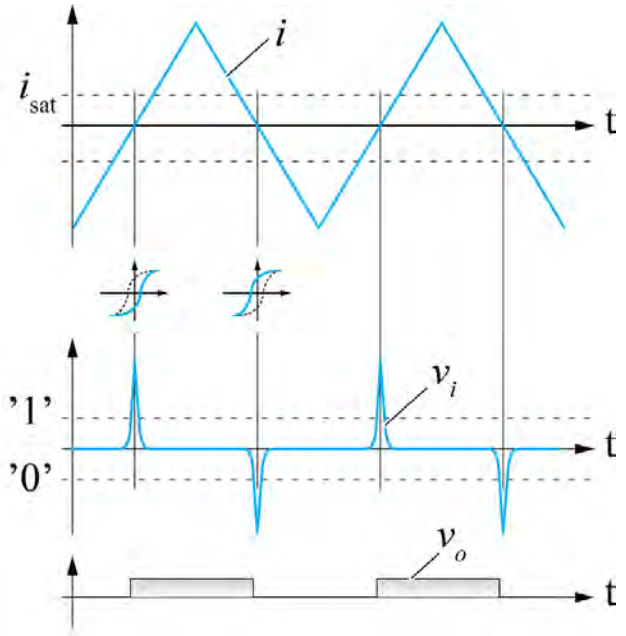
- Analyzed Methods
  - Shunt Current Measurement
  - Measurement of the $R_{ds,on}$
  - Two Antiparallel Diodes
  - Giant Magneto-Resistive Sensor
  - Hall Element

  Various Drawbacks

  Losses, No Galvanic Isolation, Low Signal-to-Noise Ratio (SNR), Size, Bandwidth, Realization Effort

  - Saturable Inductor

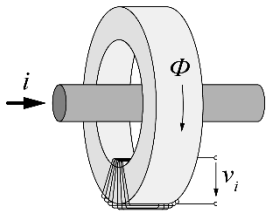


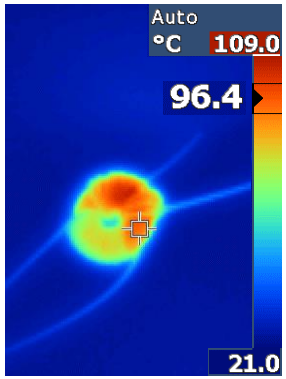


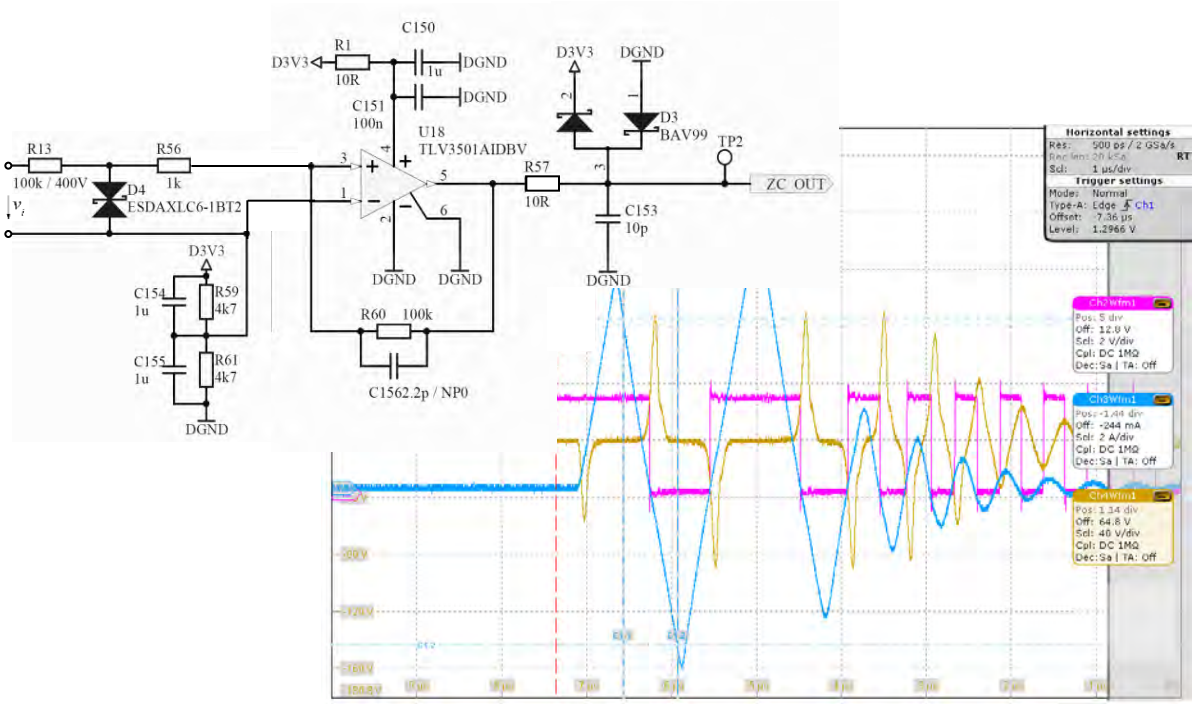
- Galvanic Isolation, High SNR, Small Size, High Bandwidth, Simple Design
- Min. Core Volume/Cross Section for Min. Core Losses

i=0 Detection

- Saturable Inductor – Toroidal Core R4 x 2.4 x 1.6, EPCOS (4mm Diameter)
  – Core Material N30, EPCOS



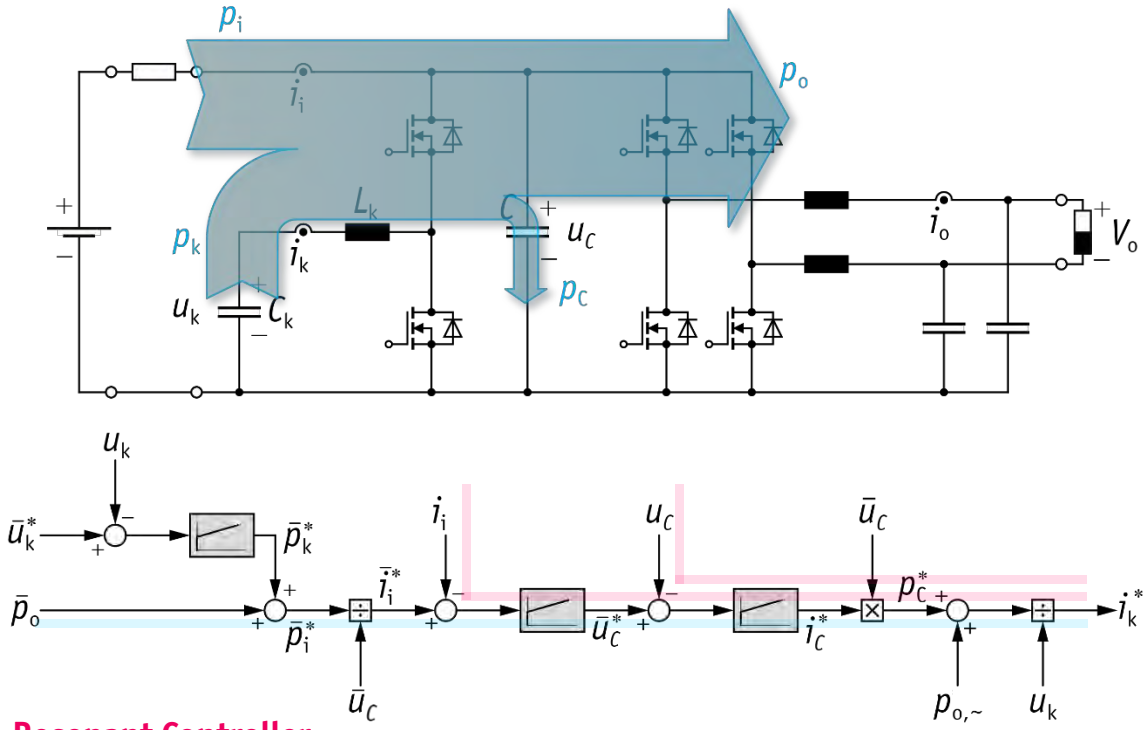




- Operation Tested up to 2.5MHz Switching Frequency

Active Power Pulsation Buffer

- New Cascaded Control Structure

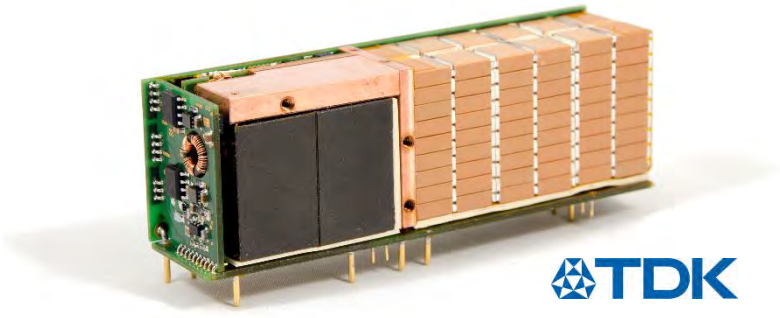


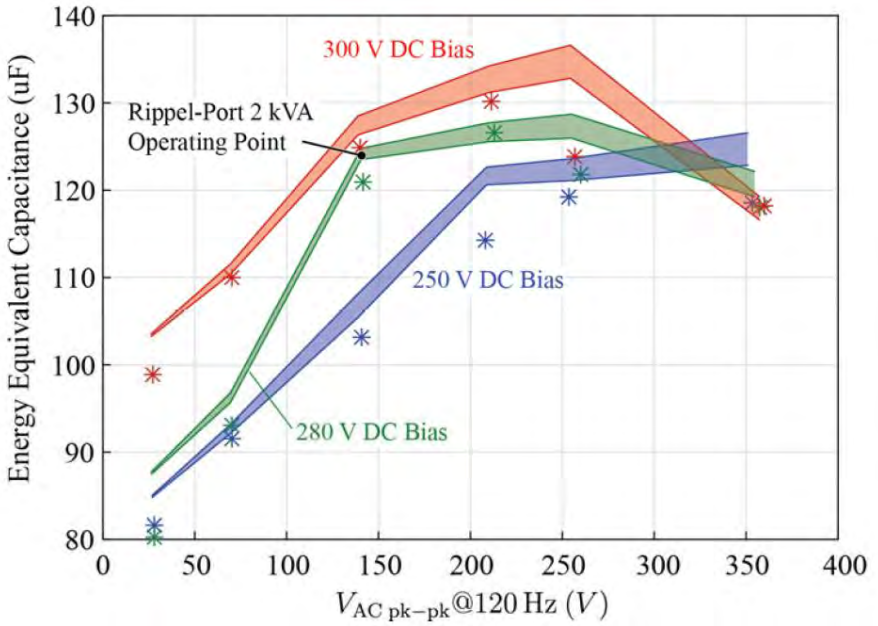
- P-Type Resonant Controller
- Feedforward of Output Power Fluctuation
- Underlying Input Current (i_i) / DC Link Voltage (u_C) Control

Final Active Power Pulsation Buffer

- High Energy Density 2nd Gen. 400VDC CeraLink Capacitors Utilized as Energy Storage
- Highly Non-Linear Behavior → Optimal DC Bias Voltage of 280VDC
- Losses of 6W @ 2kVA Output Power

- 108 x 1.2µF /400 V
- 23.7cm³ Capacitor Volume



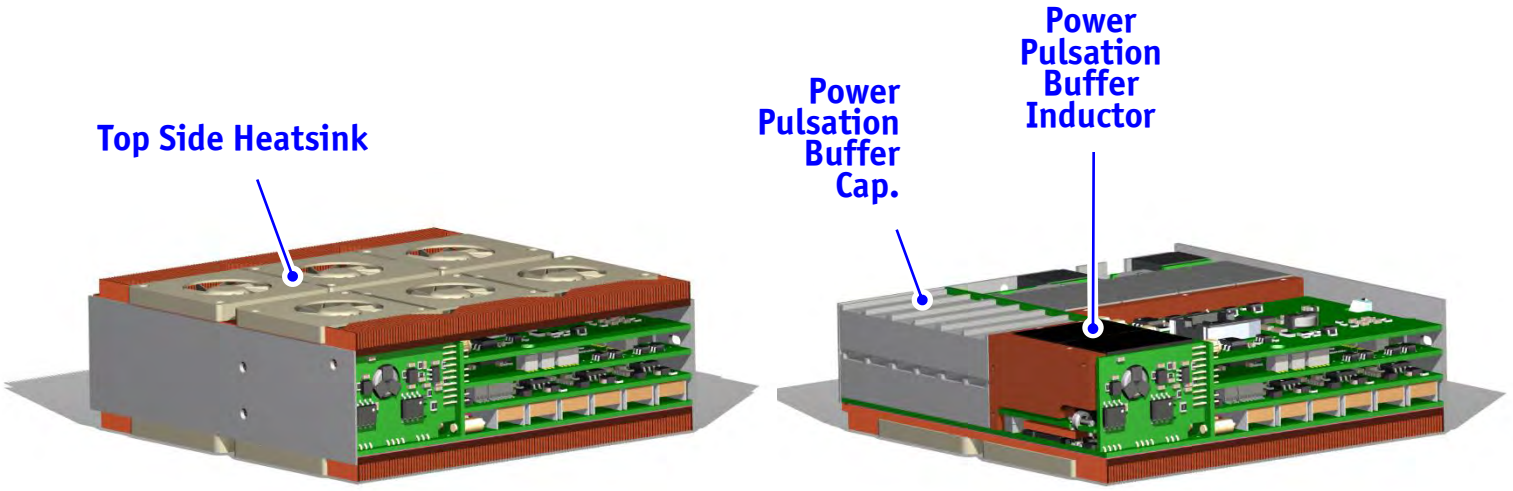


- Effective Large Signal Capacitance of C ≈160µF

3D-CAD Construction →

Mechanical Construction (1)

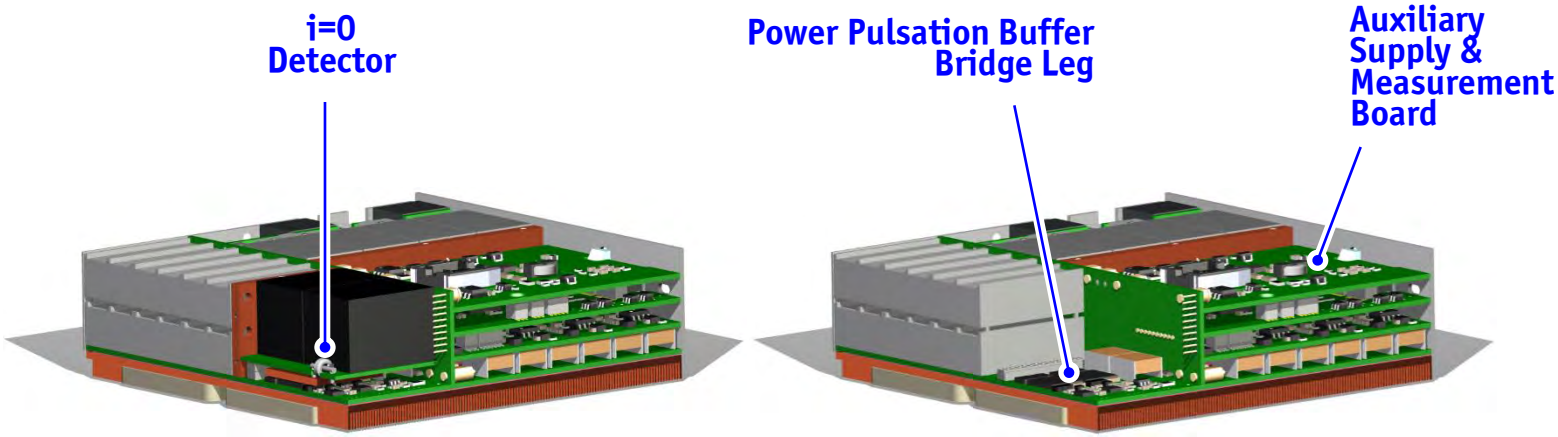
- Built to the Power Density Limit @ η= 95% / T_c < 60°C



- 88.7mm x 88.4mm x 31mm = 243cm^3 (14.8in^3) → 8.2 kW/dm^3

Mechanical Construction (2)

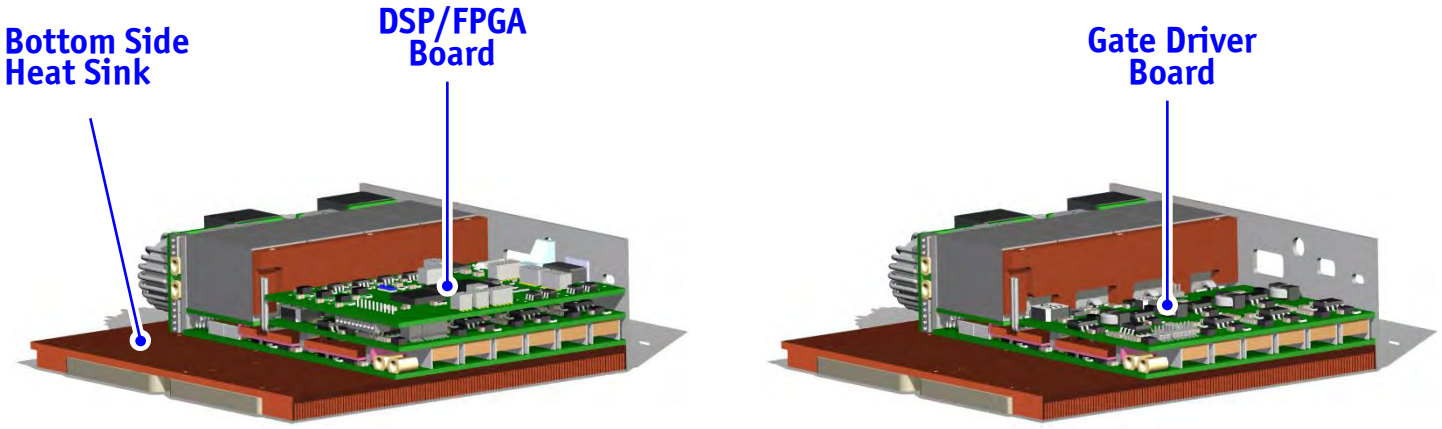
- Built to the Power Density Limit @ η= 95% / T_c < 60°C



- 88.7mm x 88.4mm x 31mm = 243cm^3 (14.8in^3) → 8.2 kW/dm^3

Mechanical Construction (3)

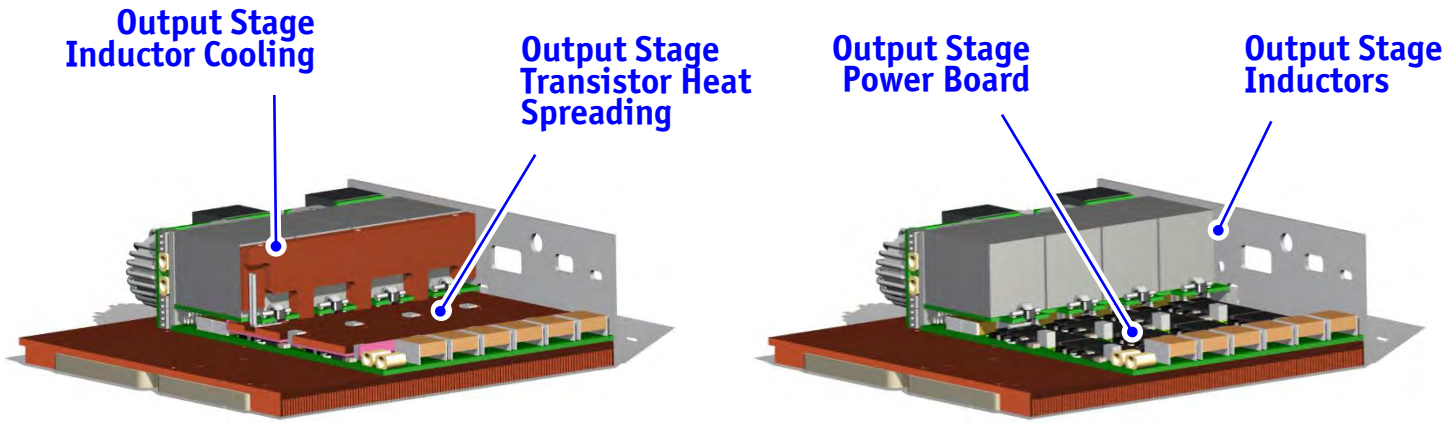
- Built to the Power Density Limit @ η= 95% / T_c < 60°C



- 88.7mm x 88.4mm x 31mm = 243cm^3 (14.8in^3) → 8.2 kW/dm^3

Mechanical Construction (4)

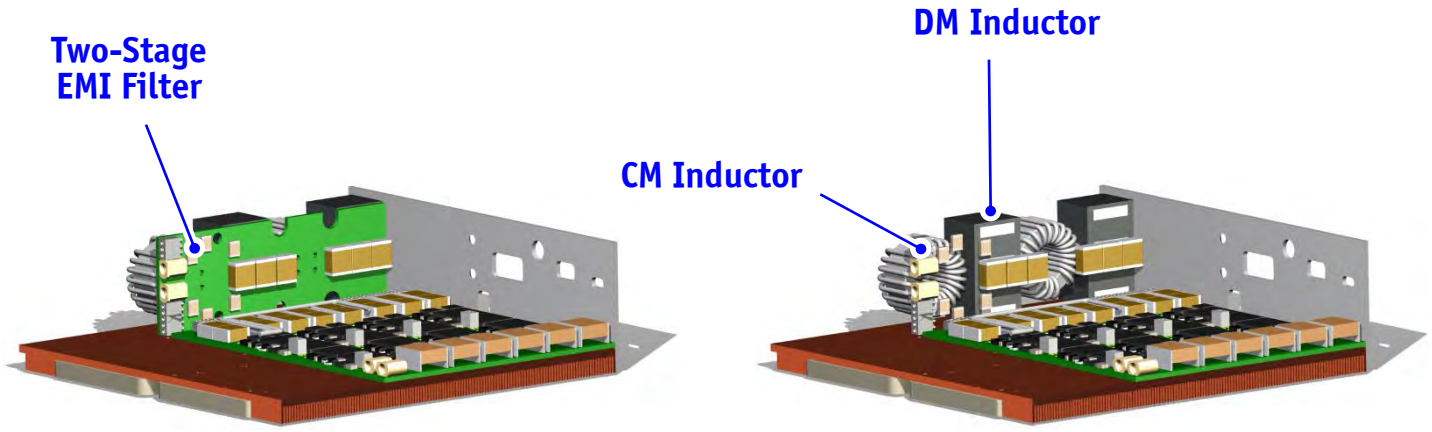
- Built to the Power Density Limit @ η= 95% / T_c < 60°C



- 88.7mm x 88.4mm x 31mm = 243cm^3 (14.8in^3) → 8.2 kW/dm^3

Mechanical Construction (5)

- Built to the Power Density Limit @ η= 95% / T_c < 60°C



- 88.7mm x 88.4mm x 31mm = 243cm^3 (14.8in^3) → 8.2 kW/dm^3

Experimental Results

Hardware

Output Voltage/Input Current Quality

Efficiency →

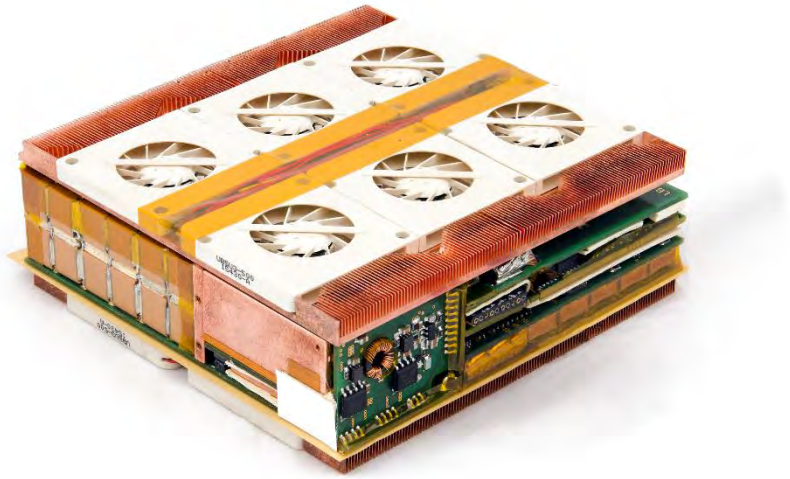
Little Box 1.0 - Prototype

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- 96,3% Efficiency @ 2kW
- T_c=58°C @ 2kW

- $\Delta u_{DC,pp}$ = 1.1%
- $\Delta i_{DC,pp}$ = 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%

★ 135 W/in³



- Compliant to All *Original* Specifications (!)

- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

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- Δi_{DC}= 2.8%
- $THD+N_U$= 2.6%
- $THD+N_I$= 1.9%

■ Compliant to All *Original* Specifications (!)

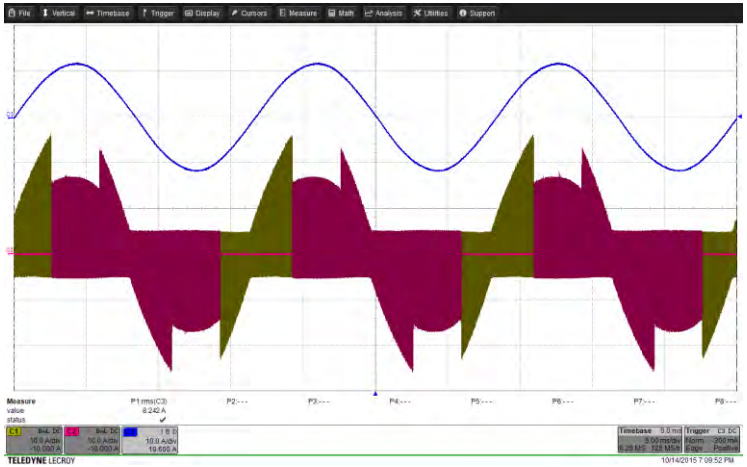
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

Little Box 1.0 - Measurement Results (1)

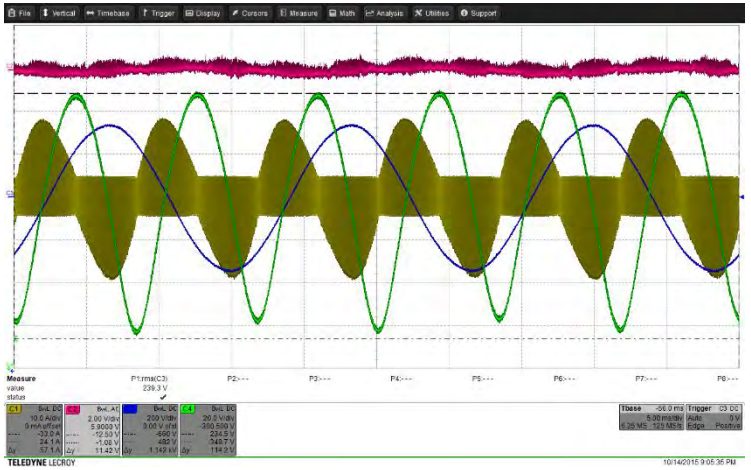
- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

- Ohmic Load / 2kW

Output Current (10 A/div)
Inductor Current Bridge Leg 1-1 (10 A/div)
Inductor Current Bridge Leg 1-2 (10 A/div)



DC Link Voltage (AC-Coupl., 2 V/div)
Buffer Cap. Voltage (20 V/div)
Buffer Cap. Current (10 A/div)
Output Voltage (200 V/div)

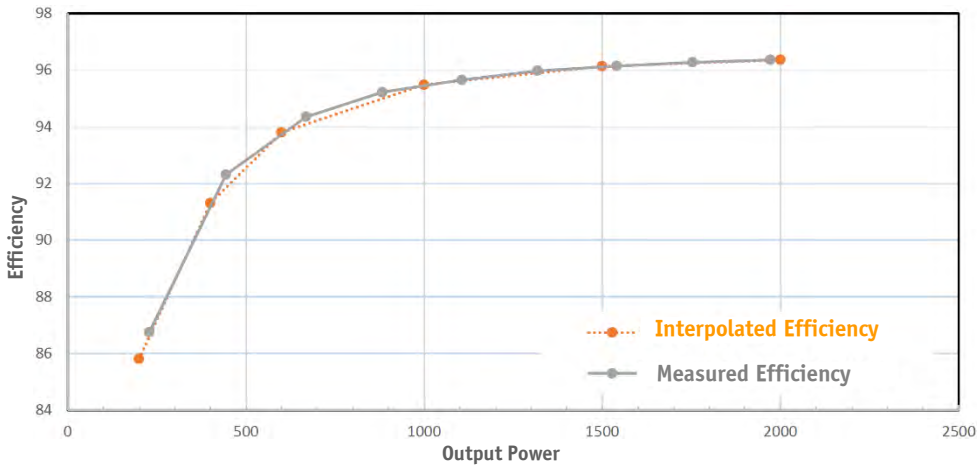


- Compliant to All Specifications

Little Box 1.0 - Measurement Results (2)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

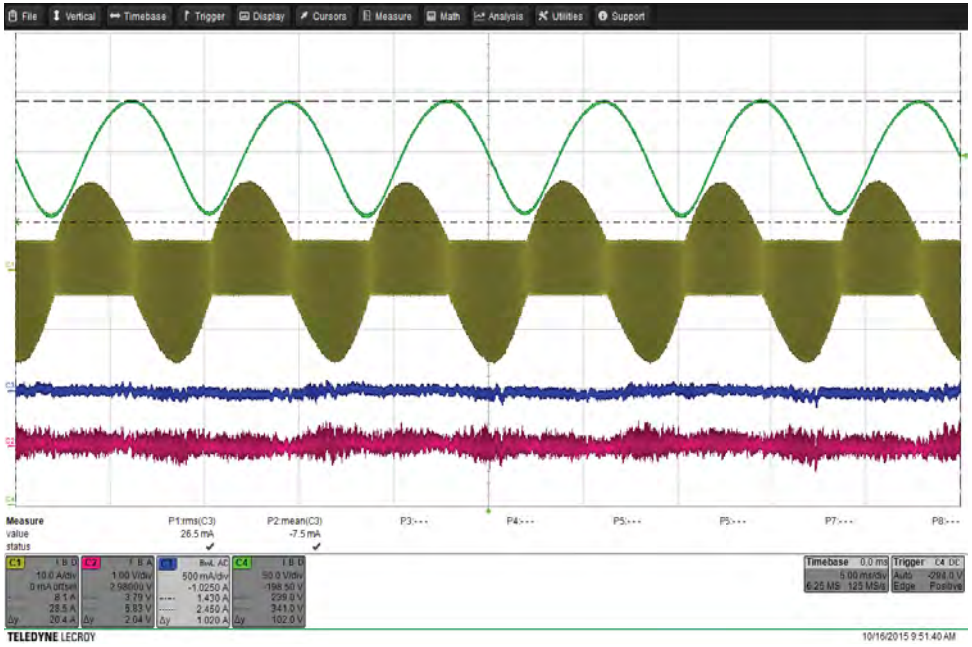
★ η_w=95.07% Weighted Efficiency



- Compliant to All Specifications

Little Box 1.0 - Measurement Results (3)

- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

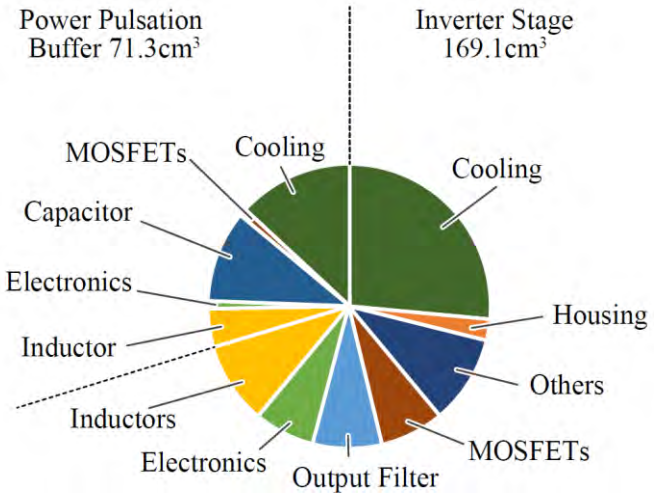


Buffer Cap. Voltage (50 V/div)
Buffer Cap. Current (10 A/div)
Conv. Inp. Curr. (AC Coupl. 500 mA/div)
DC Link Voltage (AC Coupl. 1 V/div)

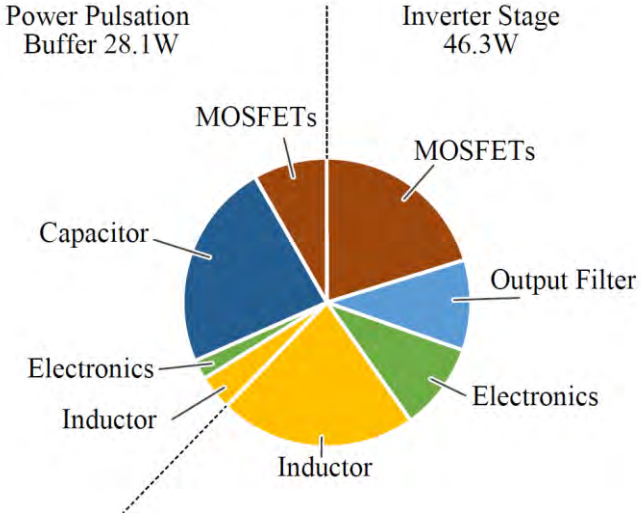
- Stationary Operation @ 2kW Output Power

Little Box 1.0 - Volume and Loss Distribution

- Volume Distribution (240cm³)



- Loss Distribution (75W)



- Large Heatsink (incl. Heat Conduction Layers)
- Large Losses in Power Fluctuation Buffer Capacitor (!)
- TCM Causes Relatively High Conduction & Switching Losses @ Low Power
- Relatively Low Switching Frequency @ High Power – Determines EMI Filter Volume

Other Finalists

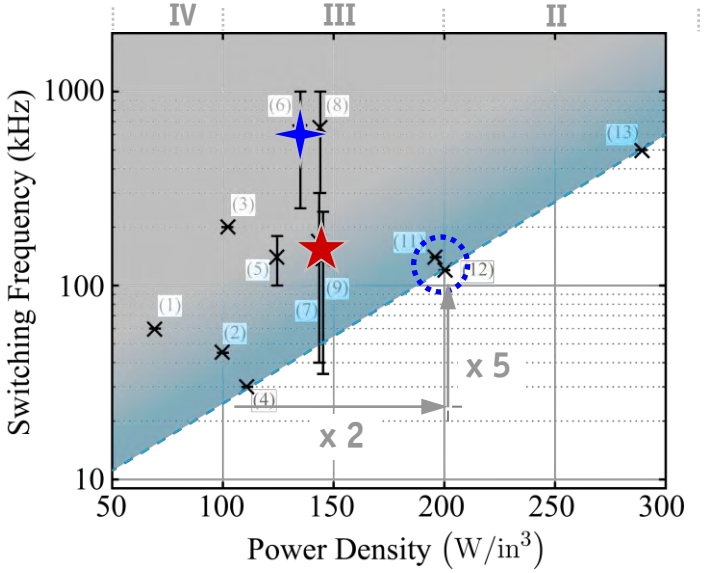
Topologies
Switching Frequencies
Power Density / Efficiency Comparison →

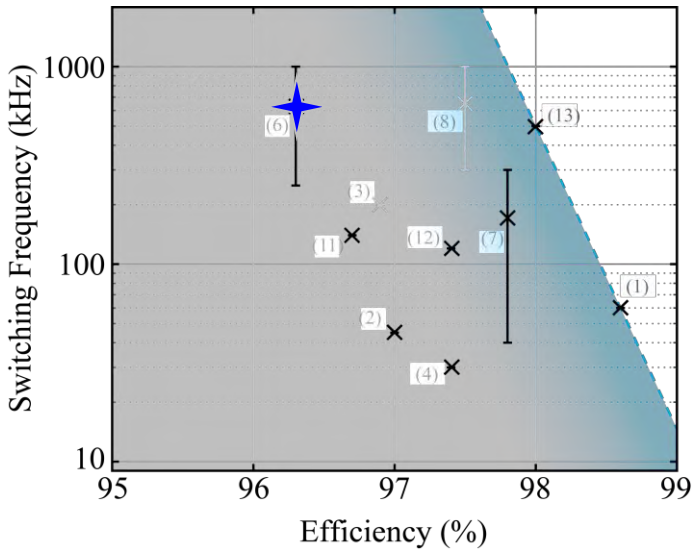
Detailed Descriptions:
www.LittleBoxChallenge.com

Finalists - Performance Overview

- **18 Finalists (3 No-Shows)**
- 7 Groups of Consultants / 7 Companies / 4 Universities

Note: Numbering of Teams is Arbitrary





- **70…300 W/in³**
- **35 kHz…500kHz…1 MHz** (up to 1MHz: 3 Teams)
- Full-Bridge or DC/|AC|Buck Converter + Unfolder
- Mostly Buck-Type Active Power Pulsation Filters (Ceramic Caps of Electrolytic Caps)
- **GaN (11 Teams)** / SiC (2 Teams) / Si (2 Teams)

Finalists - Performance Overview

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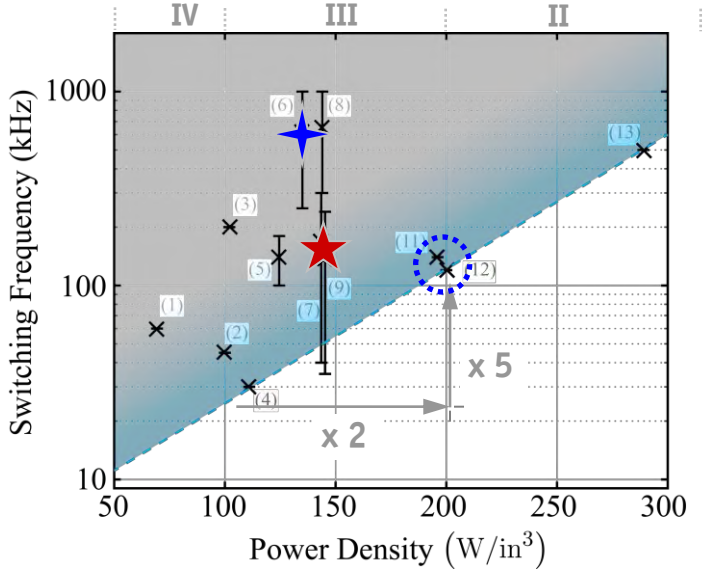

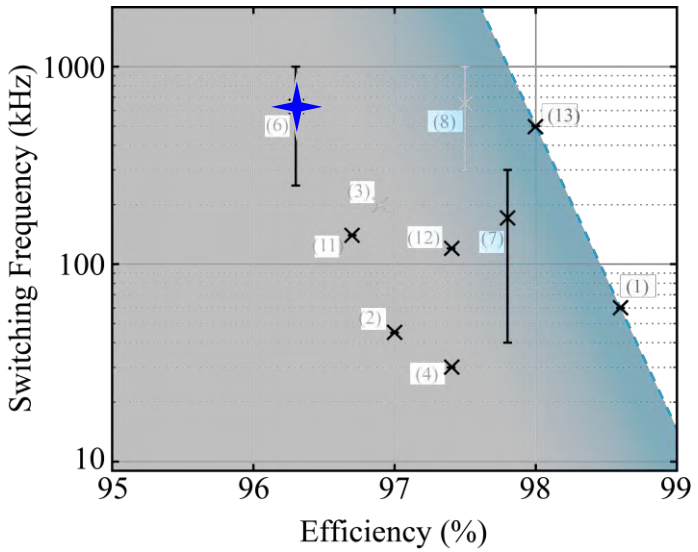

(1) Virginia Tech
(2) Schneider Electric
(3) EPRI (Univ. of Tennessee)
(4) Venderbosch
(5) Energy Layer
(6) ETH Zurich
(7) Rompower
(8) Tommasi-Bailly
(9) Red Electric Devils
(10) AHED
(11) FH IISB
(12) Univ. of Illinois
(13) AMR
(14) OKE
(15) Cambridge Magnetics

Finalists - Performance Overview

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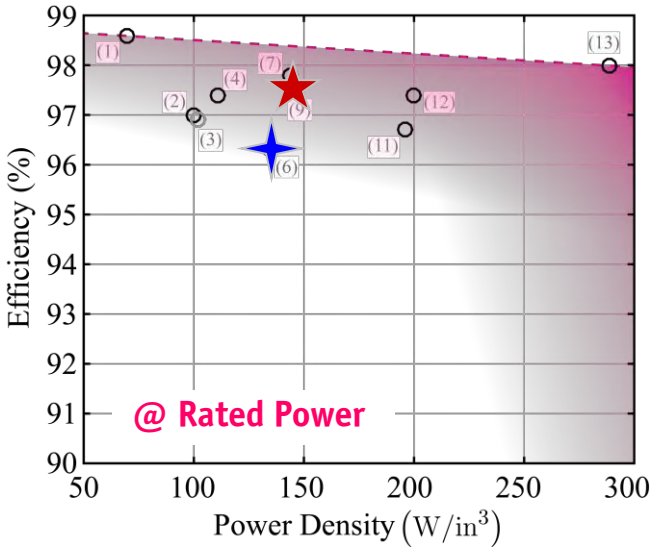

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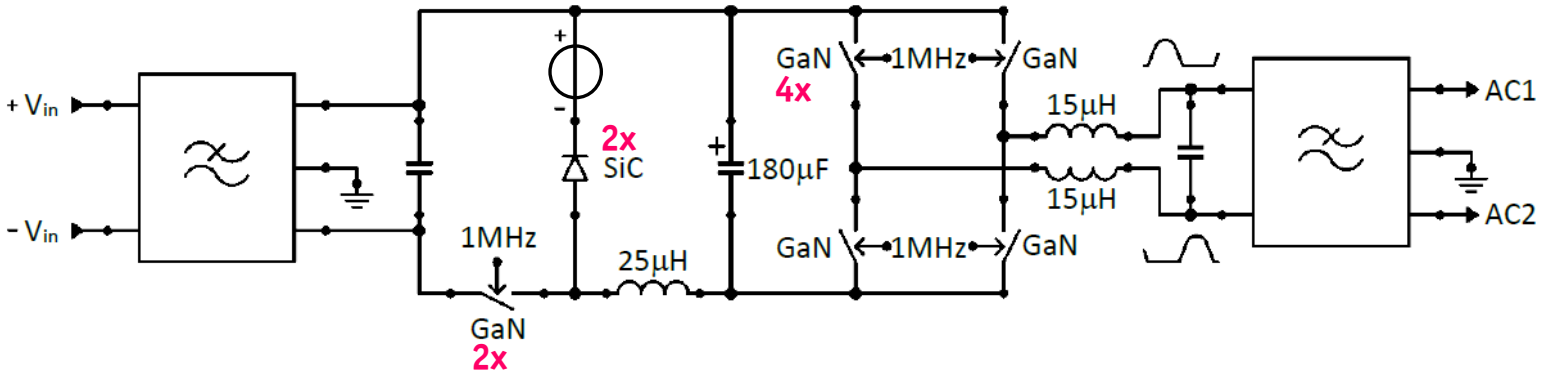
- GaN (11 Teams) / SiC (2 Teams) / Si (2 Teams)

Category I: 300 – 400 W/in³ (1 Team)

- "Over the Edge"
- Hand-Wound Overstressed & Too Small Electrolytic Capacitors (210uF/400V)
- No Voltage Margin of Power Semiconductors (450V GaN, Hard Switching)
- 50V Voltage Source for Semicond. Voltage Stress Reduction
- Low-Frequ. CM AC Output Component

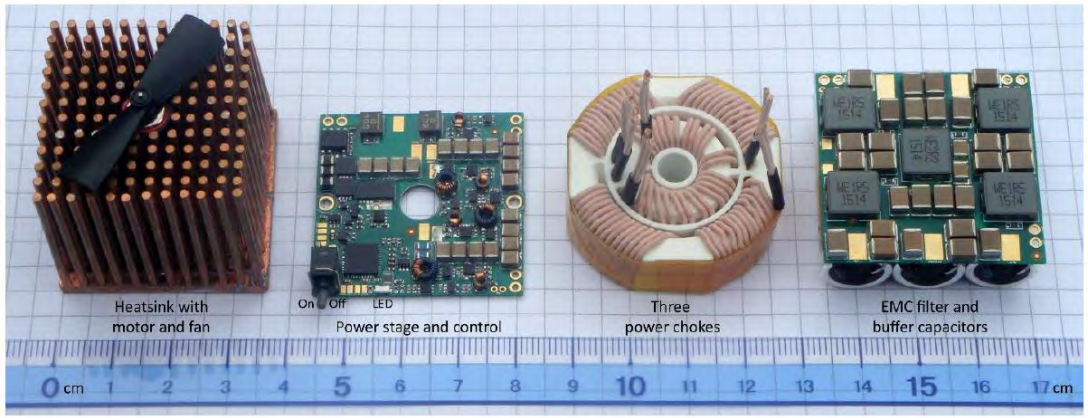


- Alternate Switching of Full-Bridge Legs
- Input Cap. of Full-Bridge Used for Power Pulsation Buffering

- 256 W/in³ (400 W/in³ Claimed) / 1MHz
- Multi-Airgap Toroidal Inductors (3F46, C_p≈1.5pF)
- Bare GaN Dies Directly Attached to Pin-Fin Heatsink
- High Speed Fan (Mini Drone Motor & Propeller)

Category I: 300 – 400 W/in³ (1 Team)

- "Over the Edge"
- Hand-Wound Overstressed Electrolytic Capacitors (210uF (?)/400V)
- No Voltage Margin of Power Semiconductors (450V GaN, Hard Switching)
- 50V Voltage Source for Semicond. Voltage Stress Reduction

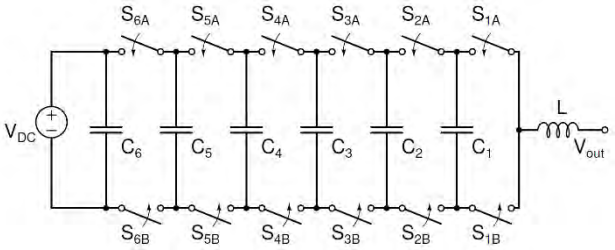


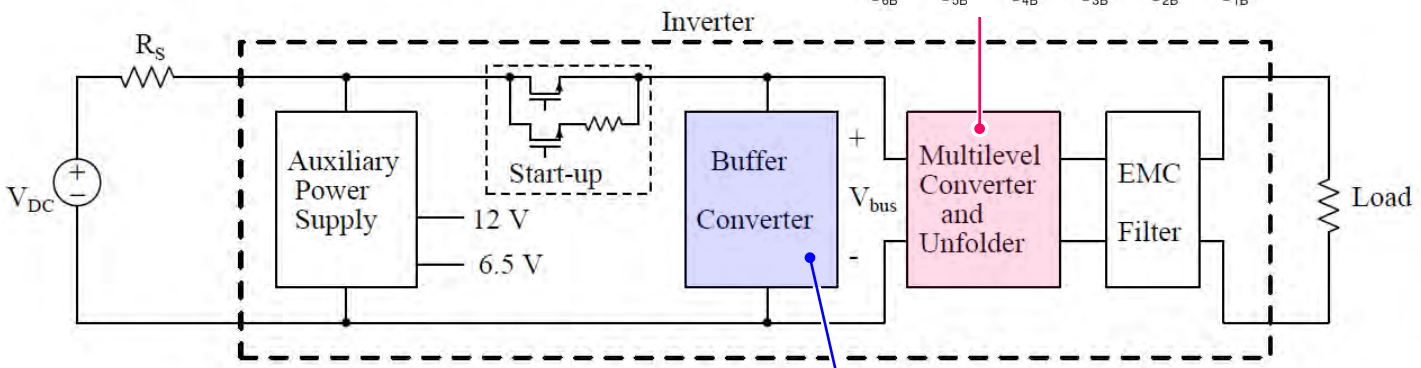
- Alternate Switching of Full-Bridge Legs
- Input Cap. of Full-Bridge Used for Power Pulsation Buffering

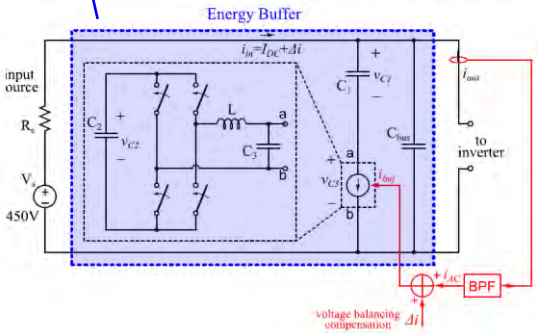
- 256 W/in³ (400 W/in³ Claimed) / 1MHz
- Multi-Airgap Toroidal Inductors (3F46, C_p≈1.5pF)
- Bare Dies Directly Attached to Pin-Fin Heatsink
- High Speed Fan (Mini Drone Motor & Propeller)

Category II: 200 – 300 W/in³ (4 Teams) – Example #1

- "At the Edge"
- High Complexity
- 7-Level Flying Capacitor Converter
- Series-Stacked Active Power Buffer



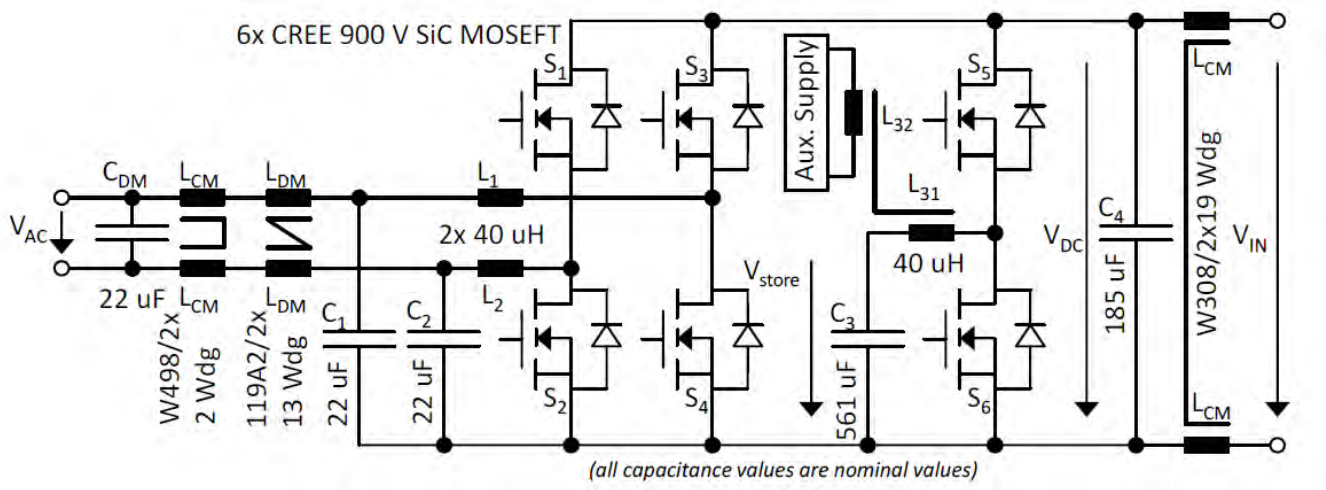




- 216 W/in³
- 100V GaN
- Integrated Switching Cell
- 720kHz Eff. Sw. Frequ. (7 x 120kHz)

Category II: 200 – 300 W/in³ (4 Teams) – Example #2

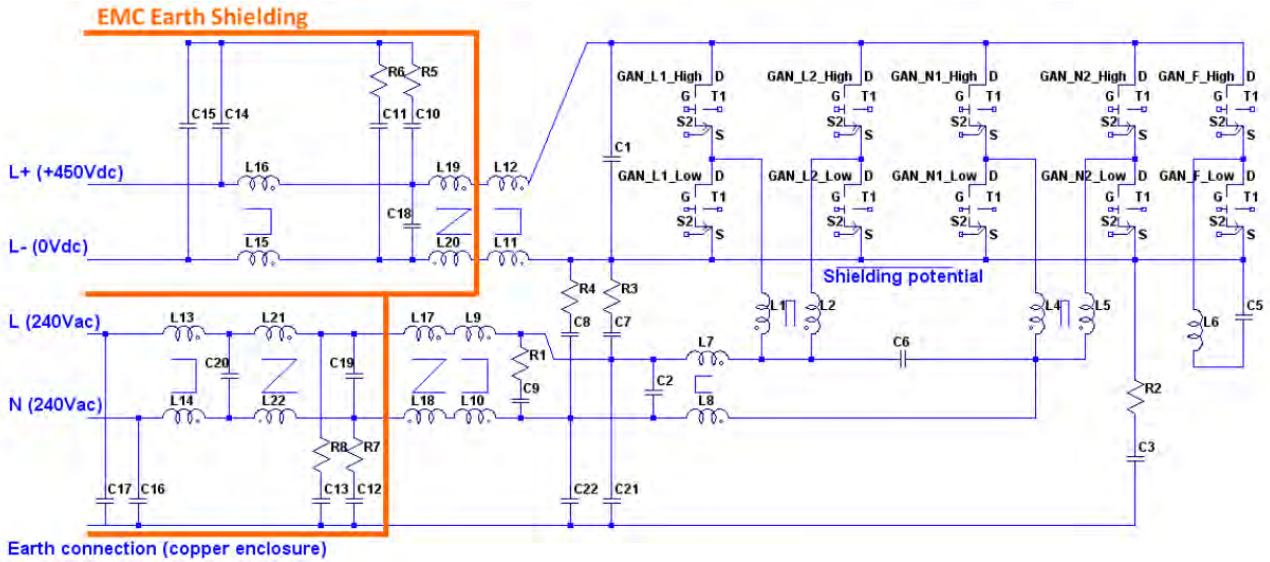
- "At the Edge"
- Very Well Engineered Assembly (e.g. 3D-Printed Heatsink w. Integr. Fans, 1 PCB Board, etc.)
- No Low-Frequ. Common-Mode AC Output Component



- 201W / in³
- Multi-Airgap (8 Gaps) Inductors
- 900V SiC @ 140kHz (PWM, Soft Sw. Around i=0 & Hard Switching)
- Buck-Type Active DC-Side Power Pulsation Filter / Ceramic Capacitors (X6S)

Category III: 100 – 200 W/in³ (8 Teams) – Example

- "Advanced Industrial"
- Sophisticated 3D Sandwich Assembly incl. Cu Honeycomb Heatsink
- Shielded Multi-Stage EMI Filter @ DC Input and AC Output
- No Low-Frequ. Common-Mode AC Output Component



- 143 W/in³
- GaN @ ZVS (35kHz...240kHz)
- 2 x Interleaving for Full-Bridge Legs
- Buck-Type DC-Side Active Power Pulsation Filter (<150µF)

Category III: 100 – 200 W/in³ (8 Teams) – Example

- "Advanced Industrial"
- Sophisticated 3D Sandwich Assembly incl. Cu Honeycomb Heatsink
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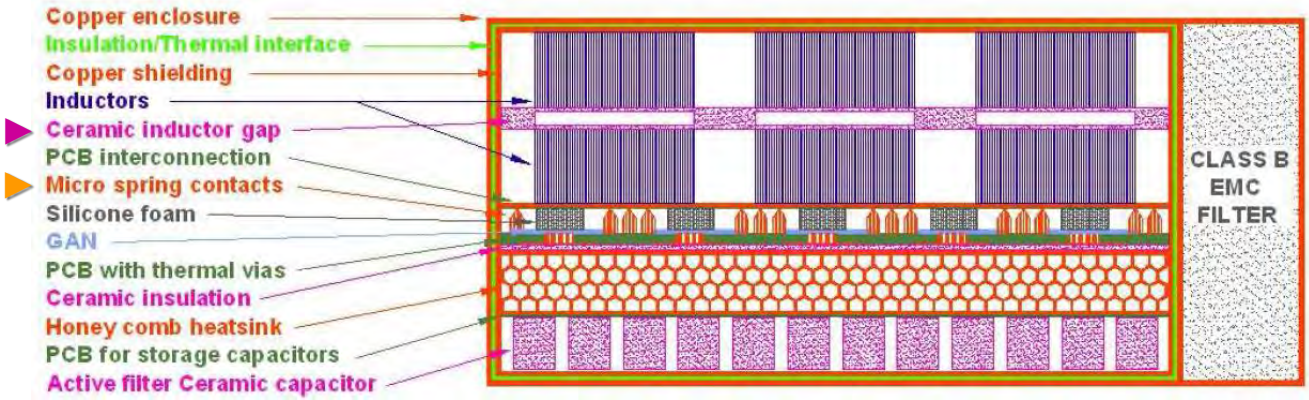
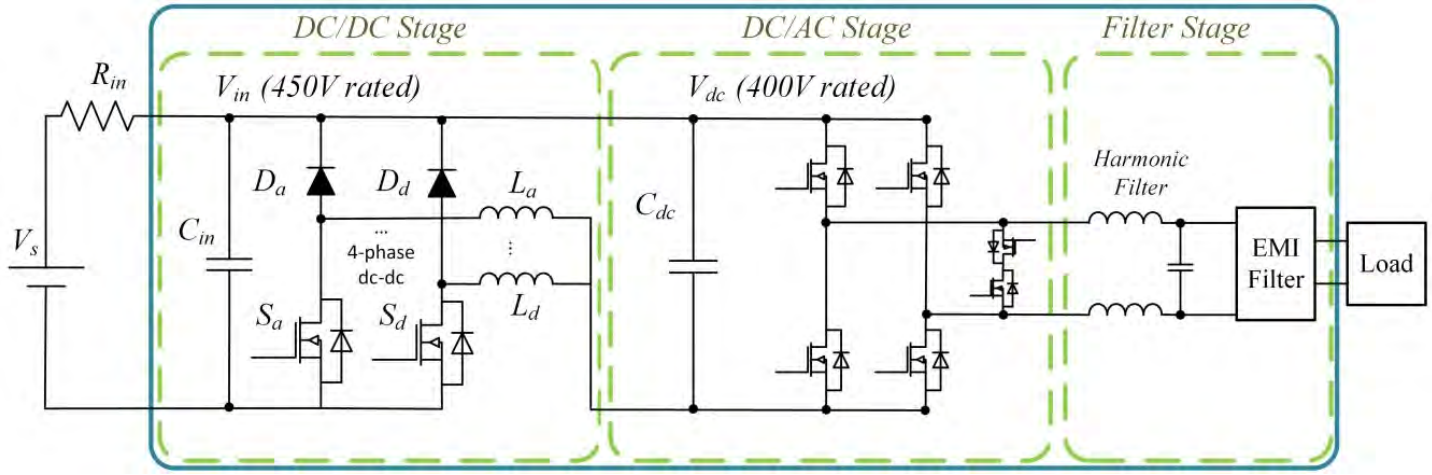


- 143 W/in³
- GaN @ ZVS (35kHz...240kHz)
- 2 x Interleaving for Full-Bridge Legs
- Buck-Type DC-Side Active Power Pulsation Filter (<150µF)

Category IV: 50 – 100 W/in³ (1 Team)

- "Industrial"
- 400V$_{max}$ Full-Bridge Input Voltage
- DC-Link Cap. Used as Power Pulsation Buffer (470uF)
- GaN Transistors / SiC Diodes (400kHz DC/DC, 60kHz DC/AC)
- Multi-Stage EMI Filter @ AC Output and L_{CM} + Feed-Trough C_{CM} @ DC Inp. (Not Shown)



- ≈70 W/ in³
- 98% CEC (Weighted) Efficiency
- 4.4% DC Input Current Ripple
- 54°C Surface Temp. / Cooling with 10 Mirco-Fans

- ***Competition***
- ***Conclusions***
  - ***Key Technologies***
  - ***Power Density Limit***

Google Little Box Challenge Summary

Overall

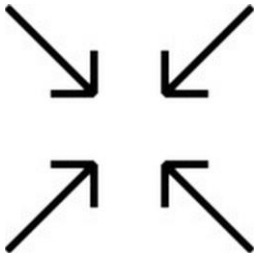
- Engineering "Jewels"
- No (Fundamentally) New Approach / Topology
- Passives & 3D-Packaging are Finally Defining the Power Density
- Careful Heat Management (Adv. Heat Sink, Heat Distrib., 2-Side Integr. Cooling, etc.)
- Careful Mechanical Design (3D-CAD, Single PCB, Avoid Connectors, etc.)
- Clear Power Density / Efficiency Trade-Off

200W/in³ (12kW/dm³) Achievable

- f_s < 150kHz (Constant)
- SiC (Not GaN)
- ZVS (Partial, i.e. Around i=0)
- Full-Bridge Output Stage
- Active Power Pulsation Buffer (Buck-Type, X6S Cap.)
- Conv. EMI Filter Structure
- Multi-Airgap Litz Wire Inductors
- DSP Only (No FPGA)

100+ Teams
3 Members / Team, 1 Year
300 Man-Years
3300 USD / Man-Year

Little Box 2.0

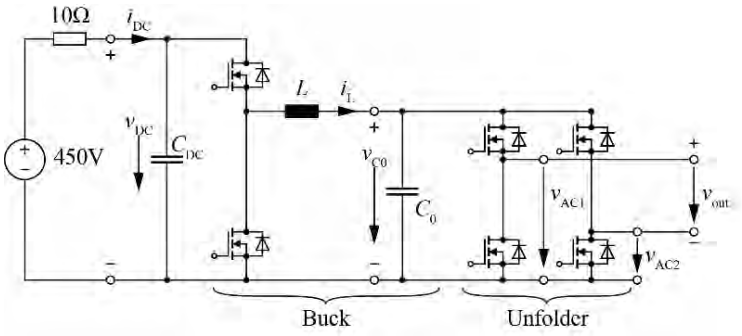


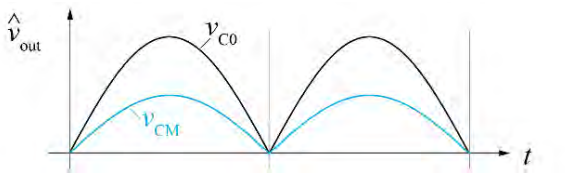
250 W/in³

DC/ | AC | Converter + Unfolder
PWM vs. TCM incl. Interleaving
ηρ-Pareto Limits for Non-Ideal Switches
Final 3D-CAD
Preliminary Exp. Results

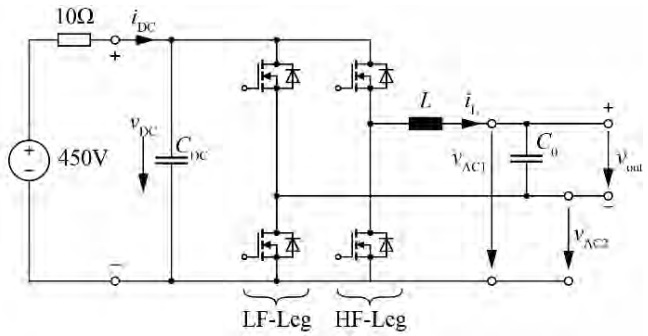
Little Box 2.0 – New Converter Topology (1)

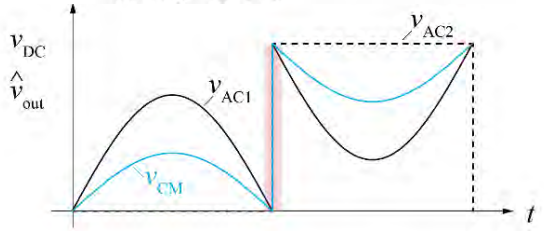
- Alternative Converter Topology → Only Single HF Bridge Leg + 60Hz-Unfolder
- DC/ | AC | - Buck Converter + Full-Bridge Unfolder OR HF Half-Bridge & Half-Bridge Unfolder





- v_{C0} Easy to Generate/Control
- Higher Conduction Losses Due to FB-Unfolder
- Lower CM-Noise (DC & n x 120Hz-Comp.)
- C_{CM}=700nF Allowed for 50mA Gnd Current

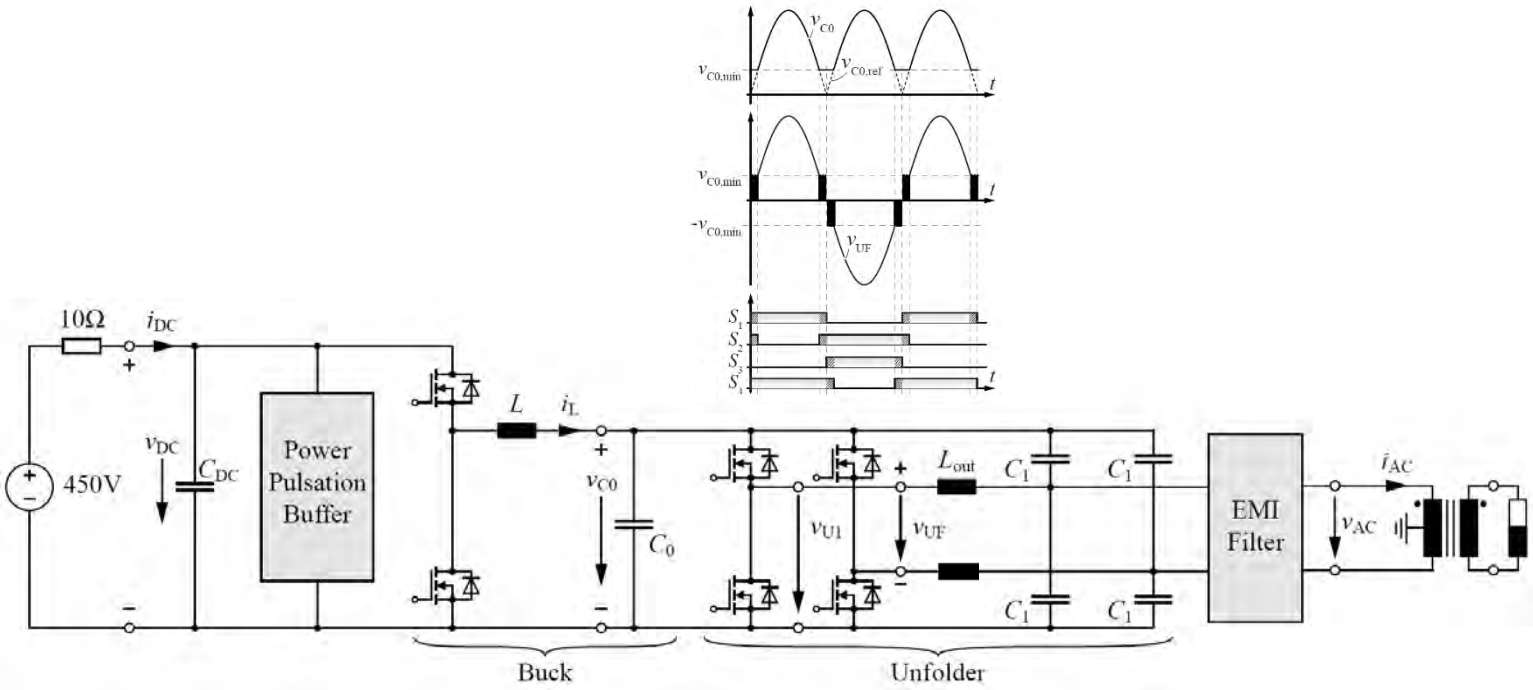




- v_{AC1} More Difficult to Generate/Control
- Lower Conduction Losses
- Higher CM-Noise (DC and n x 120Hz-Comp.)
- C_{CM}=150nF Allowed for 50mA Gnd Current

Little Box 2.0 – New Converter Topology (2)

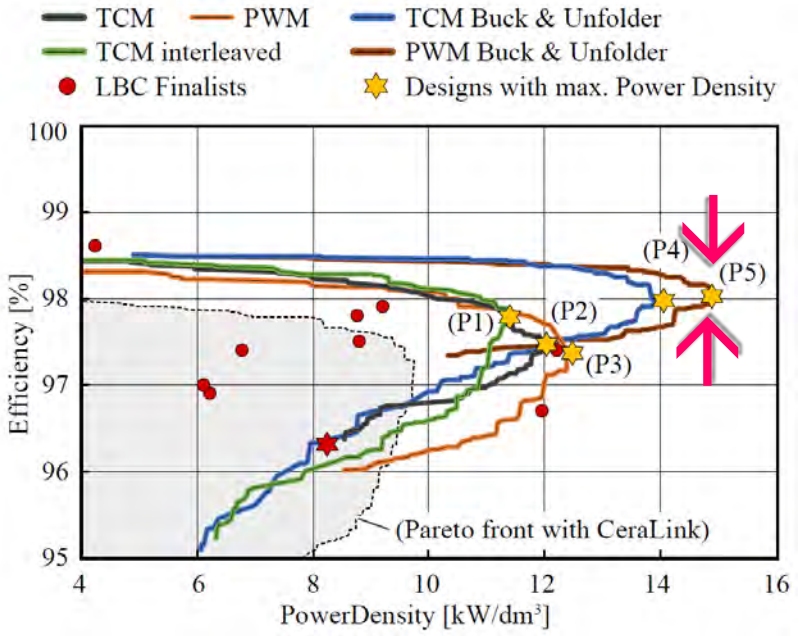
- Alternative Converter Topology - DC/ | AC | - Buck Converter + Unfolder
- 60Hz-Unfolder (Temporary PWM for Ensuring Continuous Current Control)
- TCM or PWM of DC/ | AC | - Buck-Converter



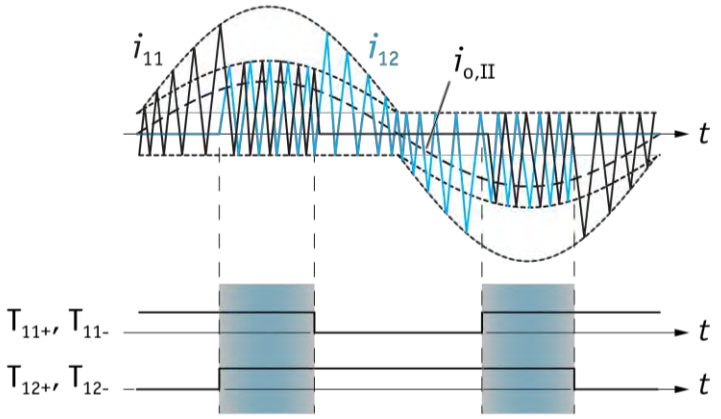
- **Full Optimization** of All Converter Options for **Real Switches** / X6S Power Pulsation Buffer

Little Box 2.0 – Multi-Objective Optimization

- DC/ | AC | - Buck Converter (Single Bridge Leg) + Unfolder & PWM Shows Best Performance
- Full-Bridge Would Employ 2 Switching Bridge Legs - Larger Volume & Losses
- Interleaving Not Advantageous – Lower Heatsink Vol. but Larger Total Vol. of Switches and Inductors

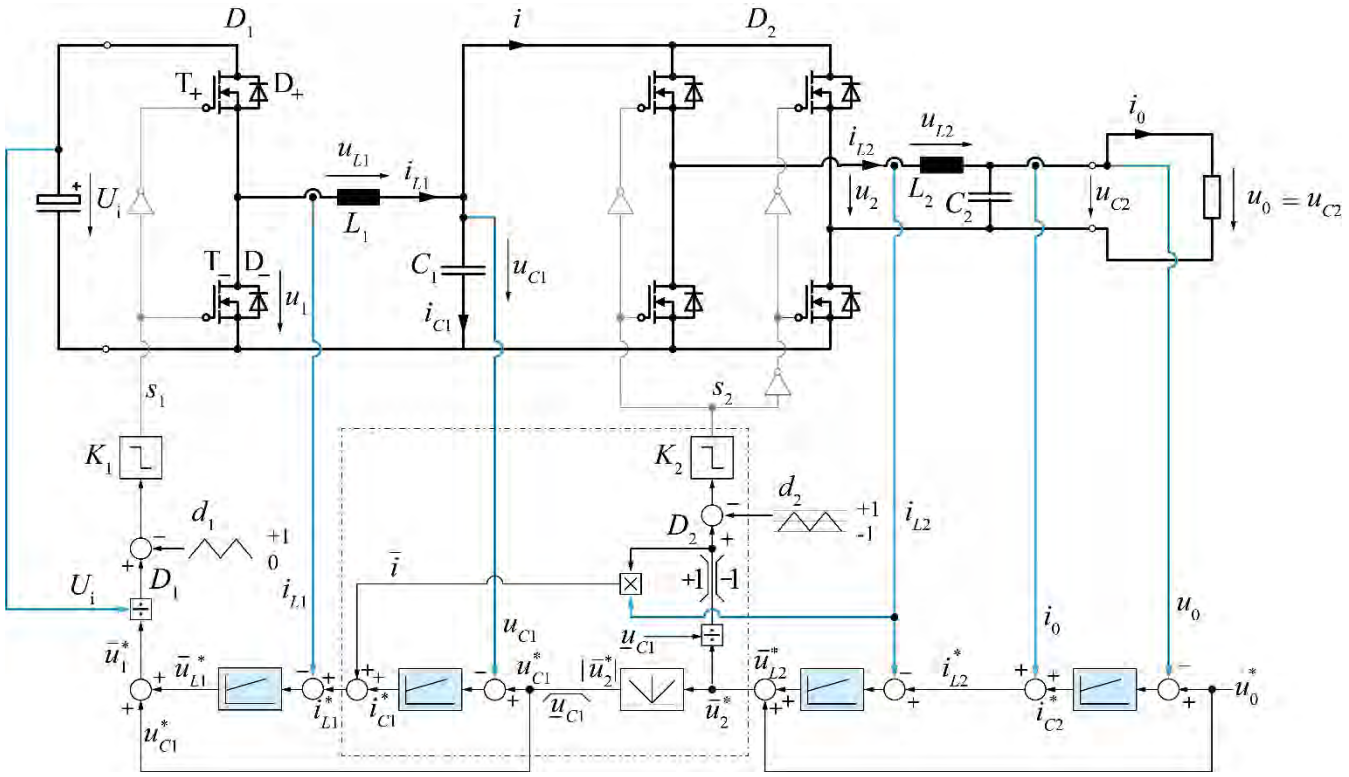


-- 4D-Interleaving Considered for TCM



- ρ= 250W/in³ (15kW/dm³) @ η= 98% Efficiency Achievable for Full Optimization

Little Box 2.0 – Control Structure

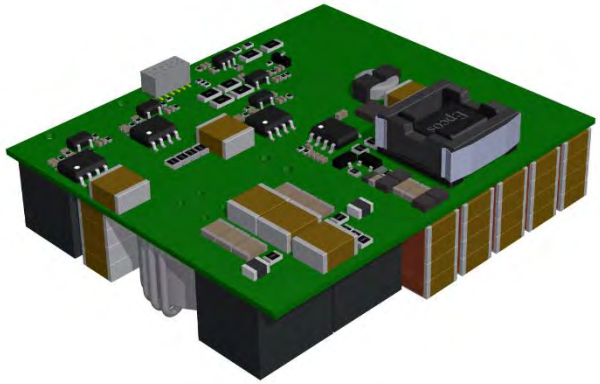


- Each Stage (Buck & Unfolder) Controlled with Cascaded Current and Voltage Loop
- Without Switching of Unfolder Control Like for Conventional Boost PFC Rectifier

3D-CAD Construction of the Final System →

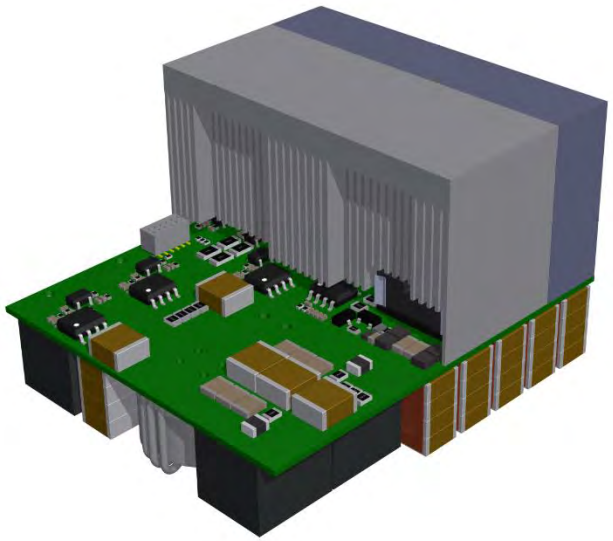
250 W/in³

Little Box 2.0 – Final Mechanical Construction (1)



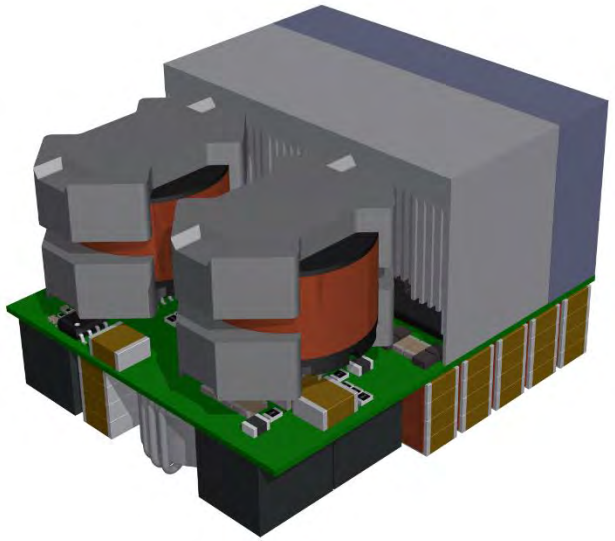
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Final Mechanical Construction (2)



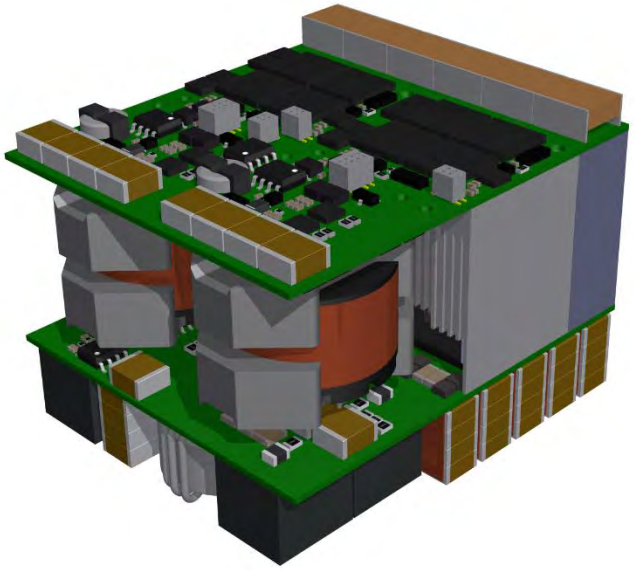
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Final Mechanical Construction (3)



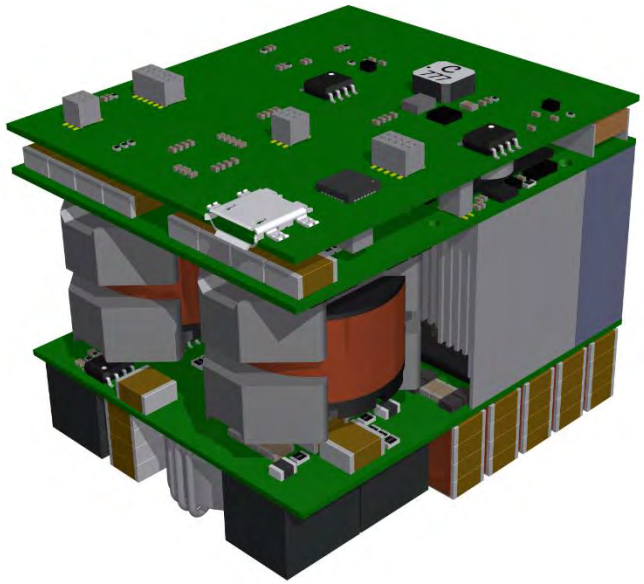
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Final Mechanical Construction (4)



- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

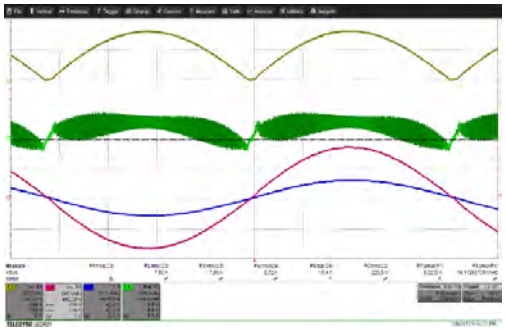
Little Box 2.0 – Final Mechanical Construction (5)



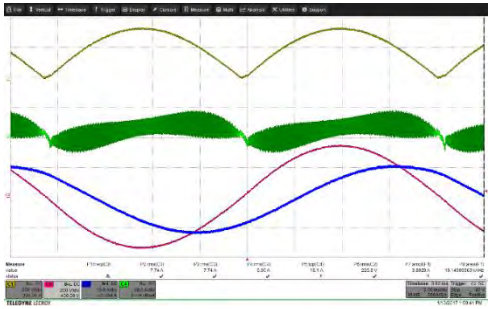
- 60 mm x 50 mm x 45 mm = 135 cm^3 (8.2in^3) → 14.8 kW/dm^3 (243 W/in^3)

Little Box 2.0 – Measured Waveforms

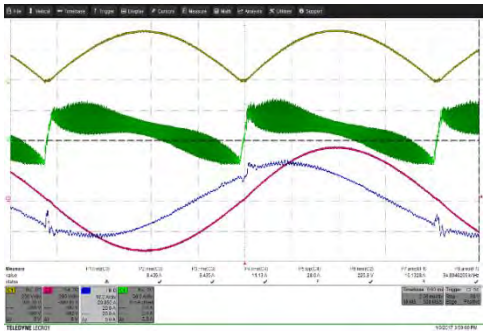
- DC/|AC| Buck-Stage Output Voltage & Inductor Current



■ Resistive Load



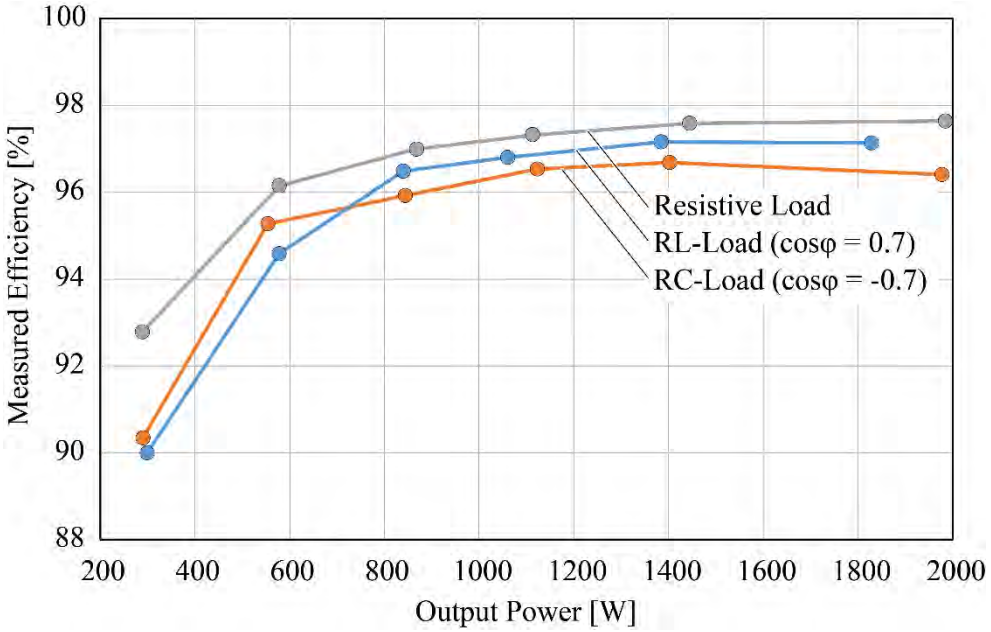
■ Inductive Load



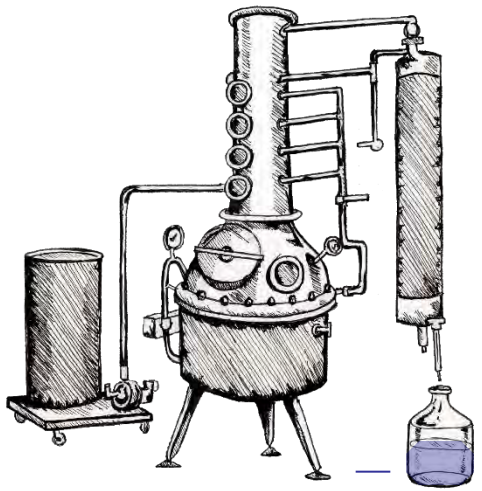
■ Capacitive Load

Little Box 2.0 – Preliminary Efficiency Measurements

- Performance of First DC/|AC|- Buck Converter + Unfolder Prototype
- PWM Operation
- Without Power Pulsation Buffer



- 98% for Res. Load Achievable if Cond. Losses of PCB (Copper Cross Sect.) & Unfolder ($R_{ds,on}$) are Red.



Source: whiskeybehavior.info

Overall Summary

Performance Limits / Future Requirements

- 220...250W/in^3 for Two-Level Bridge Leg + Unfolder
- 250...300W/in^3 for Highly Integrated Multi-Level Approach
- Isol. Distance Requirements Difficult to Fulfill
- Fulfilling Industrial Inp. Overvoltage Requirem. would Signific. Reduce Power Density

- Low Frequency (20kHz...120kHz) SiC vs. HF (200kHz...1.2MHz) GaN
- Multi-Cell Concepts for LV Si (or GaN) vs. Two-Level SiC (or GaN)

- New Integr. Control Circuits and i=0 Detection for Sw. Frequency >1MHz
- Integrated Gate Drivers & Switching Cells
- High Frequency Low Loss Magnetic Materials
- High Bandwidth Low-Volume Current Sensors
- Low Loss Ceramic Capacitors Tolerating Large AC Ripple
- Passives w. Integr. Heat Management and Sensors
- 3D Packaging

- New U-I-Probes Required for Ultra-Compact Conv. R&D
- Specific Systems for Testing → Devices Equipped with Integr. Measurement Functions
- Convergence of Sim. & Measurem. Tools → Next Gen. Oscilloscope
- New Multi-Obj. Multi-Domain Simulation/Optim. Tools

Thank You !