A Multi-Cell Cascaded Power Amplifier

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***Abstract* — A multi-cell cascaded power amplifier with a high output voltage capability, wide load range and high bandwidth is presented in this paper. The cascaded power amplifier is formed by combining a low-voltage linear power amplifier in series with multiple inverter cells. Therefore the cascaded power amplifier combines the advantages of a linear power amplifier with the advantages of a switched mode power amplifier. A high output voltage and bandwidth of 20kHz is achievable using very simple modulation and feedback control design. The dc voltages for the inverter cells and linear power amplifier are provided by an isolated, bidirectional dc-dc resonant converter. The dimensioning and physical structure of a 1.2kW, ±400V cascaded amplifier is given, and shows that a compact, flat system design is possible. Finally, digital simulation results verify the theoretical analysis of the amplifier.**

I. INTRODUCTION

Linear power amplifiers are mainly used to simulate the mains voltage during the testing of electric equipment because of their high fidelity and excellent dynamic behavior. However, these linear power amplifiers have very high losses in their output stages, which make the systems bulky and expensive due to the large heatsinks that are required. In recent years switch-mode power amplifiers, mainly class-D and class-E amplifiers, have replaced linear power amplifiers in various applications where high fidelity is not required. The main reason for their use is that they have a much higher efficiency, which results in the realization of a compact and low cost design. However, switch-mode power amplifiers produce additional EMI and a suitable low pass filter is necessary between amplifier and load. This results in two disadvantages, firstly the system bandwidth is limited by the low pass filter, and secondly the output impedance of the amplifier is only constant at one specific load impedance [1][2].

Various approaches that combine linear and switch-mode power amplifiers have been proposed in order to reduce the system losses and keep the high dynamic performance. One method is to use a switch-mode power supply with an adjustable output voltage instead of constant DC power supply. The supply voltages can then be modulated according to the required instantaneous output voltage so that the voltage drop across the output power transistors can be significantly reduced, and results in a power loss reduction [3]-[6]. However, a low pass filter is still necessary between the power supply and linear power amplifier to reduce the switching noise in the output voltage of the linear power amplifier [6] and this limits the total system's dynamic performance. Furthermore, the linear power amplifier should deliver the full output power and sustain the full output voltage stress. This makes it difficult to design the linear power amplifier for mains simulation applications, especially those that require ±400V for generating a single phase system. In [7] and [8] various switch-mode assisted linear power amplifiers are presented that are basically a class-D converter connected in parallel with a linear power amplifier. The switch-mode amplifier contributes the main load current and the linear amplifier generates the difference current. With this topology a relatively small current

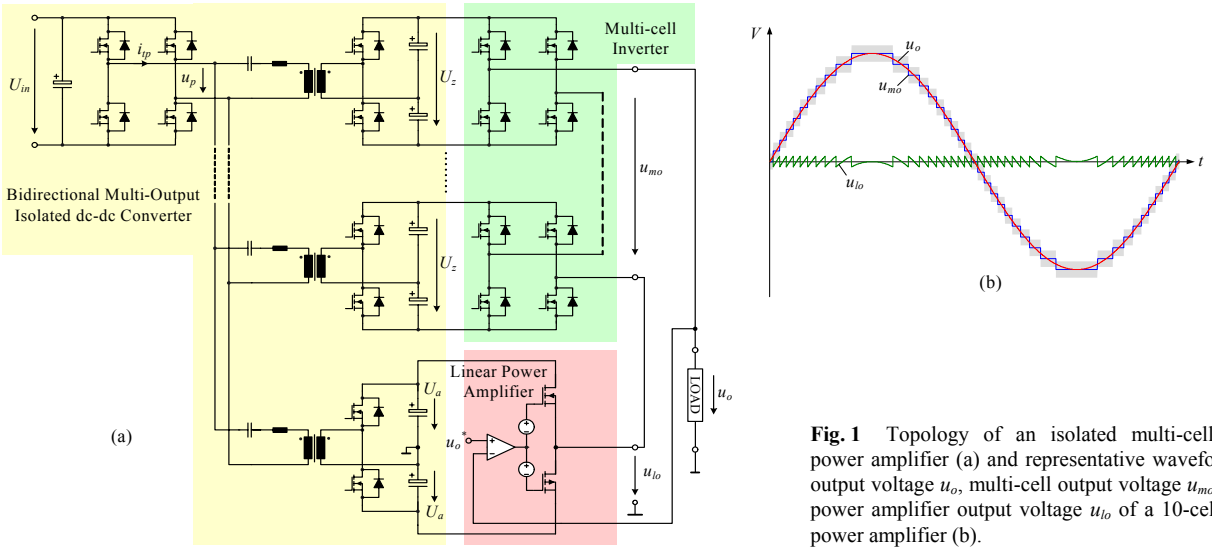

Fig. 1 Topology of an isolated multi-cell cascaded power amplifier (a) and representative waveforms of the output voltage u_o, multi-cell output voltage u_{mo} and linear power amplifier output voltage u_{lo} of a 10-cell cascaded power amplifier (b).

is flowing through the linear power amplifier so that the losses can be significantly reduced and the output impedance is defined by the linear power amplifier stage. However, a high voltage linear power amplifier is still required for a mains simulation application and switching noise can appear in the output voltage due to the increased output impedance of linear power amplifier at high frequencies.

A "Quasi-Linear Amplifier" topology has been proposed in [9] and is similar to the topology presented in this paper. The "Quasi-Linear Amplifier" consists of low switching frequency inverters connected in series with a linear power amplifier to generate gradient coil currents with fast ramp time for magnetic resonance imaging (MRI) systems. However this "Quasi-Linear Amplifier" acts as a current source, while the topology this paper operates as a voltage source that has very low output impedance and includes an isolation stage.

The topology of the multi-cell cascaded power amplifier is shown in **Fig. 1**(a), and consist of: (i) a high slew rate linear power amplifier, (ii) a multi-cell inverter, which is connected in series with the linear power amplifier to generate the output voltage, (iii) a bidirectional, multi-output, isolated dc-dc converter that provides the dc voltages for cell units and linear power amplifier and allows bidirectional energy flow in the case of non-resistive loads. The multi-cell cascaded power amplifier has advantages of a high bandwidth, high efficiency, no output filter, and utilizes a low voltage commercial linear power amplifier. The representative waveforms of a 10-cell cascaded power amplifier are shown in Fig. 1(b), where the multi-cell inverter generates the stepped high voltage u_{mo} according to the reference output voltage u_o* and the switching frequency of the cells is low. Furthermore, the output voltage of the linear power amplifier u_{la} is regulated to compensate for the small voltage difference between u_{mo} and u_o. Therefore, a low voltage linear power amplifier can be employed. The grey area between $u_{mo} - U_a$ and $u_{mo} + U_a$ is the voltage range that can be achieved by the multi-cell cascaded power amplifier.

In this paper the specifications of the multi-cell cascaded power amplifier are:

U_{in} = 400 V
U_o = 80 Vac ~ 280 Vac
P_o = 1150 W @ 280 Vac (resistive load)
Power bandwidth = 20 kHz
Load phase angle = -π/2…+π/2

where U_{in} is the DC input voltage which could be provided by a bi-directional single phase rectifier, U_o is the rms value of the output voltage and spans the universal input voltage range, and P_o is the output power.

II. Operating Principle

A. Modulation and Control

The control scheme of a simplified two-cell cascaded power amplifier is shown in **Fig. 2**. Here two H-bridges are connected in series with the linear power amplifier to form the output voltage. The H-bridge units are controlled in an open loop manner and each H-bridge cell can output three possible voltages, U_z, 0V and $-U_z$, where U_z is the DC supply voltage of the cell units. The linear power amplifier is operated in a closed loop with a high bandwidth, so that it can compensate for the voltage difference between output voltage u_o and multi-cell voltage u_{mo}.

The control signals of the H-bridge units are directly generated by comparing the reference output voltage u_o* and step voltages $-3/2U_z$, $-1/2U_z$, $+1/2U_z$ and $+3/2U_z$. For instance the output voltage of unit 1 is 0V, i.e., T_3 and T_4 are on, when u_o* is between $-1/2U_z$ and $+1/2U_z$. If u_o* increases and reaches $+1/2U_z$, T_3 is turned off and T_1 is turned on, thus unit 1 outputs $+U_z$. Alternatively, unit 1 will produce an output voltage $-U_z$ when u_o* decreases and reaches $-1/2U_z$. The total multi-cell voltage u_{mo} is dependent on the reference output voltage u_o* as is demonstrated in **Fig. 3**. Furthermore this topology can be easily expanded to an n-cell cascaded power amplifier with very low effort.

In Fig. 2, the DC voltage of the linear power amplifier U_a is required to be higher than $1/2U_z$ in order to have sufficient voltage regulation margin. The system just uses a single voltage loop control and the control signal of the linear power amplifier is formed by summing the feed forward voltage u_o* – u_{mo} and the output of the voltage regulator u_{rg}.

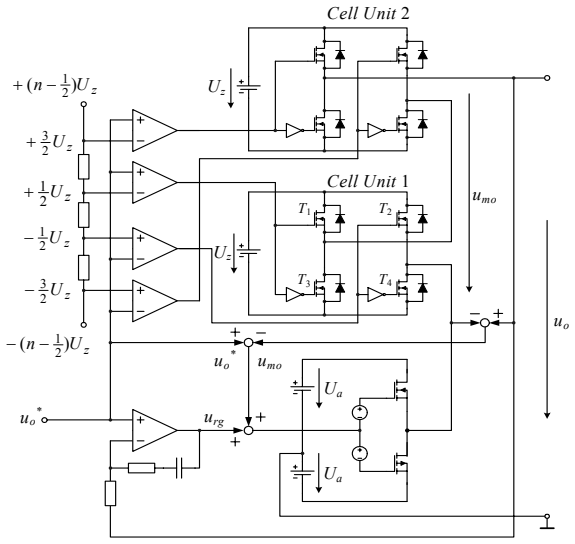

Fig. 2 Control scheme of two-cell cascaded power amplifier.

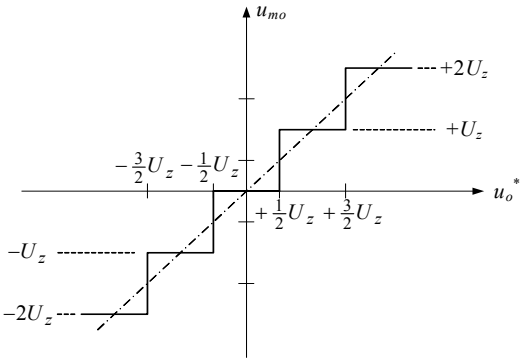

Fig. 3 Multi-cell voltage u_{mo} in dependency on the reference output voltage u_o*.

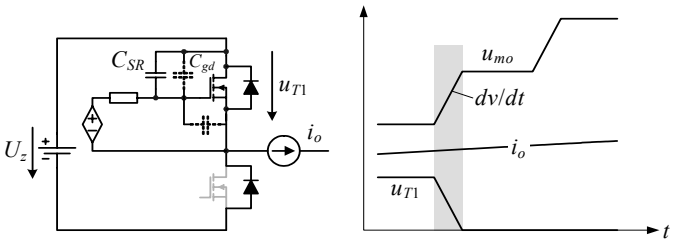

Fig. 4 Scheme of gate driver for controlling the turn-on slew rate of high side MOSFET (a) and the key waveforms of a cell unit when it's output changes from 0V to $+U_z$.

B. Slew Rate Control

It must be pointed out that the output voltage slew rate of the linear power amplifier needs to be high enough to compensate for the voltage slope during the rising or falling steps produced by the multi-cell inverter. Therefore, a slew rate control must be applied to the gate driver of the MOSFETs in the inverter cells.

The scheme of gate driver for controlling the turn-on slew rate of high side MOSFET by using an external capacitor C_{SR} in parallel with the intrinsic capacitor C_{gd} is shown in **Fig. 4**(a). It is shown in Fig. 4(b) that the output voltage of the multi-cell inverter u_{mo} is ramping up with a unique dv/dt which is mainly determined by the capacitance of C_{SR} and gate driver current.

C. Loss Calculation

For the loss calculations it is assumed that the output voltage of the linear power amplifier is

$$u_o = U_{op} \sin \omega t \tag{1}$$

and results in an output (load) current of

$$i_o = \frac{U_{op}}{Z_L} \cdot \sin(\omega t - \varphi) = I_{op} \cdot \sin(\omega t - \varphi)\,, \tag{2}$$

where Z_L is the magnitude of the load impedance and $\varphi \in (-\pi/2, +\pi/2)$ is the phase angle of the load current. The output power of the linear amplifier is then given by

$$P_o = \frac{U_{op}^2}{2Z_L} \cos\varphi\,. \tag{3}$$

In the case where the linear power amplifier is operating in a class-AB mode and the quiescent current is neglected, the losses of the output transistors in the linear power amplifier are calculated as

$$\begin{aligned} P_{lpa} &= 2\frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} (U_a - u_{lo}) \cdot \frac{U_{op}}{Z_L} \cdot \sin(\omega t - \varphi) d\omega t \\ &\approx \frac{2}{\pi} \cdot \frac{U_a \cdot U_{op}}{Z_L} \end{aligned}\,. \tag{4}$$

Since the multi-cell inverter is connected in series with the load, there are always two transistors conducting the load current for each cell unit. The conduction losses of the multi-cell inverter P_{mc_con} are

$$P_{mc\_con} = 2N \cdot R_{on} \cdot \left(\frac{U_{op}}{\sqrt{2}Z_L}\right)^2\,, \tag{5}$$

where N is the number of the cell units, R_{on} is the on resistance of a single transistor in multi-cell inverter.

In one output voltage period, there are two switch-on and two switch-off actions for each operating cell unit. If the diode reverse recovery losses are neglected, then the switching losses of the multi-cell inverter can be approximately derived as

$$P_{mc\_swt} = 4 f_o \sum_{i=0}^{n-1} \frac{1}{2} U_z \cdot \frac{U_{op}}{Z_L} \left| \sin\left(\sin^{-1}\left(\frac{(2i+1)\cdot U_z}{2U_{op}} \right) - \varphi \right) \right| \cdot \frac{U_z}{SR} \tag{6}$$

where SR is the slew rate of the rising or falling slope of the step voltages in the multi-cell inverter, f_o is the frequency of

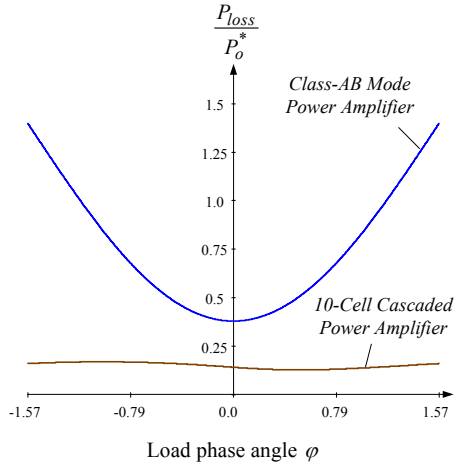

Fig. 5 Comparison of the calculated normalized power losses, P_{loss} / P_o*, of class-AB mode power amplifier and 10-cell cascaded power amplifier in dependency on load phase angle φ. Operating parameters: U_{op} = 400V, Z_L = 70 Ω, f_o = 20kHz, U_z = 40 V, U_a = 30 V, V_{CC} = 430 V. The components are listed in Session IV.

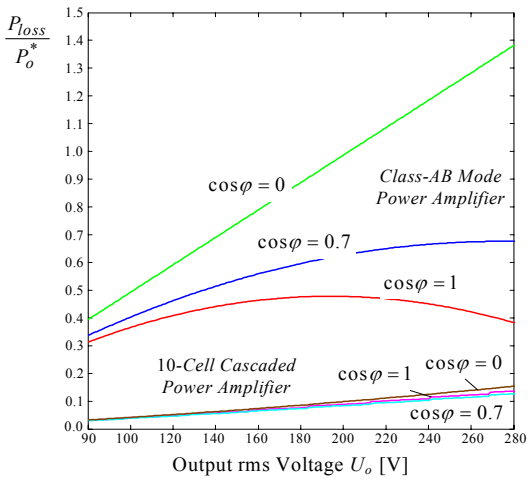

Fig. 6 Comparison of the calculated normalized power losses, P_{loss} / P_o*, of class-AB mode power amplifier and 10-cell cascaded power amplifier in dependency on output rms voltage U_o. Operating parameters: Z_L = 70 Ω, f_o = 20kHz, U_z = 40 V, U_a = 30 V, V_{CC} = 430 V. The components are listed in Session IV.

the output voltage, and n = trunc(U_{op} / U_z + 1/2), is the number of the actual operating cell units according to the amplitude of the output voltage to be generated.

The total losses of the multi-cell cascaded power amplifier is summed to be

$$P_{loss\_mc} = P_{lpa} + P_{mc\_con} + P_{mc\_swt} \cdot \qquad (7)$$

The losses in the output power transistors of a conventional class-AB mode power amplifier are [5]

$$P_{loss\_lin} = \frac{U_{op}}{\pi \cdot Z_L}\left(2V_{cc} - \frac{1}{2}\pi \cdot U_{op} \cdot \cos\varphi\right), \qquad (8)$$

where V_{CC} is the positive DC power supply voltage of a conventional class-AB mode power amplifier.

Fig. 5 compares the calculated normalized power losses (P_{loss} / P_o*) of a class-AB power amplifier and a 10-cell cascaded power, where the normalization base of the power is P_o* = U_{op}^2 / ($2Z_L$). It is shown that the cascaded power amplifier has a significant loss reduction compared to a class-AB power amplifier, furthermore the power losses of the class-AB power amplifier increase dramatically in the case of inductive or/and capacitive loads, while the losses of the cascaded power amplifier are nearly constant.

The dependency of the normalized power losses on the output rms voltage U_o is depicted in **Fig. 6**. For the complete range of the output voltage the losses of the cascaded power amplifier are not higher than half the losses of the class-AB power amplifier.

III. UNCONTROLLED BIDIRECTIONAL DC-DC CONVERTER

A mains simulator requires electric isolation and bi-directional power flow in the case where reactive power is required at the output. Therefore, an isolated bi-directional dc-dc converter has to be used to provide the DC voltages for the H-bridge units and linear power amplifier. In order to reduce the complexity of the circuit, an uncontrolled bi-directional multi-output dc-dc converter is employed (see Fig. 1). A H-bridge is utilized as a common input stage, and an individual transformer, LC tank and half bridge rectifier are used for each

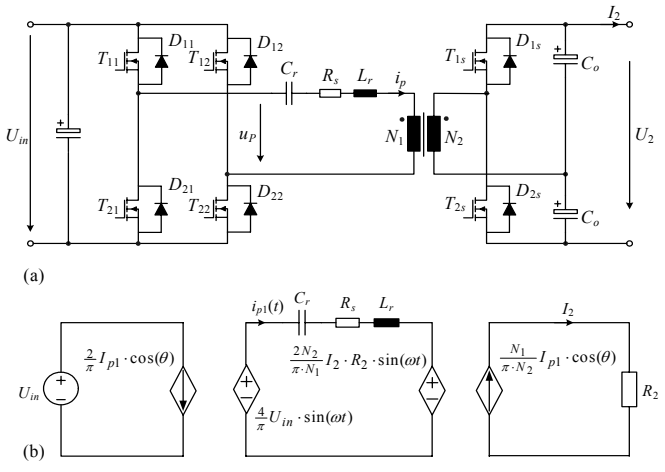

Fig. 7 Topology of the uncontrolled bi-directional dc-dc converter (a) and the according steady-state equivalent circuit (b).

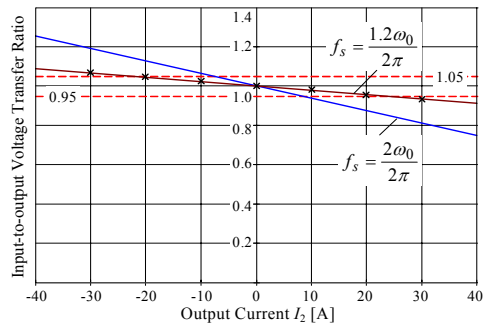

Fig. 8 Nominal input-to-output voltage transfer ratio in dependency on the output current I_2. Circuit parameters are: U_{in} = 400V, N_1:N_2 = 20:1, C_r = 0.25µF, R_s = 6.2Ω, L_r = 10µH, C_o = 1mF. The components are listed in Session IV.

output stage. It is also possible to use a single transformer with multiple secondary windings to further simply the system; however this can cause current oscillations between the different cell units when they are drawn by different power levels. However, this results in higher losses and makes the system in-flexible when trying to extend the number of the cells.

The topology of a single output, bi-directional dc-dc converter is shown in **Fig. 7(a)** [10]-[12], where synchronized 50% fixed duty cycle control is used for both the primary side H-bridge and secondary side half bridge. With this operation the converter can still guarantee an output voltage accuracy of ±1% without closed loop control. A steady-state equivalent circuit is shown in Fig. 7(b) where the capacitor C_r is the series resonant capacitor, L_r is the summation of external resonant inductor and the leakage inductor of the transformer, R_s is the lumped resistance that includes the on-resistance of the semiconductors and series equivalent resistance of resonant inductor and transformer, and θ is phase shift between full bridge output voltage u_p and the primary current i_p. The nominal input-to-output voltage transfer function can be determined as

$$\frac{U_2}{\frac{N_2}{N_1}U_{in}} = 1 - \frac{\pi^2 N_2}{4N_1} \cdot \frac{\left|j \cdot X_L - j \cdot X_C + R_s\right|^2}{R_s \cdot U_{in}} \cdot I_2 , \qquad (9)$$

where X_L = $\omega \cdot L_r$ is the impedance of the series inductor,

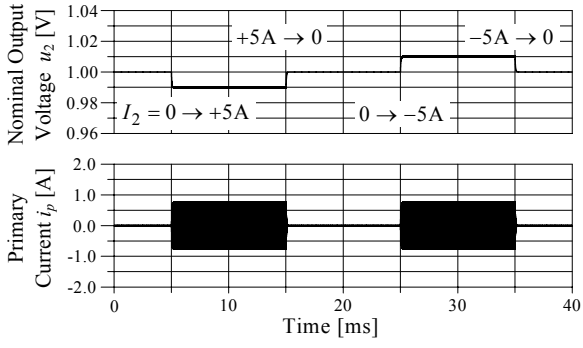

Fig. 9 Simulated load regulation of the dc/dc converter. Circuit parameters are: U_{in} = 400V, N_1:N_2 = 20:1, C_r = 0.25µF, R_s = 6.2Ω, L_r = 10µH, C_o = 1mF, f_s = 120 kHz.

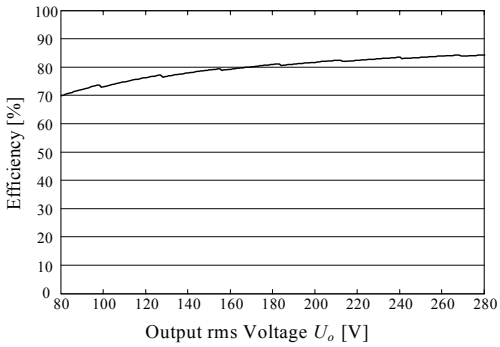

Fig. 10 Calculated efficiency of the 10-cell cascaded power amplifier in dependency on output rms voltage U_o. The operation parameters are: Z_L = 70 Ω, φ = 0°, f_o = 20kHz, U_z = 40 V, U_a = 30 V.

$X_C = 1/(\omega \cdot C_r)$ is the impedance of the resonant capacitor, and only the fundamental frequency is considered.

In **Fig. 8,** the nominal input-to-output voltage transfer ratio, with dependency on the output current I_2, is depicted for the case of different switching frequencies. It is shown that when the switching frequency is $f_s = 1.2\omega_0 / (2\pi)$, the nominal input-to-output voltage transfer ratio is (100 ± 1)% when the output current is changing from –5A to +5A. The points marked with "x" come from simulation and they show a very good match with the calculated results. The load regulation from digital simulation is shown in **Fig. 9**, and it can be seen that no overshoot occurs in case of sudden load change and that the static output voltage error is ±1%.

IV. System Dimensioning

A. Components Selection

The selected components for realizing the 10-cell cascaded power amplifier are listed in Tab. I, where the specifications given in the introduction as used. In the multi-cell inverter, if N-channel MOSFETs are used for all the transistors of the H-bridge, at least one isolation gate driver power supply is needed for the upper transistor in each leg. In order to reduce the realization effort and save the printed circuit board space, a H-bridge that uses P and N channel MOSFETs is selected for the proposed system.

The most important requirement for the linear power amplifier is that it must have a high enough slew rate to compensate for the ramp-up and ramp-down slope of the multi-cell inverter. In this design, the dv/dt of the step voltages from

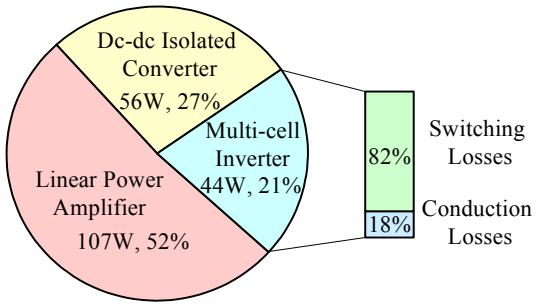

Fig. 11 Calculated power losses distribution of the 10-cell cascaded power amplifier. The operation parameters are: Z_L = 70 Ω, φ = 0°, f_o = 20kHz, U_{op} = 400 V, U_z = 40 V, U_a = 30 V.

the multi-cell inverter is 50V/μs. Therefore a commercial APEX power operational power amplifier MP111FD with a dimension of 41.4 mm x 63.2 mm x 11.5mm is selected. The main specifications of MP111FD are: SR = 130 V/μs, 15A/100VAC, maximum allowed power dissipation 130W@60°C.

B. System efficiency

According to the selected components, the calculated efficiency (dependent on output rms voltage U_o) of a 10-cell cascaded power amplifier is shown in **Fig. 10**. It is shown that the cascaded power amplifier has a good efficiency over a wide output voltage range compared to a conventional linear power amplifier. The drop in efficiency at low output voltages is mainly caused by the reduced number of conducting inverter cells.

The calculated power loss distribution in the cascaded power amplifier system is shown in **Fig. 11** for the same operating point given in Fig. 10. The switching losses of the multi-cell inverter are dominant but are comparable to the conduction losses when the output frequency is reduced to 5kHz.

C. Thermal Balance

Since the H-bridge cells are not simultaneously switched to the load (see Fig. 1), the output power of requirements of each cell is different. The comparison of the output power of the different cells for the 10-cell inverter is illustrated in **Fig. 12,** where it is clearly shown that the earlier the cell unit is switched on the more power it contributes. Since the thermal stresses of the cells and the corresponding dc/dc converter stages are different, a thermal management strategy must be utilized to equalize the thermal stresses among the cell units. A simple management strategy, which does not require any

TABLE I COMPONENTS LIST

Circuit Part	Name	Quantity	Type	Manufacture
Isolated dc-dc Converter	Input Capacitor	2	100 μF / 450V	nichicon
	Primary MosFET	16	SPD07N60S5	Infineon
	Transformer	11	E 25/13/7 N87	Epcos
	Secondary MosFET	22	SUD50N06-12	VISHAY
	Output Electrolytic Capacitor	12	390 μF / 63V	rlc
	Output Chip Capacitor	110	10 μF / 25V	muRata
Multi-cell Inverter	N Channel MosFET	20	SUD50N06-12	VISHAY
	P Channel MosFET	20	SUD50P06-15L	VISHAY
Linear Power Amplifier	Power Operational Amplifier	1	MP111FD	APEX

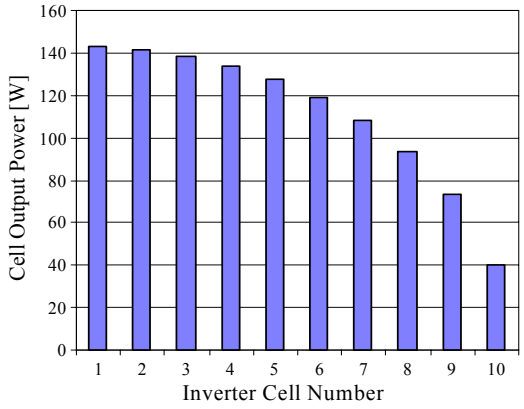

Fig. 12 Comparison of output power from different cell unit of the 10-cell inverter. The operation parameters are: Z_L = 70 Ω, φ = 0°, f_o = 20kHz, U_{op} = 400 V, U_z = 40 V, U_a = 30 V.

additional hardware, can be employed. The main idea is to derive a simplified thermal model of the cell, and then calculate the power losses of each cell unit by using a central digital processor. The sequencing of the cells is made based on the estimated semiconductor junction temperatures, such that the cell units are switched in the inverse sequence to the semiconductor junction temperature during the next output period.

D. Design Structure

According to the loss calculation and components selection, a compact and flat structure system design is graphically shown in **Fig. 13**. The overall dimension of system is 28cm (L) x 20cm (W) x 4cm (H). Since a large number of transistors are employed in this system, all the selected transistors have a small DPAK package and are soldered on the bottom side of the printed circuit board so that they can be attached to the aluminum plate via gap filler. This can significantly reduce the mounting effort for the transistors. The 10 inverter cells with isolation transformers from each dc-dc converter are symmetrically located on both sides. The linear power amplifier, Apex MP111FD, which is not shown in Fig. 13, is mounted under the DSP+PLD board and it is fixed to aluminum plate by screws. The aluminum plate is connected to both heatsinks with a very low thermal resistance.

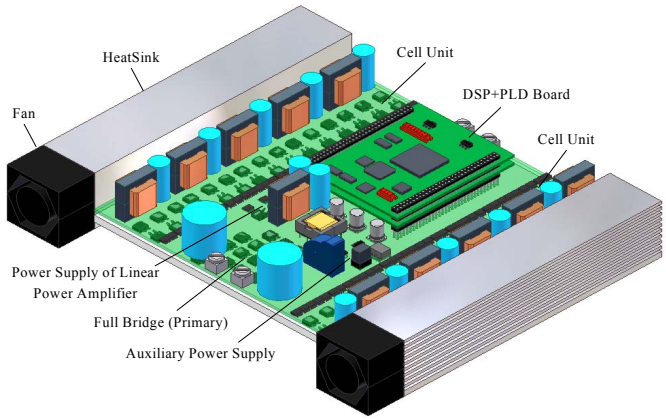

Fig. 13 System structure of a 10-cell cascaded power amplifier. Overall dimension is: 28cm (L) x 20cm (W) x 4cm (H).

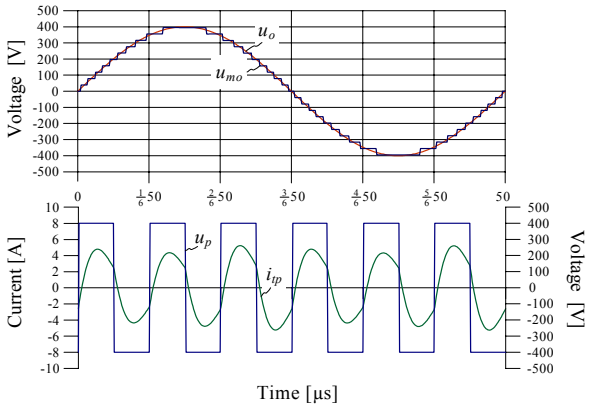

Fig. 14 Simulated time behaviors of the multi-cell inverter voltage u_{mo}, output voltage u_o, the output voltage u_p and output current i_{tp} of the primary full bridge in case of resistive load (see Fig. 1(a)). The operating parameters are: Z_L = 70 Ω, φ = 0°, U_{in} = 400V, f_s = 120 kHz, U_{op} = 400 V, f_o = 20 kHz, U_z = 40 V, U_a = 30 V. The dc-dc converter parameters are same as given in section III.

V. SIMULATION RESULTS

In order verify the theoretical analysis; a numerical simulation assuming ideal transistors and a linear power amplifier is undertaken. **Fig. 14** shows the simulated time behavior of the multi-cell inverter for a 20 kHz output frequency and a resistive load. The output voltage u_o is a pure sinusoidal waveform and u_{mo} demonstrates that the waveform contains 21 voltage steps.

In on output period, there are six switching periods of the dc-dc converter because the switching frequency f_s is selected as 120 kHz. This frequency is 1.2 times the natural frequency of the LC tank of the resonant dc-dc converter, therefore the primary full bridge output current i_{tp} lags the full bridge output voltage u_p to guarantee the zero voltage switch on of the transistors in the primary full bridge. Furthermore, the amplitude of i_{tp} slightly varies due to the output power

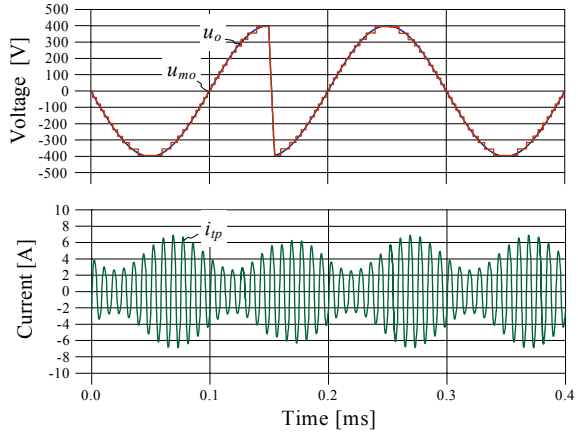

Fig. 15 Simulated transient behaviors of the multi-cell inverter voltage u_{mo}, output voltage u_o, and the primary full bridge output current i_{tp} (see Fig. 1(a)). The operating parameters are: Z_L = 70 Ω, φ = 0°, U_{in} = 400V, f_s = 120 kHz, U_{op} = 400 V, f_o = 5 kHz, U_z = 40 V, U_a = 30 V. The dc-dc converter parameters are same as given in section III.

changing. This amplitude variation also increases when the output frequency is lowered (see Fig. 15).

A good transient behavior is required to perform voltage surge testing of a power supply. The simulated transient behavior of the multi-cell cascaded power amplifier is shown in **Fig. 15** where the output voltage u_o responds from +400V to -400V in 10 µs (SR = 80 V/µs) due a change in the reference voltage. This slew rate is achievable in the proposed hardware by employing a high slew rate linear power amplifier, such as the MP111FD, and an advanced modulation scheme of the multi-cell inverter.

VI. CONCLUSION

An isolated multi-cell cascaded power amplifier with high efficiency, high bandwidth, and wide load displacement range is presented. The cascaded power amplifier is produced by series connecting a linear power amplifier and multi-cell inverter. Loss calculations show a significant efficiency improvement compared to a conventional class-AB power amplifier.

An isolated, bidirectional dc-dc converter with open loop control and ±1% load regulation provides the power for the inverter cells and the linear power amplifier. The dimensioning of the system shows that the cascaded power amplifier can be realized with a very compact and flat design.

Currently, the proposed hardware design is under construction, and the performance will be compared with a commercial mains simulator based on linear power amplifiers.

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