Novel Tracking Power Supply for Linear Power Amplifiers

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***Abstract*—Conventional linear power amplifiers (LPAs) show a high output voltage quality but are characterized by high power losses and/or low power density. Therefore, there is a growing interest in increasing the efficiency of LPAs, e.g., for the realization of high power testing voltage sources. In this paper, a high-frequency isolated boost-type tracking power supply (TPS) system is proposed for the conditioning of the input voltage of an LPA. The output voltage of the TPS is varied according to the voltage to be formed by the LPA so that the voltage drop across the power amplifier output transistors is reduced to low values. This results in a significant increase of the total system efficiency. The operating principle of the proposed system is described. A design method for the output filter using the power supply rejection ratio of the LPA is proposed. This method ensures that the amplifier output voltage has minimal switching frequency components. Furthermore, a control system design method is presented that ensures good performance in the control of the constant inductor current of the switch-mode tracking stage. Finally, the theoretical considerations are verified by measurements on a 1-kW laboratory prototype.**

***Index Terms*—Linear power amplifier (LPA), supply voltage conditioning, testing power supply, tracking power supply (TPS).**

I. Introduction

CONVENTIONAL linear power amplifiers (LPAs), as schematically shown in Fig. 1(a), are widely employed in the industry because of their high output voltage quality and excellent dynamic behavior. As shown in Fig. 1(b), such amplifiers are usually supplied with constant voltages. The time behavior of the current, voltage and instantaneous power of the output power transistor $T_{\rm p1}$ of an LPA is shown in Fig. 1(c) for class-AB operation. High losses occurring in the transistors result in a low efficiency, especially for supplying reactive loads. This constitutes a serious problem in particular for high power systems, which tend to be very bulky and expensive because of the large heat sinks required and the large power consumption. Consequently, there is a growing interest in increasing the efficiency of high power linear amplifier systems.

A very efficient way to avoid the aforementioned drawbacks is conditioning the supply voltage, i.e., varying the supply voltage of the LPA by using a tracking power supply (TPS) that adjusts the supply voltages according to the required linear amplifier output voltage [1]–[5]. With this, the voltage drop across the linear amplifier power transistors could be reduced considerably, resulting in a corresponding reduction of the amplifier power losses. In [1], two buck converters, which have series connected output voltages, are proposed for achieving a variable amplifier supply voltage. In [2] a "class-I" power amplifier, which combines a class-A amplifier and a class-D switching power amplifier, is presented. Multiphase buck converters have been employed as the TPS for RF power amplifiers [3], and a 4.3 MHz buck converter is implemented as a TPS for polar Enhanced Data Rates for GSM Evolution transmitters [4]. Different analog voltage-mode control methods, self-oscillation and fixed-frequency PWM control for a TPS are compared in [5], where the self-oscillation control is claimed to show better dynamic performance. Besides using

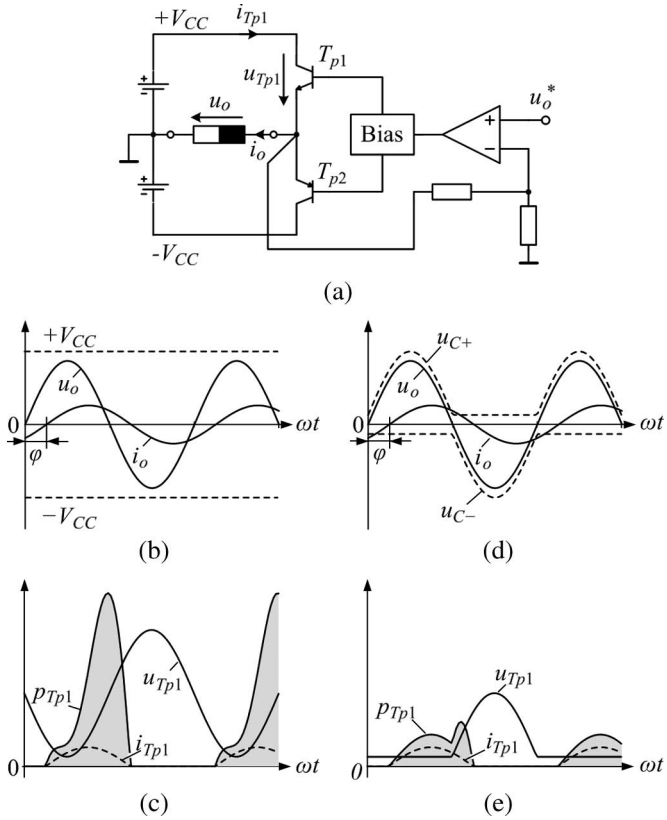

Fig. 1. (a) Conventional LPA; (b) basic waveforms for constant supply voltage; (c) current, voltage and instantaneous power loss of transistor $T_{\rm p1}$ for constant supply voltage; (d) variation of the supply voltage according to the time behavior of the voltage to be generated by the LPA; (e) current, voltage, and instantaneous power loss of transistor $T_{\rm p1}$ for conditioned supply voltage.

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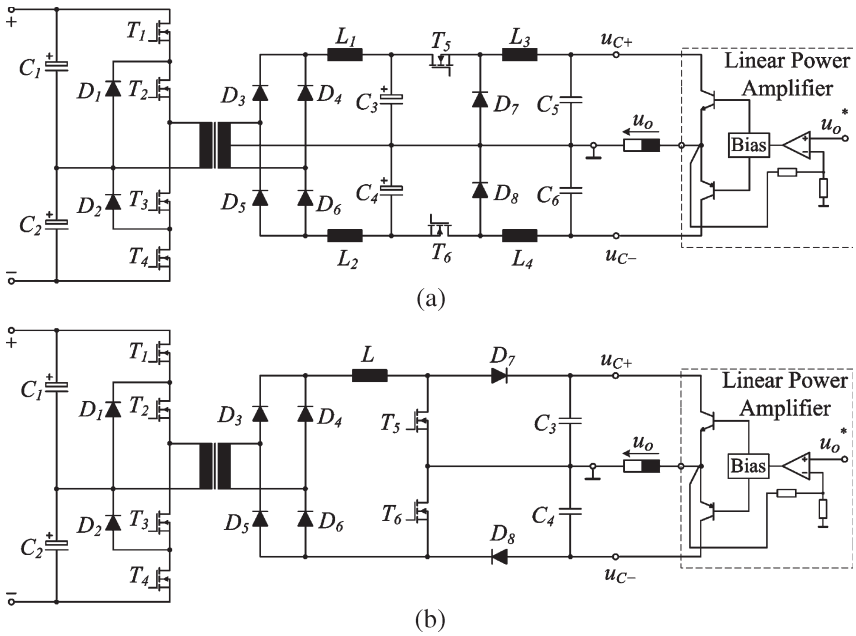

Fig. 2. TPS topologies for a LPA. (a) Conventional realization [1]; (b) Proposed system [10].

TPS for conditioning the supply voltages of LPAs to improve the overall system efficiency, another attractive approach is to connect the outputs in parallel of a class-D amplifier which contributes the main load current and an LPA that generates a low amplitude difference current [6]–[9].

While the TPS topologies in [1]–[5] are based on buck-type converters, in this paper, a new isolated boost-type TPS topology is proposed for controlling the supply voltage of an LPA according to Fig. 1(d) [10], [11]. In principle, a TPS such as that shown in Fig. 2(a) could be employed for realizing a variable supply voltage according to Fig. 1(d). There, the input stage is formed by a three-level dc–dc converter topology [12], which reduces the blocking voltage stress on the primary side power transistors as compared to a full-bridge topology. Therefore, the concept is especially advantageous for high input voltage applications. The system output stage is formed by two buck converters with series-connected outputs. The control of the power amplifier supply voltages could be implemented with underlying current control. However, the system shows a high realization effort since a center-tapped transformer, four inductors, and four capacitors are employed on the secondary side. A further drawback is the limited maximum rate of change in output voltage by the output filter.

In this paper, a novel boost-type topology for realizing a TPS with comparably low effort is proposed and depicted in Fig. 2(b). Only a single inductor and two capacitors are required on the secondary side, although in a practical implementation an additional high frequency output filter might be required. However, the size of this filter is much smaller than the output filter of the buck-type converter [Fig. 2(a)] for the same LPA supply voltage ripple value. In this topology, a control loop is provided for impressing the secondary inductor current. Based on this, a tolerance band control of the supply voltages of the linear amplifier is performed by proper gating of the power transistors T_5 and T_6, and an excellent dynamic behavior of the voltage control can be achieved.

There are different possible applications for this novel approach. In this paper, we aim to use this system as a single-phase testing voltage source for aircraft equipment; however, the considerations will be as far as possible in general terms. The power level is selected as 1 kW, which is used for low power experimental systems. The system operation specifications are defined as

$$U_{\mathrm{o,rms}} = 115\ \mathrm{V} \pm 15\% \approx 98\ \mathrm{V} \sim 132\ \mathrm{V}$$
$$f_{\mathrm{o}} = \mathrm{dc} \sim 1\ \mathrm{kHz}$$
$$I_{\mathrm{op,max}} = 10\ \mathrm{A}$$

where $U_{\mathrm{o,rms}}$ is the RMS value of the output voltage, f_{o} is the output frequency and $I_{\mathrm{op,max}}$ is the maximum output peak current. The output voltage range covers the abnormal single-phase voltage range, 97∼134 V, of the 115 Vrms ac mains in aircraft according to DO-160D Change No. 2. The specified output frequency is selected with respect to the widest abnormal mains frequency range, 360∼800 Hz, which is defined for testing A(WF) catalog equipment as well as referring to DO-160D Change No. 2.

In the following analysis, the LPA transistor losses are first compared in case of different input voltage conditions in Section II. Then the key issues of the TPS design will be discussed in Section III. In Section IV, the output filter will be designed to limit the switching noise at the output voltage. Furthermore, a current loop design with feedforward control based on the derived small signal model of the TPS will be treated in Section V. Finally, Section VI shows the experimental results.

II. LPA Transistor Losses for Different Input Voltage Conditions

For the following calculations, we assume the output voltage of the LPA as:

$$u_{\rm o} = U_{\rm op} \sin \omega t. \tag{1}$$

Assuming a linear load, the resulting output (load) current is

$$i_{\rm o} = \frac{U_{\rm op}}{Z_{\rm L}} \sin(\omega t - \varphi) = I_{\rm op} \sin(\omega t - \varphi) \tag{2}$$

where $Z_{\rm L}$ is the magnitude of the load impedance and $\varphi \in (-\pi, +\pi)$ is the phase angle of the load current. The output power of the linear amplifier then is

$$P_{\rm o} = \frac{U_{\rm op}^2}{2Z_{\rm L}} \cos \varphi. \tag{3}$$

For an LPA operating in class-AB mode, the low quiescent current can be neglected for the losses calculation. Therefore, the losses resulting for transistor $T_{\rm p1}$ [see Fig. 1(c)] are

$$P_{T_{\rm p1},\rm lin} = \frac{1}{2\pi} \int_{\varphi}^{\varphi+\pi} (V_{\rm CC} - U_{\rm op} \sin \omega t) \cdot \frac{U_{\rm op}}{Z_{\rm L}} \sin(\omega t - \varphi) d\omega t$$

$$= \frac{U_{\rm op}}{2\pi \cdot Z_{\rm L}} \left(2V_{\rm CC} - \frac{1}{2} \pi \cdot U_{\rm op} \cos \varphi \right). \tag{4}$$

In case the class-AB power amplifier is supplied by the proposed converter, we have for the power losses of transistor $T_{\rm p1}$ [see Fig. 1(e)] and $\varphi \in (0, +\pi)$

$$P_{T_{\rm p1},\rm pro} = \frac{1}{2\pi} \left[\int_{\varphi}^{\pi} V_{\rm a} \cdot \frac{U_{\rm op}}{Z_{\rm L}} \cdot \sin(\omega t - \varphi) d\omega t + \int_{\pi}^{\pi+\varphi} (V_{\rm a} - U_{\rm op} \sin \omega t) \cdot \frac{U_{\rm op}}{Z_{\rm L}} \cdot \sin(\omega t - \varphi) d\omega t \right]$$

$$= \frac{U_{\rm op}}{2\pi \cdot Z_{\rm L}} \left[2V_{\rm a} + \frac{1}{2} U_{\rm op} (\sin \varphi - \varphi \cos \varphi) \right] \tag{5}$$

where $V_{\rm a} = V_{\rm CC} - U_{\rm op}$ denotes the voltage remaining across a conducting power transistor. For $\varphi \in (-\pi, 0)$, the power losses in transistor $T_{\rm p1}$ are

$$P_{T_{\rm p1},\rm pro} = \frac{1}{2\pi} \left[\int_{\varphi}^{0} (V_{\rm a} - U_{\rm op} \sin \omega t) \cdot \frac{U_{\rm op}}{Z_{\rm L}} \cdot \sin(\omega t - \varphi) d\omega t + \int_{0}^{\pi+\varphi} V_{\rm a} \cdot \frac{U_{\rm op}}{Z_{\rm L}} \cdot \sin(\omega t - \varphi) d\omega t \right]$$

$$= \frac{U_{\rm op}}{2\pi \cdot Z_{\rm L}} \left[2V_{\rm a} + \frac{1}{2} U_{\rm op} (\varphi \cos \varphi - \sin \varphi) \right]. \tag{6}$$

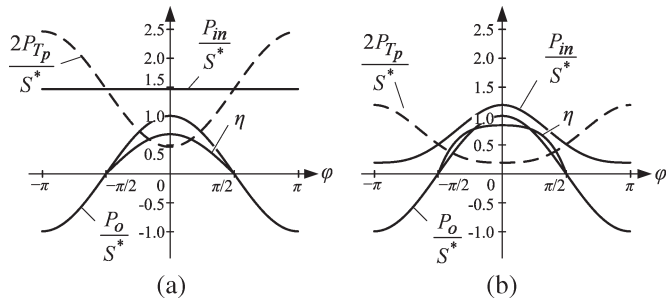

Fig. 3. Dependency of the normalized transistor losses [normalization with reference to S^* as defined in (8)], input power, output power, and efficiency of a linear class-AB power amplifier on the load phase angle (a) for a constant supply voltage and (b) for the proposed supply voltage conditioning.

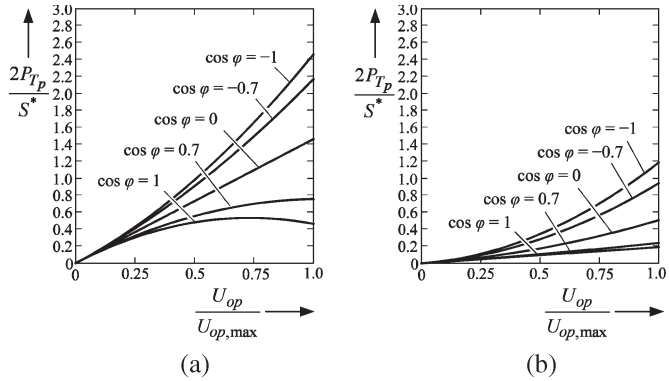

Fig. 4. Dependence of the normalized transistor power losses on the normalized amplifier output voltage amplitude (a) for constant supply voltage and (b) for supply voltage conditioning according to Fig. 1(d).

By combining (5) and (6) the power losses of transistor $T_{\rm p1}$ for $\varphi \in (-\pi, +\pi)$ result in

$$P_{T_{\rm p1},\rm pro} = \frac{U_{\rm op}}{2\pi \cdot Z_{\rm L}} \left(2V_{\rm a} + \frac{1}{2} U_{\rm op} \left| \sin \varphi - \varphi \cos \varphi \right| \right). \tag{7}$$

In Fig. 3, the normalized transistor losses, the input power $P_{\rm in} = P_{\rm o} + 2P_{\rm Tp}$, the output power $P_{\rm o}$ and the efficiency η of the linear class-AB power amplifier are given for different load conditions for the assumed operating parameters of $V_{\rm CC} = 230$ V, $V_{\rm a} = 30$ V, $U_{\rm op} = 200$ V, and $Z_{\rm L} = 20\ \Omega$. Here, the normalization basis for the power is defined as

$$S^* = \frac{U_{\rm op}^2}{2 \cdot Z_{\rm L}} \tag{8}$$

and $P_{\rm Tp}$ denotes the losses of a power transistor. To employ the proposed concept, the transistor power losses can be significantly reduced in comparison to a constant supply voltage and this results in a significant improvement of the amplifier efficiency [in Fig. 3, the efficiency is only shown for passive loads, i.e., for phase angle values $\varphi \in (-\pi/2, +\pi/2)$].

In Fig. 4, the normalized transistor power losses are depicted depending on the normalized output voltage amplitude, where the normalization basis is the maximum output voltage amplitude $U_{\rm op,max}$; and the operating parameters are $V_{\rm CC} = 230$ V, $V_{\rm a} = 30$ V, $U_{\rm op,max} = 200$ V, and $Z_{\rm L} = 20\ \Omega$. Evidently, the losses are reduced significantly due to the conditioning of the supply voltage.

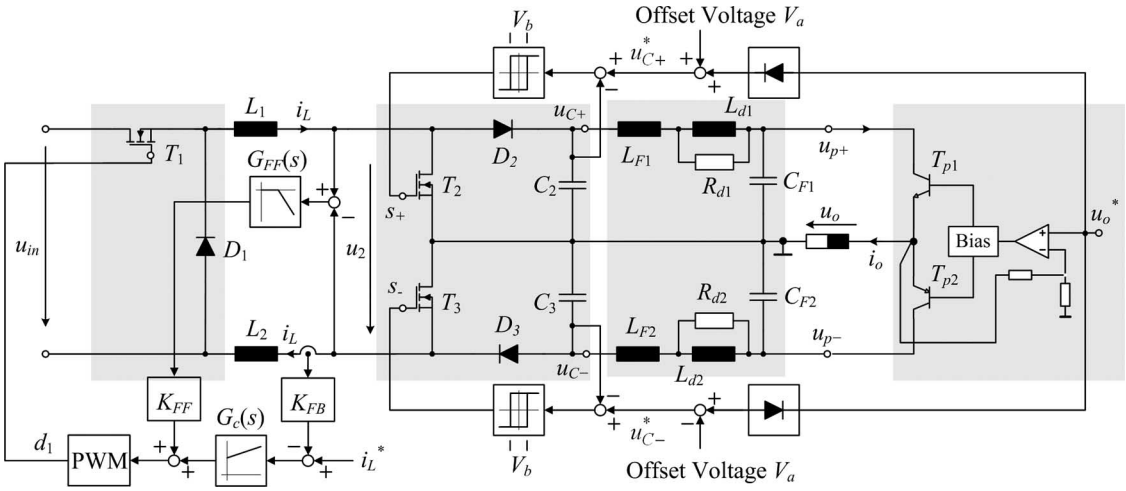

Fig. 5. Structure of the proposed TPS using a buck converter as the input stage instead of a three-level isolated dc–dc converter. $V_{\rm a}$ is the offset voltage; $V_{\rm b}$ is the width of the tolerance band.

III. TPS Design

First, the operating principle of the TPS will be described in this section, then the switching frequency of the boost stage MOSFET is analyzed and the dimensioning of the output capacitors is explained. Furthermore, the equations for calculating the current stresses on the components are given and the calculated results are verified by numerical simulation, and finally the components are selected according to the defined specifications.

A. Basic Operating Principle

To simplify the analysis of the system and focus on the main aspects, the three-level isolated dc–dc converter is replaced by a buck converter in the following analysis. The control structure of the proposed TPS is shown in Fig. 5. The proposed converter consists of: 1) a buck stage, in which the main inductor is split into two inductors L_1 and L_2 in order to have the same common-mode noise rejection in both paths. The inductor current $i_{\rm L}$ is controlled to a constant value and the constant-frequency, average current-mode control and feedforward of the local average value of the voltage across the power transistors T_2 and T_3 are employed; 2) a boost stage where a tolerance band control is performed to achieve high dynamics with a low realization effort; and 3) an output filter that reduces the supply voltage switching ripple to guarantee a good output voltage THD plus noise (THD+N) figure of the LPA [13].

The conduction states of the output stage are shown in Fig. 6 for positive load current. There, the buck-type input stage is represented by a current source $i_{\rm L}$ and the output filter is neglected. To realize the control of the supply voltages of the LPA according to Fig. 5, T_3 remains in the ON-state in case $u_{\rm C-}$ is higher than the reference value $u^*_{\rm C-} - (1/2)V_{\rm b}$, where $V_{\rm b}$ is the width of the tolerance band. When the positive supply voltage $u_{\rm C+}$ due to the current consumption of the linear amplifier [see Fig. 6(a)] reaches the lower boundary of the tolerance band $u^*_{\rm C+} - (1/2)V_{\rm b}$, T_2 is turned off [see Fig. 6(b)] and the current $i_{\rm L}$ commutates into D_2 and recharges the output capacitor C_2. If $u_{\rm C+}$ reaches the upper boundary of the tolerance band $u^*_{\rm C+} + (1/2)V_{\rm b}$, T_2 is turned on, accordingly diode D_2 blocks [see Fig. 6(a)], and $i_{\rm L}$ free-wheels through T_2 and T_3.

B. Switching Frequency Analysis

The switching frequency range of the boost switches is now analyzed and this information is used for calculating the switching losses and designing the output filter. Since the switching frequency is much higher than the output current frequency, a balanced charge flow of the output capacitors is assumed over a switching period. The charge flow balance of the capacitor C_2 is given by

$$(I_{\rm L} - I_{\rm op} \cdot \sin(\omega t - \varphi)) \cdot T_{\rm on} = I_{\rm op} \cdot \sin(\omega t - \varphi) \cdot T_{\rm off} \quad (9)$$

where $\omega t \in (\varphi, \pi + \varphi)$. The discharge time can be calculated as

$$T_{\rm off} = C \cdot \frac{V_{\rm b}}{I_{\rm op} \cdot \sin(\omega t - \varphi)} \quad (10)$$

where $C = C_2 = C_3$. Therefore, the local switching frequency $f_{\rm s}$ can be derived as

$$f_{\rm s} = \frac{1}{T_{\rm on} + T_{\rm off}} = \frac{\sin \omega t \cdot (\alpha - \sin \omega t)}{\alpha \cdot C \cdot V_{\rm b}} \cdot I_{\rm op} \quad (11)$$

where α denotes the current ratio $\alpha = I_{\rm L}/I_{\rm op}$. The maximum switching frequency therefore is given by

$$f_{\rm s,max} = \frac{\alpha \cdot I_{\rm op}}{4C \cdot V_{\rm b}} = \frac{I_{\rm L}}{4C \cdot V_{\rm b}} \quad (12)$$

and the average switching frequency is

$$f_{\rm s,avg} = \frac{1}{2\pi} \int_0^{\pi} f_{\rm s} d\omega t = \frac{I_{\rm op}}{2\alpha \cdot C \cdot V_{\rm b}} \left(\frac{2\alpha}{\pi} - \frac{1}{2} \right). \quad (13)$$

As shown in (12) and (13), the switching frequency of the boost stage is inversely proportional to the width of the

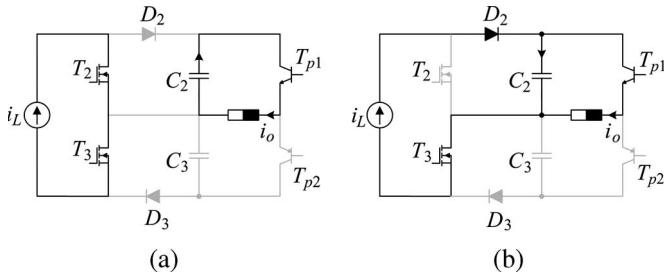

Fig. 6. Simplified equivalent circuit of the proposed converter and conduction states of the output stage for positive load current.

hysteresis band $V_{\rm b}$. To select the width of the hysteresis band, we need a compromise between the boost stage switching frequency and the output switching noise. For example, if we reduce $V_{\rm b}$, the switching frequency of the boost stage will be increased, which results in higher switching losses. On the other hand, the switching noise contained in the output voltage of the converter is lowered, which decreases the filtering requirement of the output filter.

C. Dimensioning of the Output Capacitors C_2 and C_3

The capacitance C of the output capacitors C_2 and C_3 has a significant influence on the required current source value $I_{\rm L}$ and the switching frequency of the boost stage. Decreasing the capacitance of C_2 and C_3 can bring the benefit of lower required value of $I_{\rm L}$ that will reduce the current stresses of the power components [see (15)], but increases the switching frequency of the boost stage as given in (12) and (13). A practical selection of the output capacitor value is to limit the maximum capacitor current value to 20% of the peak current of the LPA. The capacitor value then can be calculated as

$$C \approx \frac{0.2 \cdot I_{\rm op}}{2\pi \cdot f_{\rm o} \cdot U_{\rm op}} \tag{14}$$

where $f_{\rm o}$ is the output frequency.

D. Constant Inductor Current $I_{\rm L}$

To ensure the good performance of the supply voltages conditioning, the constant inductor current $I_{\rm L}$ must always be higher than the summed current $I_{\rm sum}$ needed by the LPA and output capacitors, which is

$$I_{\rm sum} = I_{\rm op}\sin(\omega t - \varphi) + \omega \cdot C \cdot U_{\rm op}\cos(\omega t). \tag{15}$$

The required maximum value $I_{\rm sum,max}$ of the inductor current (which occurs for capacitive loading of the amplifier) can be calculated as

$$I_{\rm sum,max} = I_{\rm op} + \omega \cdot C \cdot U_{\rm op}. \tag{16}$$

With respect to the switching ripples in the inductor current and providing a modulation margin for T_2 and T_3, the constant inductor current is set to

$$I_{\rm L}^{*} = 1.4 \cdot I_{\rm sum,max}. \tag{17}$$

TABLE I
COMPARISON OF THE CALCULATED AND SIMULATED COMPONENT STRESSES

		Current [A]	
		Calculated	Simulated
T_1	avg	5.46	5.48
	rms	9.05	9.05
D_1	avg	9.54	9.52
	rms	11.96	11.99
$T_{2,3}$	avg	11.82	11.82
	rms	13.31	13.34
$D_{2,3}$	avg	3.18	3.19
	rms	6.91	6.90
$C_{2,3}$	rms	4.77	4.82

E. Current Stresses on the Components

For the calculation of the current stresses, it is assumed that the circuit is operating symmetrically, i.e., the current stresses of T_2, D_2 and C_2 are the same as the current stresses of T_3, D_3 and C_3, respectively, and all components are ideal, i.e., the output power of the system is equal to the input power. With this, we have for the average and rms value of the current through transistor T_1

$$I_{T_1,\rm avg} = \frac{P_{\rm o} + 2P_{T_{\rm p1},\rm pro}}{U_{\rm in}} \tag{18}$$

$$I_{T_1,\rm rms} = \sqrt{I_{T_1,\rm avg} \cdot I_{\rm L}}. \tag{19}$$

Furthermore, the diode D_1 values are

$$I_{D_1,\rm avg} = I_{\rm L} - I_{T_1,\rm avg} \tag{20}$$

$$I_{D_1,\rm rms} = \sqrt{I_{D_1,\rm avg} \cdot I_{\rm L}}. \tag{21}$$

The average and rms value of the current through D_2 is

$$I_{D_2,\rm avg} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} I_{\rm op}\sin(\omega t - \varphi)d\omega t = \frac{I_{\rm op}}{\pi} \tag{22}$$

$$I_{D_2,\rm rms} = \sqrt{\frac{I_{D_2,\rm avg}}{I_{\rm L}}} \cdot I_{\rm L} = \sqrt{\frac{I_{\rm op} \cdot I_{\rm L}}{\pi}}. \tag{23}$$

Finally, we have for the average value and the rms value of the current through the boost transistors T_2

$$I_{T_2,\rm avg} = I_{\rm L} - I_{D_2,\rm avg} = \left(\alpha - \frac{1}{\pi}\right) I_{\rm op} \tag{24}$$

$$I_{T_2,\rm rms} = \sqrt{\frac{I_{T_2,\rm avg}}{I_{\rm L}}} \cdot I_{\rm L} = \sqrt{\left(\alpha - \frac{1}{\pi}\right) \cdot I_{\rm op} \cdot I_{\rm L}}. \tag{25}$$

To calculate the rms value of the currents through C_2 and C_3, it is assumed that the current through the output capacitor C_2 (or C_3) only occurs when the corresponding transistor $T_{\rm p1}$ (or $T_{\rm p2}$) is conducting, and the output current $i_{\rm o}$ is constant

TABLE II
POWER COMPONENTS OF THE TPS

Components	Denomination	Type
Input Electrolytic Capacitor	C_1	2 x 470μF/220VDC
CoolMOS	T_1	SPW20N60C3
Power Diode	D_1	RHRG3060
Inductor	L_1, L_2	120μH, 58439-A2, AWG13, 38 turns
CoolMOS	T_2, T_3	SPW47N60C3
Power Diode	D_2, D_3	ISL9R1560P2
Film Capacitor	C_2, C_3	0.47μF/275VAC
Output Filter Inductor	L_{F1},L_{F2}	24μH, 58550-A2, AWG15, 30 turns
Damping Inductor	L_{d1},L_{d2}	34μH, 58550-A2, AWG15, 37 turns
Output Filter Capacitor	C_{F1}, C_{F2}	0.33μF/275 VAC

during the switching period. Here, the square of the local rms value of the capacitor current i_c in a single switching period is defined as

$$\begin{aligned} i_{cs}^2 &= \frac{1}{T_s}\int_0^{T_s} i_c^2 dt \\ &= \frac{1}{T_s}\Big((I_L - I_{op}\sin(\omega t-\varphi))^2 \cdot T_{on} \\ &\qquad + (I_{op}\sin(\omega t-\varphi))^2 \cdot T_{off}\Big). \end{aligned} \tag{26}$$

By combining (26) with (9) and (10), we have

$$i_{cs}^2 = I_{op}\sin(\omega t-\varphi)\cdot(I_L - I_{op}\sin(\omega t-\varphi)). \tag{27}$$

Therefore, the rms value of the output capacitor current during one output period T_o can be calculated as

$$\begin{aligned} I_{C2,rms} &= \sqrt{\frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} i_{cs}^2 d\omega t} \\ &= \sqrt{\frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} I_{op}\sin(\omega t-\varphi)\cdot(I_L - I_{op}\sin(\omega t-\varphi))\, d\omega t} \\ &= I_{op}\sqrt{\frac{\alpha}{\pi}-\frac{1}{4}}. \end{aligned} \tag{28}$$

The stresses on the components have to be calculated for the worst operation point, i.e., the output voltage $U_{o,rms} = 132$ V and the output current $I_{op} = 10$ A for a resistive load. The calculated components current stresses are compared to the simulated results, as shown in Table I, there, for the operating parameters $U_{in} = 200$ V, $V_a = 25$ V, $I_L = 15$ A, $U_{o,rms} = 132$ V, $I_{op} = 10$ A, $R_L = 18.6\ \Omega$ and $f_o = 400$ Hz have been selected. The simulated results show a very good correspondence to the calculated values. According to the components current stresses listed in Table I, the main power devices are selected (see Table II in Section VI).

IV. OUTPUT FILTER DESIGN

The power supply voltages for the LPA include switching frequency ripples and this can reduce the quality of the output voltage due to the nonideal power supply rejection ratio (PSRR) of the LPA. Therefore, a filter is placed between the converter and the LPA to limit the switching noise. However, the cutoff frequency of this filter should not be made too low as it can reduce the performance of the output voltage tracking.

In this section, a small signal model of a feedforward controlled LPA is considered to derive the PSRR. Then, for a given THD+N limitation, a guide line to specify the harmonics of the supply voltages is calculated by using the derived PSRR. Finally, the output filter is designed to meet the harmonic requirement of the supply voltages for the LPA.

A. PSRR Consideration of the LPA

First, the PSRR of a simplified LPA is analyzed to specify the ripple limitation of the power supply voltage. The PSRR is very dependent on the configuration and on component parameters of the LPA [13], [14]. To verify the proposed TPS, a simple class-AB power amplifier using feedforward control is experimentally analyzed. The schematic of the amplifier is shown in Fig. 7. An integrated, high-voltage, power amplifier device, APEX PA97, is employed to amplify the input voltage and provide the driver signal u_{vas} for the output power stage. After biasing the driver signal u_{vas}, two gate voltages u_{g1} and u_{g2} are generated and applied to the output power stage, which is a typical push-pull complementary stage.

In the experimental system, only the output power stage is supplied by the TPS while the voltage gain stage is supplied by additional constant power supplies V_{S+} and V_{S-} (see Fig. 7). Therefore, the switching noise from the TPS is coupled to the system only through the output power stage of the LPA. To simplify the derivation of the PSRR of the LPA, we assume during the following analysis that: 1) the current is equally distributed

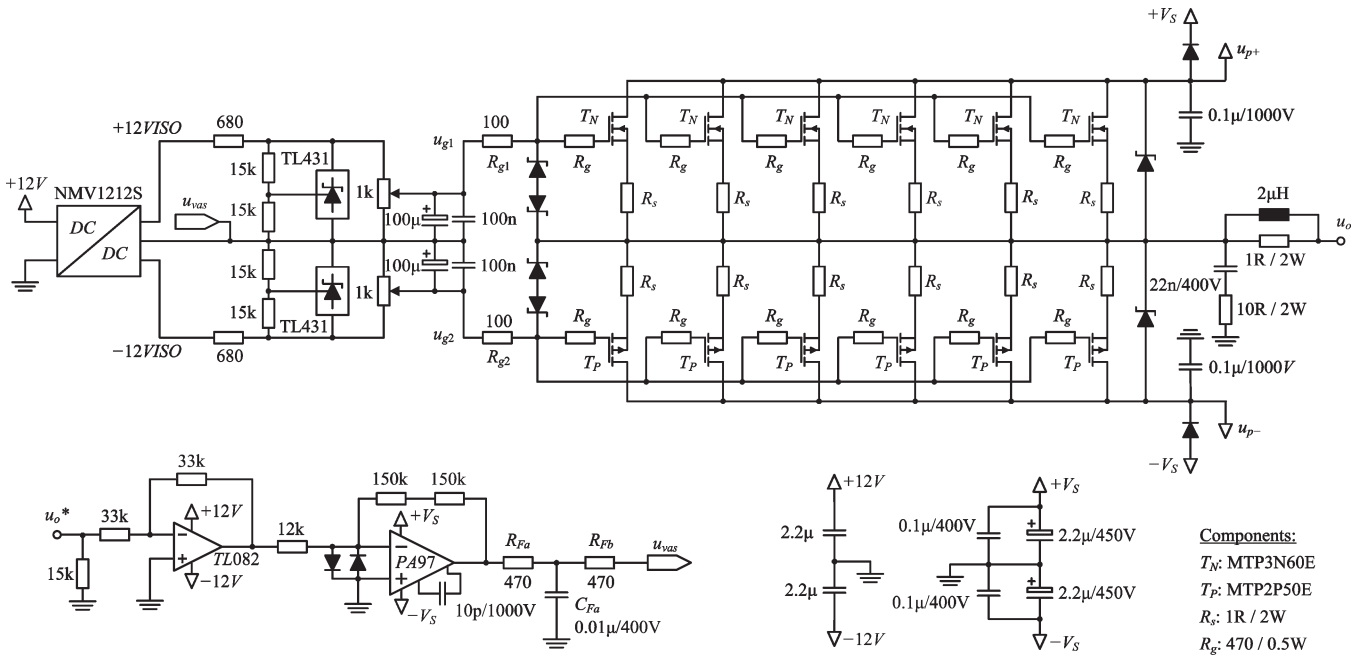

Fig. 7. Circuit schematic of a simple laboratory class-AB power amplifier employing feedforward control.

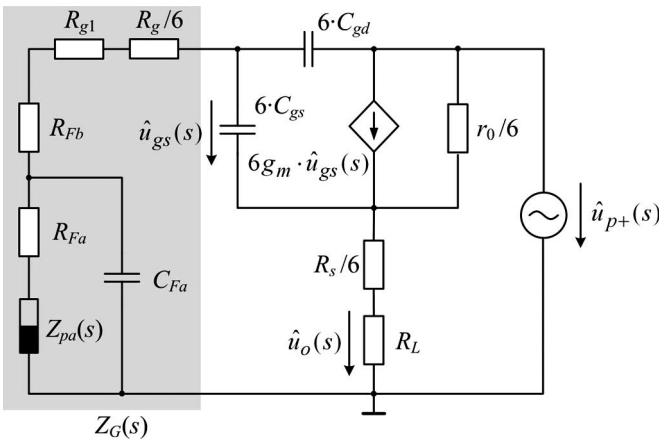

Fig. 8. Simplified small signal model for deriving the positive PSRR. (refer to Fig. 7).

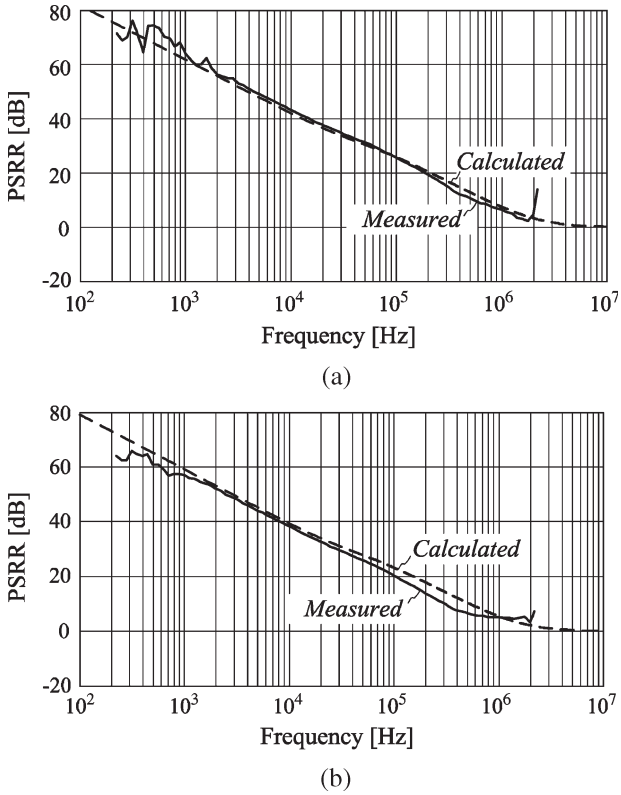

Fig. 9. Comparison of calculated and measured PSRR for (a) positive supply-rail and (b) negative supply-rail. The parameters for testing positive PSRR are: $U_{\rm o} = 100$ V, $U_{\rm ds} = 25$ V, $R_{\rm L} = 30\ \Omega$, $C_{\rm gs} = 751$ pF, $C_{\rm gd} = 19$ pF, $g_{\rm m} = 0.8$ S, $r_0 = 1.8$ MΩ [15]; the parameters for testing negative PSRR are: $U_{\rm o} = -100$ V, $U_{\rm ds} = -25$ V, $R_{\rm L} = 30\ \Omega$, $C_{\rm gs} = 819$ pF, $C_{\rm gd} = 26$ pF, $g_{\rm m} = 0.9$ S, $r_0 = 1.6$ MΩ [16].

in the power MOSFETs both in positive and negative power stages; 2) all the passive components are ideal.

Fig. 8 shows the simplified small signal model for deriving the positive PSRR. In this model, the gate-to-source capacitance is defined as $C_{\rm gs}$; $C_{\rm gd}$ is the gate-to-drain capacitance; $g_{\rm m}$ and r_0 are the transconductance and output impedance of the MOSFET, respectively; $R_{\rm s}$ is the resistance of the current sharing resistors; $R_{\rm L}$ is the load resistance; $Z_{\rm G}(s)$ is the impedance of the drive stage (shaded gray area in Fig. 8), where the impedance of the bias stages is neglected since the impedance of the bias stages is relatively smaller compared to the other series-connected components in this branch, and $Z_{\rm pa}(s)$ is the output impedance of the PA97 with the designed negative feedback (parameters given in Fig. 7).

The negative PSRR can be deduced analogically. The calculated and measured PSRR for positive supply-rail and negative supply-rail are compared in Fig. 9. The calculated PSRRs have good matching with the measured results from the laboratory hardware. Furthermore, the results show that the negative PSRR is less than positive PSRR. The main reason is that the gate-to-drain capacitance of P-channel MOSFET MTP2P50E employed in the negative power stage is higher than that of

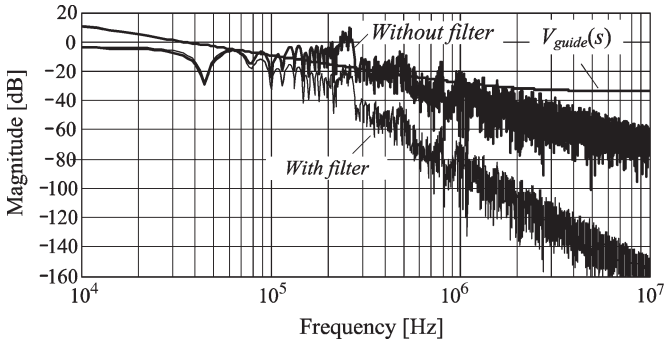

Fig. 10. Simulated TPS voltage spectrum with/without filter. Simulation parameters are: $I_{\rm L} = 15$ A, $V_{\rm b} = 25$ V, $U_{\rm o,rms} = 115$ V, $f_{\rm o} = 400$ Hz, $R_{\rm L} = 16.2\,\Omega$.

N-channel MOSFET MTP3N60E used in the positive power stage, since the PSRR can be approximated as

$$\mathrm{PSRR}(s) = \frac{\hat{u}_{\rm p+}(s)}{\hat{u}_{\rm o}(s)} \approx \frac{s \cdot C'_{\rm gd} \cdot Z_{\rm G}(s) + 1}{s \cdot C'_{\rm gd} \cdot Z_{\rm G}(s)} \tag{29}$$

where $C'_{\rm gd} = 6 \cdot C_{\rm gd}$. It has been verified numerically that this approximated function closely matches the calculated PSRR resulting from the model given in Fig. 8. Therefore, the dominant parameters of the output stage for determining the PSRR are the gate-to-drain capacitance $C_{\rm gd}$ and the drive stage impedance $Z_{\rm G}(s)$. In Fig. 9, it is shown that the PSRR has a slope of -20 dB/dec for low frequencies, and if the frequency increases beyond a certain frequency, then the LPA can no longer attenuate the supply voltage ripple and the ripple appears directly on the output voltage of the LPA.

As seen in (29), the gate-to-drain capacitance $C_{\rm gd}$ has a strong impact on the PSRR; however, $C_{\rm gd}$ is highly dependent on the drain-to-source voltage $U_{\rm ds}$ of the power MOSFET. For a higher $U_{\rm ds}$ across the MOSFET, a higher PSRR can be achieved in the LPA, but on the other hand, this increases the voltage drop across the MOSFET and results in higher power losses. Moreover, the closed loop control of the LPA output voltage can increase the low frequency PSRR, but this is limited by the bandwidth of the control loop.

B. Output Filter Design

For LPAs, the required THD+N figure that characterizes the output voltage quality (output distortion due to the nonlinearities in the signal path of amplifiers [17]) is dependent on the application, and in this paper a value of 0.1% is assumed to be suitable. The aim of the filter design is to limit the output voltage noise caused by the switching frequency ripple of the supply voltages so as not to significantly influence the THD+N figure.

The simulated spectrum of the switching frequency voltage ripple in the output voltage of the TPS without a filter is shown in Fig. 10. The spectrum illustrates that the switching noise is mainly between 100 and 300 kHz.

Before undertaking the filter design, a guideline for the rms amplitude of any output voltage harmonic component caused by the switching power supply must be specified, and in this case a value of less than 10% of the THD+N figure is used.

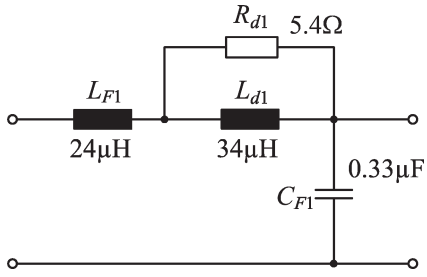

Fig. 11. Topology and parameters of the output filter.

The guideline is given by (30) and is shown in Fig. 10, where the THD+N figure is assumed to be 0.1% for testing power supply applications

$$V_{\rm guide}(s) = 0.1 \cdot 0.1\% \cdot U_{\rm op} \cdot \mathrm{PSRR}(s). \tag{30}$$

In the previous equation, the negative supply-rail rejection ratio is used since it is worse than the positive supply-rail rejection ratio. A filter topology is selected and the parameters of the components are calculated to fulfill the criteria, as shown in Fig. 11. The design of the filter parameters uses the procedure referred to in [18] and [19]. The spectrum of the filtered output voltage of the TPS is shown in Fig. 10, where all the frequency components are lower than the required level. The total noise in the output voltage caused by the supply switching noise in case of no output filter is about 0.6% of the output fundamental for the nominal operating point; with the output filter, the noise figure is significantly reduced to 0.05%.

V. Controller Design

In this section, the small signal model of the TPS is firstly derived, then feedforward control is implemented to improve the stability of the system, and finally the design of the constant current controller is described.

A. Linearized Small Signal Model

The equivalent circuit of the TPS when the upper output stage is operating is given in Fig. 12(a), and the corresponding linearized small signal model including the main damping resistance is shown in Fig. 12(b) [20]. The damping resistances include the equivalent resistances $R_{\rm e1}$ and $R_{\rm e2}$ of the semiconductors in the buck stage and boost stage, the resistances $R_{{\rm s},u1}$, $R_{{\rm s},i1}$ and $R_{{\rm s},u2}$, $R_{{\rm s},i2}$ represent the switching losses of the buck stage and boost stage; the resistances $R_{\rm LM}$ is the summation of the equivalent series resistances of the inductor L_1 and L_2; $R_{\rm LF1}$ and $R_{\rm Ld1}$ are the equivalent series resistances of the output filter inductors. The equivalent semiconductor resistances $R_{\rm e1}$ and $R_{\rm e2}$ representing the semiconductor conduction losses can be determined from

$$\begin{aligned} R_{\rm e1} &= D_1 \cdot R_{T_1} + (1 - D_1) \cdot r_{D_1} \\ R_{\rm e2} &= D_2 \cdot R_{T_2} + (1 - D_2) \cdot r_{D_2} \end{aligned} \tag{31}$$

where D_1 and D_2 are the static duty cycle of the buck stage and boost stage, R_{T_1} and r_{D_1} are the on-resistance of the switch and

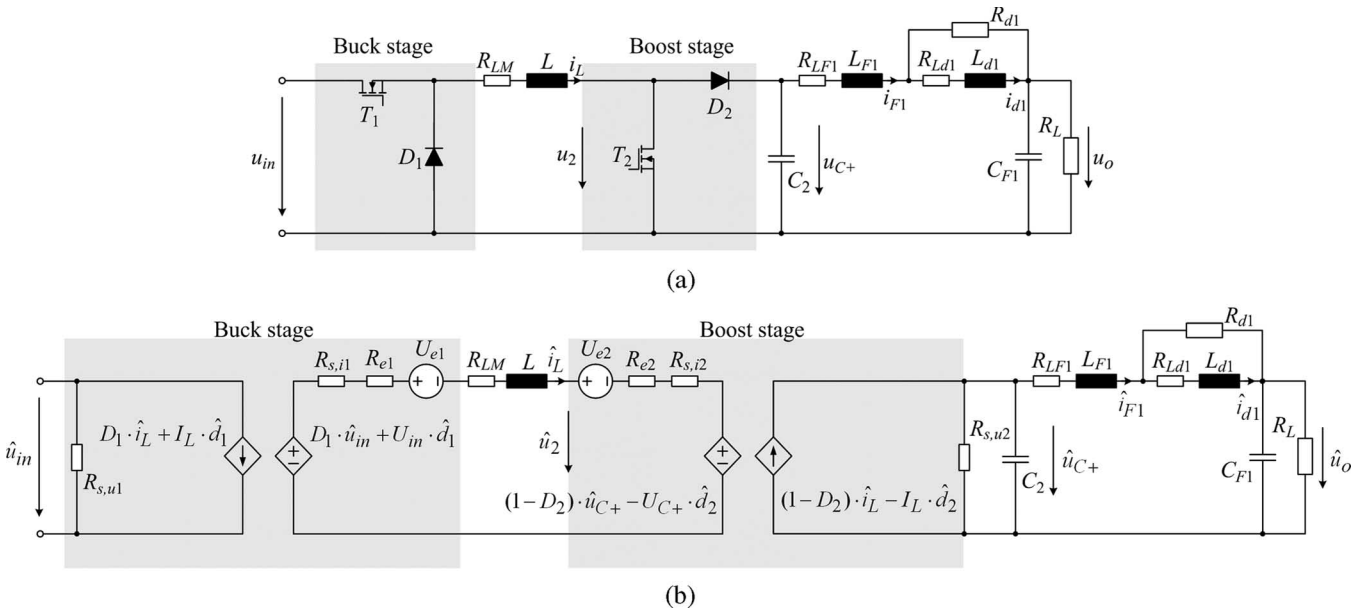

Fig. 12. (a) Equivalent circuit of the TPS when the upper output stage is operating, and (b) the corresponding linearized small signal model including the main damping resistances.

diode of the buck stage, and R_{T_2} and r_{D_2} are the on-resistance of the switch and diode of the boost stage. The voltage sources $U_{\rm e1}$ and $U_{\rm e2}$ denote the equivalent voltage drops of the diodes in the buck stage and boost stage. These voltage sources do not influence the small signal model but slightly alter the dc operating point of the system.

The influence of the switching losses in the buck stage (or the boost stage) to the small signal model can be represented by damping resistors $R_{\rm s,u}$ and $R_{\rm s,i}$ [21]. This consideration is based on an approximation that the switching losses including turn on losses, turn off losses and reverse recovery losses are proportional to the multiplication of the switching voltage $U_{\rm sw}$ and switching current $I_{\rm sw}$ at a given operating point as given by

$$P_{\rm sw} = k_{\rm tt} \cdot f_{\rm sw} \cdot U_{\rm sw} \cdot I_{\rm sw} \tag{32}$$

where $k_{\rm tt}$ is the switching losses coefficient which can be obtained by using (32) to fit the switching losses measurement results and $f_{\rm sw}$ is the switching frequency. The damping resistors $R_{\rm s,u}$ and $R_{\rm s,i}$ can be calculated as [21]

$$R_{\rm s,u} = \frac{2U_{\rm sw}}{k_{\rm tt} \cdot f_{\rm sw} \cdot I_{\rm sw}} \tag{33}$$

$$R_{\rm s,i} = \frac{k_{\rm tt} \cdot f_{\rm sw} \cdot U_{\rm sw}}{2I_{\rm sw}}. \tag{34}$$

By applying (33) and (34) to the switches of buck and boost stages, respectively, the damping resistors $R_{{\rm s},u1}$, $R_{{\rm s},i1}$, $R_{{\rm s},u2}$ and $R_{{\rm s},i2}$ can be calculated as

$$R_{\rm s,u1} = \frac{2U_{\rm in}}{k_{\rm tt1} \cdot f_{\rm buck} \cdot I_{\rm L}}, \quad R_{\rm s,i1} = \frac{k_{\rm tt1} \cdot f_{\rm buck} \cdot U_{\rm in}}{2I_{\rm L}} \tag{35}$$

$$R_{\rm s,u2} = \frac{2U_{\rm C+}}{k_{\rm tt2} \cdot f_{\rm boost} \cdot I_{\rm L}}, \quad R_{\rm s,i2} = \frac{k_{\rm tt2} \cdot f_{\rm boost} \cdot U_{\rm C+}}{2I_{\rm L}}. \tag{36}$$

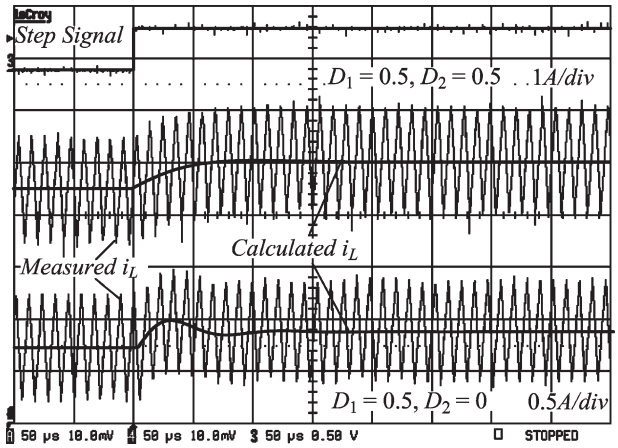

Fig. 13. Comparison of the step responses between measurement results and calculation results, at the operating points of $D_1 = 0.5$ and $D_2 = 0.5$ (buck-boost mode) and $D_1 = 0.5$ and $D_2 = 0$ (buck mode). The operating parameters are: input voltage $U_{\rm in} = 100$ V, $R_{\rm L} = 30\ \Omega$, $f_{\rm buck} = 100$ kHz, $f_{\rm boost} = 100$ kHz, $U_{\rm C+} = 100$ V (buck-boost mode)/50 V (buck mode). Time scale: 50 μs/div.

where $f_{\rm buck}$ is the switching frequency of the buck stage, $f_{\rm boost}$ is the average switching frequency of the boost stage for the considered operating point, $k_{\rm tt1}$ and $k_{\rm tt2}$ are the measured switching losses coefficient of the buck stage and boost stage, respectively.

The step responses of the inductor current, $i_{\rm L}$, for a small change in the buck-stage duty cycle ($\Delta d_1 = 8\%$) are shown in Fig. 13. The results from two typical operating points, a buck-boost mode ($D_1 = 0.5$ and $D_2 = 0.5$) and buck mode ($D_1 = 0.5$ and $D_2 = 0$), are measured experimentally and compared with the theoretical responses. Here, the semiconductor parameters employed to perform the theoretical calculation are obtained from the components' datasheets, assuming the junction temperature of 125 °C. These parameters are: $R_{T_1} = 0.29\ \Omega$, $r_{D_1} = 0.037\ \Omega$, $k_{\rm tt1} = 1.0 \times 10^{-7}$ s, $R_{\rm LM} = 0.03\ \Omega$,

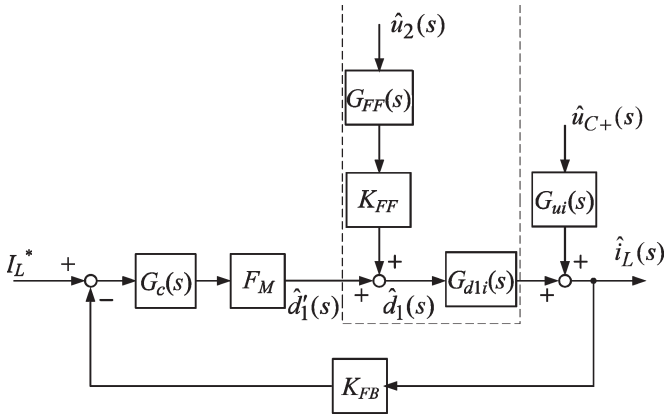

Fig. 14. Small signal block diagram for inductor current control.

$R_{T_2} = 0.11\ \Omega$, $r_{D_2} = 0.06\ \Omega$, $k_{\mathrm{tt2}} = 7.8 \times 10^{-8}$ s. The calculated damping resistances in buck mode are: $R_{\mathrm{s},u1} = 12$ kΩ, $R_{\mathrm{s},i1} = 0.3\ \Omega$, $R_{\mathrm{e1}} = 0.16\ \Omega$, $R_{\mathrm{e2}} = 0.06\ \Omega$, $R_{\mathrm{s},i2} = 0.09\ \Omega$, $R_{\mathrm{s},u2} = 9.7$ kΩ. In buck-boost mode, these resistances are: $R_{\mathrm{s},u1} = 3$ kΩ, $R_{\mathrm{s},i1} = 0.075\ \Omega$, $R_{\mathrm{e1}} = 0.16\ \Omega$, $R_{\mathrm{e2}} = 0.085\ \Omega$, $R_{\mathrm{s},i2} = 0.05\ \Omega$, $R_{\mathrm{s},u2} = 4.9$ kΩ. The figure shows that the theoretical model closely predicts the actual response. It can also be seen that the buck-boost mode of operation has higher damping and a longer rise time compared to the buck mode of operation.

B. Feed-Forward Control and Current Loop Design

From the system small signal model, the transfer function $G_{d_1 i}(s)$ from buck stage duty cycle variations, $\hat{d}_1(s)$, to the inductor current small signal, $\hat{i}_{\mathrm{L}}(s)$, and the transfer function $G_{ui}(s)$ from the output voltage variations of boost stage, $\hat{u}_{\mathrm{C}+}(s)$, to $\hat{i}_{\mathrm{L}}(s)$ can be derived. Since the boost stages utilize hysteresis control, the output voltage $u_{\mathrm{C}+}$ can be assumed to be identical to the reference voltage (ignoring the switching ripple and small time delays). The boost stage output voltage variations, $\hat{u}_{\mathrm{C}+}(s)$, can be considered as a disturbance to $\hat{i}_{\mathrm{L}}(s)$ and therefore the focus is on analyzing $G_{d_1 i}(s)$ in order to design the proper controller $G_{\mathrm{c}}(s)$ for the constant current control. The control block diagram for the inductor current control schematic of Fig. 5 is illustrated in Fig. 14, where the inductor current feedback coefficient K_{FB} is 0.2; $G_{\mathrm{FF}}(s)$ is the low-pass filter for the feedforward voltage u_2 (voltage across the boost transistors T_2 and T_3 as shown in Fig. 5), the feedforward coefficient $K_{\mathrm{FF}} = 1/U_{\mathrm{in}}$, and the triangular carrier coefficient F_{M}, which is the reciprocal value of the peak-to-peak amplitude of the triangular carrier of the PWM.

From Fig. 12 the derivative equation of $\hat{i}_{\mathrm{L}}$ can be written as (with $U_{\mathrm{in}} = \text{const}$ and $U_{\mathrm{C}+} = \text{const}$)

$$L\frac{d\hat{i}_{\mathrm{L}}}{dt} + R_{\mathrm{total}} \cdot \hat{i}_{\mathrm{L}} = U_{\mathrm{in}} \cdot \hat{d}_1 + U_{\mathrm{C}+} \cdot \hat{d}_2 \tag{37}$$

where $R_{\mathrm{total}} = R_{\mathrm{s},i1} + R_{\mathrm{e1}} + R_{\mathrm{LM}} + R_{\mathrm{e2}} + R_{\mathrm{s},i2}$. Since $\hat{u}_{\mathrm{C}+} = 0$, there should be no charge of the local average output current and/or no current through C_2, therefore we have

$$(1 - D_2) \cdot \hat{i}_{\mathrm{L}} - I_{\mathrm{L}} \cdot \hat{d}_2 = 0. \tag{38}$$

By combining (37), (38) and performing Laplace transformation, the transfer function $G_{d_1 i}(s)$ can be derived as

$$G_{d_1 i}(s) = \frac{\hat{i}_{\mathrm{L}}(s)}{\hat{d}_1(s)} = \frac{U_{\mathrm{in}}}{s \cdot L + R_{\mathrm{total}} - \frac{U_{\mathrm{C}+} \cdot (1 - D_2)}{I_{\mathrm{L}}}}. \tag{39}$$

For most operating points, the transfer function $G_{d_1 i}(s)$ has a pole in the right half-plane, but by using feedforward control (see Fig. 5) the poles can be shifted to the left half-plane. Here, the feedforward voltage variation $\hat{u}_2(s)$ is

$$\hat{u}_2(s) = (R_{\mathrm{e2}} + R_{\mathrm{s,i2}}) \cdot \hat{i}_{\mathrm{L}}(s) - U_{\mathrm{C}+} \cdot \hat{d}_2(s). \tag{40}$$

By employing the feedforward control, as shown in Fig. 14, the control duty cycle variation $\hat{d}_1(s)$ is changed to

$$\hat{d}_1(s) = \hat{d}_1'(s) + K_{\mathrm{FF}} \cdot \hat{u}_2(s) \tag{41}$$

where the low-pass filter $G_{\mathrm{FF}}(s)$ is considered as a unity gain since the pole frequency is higher than the current control loop bandwidth. Furthermore, combining (38)–(41), the new plant transfer function $G_{d_1' i}(s)$, inside the dashed frame shown in Fig. 14, can be obtained as

$$G_{d_1' i}(s) = \frac{\hat{i}_{\mathrm{L}}(s)}{\hat{d}_1'(s)} = \frac{U_{\mathrm{in}}}{s \cdot L + R_{\mathrm{s,i1}} + R_{\mathrm{e1}} + R_{\mathrm{LM}}} \tag{42}$$

where we can see that the feedforward control effectively cancels the influence of dc operating value $U_{\mathrm{C}+}$ on the plant transfer function.

A PI controller with an additional pole at high frequency $G_{\mathrm{c}}(s)$ is employed to compensate the system to guarantee a good performance of the system at all operating points. The transfer function of $G_{\mathrm{c}}(s)$ is

$$G_{\mathrm{c}}(s) = K_{\mathrm{p}} \frac{1 + s \cdot a_1}{s \cdot (1 + s \cdot b_1)} \tag{43}$$

where $K_{\mathrm{p}} = 50\ \mathrm{A}^{-1}\mathrm{s}^{-1}$, $a_1 = 4 \times 10^{-3}$ s, $b_1 = 1.6 \times 10^{-6}$ s. With the designed controller, the inductor current loop has a phase margin of around 70° and an overall crossover frequency of 10 kHz, which is 10% of the switching frequency, as shown in Fig. 15.

C. Active Damping of Output Filter

To increase the damping factor of the output filter, especially in case of light load condition, a simple active damping circuit is implemented to avoid using a higher damped passive filter that has more losses [22]–[24]. The structure used to implement the active damping is shown in Fig. 16(a). Since the capacitor voltage u_{C} (upper capacitor voltage $u_{\mathrm{C}+}$ or lower capacitor voltage $u_{\mathrm{C}-}$) is controlled by a hysteresis controller, there is no direct access to control the duty cycle of the switch, and therefore the active damping signal alters the reference signal of the hysteresis controller. Active damping is implemented by measuring and low-pass filtering the filter inductor voltage u_{F1}, and adding it to the reference signal. For the active damping analysis in this paper, the closed loop transfer function of

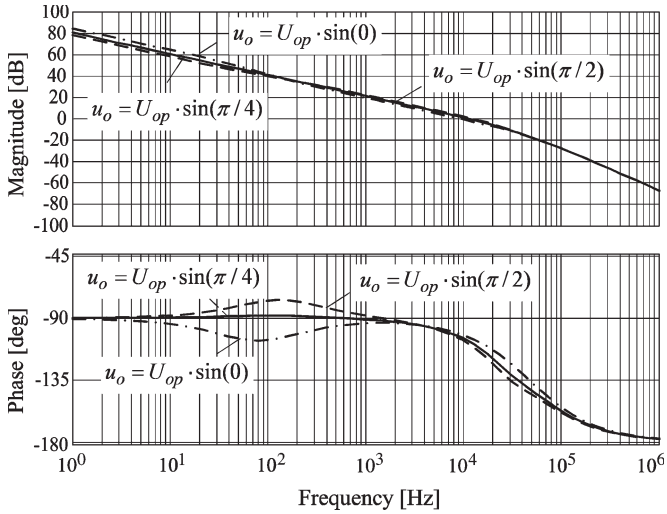

Fig. 15. Bode plots of the compensated current loop at three typical operating points.

hysteresis control is assumed to have unity gain. Therefore, the circuit can be simplified to the scheme as shown in Fig. 16(b), where the active stage is replaced by an ideal voltage source $u_{\rm ref}$ in series with a current controlled voltage source $u_{\rm ad}$. This controlled voltage source in frequency domain $u_{\rm ad}(s)$ is depicted as

$$u_{\rm ad}(s) = K_{\rm A} \cdot \frac{1}{1 + s \cdot a} \cdot s \cdot L_{\rm F1} \cdot i_{\rm F1}(s). \qquad (44)$$

According to

$$Z_{\rm ad}(s) = \frac{u_{\rm ad}(s)}{i_{\rm F1}(s)} = K_{\rm A} \cdot \frac{s \cdot L_{\rm F1}}{1 + s \cdot a} = \frac{s \cdot a}{1 + s \cdot a} \cdot R_{\rm a} \qquad (45)$$

this active damping scheme acts as a virtual variable impedance $Z_{\rm ad}(s)$ in series with the inductor $L_{\rm F1}$ as shown in Fig. 16(c). This virtual impedance has very low absolute value at low frequencies in order not to impact the dc character of the output filter and has a pure resistive behavior with a resistance of $R_{\rm a}$ for high frequencies, which covers the natural frequency of the output filter so that a higher damping factor can be performed. Furthermore, the resistance $R_{\rm a}$ can be derived from (45) as

$$R_{\rm a} = \frac{K_{\rm A} \cdot L_{\rm F1}}{a} \qquad (46)$$

which shows its dependency on the parameters $K_{\rm A}$, $L_{\rm F1}$ and a.

When designing the parameters of the active damping, there are three main following points that should be considered. Firstly, the active damping must not increase the output impedance of the output filter. Secondly, a sufficient damping should be provided at a natural frequency of the output filter. Lastly, the phase shift occurring in the supply voltages at output frequency caused by the active damping must be minimized. According to the three requirements above, the active damping parameters are designed to be: $R_{\rm a} = 5.8\ \Omega$ and

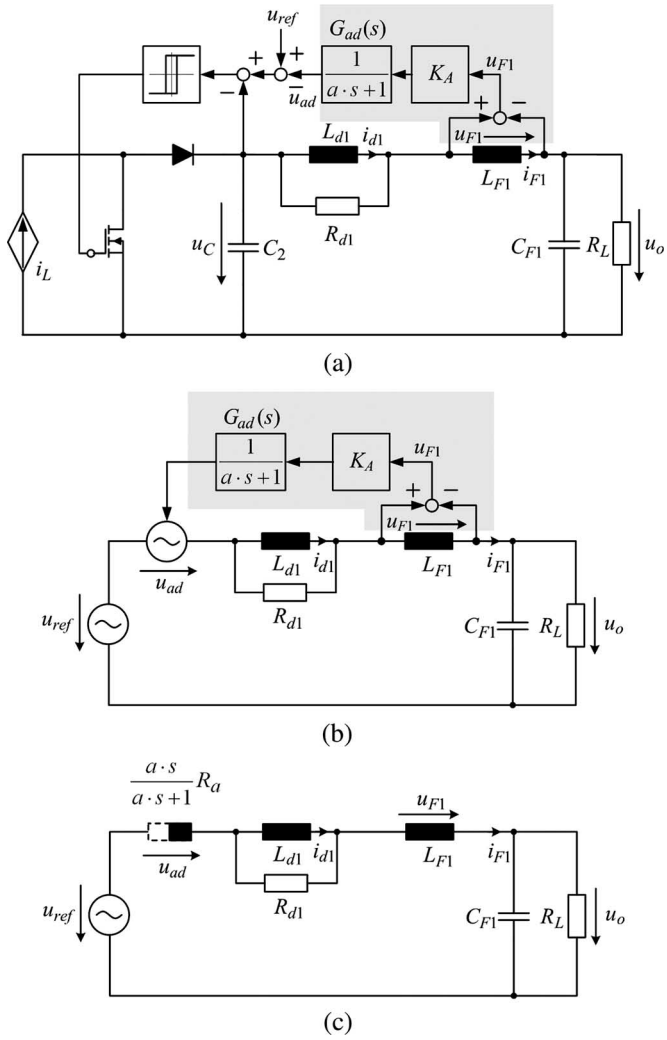

Fig. 16. (a) Structure for implementing active damping of the output filter; (b) the equivalent circuit by assuming ideal hysteresis control and (c) the equivalent circuit with inserted virtual variable impedance $(as/(as+1)) \cdot R_{\rm a}$ to increase the system damping factor.

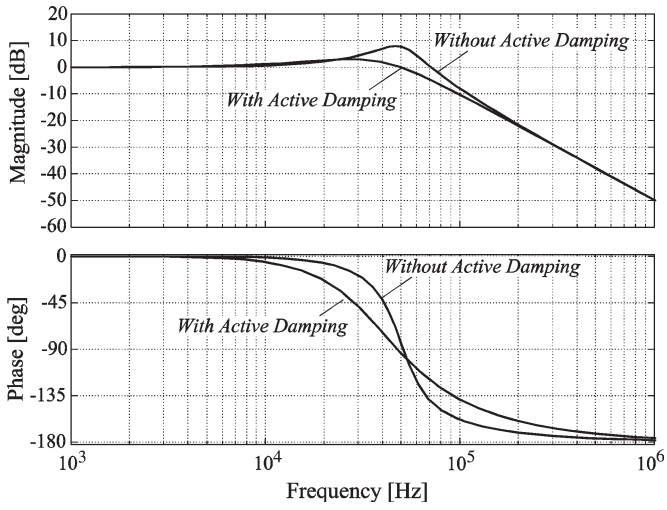

Fig. 17. Comparison of the bode plots of the transfer function from $u_{\rm ref}$ to $u_{\rm o}$ with active damping and without active damping ($R_{\rm L} = 5\ {\rm k}\Omega$).

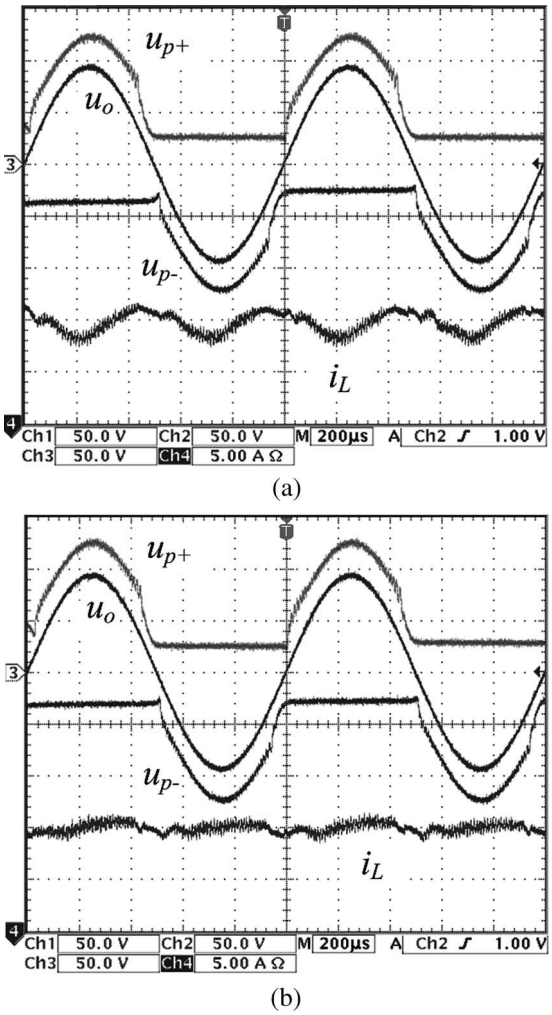

Fig. 18. Performance comparison without feedforward control (a) and with feedforward control (b). Operating parameters are: $U_{\rm in} = 100$ V, $I_{\rm L} = 10$ A, $V_{\rm b} = 30$ V, $U_{\rm op} = 100$ V, $f_{\rm o} = 1$ kHz, $R_{\rm L} = 30\ \Omega$, and buck stage switching frequency $f_{\rm buck} = 100$ kHz. Voltage scale: 50 V/div; current scale: 5 A/div.

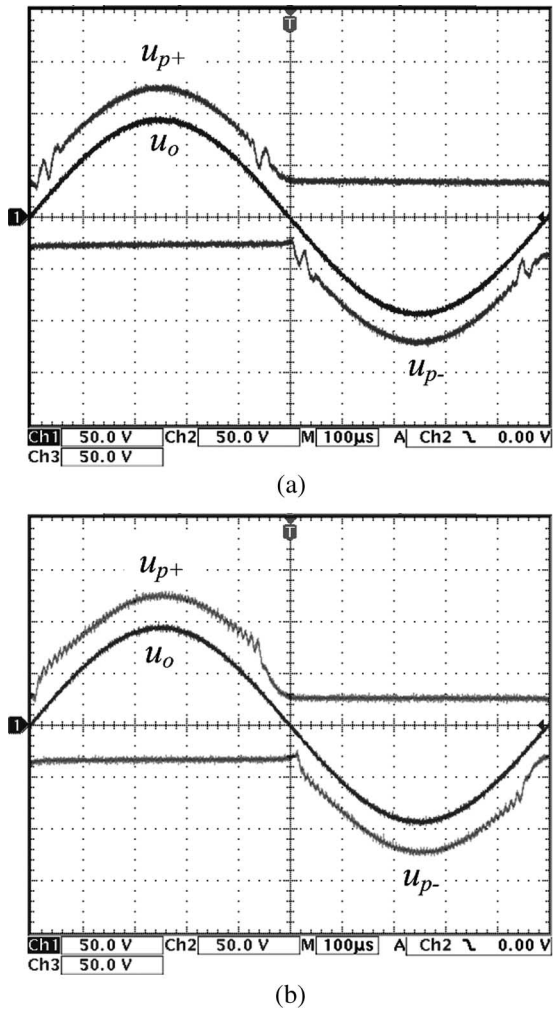

Fig. 19. Comparison of the measured performance of the output voltages of the TPS without active damping (a) and with active damping (b). The operation parameters are: $U_{\rm in} = 100$ V, $I_{\rm L} = 10$ A, $V_{\rm b} = 30$ V, $U_{\rm op} = 100$ V, $f_{\rm o} = 1$ kHz, $f_{\rm buck} = 100$ kHz, and $R_{\rm L} = 30\ \Omega$. Voltage scale: 50 V/div.

$a = 1.7 \times 10^{-5}$ s. Fig. 17 compares the transfer function from $u_{\rm ref}$ to $u_{\rm o}$ (when $R_{\rm L}$ is 5 kΩ) with the case of active damping and without active damping. This figure shows that the damping of the system at the frequencies around the natural frequency of the output filter is significantly increased. If we would like to further reduce the phase shift of the supply voltages while keeping the same damping factor, a higher order filter $G_{\rm ad}(s)$ can be applied, which can lower the virtual variable impedance in the low frequency range. Moreover, the reason that we cannot only use active damping in the output filter is that the active damping just works when the switches are operating; however, sufficient passive damping is still required when the switches are not switching in case of very light load current.

VI. Experimental Results

To verify the theoretical considerations, a 1.5-kW prototype of the TPS shown in Fig. 5 has been realized for feeding a 1 kW LPA. The main components employed in the TPS are listed in Table II.

The experimental results, measured from the laboratory prototype, are shown in Fig. 18 and compared to the system performance with and without feedforward control. It is shown that with the help of feedforward control the shape of the inductor current $i_{\rm L}$ [Fig. 18(b)] shows a significant improvement in the rejection of the variation of output voltage compared to the inductor current $i_{\rm L}$ without feedforward control [Fig. 18(a)].

Experimental results are shown in Fig. 19 to compare the system performance without active damping (a) and with active damping (b). It is shown that the oscillations occurring in Fig. 19(a) are no longer present in Fig. 19(b) due to the active damping.

The experimental verification has been also performed for three different loads, i.e., ohmic load ($\varphi = 0^\circ$), 16 Ω, ohmic-inductive load ($\varphi \approx 45^\circ$), 10 Ω/2 mH in series, and ohmic-capacitive load ($\varphi \approx -45^\circ$), 12 Ω/10 μF in series, for nominal output voltage $U_{\rm o,rms} = 115$ V, maximum output current $I_{\rm op} = 10$ A and maximum output frequency $f_{\rm o} = 1$ kHz. The time behavior of the LPA supply voltages, $u_{\rm p+}$ and $u_{\rm p-}$, and the amplifier output voltage, $u_{\rm o}$, is shown in Fig. 20 for ohmic and ohmic-reactive loads. As the output current of the buck input

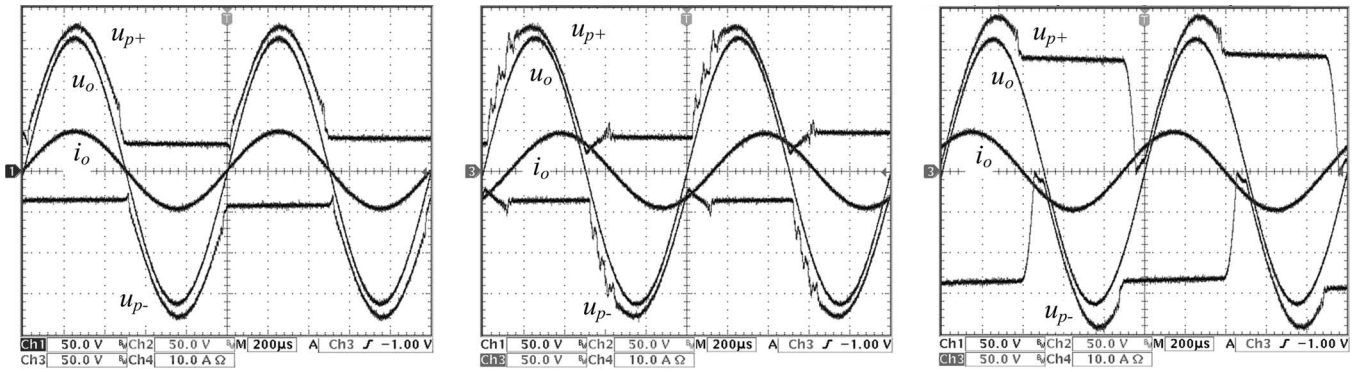

Fig. 20. Experimental results for different loads; Operating parameters are: $U_{\rm in} = 200$ V, $I_{\rm L} = 15$ A, $V_{\rm a} = 25$ V, $V_{\rm b} = 25$ V, $U_{\rm op} = 162$ V, $I_{\rm op} = 10$ A, $f_{\rm o} = 1$ kHz, $f_{\rm buck} = 100$ kHz; ohmic load, $Z_{\rm L} = R_{\rm L} = 16\ \Omega$ (a); inductive load, 10 Ω/2 mH in series (b); capacitive load, 12 Ω/15 μF in series (c). Voltage scale: 50 V/div; current scale: 10 A/div.

stage (see Fig. 5) is controlled to a constant value, the LPA supply voltage can respond to variations with high dynamics. In Fig. 20(b), it can be seen that there are discrete steps in the supply voltage when the output capacitor voltage of the upper/lower stage is being charged and no load current is supplied by the upper/lower stage. Each step duration is one switching period, therefore the active damping cannot help reduce this ringing; however, an output filter with a higher damping factor can eliminate this ringing (see [11, Fig. 10(e)]) but has a greater volume and losses. In the case of capacitive load [see Fig. 20(c)] the supply voltages $u_{\rm p+}$ and $u_{\rm p-}$ of the linear amplifier cannot follow the reference value because there is no current for discharging the capacitor C_2 or C_3. However, this does not affect the losses of the LPA since the corresponding transistors do not carry a load current.

The excellent transient behavior of the system is clearly shown in Fig. 21 where a sawtooth-shaped output signal with a slope of the trailing edge of ≈ 6 V/μs is generated and the switch-mode stage adjusts the supply voltage such that some voltage margin is left and no distortion in the linear amplifier output signal occurs.

Fig. 22 compares the power losses and efficiencies of the proposed TPS+LPA system and of a class-AB LPA. The testing conditions are that both systems output 400 Hz, 10 A peak value sinusoidal currents over the full range of the specified output voltage. The efficiencies and power losses of the class-AB LPA supplied by constant voltages are calculated by using (4) and not measured from the hardware, since the maximum allowed power dissipation of the experimental LPA is only 280 W. However, it has been verified that the calculation results of (4) closely match the measured results of the experimental LPA operating at lower power levels. It is shown in Fig. 22 that the proposed TPS+LPA system has an overall higher efficiency compared to the conventional class-AB LPA in the full output voltage range. The power losses reduction advantage for the proposed system is most obvious when generating lower output voltages. There, the full output current capacity is available, while conventional class-AB LPAs often require downgrading their output current capacity in the lower voltage region because of the dramatically increased power losses as illustrated in Fig. 22. Furthermore, the calculated efficiencies of the proposed system have good matching with the measured results (maximum 2.5% difference at $U_{\rm o,rms} = 98$ V).

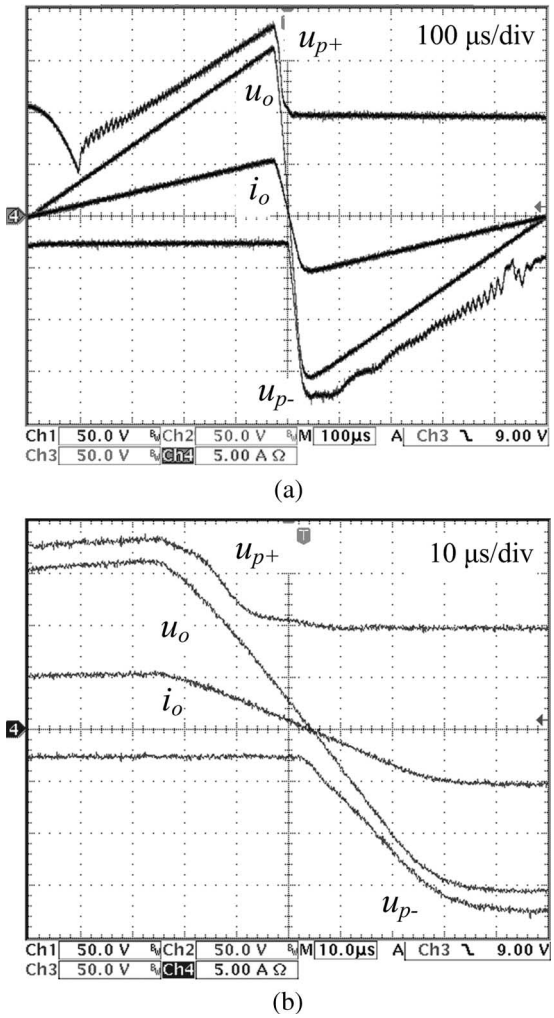

Fig. 21. Experimental results for generating a sawtooth-shaped 1 kHz linear amplifier output $u_{\rm o}$; ratio of rise time to fall time is 19:1; (a) Waveforms at one output period, (b) Zoon in waveforms at the falling edge of the output voltage. Operating parameters are: $U_{\rm in} = 200$ V, $I_{\rm L} = 15$ A, $V_{\rm a} = 25$ V, $V_{\rm b} = 25$ V, $U_{\rm op} = 162$ V, and $R_{\rm L} = 30\ \Omega$. Voltage scale: 50 V/div; current scale: 5 A/div.

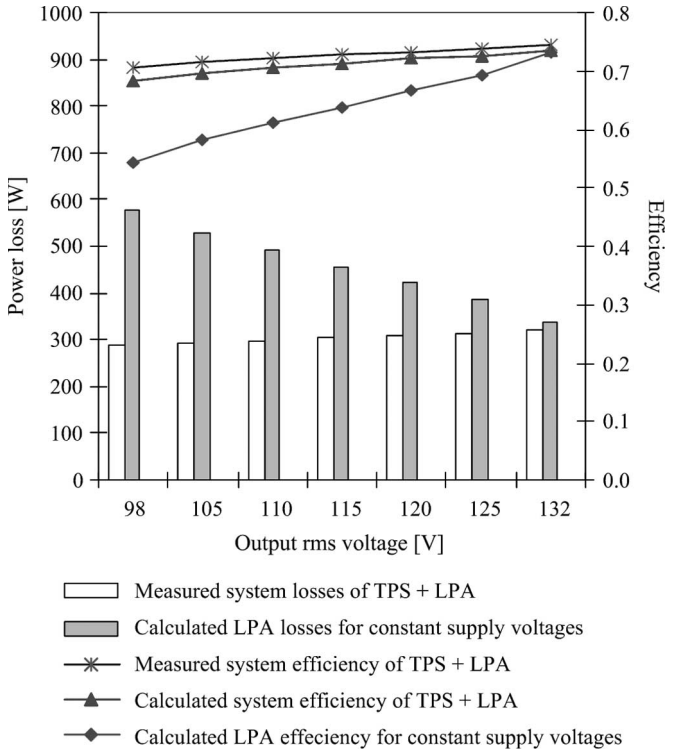

Fig. 22. Power loss and efficiency comparison of the proposed system, TPS+ LPA, and the LPA with constant supply voltages. Operation parameters of TPS+ LPA are: $U_{\rm in} = 200$ V, $I_{\rm L} = 15$ A, $V_{\rm a} = 25$ V, $V_{\rm b} = 25$ V, $I_{\rm op} = 10$ A, $f_{\rm o} = 400$ Hz, $f_{\rm buck} = 100$ kHz, while the operation parameters of LPA with constant supply voltages are: $V_{\rm CC} = \pm 200$ V, $I_{\rm op} = 10$ A, $f_{\rm o} = 400$ Hz.

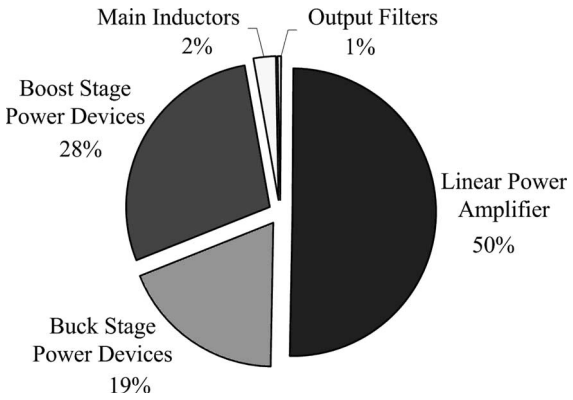

Fig. 23. Calculated power loss distribution of the proposed TPS+ LPA system at maximum output power. The operation parameters of TPS+ LPA are: $U_{\rm in} = 200$ V, $I_{\rm L} = 15$ A, $V_{\rm a} = 25$ V, $V_{\rm b} = 25$ V, $U_{\rm o,rms} = 132$ V, $I_{\rm op} = 10$ A, $f_{\rm o} = 400$ Hz, $f_{\rm buck} = 100$ kHz.

The power losses distribution of the proposed TPS+LPA system at maximum output power is demonstrated in Fig. 23, where TPS and LPA each produces about 50% of the total system losses. Here, the efficiency of TPS stage is relatively low (about 87%) due to the high current stresses on the components and hard switching of the MOSFETs. However, the current stresses on the components can be reduced by applying the variable current control scheme proposed in [11] and the hard switching losses could be lowered by employing soft switching techniques.

VII. Conclusion

A new TPS topology for conditioning the supply voltages of a LPA has been proposed which reduces the voltage drops across the linear amplifier power transistors to low values and therefore considerably lowers the amplifier power losses. This proposed boost-type TPS has some major advantages over the existing buck-type tracking power supplies, such as no requirement for dc bus voltage higher than the output voltage, small output filter and high output voltage dynamic. These benefits make the boost-type TPS more competent for high output voltage application, e.g., testing power supplies. However, the maximum output current is limited by the constant inductor current value.

In this paper, the theoretical calculations demonstrate that the power transistors losses in the LPA are significantly reduced when employing variable supply voltages. The current stresses on the power semiconductors of the proposed system are calculated analytically. The output filter is implemented and dimensioned according to the PSRR of the LPA to ensure a high output voltage quality of the system. Furthermore, the small signal model of the TPS is derived, and based on this model the constant current loop and feedforward control are designed to insure the inductor current remaining constant even when the output power is varying in high frequency. An active damping strategy for the output filter which is easy to implement is designed. As an example for testing application of single-phase aircraft equipment, a 1 kW laboratory prototype including TPS and LPA is built to verify the theoretical analysis. The experimental system shows a clear system efficiency improvement compared to a conventional class-AB LPA and a high output voltage dynamic 6 V/μs is achieved. As a result, the proposed system is applicable for linear amplifiers generating large amplitude output signals in the kilohertz range.

In the course of further research the experimental hardware could be extended to the topology shown in Fig. 2(b), i.e., an isolated three-level buck-type dc–dc converter will be employed as input stage. The output filter could be substituted by a higher order circuit in order to reduce the supply voltage phase shift when outputting high frequency signal. Furthermore, the adaptive current control scheme depicted in Fig. 7 [11] could be implemented in order to further reduce the system losses. When the TPS+LPA system is used to perform specific equipment testing, where the output voltage waveform shape is known, it is possible to lower the system losses by preshaping the inductor current. Therefore, we can calculate the required inductor current reference such that the inductor current can ramp up to a high current level before the load requires the high current. In this way, we can lower the inductor current slew rate requirement and reduce the system losses.

The proposed TPS+LPA system has shown an obvious system losses reduction over the conventional class-AB LPA in high output voltage applications (see Fig. 22). The other future option for this application is to use pure switching mode power amplifiers. By employing advanced semiconductor devices, e.g., SiC Schottky diodes in combination with superjunction silicon MOSFETs, to increase the switching frequency

or apply interleaving or/and multilevel methods to increase the equivalent switching frequency, it is possible to realize a high bandwidth, high voltage power amplifier of similar performance.

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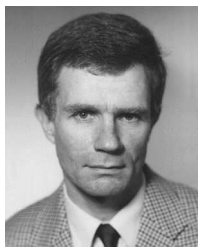

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