High-Frequency Isolated DC/DC Converter for Input Voltage Conditioning of a Linear Power Amplifier

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Abstract – *Conventional linear power amplifiers show a high output voltage quality but are characterized by high power losses and/or low power density. Therefore, there is a growing interest in increasing the efficiency of linear power amplifiers, e.g. for the realization of high power testing voltage sources.*

In this paper a high-frequency isolated DC/DC converter system is proposed for the conditioning of the input voltage of a linear power amplifier. The output voltage of the DC/DC converter is varied according to the output voltage to be formed by the linear power amplifier so that the voltage drop occurring across the power amplifier output transistors is reduced to low values which results in a significant increase of the total system efficiency. The control design of the DC/DC converter is for fast output voltage response according to the high large signal bandwidth of the linear power amplifier. The three-level input stage of the proposed system does allow a direct connection to the output of a three-phase three-level PWM rectifier ensuring low effects on the supplying mains.

The operating principle of the proposed system is described and the design of the output voltage control is treated in detail. The resulting dynamic behavior of the system is analyzed by digital simulation. Finally, the theoretical considerations are verified by measurements on a 1.5kW laboratory prototype.

I. Introduction

Conventional linear power amplifiers, as schematically shown in **Fig.1**(a), are widely employed in industry applications because of high output voltage quality and excellent dynamic behavior. As shown in Fig,1(b) conventional linear power amplifiers are usually supplied with constant voltage. The time behavior of the current, voltage and instantaneous power of the output power transistor T_{p1} of a linear amplifier are shown in Fig.1(c) for class-AB operation. High losses occurring in the transistors do resulting in an extremely low efficiency, especially in case of supplying reactive loads. This constitutes a serious problem especially for high power systems which tend to be very bulky and expensive because of the large heat sinks required and the large power consumption. Consequently, there is a growing interest in increasing the efficiency of high power linear power amplifier systems.

A very efficient way for avoiding the aforementioned drawbacks is the conditioning, i.e. variation of the supply voltage of the linear power amplifier by a DC/DC converter according to the voltage to be generated at the linear amplifier output [1],[2]. With this, the voltage drop across the linear amplifier power transistors could be reduced considerably resulting in a corresponding reduction of the amplifier power losses. In [1] two buck converters which series connected output voltages are proposed for achieving a variable amplifier supply voltage. However, no isolation of the output voltage is provided which would however be required for high power testing systems [3].

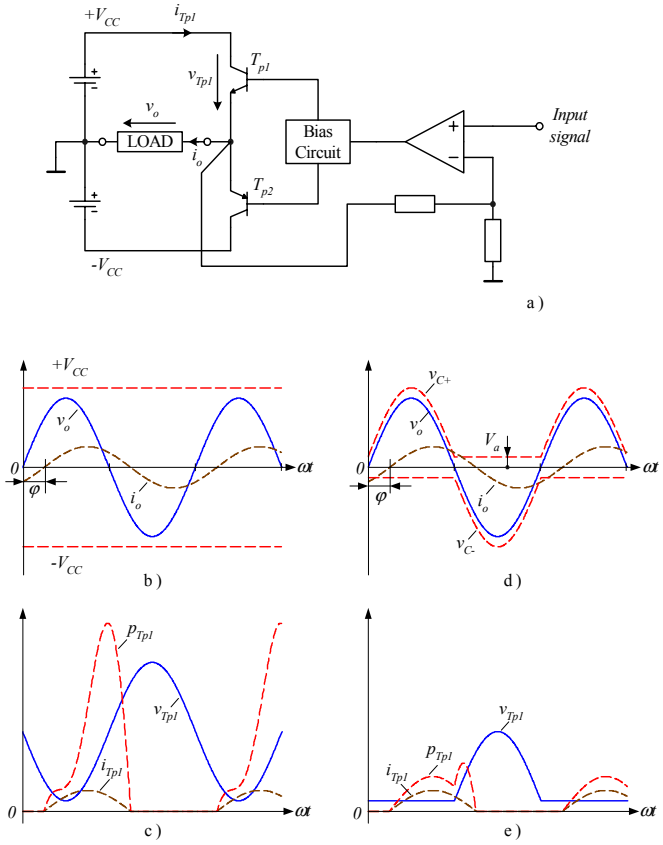

Fig.1: Conventional linear power amplifier **(a)**; basic waveforms for constant supply voltage **(b)**; current, voltage and instantaneous power loss of transistor T_{p1} for constant supply voltage **(c)**; variation of the supply voltage according to the time behavior of the voltage to be generated by the linear power amplifier **(d)**; current, voltage and instantaneous power loss of transistor T_{p1} for controlled supply voltage **(e)**.

In this paper, a new isolated DC/DC converter topology for controlling the supply voltage of a linear power amplifier according to Fig.1(d) is proposed [4].

In principle, a DC/DC converter as shown in **Fig.2**(a), could be employed for realizing a variable supply voltage. There, the input stage is formed by a three-level DC/DC converter topology [4]

which does reduce the blocking voltage stress on the primary side power transistors as compared to a conventional full-bridge topology. Therefore, the concept is especially advantageous for high input voltage applications. The system output stage is formed by two buck converters with series connected outputs. The control of the power amplifier supply voltages could be implemented with underlying current control. However, the system shows a high realization effort as a center-tapped transformer, four inductors and four capacitors are employed on the secondary side. Another drawback is the limitation of the maximum rate of change of the output voltage by the output filter.

The proposed boost-type topology [4] depicted in Fig.2(b) is characterized by a comparably low realization effort. Only a single inductor and two capacitors are required at the secondary side. In this topology, a control loop is provided for impressing the secondary inductor current; based on this, a tolerance band control of the supply voltages of the linear amplifier is performed by proper gating of the power transistors T_5 and T_6 where an excellent dynamic behavior of the voltage control can be achieved.

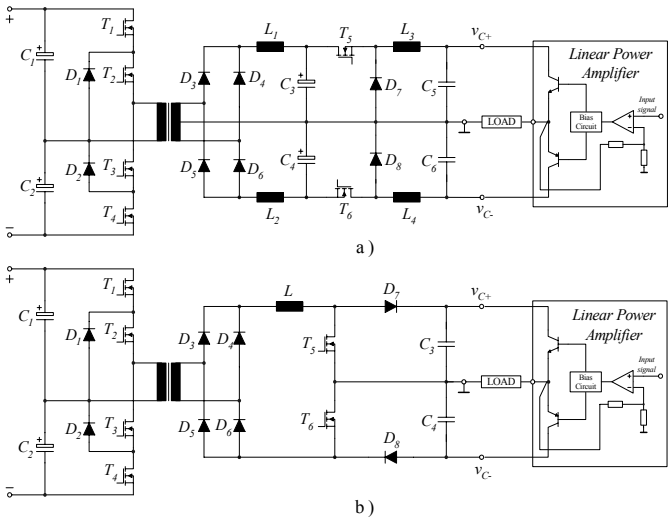

Fig.2: DC/DC converter topologies for conditioning the supply voltage of a linear power amplifier; **(a)** conventional realization; **(b)** proposed system [4].

II. Transistor Losses of a Linear Power Amplifier for Different Input Voltage Conditions

For the following calculations we assume the output voltage of the linear power amplifier

$$v_o = V_p \sin \omega t \tag{1}$$

resulting for the linear load in an output (load) current

$$i_o = \frac{V_p}{Z_L} \sin(\omega t - \varphi) \tag{2}$$

where Z_L is the magnitude of the load impedance and $\varphi \in (-\pi, +\pi)$ is the phase angle of the load current. The output power of the linear amplifier then is given by

$$P_o = \frac{V_p^2}{2Z_L} \cos\varphi \,. \tag{3}$$

For a linear power amplifier operating in class-AB mode, the quiescent current is neglected. Therefore, the losses resulting for transistor T_{p1} (cf. Fig.1(c)) are

$$P_{Tp1\_lin} = \frac{1}{2\pi} \int_{\varphi}^{\varphi+\pi} (V_{cc} - V_p \sin \omega t) \frac{V_p}{Z_L} \sin(\omega t - \varphi) d\omega t = \frac{V_p}{2\pi Z_L} \left(2V_{cc} - \tfrac{1}{2} V_p \pi \cos\varphi\right) \tag{4}$$

In case the class-AB power amplifier is supplied by the proposed converter we have for the power losses of transistor T_{p1} (cf. Fig.1(e)) and $\varphi \in (0, +\pi)$

$$P_{Tp1\_pro} = \frac{1}{2\pi} \left[\int_{\varphi}^{\pi} V_a \cdot \frac{V_p}{Z_L} \cdot \sin(\omega t - \varphi) d\omega t + \int_{\pi}^{\pi+\varphi} (V_a - V_p \sin \omega t) \cdot \frac{V_p}{Z_L} \cdot \sin(\omega t - \varphi) d\omega t \right] = \frac{V_p}{2\pi Z_L} \left[2V_a + \tfrac{1}{2} V_p (\sin\varphi - \varphi \cos\varphi) \right] \tag{5}$$

where $V_a = V_{cc} - V_p$ denotes the voltage remaining across a conducting power transistor. For $\varphi \in (-\pi, 0)$, the power losses in transistor T_{p1} are

$$P_{Tp1\_pro} = \frac{1}{2\pi} \left[\int_{\varphi}^{0} (V_a - V_p \sin \omega t) \cdot \frac{V_p}{Z_L} \cdot \sin(\omega t - \varphi) d\omega t + \int_{0}^{\pi+\varphi} V_a \cdot \frac{V_p}{Z_L} \cdot \sin(\omega t - \varphi) d\omega t \right] = \frac{V_p}{2\pi Z_L} \left[2V_a + \tfrac{1}{2} V_p (\varphi \cos\varphi - \sin\varphi) \right] \tag{6}$$

Combining (5) and (6) there results for $\varphi \in (-\pi, +\pi)$.

$$P_{Tp1\_pro} = \frac{V_p}{2\pi Z_L} \left(2V_a + \tfrac{1}{2} V_p \left|\sin\varphi - \varphi\cos\varphi\right|\right). \tag{7}$$

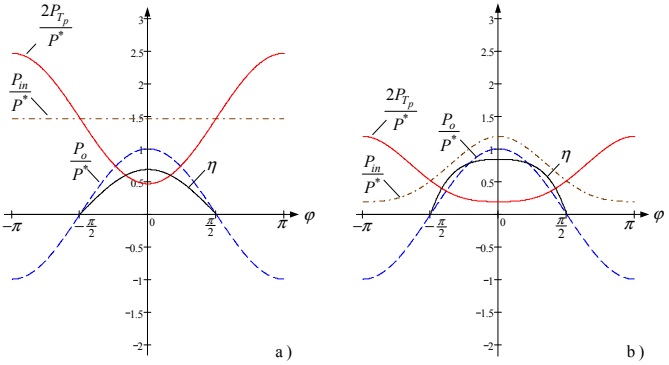

Fig.3: Dependency of the normalized transistor losses (normalization with reference to P^* as defined in (8)), input power, output power and efficiency of a linear class-AB power amplifier on the load phase angle for constant supply voltage **(a)** and for the proposed varying supply voltage **(b)**.

In **Fig.3** the normalized transistor losses, the input power, the output power and the efficiency of the linear class-AB power amplifier are given for different load conditions for the following operating parameters: V_{cc} = 230 V, V_a = 30 V, V_p = 200 V, Z_L = 20 Ω. Here, the normalization basis of the power is defined as

$$P^* = \frac{V_p^2}{2Z_L}; \tag{8}$$

P_{Tp} denotes the losses of a power transistor. For employing the proposed concept the transistor power losses can be significantly reduced in comparison to constant supply voltage what does result

in a significant improvement of the amplifier efficiency (in Fig.3, the efficiency is only shown for passive loads, i.e., for phase angle values $\varphi \in (-\pi/2, +\pi/2)$).

In **Fig.4** the normalized transistor power losses are depicted in dependency on the normalized output voltage amplitude; the operating parameters are identical to Fig.3. The reduction of the losses due to the conditioning of the supply voltage is immediately obvious.

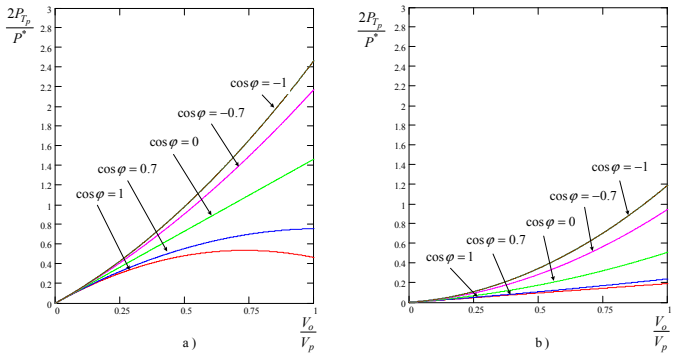

Fig.4: Dependency of the normalized transistor power losses on the normalized amplifier output voltage amplitude for constant supply voltage **(a)** and for supply voltage conditioning **(b)** according to Fig.1(d).

III. Converter Control for Input Voltage Conditioning of the Linear Power Amplifier

The control structure of the proposed converter is shown in **Fig.5**. The converter is formed by a three-level buck-type input stage and a three-level boost-type output stage. The input stage output current is controlled to a constant value where constant-frequency average current-mode control and a feed-forward of the local average value of the voltage across the power transistors is employed. For controlling the boost-stage output voltages a tolerance band control is provided in order to achieve high dynamics at low realization effort.

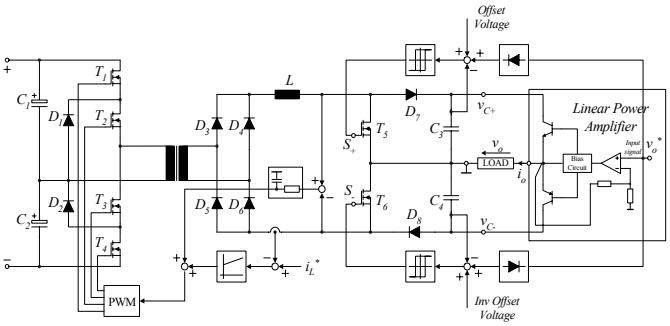

Fig.5: Control scheme of the proposed converter [4].

The conduction states of the output stage are shown in **Fig.6** for positive load current. There, the buck-type input stage is considered by a current source i_L. For realizing the control of the supply voltages of the linear power amplifier according to Fig.5, T_6 is remaining in the on-state in case V_{C-} is lower than the reference value. When the positive supply voltage V_{C+} due to the current consumption of the linear amplifier reaches the corresponding reference value, T_5 is turned off (cf. Fig.6(a)) and the current i_L commutates into D_7 and does recharge the output capacitor C_5. If on the other hand the voltage V_{C+} reaches the upper boundary of the tolerance band, T_5 is turned on, accordingly diode D_7 blocks (cf. Fig.6(b)), and i_L free-wheels through T_5 and T_6.

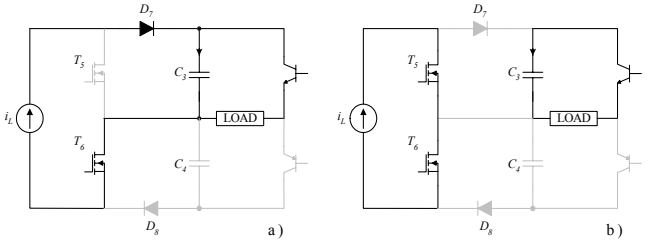

Fig.6: Simplified equivalent circuit of the proposed converter and conduction states of the output stage for positive load current.

For controlling the output current I_L of the buck-stage to a constant value according to the maximum load current and the maximum charging current of the capacitors C_3 and C_4 a highly dynamic control of the linear amplifier supply voltage is achieved, however higher conduction losses do occur.

In order to reduce the conduction losses, an inductor current control as depicted in **Fig.7** could be employed [4]. There, the current reference value i_L^* is formed by the rectified linear amplifier load current i_O, the charging current of C_3 and/or C_4 dependent on the rate of change of the linear amplifier output voltage reference value v_O^*, and by an offset signal which guarantees a sufficient control margin. In case the duty cycle of T_5 or T_6 reaches values lower than 10% the offset is increased so that the control margin is maintained also for inaccurate pre-control of the amplifier load current and/or capacitor charging current.

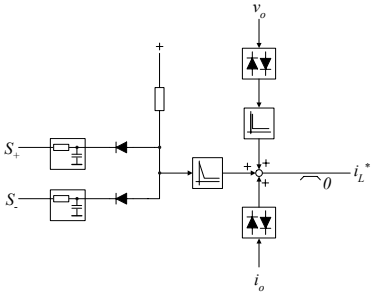

Fig.7: Schematic circuit of the buck stage output current reference value generation.

IV. Simulation and Dimensioning

In the following the current stresses on the power semiconductor devices is calculated and verified by digital simulation. There, the three-level isolated DC/DC converter input stage is replaced by a basic buck stage for the sake of simplicity (cf. **Fig.8**). Furthermore, constant output current of the buck-stage is assumed.

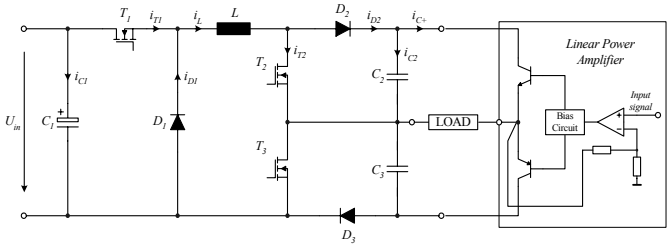

Fig.8: Simplified circuit diagram of the proposed converter for replacing the isolated input stage by a basic buck converter.

A Constant inductor current

The required maximum value $I_{L\max}$ of the inductor current (which occurs for capacitive loading of the amplifier) can be calculated as

$$I_{L\max} = \frac{V_p}{Z_L} + C_o V_p \omega \,, \tag{9}$$

where C_o is the output capacitor of DC/DC converter. With respect to providing a modulation margin for T_2 and T_3, (cf. Fig.8) the constant inductor current is set to

$$I_L = 1.1 I_{L\max} \,. \tag{10}$$

B Current stress on the components

For the calculation of the current stresses all components are assumed ideal, consequently the output power of the system is equal to the input power. With this, we have for the average and rms value of the current through transistor T_1

$$I_{T1\_avg} = \frac{P_o + 2P_{Tp1\_pro}}{V_{in}} \,, \tag{11}$$

$$I_{T1\_rms} = \sqrt{\frac{I_{T1\_avg}}{I_L}} \cdot I_L \,. \tag{12}$$

Furthermore, we receive for diode D_1

$$I_{D1\_avg} = I_L - I_{T1\_avg} \,, \tag{13}$$

$$I_{D1\_rms} = \sqrt{\frac{I_{D1\_avg}}{I_L}} \cdot I_L \,. \tag{14}$$

The average and rms value of the current through D_2 and D_3 is

$$I_{D2,3\_avg} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} \frac{V_p}{Z_L} \sin(\omega t - \varphi) d\omega t = \frac{V_p}{\pi \cdot Z_L} \tag{15}$$

$$I_{D2,3\_rms} = \sqrt{\frac{I_{D2,3\_avg}}{I_L}} \cdot I_L \,. \tag{16}$$

Finally, we have for the average and rms value of the current through the boost transistors T_2 and T_3

$$I_{T2,3\_avg} = I_L - I_{D2,3\_avg} \tag{17}$$

$$I_{T2,3\_rms} = \sqrt{\frac{I_{T2,3\_avg}}{I_L}} \cdot I_L \,. \tag{18}$$

The calculated current stress on the components are compiled in **Tab.I** for different load conditions with equal load impedance magnitude Z_L and 5 kHz linear amplifier output frequency. For the operating parameters V_{in} = 200 V, V_a = 30 V, V_p = 200 V, Z_L = 20 Ω has been assumed. Furthermore, simulation results are given which show a very good correspondence to the calculated values.

TABLE I
CALCULATED AND SIMULATED COMPARISON OF COMPONENTS STRESS

		Current [A] Resistive load, 20Ω		Current [A] Inductive load, 0.63mH		Current [A] Capacitive load, 1.6uF	
		Calculated	Simulated	Calculated	Simulated	Calculated	Simulated
T_1	avg	5.96	6.10	2.55	2.72	2.55	2.92
	rms	9.13	9.20	5.97	6.12	5.97	6.42
D_1	avg	8.04	7.85	11.4	11.3	11.4	11.1
	rms	10.6	10.4	12.7	12.5	12.7	12.2
$T_{2,3}$	avg	10.8	10.7	10.8	11.1	10.8	10.7
	rms	12.3	12.2	12.3	12.5	12.3	12.2
$D_{2,3}$	avg	3.18	3.15	3.18	2.90	3.18	3.21
	rms	6.68	6.59	6.68	6.36	6.68	6.69

C Simulation Results

Characteristic voltage and current waveforms as gained by digital simulation for ohmic, inductive and capacitive load behavior are shown in **Fig.9** for V_{in} = 200 V, V_a = 30 V, V_p = 200 V, and Z_L = 20 Ω; the width of the tolerance band is set to 20 V, the linear amplifier output frequency is set to 5 kHz. In case of capacitive load (cf. Fig.9(c)) the converter output voltages and/or the supply voltages V_{C+} and V_{C-} of the linear amplifier cannot follow the reference value because there is no current for discharging the capacitor C_2 or C_3. However, this does not affect the losses of the linear power amplifier as the corresponding transistors do not carry any current.

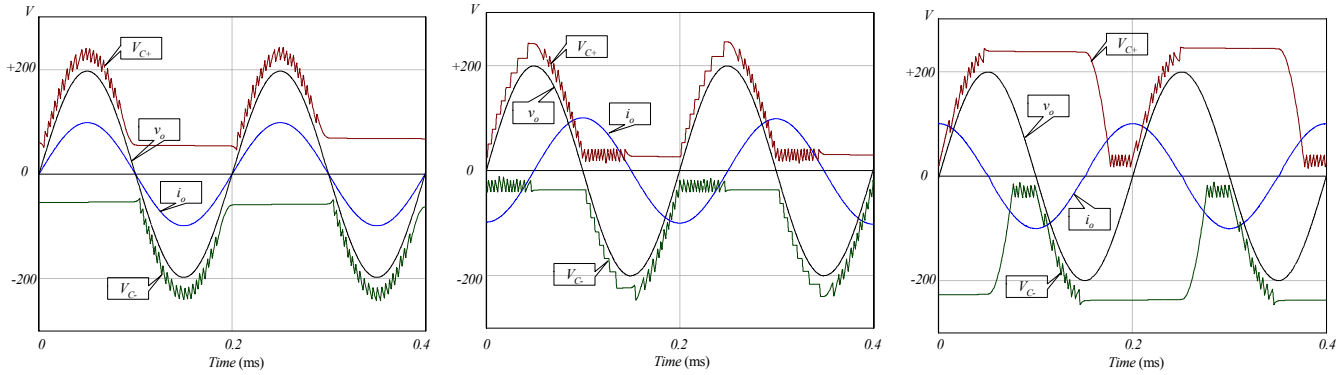

Fig. 9: Simulation of the converter system shown in Fig.8 for V_{in} = 200 V, V_a = 30 V, V_p = 200 V, and Z_L = 20 Ω; **(a)** ohmic load; **(b)** inductive load; **(c)** capacitive load.

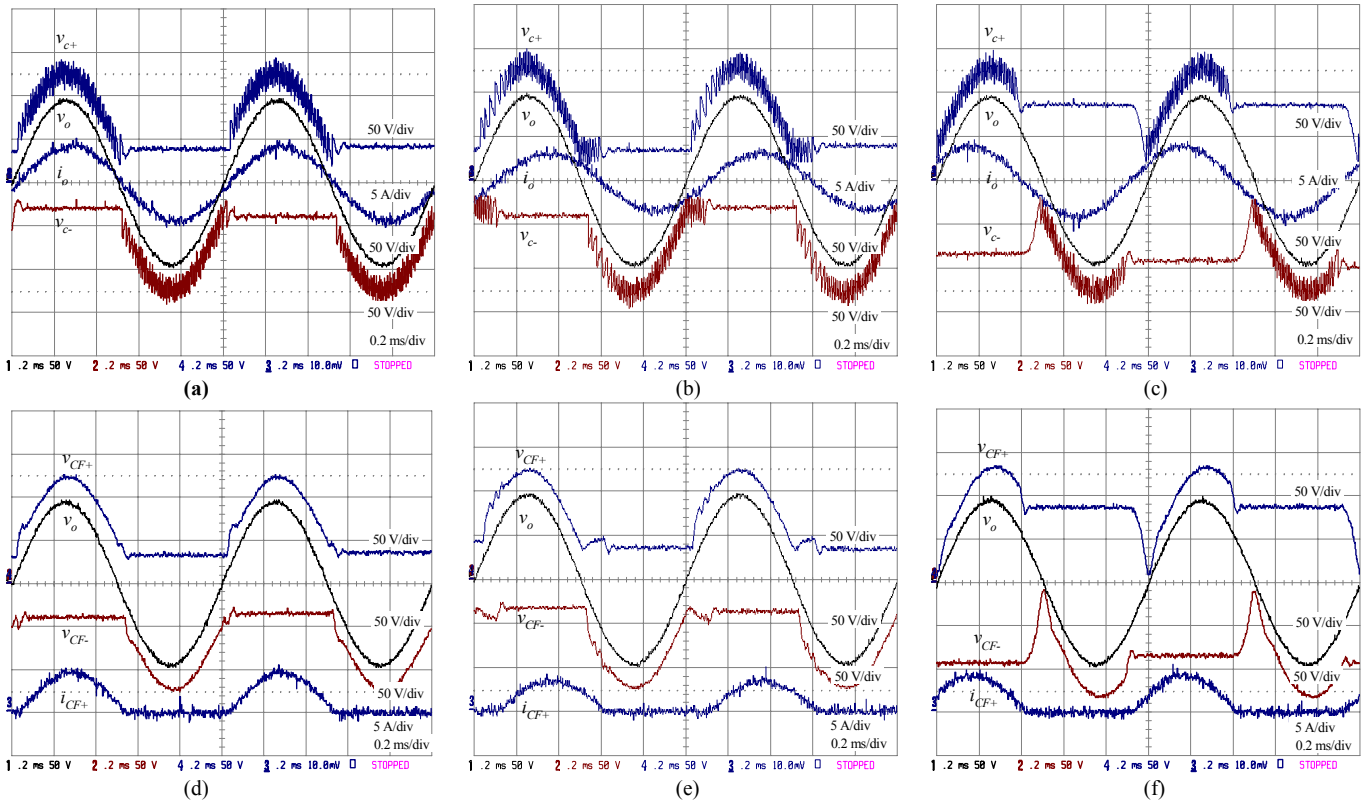

Fig. 10: Experimental results for different loads; linear power amplifier sinusoidal output voltage amplitude: 100V, 1kHz output frequency; ohmic load, 17Ω **(a),(d)**; inductive load, 17Ω + 2mH in series **(b),(e)**; capacitive load, 17Ω + 10µF in series **(c),(f)**. Supply voltages show in (a),(b),(c) measured at the input of the low-pass filter (cf. Fig.11), v_{CF+} and v_{CF-} shown in (d),(e),(f) are the actual supply voltages of the linear power amplifier.

V. Experimental Results

For verifying the theoretical considerations a 1.5kW prototype of the DC/DC converter shown in Fig.8 has been realized for feeding a 1kW linear power amplifier (cf. Fig.14). The main components employed in the DC/DC converter are listed in **Tab.II**.

TABLE II
List of Power Components of the DC/DC Converter

Name	Denomination	Type
Electrolytic Capacitor	C_1	2 × 470µF/220 VDC
CoolMOS	T_1	SPW20N60C3
Power Diode	D_1	RHRG3060
Inductor	L	200µH, ELP 43/10/28
CoolMOS	T_2, T_3	SPW47N60C3
Power Diode	D_2, D_3	ISL9R1560P2
Film Capacitor	C_2, C_3	0.47µF/275 VAC

The experimental verifications has been performed for three different loads, i.e., ohmic load, 17Ω, ohmic-inductive load, 17Ω+2mH in series, and ohmic-capacitive load, 17Ω+10µF in series (cf. **Fig.10**) for the following operating parameters:

input voltage of DC/DC converter V_{in} = 100 V
output voltage amplitude of linear power amplifier V_p = 100 V
output frequency of linear power amplifier f = 1 kHz.

Remark: Due to switch-mode DC/DC converter operation the linear amplifier supply voltages v_{C+} and v_{C-} would show a significant triangular-shaped ripple component (cf. Fig.9). Without additional means this ripple would result in a distortion of the linear amplifier output voltage due to the non-ideal power supply rejection ratio of the linear power amplifier. Accordingly, as shown in **Fig.11** a low-pass LC filter in combination with a RC damping network connected in parallel to the filter capacitor is inserted in between the switch-mode DC/DC converter and the linear power amplifier. The time behavior of the converter output voltage and of the linear amplifier supply voltage and output voltage is shown in Fig.11 for ohmic and ohmic-reactive loads.

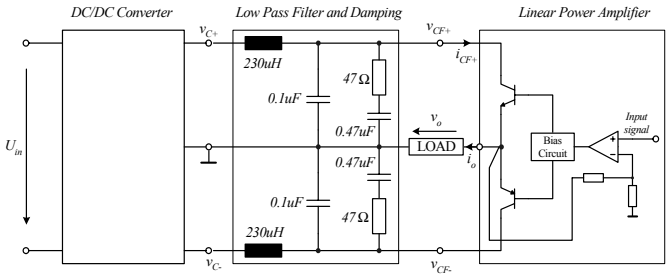

Fig.11: Insertion of a low-pass filter (including RC-damping) in between switch-mode DC/DC converter and linear amplifier input.

As the output current of the buck input stage (cf. Fig.8) is controlled to a constant value the variation of the linear power amplifier supply voltage can be with high dynamics. The experimental results for operation of the linear amplifier at 5 kHz output frequency and 100V output voltage amplitude are depicted in **Fig.12**. The excellent transient behavior of the system is also clearly shown in **Fig.13** where a sawtooth-shaped output signal with a slope of the trailing

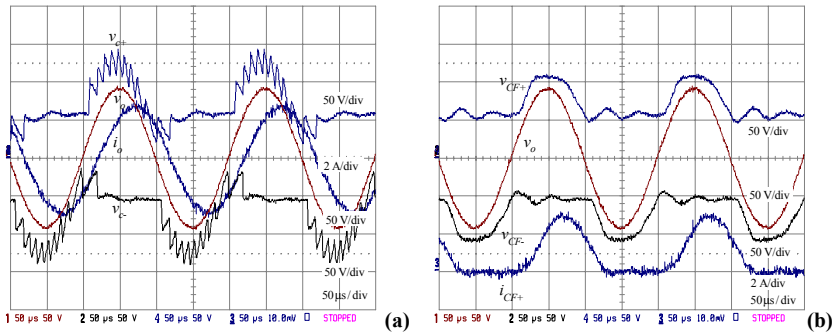

Fig.12: Experimental results for generating a sinusoidal 5kHz linear amplifier output v_O; **(a)** waveforms at the input of the supply voltage low-pass filter (cf. Fig.10), **(b)** after low-pass filtering.

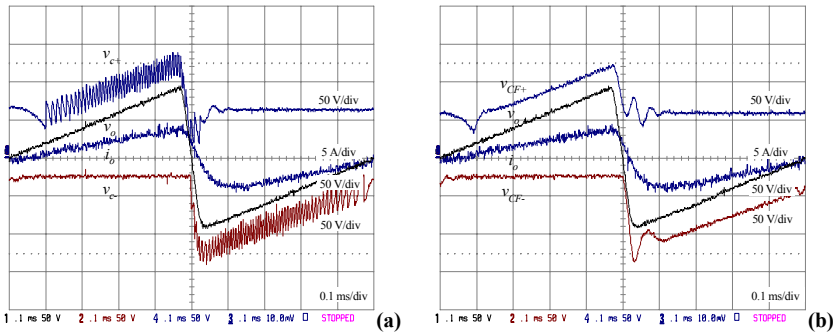

Fig. 13: Experimental results for generating a sawtooth-shaped 1kHz linear amplifier output v_O; ratio of rise-time to fall time is 20:1; **(a)** waveforms at the input of the supply voltage low-pass filter (cf. Fig.10), **(b)** after low-pass filtering.

edge of ≈3V/µs is generated and the switch-mode system does accordingly adjust the supply voltage still leaving some voltage margin so that no distortion of the linear amplifier output signal does occur.

A prototype of the proposed DC/DC converter and of the linear power amplifier is shown in **Fig. 14** where the comparably low volume (overall dimensions: 10cm × 9cm × 11cm) of the novel switch-mode converter should be pointed out.

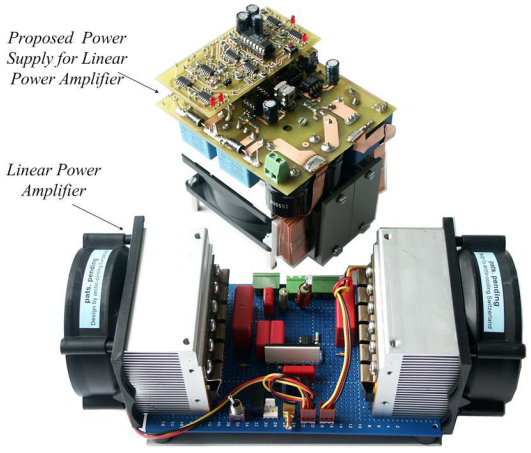

Fig. 14 Experimental hardware.

VI. Conclusions

A new DC/DC converter topology for conditioning the supply voltages of a linear power amplifier has been proposed which does allow to reduce the voltage drop across the linear amplifier power transistors to low values what does considerably reduce the amplifier power losses, especially in case of supplying reactive loads.

The current stresses on the active components of the proposed system are calculated analytically what does provide an excellent basis for the converter design. Digital simulations and experimental results taken from a 1.5kW laboratory prototype do verify the high dynamics of the linear amplifier supply voltage control which makes the proposed system applicable for linear amplifiers generating large amplitude output signals in the kHz range.

In the course of further research the experimental hardware will be extended to the topology shown in Fig.2(b), i.e. an isolated three-level buck-type DC/DC converter will be employed as input stage. The efficiency of this system including the power amplifier will be compared to a conventional linear power amplifier with passive power supply and/or constant supply voltage. Furthermore, the current control scheme depicted in Fig.7 will be implemented in the DC/DC converter prototype in order to further reduce the system losses.

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