The Delta-Rectifier: Analysis, Control and Operation

Roland Greul, *Member, IEEE*, Simon D. Round, *Senior Member, IEEE*, and Johann W. Kolar, *Senior Member, IEEE*

***Abstract*—The three-phase Delta-Rectifier is formed by a delta-connection of single-phase pulsewidth modulation (PWM) rectifier modules and has the advantage that it can provide full rated output power in the case of a mains phase loss. In this paper the Delta-Rectifier, implemented with a standard (two-level and/or three-level) boost converter, is analyzed based on an equivalent star connection. Analysis of the Delta-Rectifier shows a redundancy in the switching states concerning the input voltage formation. Furthermore, the Delta-Rectifier has reduced current ripple in the mains phase currents if the modulation is implemented with synchronized PWM. A disadvantage of two-level Delta-Rectifier is the higher voltage stress on the switching devices; however this is mitigated when the boost converter is implemented with a three-level topology as realized for a 10.5-kW laboratory prototype. The Delta-Rectifier concept is proposed based on theoretical considerations and is verified experimentally. The influence of non-idealities on the current ripple formation in the practical realization is analyzed and a high quality mains phase current is demonstrated.**

***Index Terms*—Pulsewidth modulation (PWM), total harmonic distortion (THD).**

I. Introduction

MODERN high-power telecom power supply modules are designed for a rated output power of typically 10 kW and are normally constructed using a two-stage topology, which comprises of a three-phase high power factor rectifier that supplies a step-down dc–dc converter. The input rectifier stage is frequently realized as a star connection of single-phase boost unity power factor rectifier systems as shown in Fig. 1(a) [1]–[5]. The rectifier stage can also be implemented as a direct three-phase rectifier using a topology such as the Vienna Rectifier [6] or the conventional direct rectifier [Fig. 1(b), [7]]. This paper presents another alternative, that is by making a delta-connection of three single-phase boost rectifier modules [Fig. 1(c)] and is called a Delta-Rectifier (Δ-Rectifier). A delta-connection of single-phase modules based on a buck-boost topology has been presented in [8] and [9]. The implementation of the input rectifier using single-phase unity power factor rectifier modules has an advantage since they are highly developed and well known in the industry. Furthermore, the Δ-Rectifier can be shown to have advantages of high modularity, providing mains current balancing and the possibility to deliver full output power in case of a missing mains voltage when the input diode rectifiers are replaced with thyristors as introduced in [9].

An advantage the star-connection of the rectifier modules has over the Delta-Rectifier is a lower voltage stress on the power semiconductors since the line to neutral voltage is applied to the module compared to the line-to-line voltage for the delta-connection. However, when the three-phase rectifier is connected to a three-wire mains system with no available neutral point, N in Fig. 1(a), there is no connection of the modules' star point, N_Y, to the mains. Individual control of each module can not be implemented as each rectifier modules' operation is now coupled with the other two modules' operation [10]. Therefore, to control the star-connected rectifier there needs to be an overall controller that coordinates modules and effectively decouples their operation. This requires the implementation of a complex controller to ensure the stability of the system. In [2], the overall controller uses balanced signal resistors, connected to each phase voltage, to produce an artificial mains neutral potential that is related to N_y and then used to control the individual modules. Alternatively, rather than adding additional control complexity the point N_Y could be connected to an artificial mains star point formed by a low-frequency three-phase coupled inductor arrangement with low zero-sequence impedance as proposed in [3]. However, this implementation results in a reduced power density and higher realization costs, and therefore, the Delta-Rectifier is a promising alternative for three-wire mains systems.

Both the star and Delta-Rectifier have three separate dc output voltages that can not be connected together due to the different reference potentials. For telecommunication applications, an isolated dc–dc converter is usually connected to each rectifier output, with the low voltage output side of the dc–dc converters connected in parallel. Therefore, for this application there is no disadvantage in using the Delta-Rectifier as the dc–dc converter provides the isolation. An advantage is that each of the rectifier plus dc–dc converter modules processes one third of the power and therefore provides a degree of redundancy to the system.

In this paper, the Delta-Rectifier is analyzed in detail, starting with the standard two-level boost implementation as shown in Fig. 1(c). Since the Delta-Rectifier has higher voltage stresses than the star point connected rectifier, the use of a three-level Delta-Rectifier is proposed. The use of a three-level module results in the voltage stress on the power switches being reduced by 50% since an additional switch is placed in the boost stage. The circuit operation, analysis and component stress calculations of the three-level Delta-Rectifier are then presented. Simulation and experimental results are used to confirm the operating behavior of the rectifier, including efficiency measurements.

II. Two-Level Delta-Rectifier Circuit Operation and Analysis

The operation of the individual, near-unity power factor rectifier modules is not presented as it has been previously well discussed in the literature. Since most three-phase rectifier topologies are analyzed in a star connection, it is easier to compare the

Manuscript received October 14, 2004; revised April 20, 2006. Recommended by Associate Editor R. Zhang.

The authors are with the Power Electronic Systems Laboratory, ETH Zurich, Zurich CH-8092, Switzerland (e-mail: kolar@lem.ee.ethz.ch).

Digital Object Identifier 10.1109/TPEL.2006.882961

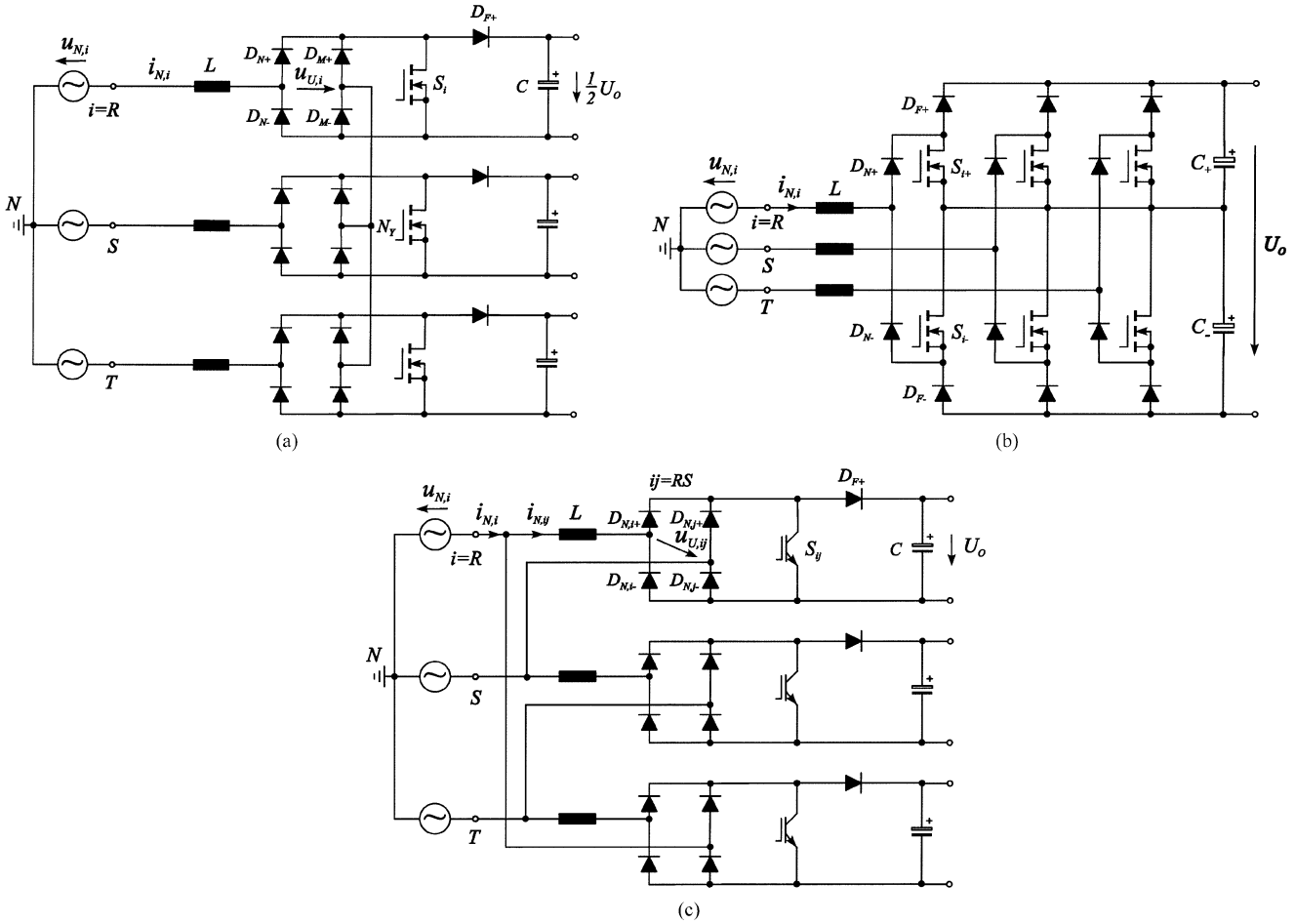

Fig. 1. Realization of a three-phase boost unity power factor rectifier with low effects on the mains by (a) combination of single-phase units in star connection, (b) conventional direct rectifier, or (c) delta connection (Δ-Rectifier). Note that the output voltage of (a) is $1/2U_O$ in order to compare the three topologies.

Delta-Rectifier if it is transformed into an equivalent star network.

A. Star Connection Equivalent Circuit

An equivalent circuit of the Δ-Rectifier ac side system is shown in Fig. 2(a). Due to the input side rectification both the switching state, s_{ij}, of a power transistor S_{ij}, and the sign, $\mathrm{sign}(i_{N,ij})$, of the line-to-line current, $i_{N,ij}(ij = RS, ST, TR)$, have influence on the formation of the corresponding input voltage

$$u_{U,ij} = \mathrm{sign}(i_{N,ij})(1 - s_{ij})U_O \tag{1}$$

where s_{ij} =1 denotes the turn-on state of S_{ij}, s_{ij} =0 denotes the turn-off state.

The line-to-line rectifier input voltages, $u_{U,ij}$, in general will contain a zero sequence, which equals the common mode component of the instantaneous rectifier input voltages, $u_{U,ij}$, and is calculated by

$$u_0 = 1/3(u_{U,RS} + u_{U,ST} + u_{U,TR}). \tag{2}$$

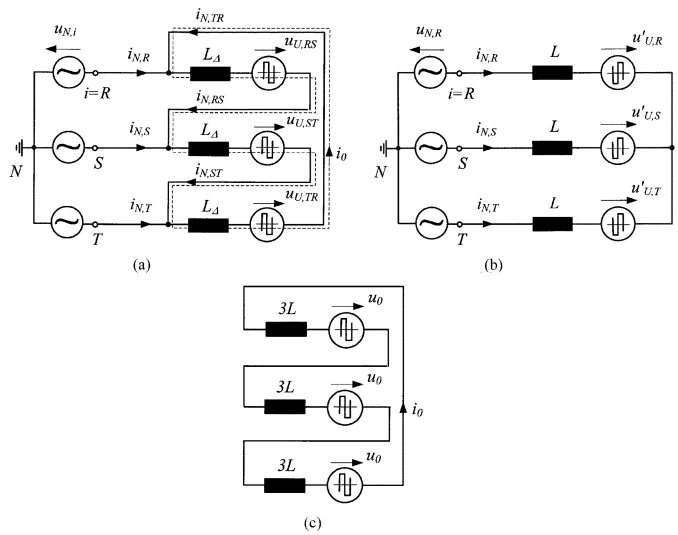

Fig. 2. Equivalent circuit (a) of the ac side system part of the Δ-Rectifier depicted in Fig. 1(c) ($L_\Delta = 3L$) and star connection (b) being equivalent to (a) concerning the formation of the mains phase currents $i_{N,i}$. Furthermore, the equivalent circuit is shown (c) for the calculation of the zero sequence component i_0 of the line-to-line currents $i_{N,ij}$ resulting from the zero sequence component u_0 of the line-to-line rectifier input voltages $u_{U,ij}$.

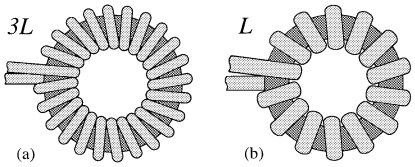

Fig. 3. Practical realization of an input inductor $L_\Delta(=3L)$ of (a) Δ-Rectifier and of an input inductor L of the (b) Vienna Rectifier of equal output power using equal magnetic (e.g., iron powder) cores. According to $N_\Delta = \sqrt{3}N, L_\Delta = 3L$ is valid.

This voltage component causes a zero sequence current, i_0, in the line-to-line currents

$$i_{N,ij} = i'_{N,ij} + i_0. \tag{3}$$

The zero sequence current, i_0, circulates inside the delta-connection of the line-to-line units [Fig. 2(a) and (c)] and does not have any influence on the formation of the mains phase currents $i_{N,i}(i = R,S,T)$ according to (4), which is only shown for phase R

$$i_{N,R} = i_{N,RS} - i_{N,TR} = i'_{N,RS} - i'_{N,TR}. \tag{4}$$

The line-to-line current system, $i'_{N,ij}(ij = RS,ST,TR)$, is defined in connection with the mains voltage by the line-to-line rectifier input voltage system remaining after subtraction of the zero sequence voltage component

$$u'_{U,ij} = u_{U,ij} - u_0. \tag{5}$$

The line-to-line voltage system defined by (5) can now be transformed into an equivalent phase voltage system [shown in Fig. 2(b)] as given by

$$\begin{aligned} u'_{U,R} &= 1/3(u'_{U,RS} - u'_{U,TR}) \\ u'_{U,S} &= 1/3(u'_{U,ST} - u'_{U,RS}) \\ u'_{U,T} &= 1/3(u'_{U,TR} - u'_{U,ST}). \end{aligned} \tag{6}$$

Accordingly, the analysis of the system behavior could be based on an equivalent star connection as shown in Fig. 2(b). In this case, the inductance of the inductors connected in series at the ac side has to be reduced by a factor of 3

$$L = 1/3L_\Delta \tag{7}$$

in order to achieve equal inner impedances of the actual delta and of the equivalent star connection. It is interesting to note that the input inductors of the Δ-Rectifier and of the Vienna Rectifier in a first approximation (not considering losses) show equal volumes (see Fig. 3). For example, if a toroidal iron power core is employed for the realization of the inductors, the number of turns of L_Δ could be higher by a factor of $\sqrt{3}$ for a given admissible maximum magnetic flux density. However, since the amplitude of the line-to-line currents is lower by a factor of $1/\sqrt{3}$, as compared to the amplitude of the mains phase currents (ripple current neglected), the volume of the inductor is similar.

The magnetic core losses of the Δ-Rectifier inductors are mainly determined by the switching component $i_{N,ij,(n)}$ of the line-to-line current. The line-to-line current can be decomposed into a mains frequency fundamental [index (1)) and a switching frequency ripple component (index (n)]

$$i_{N,ij} = i_{N,ij,(1)} + i_{N,ij,(n)} \tag{8}$$

with

$$\begin{aligned} i_{N,ij,(n)} = \quad & \underbrace{i'_{N,ij,(n)}}_{\substack{\text{differential mode} \\ \text{component}}} \\ & + \quad \underbrace{i_{0,(n)}}_{\substack{\text{common mode component} \\ \text{and/or circulated component.}}} \end{aligned} \tag{9}$$

For the Delta-connection of two-level rectifier modules, the line-to-line current ripple causes higher magnetic losses compared to the core losses in direct three-phase and/or star connected rectifier systems, which are caused by the mains current ripple $i_{N,i,(n)}$.

The star equivalent circuit is valid also for the Vienna Rectifier, where the rectifier phase voltages without zero sequence component are defined by $u'_{U,i} = u_{U,i} - 1/3(u_{U,R} + u_{U,S} + u_{U,T})$. The total $u_{U,i}$ phase voltages could be measured with reference to the capacitive center point of the output voltage U_O. Therefore, referring the analysis of the Δ-Rectifier to a star equivalent circuit provides a basis to compare the Δ-Rectifier to other star connected systems.

B. Input Voltage Space Vectors

The space vectors of the input phase voltages $u_{U',i}$ are defined by

$$\underline{u'}_{U,i} = 2/3\left(u'_{U,R} + \underline{a}\cdot u'_{U,S} + \underline{a}^2.u'_{U,T}\right) \quad \text{where } \underline{a} = e^{j\frac{2\pi}{3}}. \tag{10}$$

Fig. 4 depicts the different switching state combinations $s_\Delta = (s_{RS}\ s_{ST}\ s_{TR})$ for the case of $i_{N,RS} > 0, i_{N,ST} < 0, i_{N,TR} < 0$. The respective zero sequence components u_0 of the line-to-line input voltages $u_{U,ij}$ [see (2)] are shown as indices.

For the suppression of low-frequency component of the zero sequence current

$$i_0 = 1/3(i_{N,RS} + i_{N,ST} + i_{N,TR}) \tag{11}$$

being contained in the line-to-line currents $i_{N,ij}$, one has to ensure within each pulse period and/or within each switching state sequence [e.g., (100)–(000)–(010)–(011)] the local average value of u_0 (12) is equal to zero

$$u_{0,\text{avg}} = 1/T_P \int u_0 dt_\mu = 0 \tag{12}$$

where t_μ denotes a local time running within a pulse period T_P.

This is achieved by the proper partitioning of the total on-time of the voltage space vector $\underline{u}_{U,(100)}$ and $\underline{u}_{U,(011)}$ to the (redundant) switching states (100) and (011), which result in zero-sequence voltages of different signs and amplitudes. In Fig. 4, it

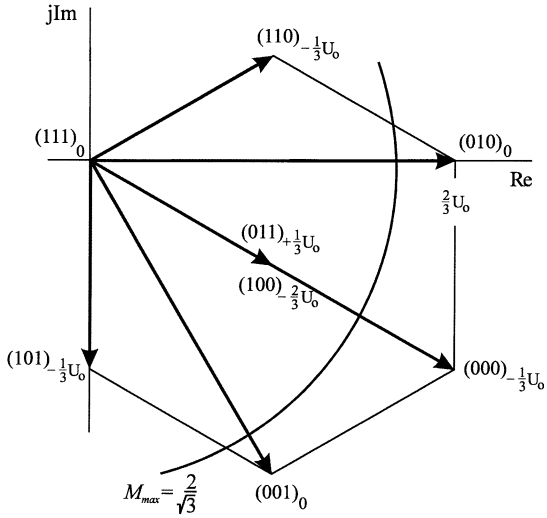

Fig. 4. Space vectors of the equivalent input phase voltages $u_{U,i'}$ for $i_{N,RS} > 0, i_{N,ST}, i_{N,TR} < 0$. Each space vector is given by the corresponding combination of switching functions $s_\Delta = (s_{RS} s_{ST} s_{TR})$ of the power transistors S_{RS}, S_{ST}, S_{TR}. The zero sequence component u_0 of the line-to-line input voltages [see (2)] occurring for a combination s_Δ is given as index. The circular line marks the modulation amplitude $M_{\max}$.

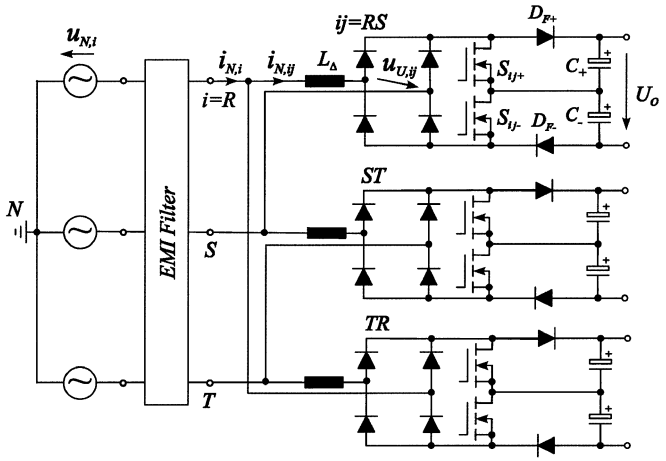

Fig. 5. Circuit of the three-level Δ-Rectifier. The inductors L_Δ can also be placed after the input rectifier.

can be seen that for $s_\Delta = (100)$ we have $u_0 = -2/3U_{\rm O}$, and for $s_\Delta = (011) u_0 = +1/3U_O$.

The modulation index is given by (13) and is limited to a maximum value of $2/\sqrt{3}$ [11]. Although a higher modulation index can be used, once it exceeds $2/\sqrt{3}$ a proper selection of the switching states can not be obtained to suppress the low-frequency component of the circulating current, that is, above this limit the mains phase currents can not be controlled to be sinusoidal

$$M = \frac{\hat{U}'_U}{\frac{1}{2}U_O} \tag{13}$$

where $\hat{U}'_U$ denotes the amplitude of the fundamental of the equivalent phase voltages $u'_{U,i}$ shown in Fig. 2(b). By neglecting the fundamental voltage drop across $L_\Delta, u_{N,i} \approx u'_{U,i}$ can be assumed.

Although the space vectors for the Δ-Rectifier have been shown in Fig. 4, it is not necessary to use space vector control to suppress the low frequency component of the zero sequence voltage, u_0. A control method, which is based on average current mode (ACM) control for each module using a line-to-line reference current, is generally sufficient and enables that, for the formation of the line-to-line input voltages $u_{U,ij}$, the redundant switching states are incorporated in a such a way that no low frequency component of the zero sequence voltage u_0 occurs [11]. A low frequency component of u_0 would result in a corresponding low-frequency distortion of the line-to-line currents $i_{N,ij}$, which is prevented by the line-to-line current controllers.

One of the aims of selecting the switching states of the Delta-Rectifier is to minimize the ripple of the mains phase currents. To achieve this, the voltage space vectors lying in the immediate vicinity of the mains voltage space vector should be employed for the formation of the rectifier input voltage. This can also be fulfilled by an ACM controller if the three modules are operated synchronously through the proper coordination of the triangular carrier waveforms. In [11], three different triangular carrier waveforms have been compared for use by the ACM controller to minimize the mains current ripple and/or maximize the ripple of the zero sequence component i_0 circulating inside the delta-connection. The three carrier types are: using the same triangular carrier for all three modules, the triangular carrier in each module is symmetrically phase displaced from the other modules' carriers, and finally, the triangular carrier signal for a module is inverted if the sign of the module's mains line-to-line voltage is negative. It was found in [11] that the ripple is minimized over the complete modulation range if the triangular carrier inversion method is implemented.

III. Three-Level Delta-Rectifier Circuit Operation and Analysis

A main advantage of the two-level Δ-Rectifier compared to the conventional direct rectifier is its high degree of modularity, however, it has the disadvantage of a high blocking voltage stress on the power transistors and free-wheeling diodes, which without additional means results in a relatively low system efficiency. This weakness however can be eliminated in the case where three-level boost converters are employed to realize the line-to-line units. The resulting system structure is depicted in Fig. 5 and will be shown to be characterized by a very low RMS value of the mains current ripple.

A. Space Vector

The voltage space vectors of the equivalent input phase voltages $u_{U,i}$' for the three-level Δ-Rectifier are shown in Fig. 6. Although for the three-level Δ-Rectifier there are 64 possible switch combinations, these combinations only result in 19 distinct space vectors [12]. Each of the space vectors $\alpha_i, \beta_i, \gamma_i$, and δ can be formed by different switching states that have a redundancy of 1, 2, 6, and 10, respectively. Each vector is formed from the independent switching functions, $s_{ij,+-}$ where $ij = RS, ST, TR$, and is given in the form $\begin{pmatrix} s_{RS+} & s_{ST+} & s_{TR+} \\ s_{RS-} & s_{ST-} & s_{TR-} \end{pmatrix}_{u_o}$. The voltage space vector, $\underline{u}_U$,

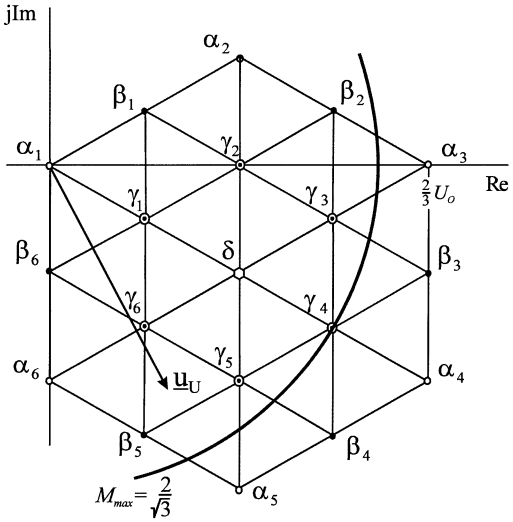

Fig. 6. Voltage space vectors available for input current control of three-level Δ-Rectifier, where α_i represents a single switch combination, β_i represents two redundant switch combinations, γ_i represents six and δ represents ten redundant switch combinations.

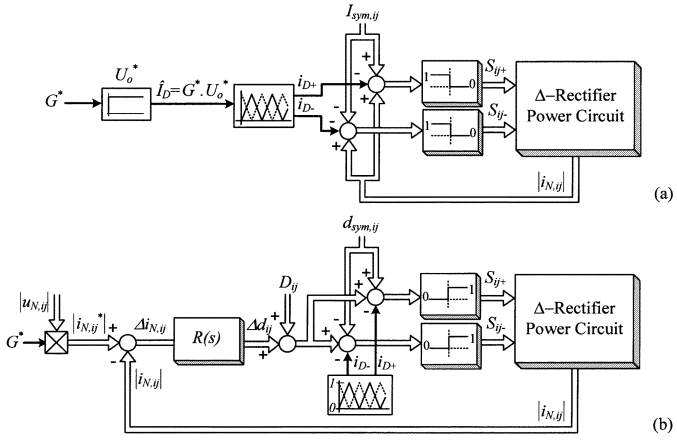

Fig. 7. Block diagram of the current controller in (a) multiplier-less current control ideal for a hybrid control design and (b) using conventional average current mode control with a duty cycle feed-forward path $D_{ij} = 1 - |u_{N,ij}|/U_{O,ij}$. No multiplication of G^* with the rectifiers mains input voltage $u_{N,ij}$ is required in (a), and the conductance information is directly transferred into the amplitude $\hat{I}_{D+} = \hat{I}_{D-}$ of the carrier signals i_{D+} and i_{D-}.

shown in Fig. 6 could be realized by using the one of the space vector combinations given in

$$\begin{pmatrix}001\\111\end{pmatrix}_0, \begin{pmatrix}001\\101\end{pmatrix}_{-\frac{1}{6}U_o} \text{ and } \begin{pmatrix}001\\011\end{pmatrix}_{+\frac{1}{6}U_o} \text{ or}$$
$$\begin{pmatrix}011\\101\end{pmatrix}_0, \begin{pmatrix}101\\001\end{pmatrix}_{-\frac{1}{6}U_o} \text{ and } \begin{pmatrix}011\\001\end{pmatrix}_{+\frac{1}{6}U_o}. \quad (14)$$

The modulation limit of $2/\sqrt{3}$ (the same value as for the two-level Δ-Rectifier) results from the fact that the zero-sequence component, u_0, of the pulsewidth modulation (PWM) line-to-line rectifier module voltages has to have a local average value equal to zero ($u_{0,\text{avg}} = 0$).

As in the case for the two-level Δ-Rectifier, the three-level Δ-Rectifier does not have to employ a space vector modulation technique for the input current control. An average current mode controller based on the absolute value of the line-to-line current references can be implemented. The current controller automatically takes care of the selection of the appropriate space vectors if adapted triangular carriers signals are employed. The implementation of the current control should ensure that the low frequency zero sequence components are eliminated and that the high frequency current ripple in each phase is minimized by maximizing the zero current component i_0 circulating inside the delta connection. This can be realised if two triangular carrier signals, shifted by half-period, are used for generating the gate signals in all three modules. Then, the three modules operate synchronously and the switching of the two MOSFETs in each module is interleaved by half a switching period.

B. Modular Current Control

To ensure a low realization effort a current control concept that, in contrast to conventional average current mode control, does not rely on a multiplication of a reference conductance with the absolute value of the respective mains line-to-line voltage is employed for the Δ-Rectifier modules [13] of the first prototype. As shown in Fig. 7, the boost inductor current $|i_{N,ij}|$ is directly compared with switching frequency triangular carrier signals that are interleaved in order to utilize the three-level module characteristic. This results in ideal switching harmonics of $i_{N,ij}$ that are multiples of twice the switching frequency. The sign of input voltage is not necessary for the three-level controller because of the interleaved operation of the MOSFETs. The partial module output voltages are balanced by an opposite shift of the the triangular carrier signals i_{D+} and i_{D-} through $I_{\text{sym},ij}$.

The turn-off time of the power transistors and, therefore, the local average value $\bar{u}_{U,ij}$ of the voltage across the power transistors S_+ and S_- shows a proportional relationship to $|i_{N,ij}|$ for operation in the continuous conduction mode. Therefore, with rising current, the voltage $\bar{u}_{U,ij}$ increases until it balances the local mains voltage $|u_{N,ij}|$

$$|u_{N,ij}| = \bar{u}_{U,_{ij}} = d'U_0 = \frac{|i_{N,ij}|}{\hat{I}_D}U_0. \quad (15)$$

This results in the system showing an ohmic input characteristic

$$|i_{N,ij}| = \frac{\hat{I}_D}{u_0}|u_{N,ij}| \quad (16)$$

where the reference value of the conductance can be defined (for constant output voltage U_O) by the amplitude of the carrier signals

$$G^* = \frac{\hat{I}_D}{U_0} \quad (17)$$

which can be varied with low circuit realization effort.

For the current control concept described, any non-ideality in the carrier signals, from the gate drive circuits or from the power circuit, directly influences the quality of the input current. Therefore, in a practical realization the PWM carrier signals have to be implemented with high linearity, symmetry and a low offset and the switching circuit must have equal turn-on and turn-off switching delay times. In contrast, for the conventional

average current mode control the non-idealities of the PWM and/or of the gate drive circuits are largely suppressed since the current controller performs a comparison of the actual and the reference current shape. Therefore, this is the preferred solution for a fully digital implemented controller.

IV. Component Stresses

To design the Delta-Rectifier the component current and voltage ratings are required. In this section the average and the rms values of the current stresses on the power semiconductor components are calculated. Simple analytical approximations are derived which can be used for the dimensioning of the power components of a Δ-Rectifier. In this paper it is assumed that the rectifier has:

- a purely sinusoidal phase current shape;
- ohmic fundamental mains behavior;
- no low frequency voltage drop across the boost inductor for the shaping of the current according to the absolute value of a line-to-line mains voltage;
- a constant switching frequency;
- linear behavior of the boost inductors (inductance is not dependent on the current level).

By restricting the analysis to the positive half wave of a mains line-to-line voltage, $u_{N,ij} = \sqrt{3}\hat{U}_N \sin(\varphi_N)$, we have to provide, by proper modulation, a local average value of the voltage across the corresponding switches S_{ij+} and S_{ij-} of $\bar{u}_{U,ij} \approx u_{N,ij}$.

A. Inductor Current Ripple

For the calculation of the input inductor current ripple two modes of operation of the three-level boost converter must be taken into account

$$u_{N,ij}(t) < U_O/2 \text{ for } t < \xi \text{ or } t > \pi - \xi \tag{18}$$

$$u_{N,ij}(t) \geqslant U_O/2 \text{ for } \xi \leqslant t \leqslant \pi - \xi \tag{19}$$

where

$$\xi = \arcsin\left(\frac{U_o}{2\hat{U}_{N,ij}}\right). \tag{20}$$

For $u_{N,ij}(t) < U_O/2[M \in (0 \cdots (1/\sqrt{3}))$, cf. (13) and (18)] the ripple envelope is defined by

$$\Delta\hat{i}_{N,ij} = (2d-1)(1-d)\frac{U_o T_p}{4L_\Delta} \text{ where} \tag{21}$$

$$d = 1 - \frac{\hat{U}_{N,ij}\sin(\omega_N t)}{U_o}. \tag{22}$$

Using (22) in (21) it follows:

$$\Delta\hat{i}_{N,ij} = \Delta i\sqrt{3}M\sin(\omega_N t)\left(1-\sqrt{3}M\sin(\omega_N t)\right) \tag{23}$$

where

$$\Delta i = \frac{U_o T_p}{8L_\Delta}. \tag{24}$$

For the case of $u_{N,ij}(t) \geqslant U_O/2[M \in ((1/\sqrt{3}) \cdots (2/\sqrt{3}))$, cf. (19)] the envelope of ripple can be determined and is given by

$$\Delta\hat{i}_{N,ij} = \Delta i 2\sqrt{3}\left(M\sin(\omega_N t) - \frac{1}{\sqrt{3}}\right) \times \left(1 - \frac{\sqrt{3}}{2}M\sin(\omega_N t)\right). \tag{25}$$

The maximum value of the envelope of the inductor ripple current within a mains half period is determined by differentiation of (23) and/or (25), depending on the level of M, and is given by (26). The maximum value of ripple is reduced by a factor of 4 as compared to a two-level boost converter realization [11]

$$\Delta\hat{i}_{N,ij} = \frac{1}{4}\Delta i. \tag{26}$$

For calculating the inductor losses caused by the current ripple a global rms value of the ripple current is determined by integration of (23) and (25) over a mains quarter period. Additionally the proportional factor of $1/\sqrt{3}$ between the peak-value and the rms-value of a triangular waveform is taken into account in (27), shown at the bottom of the page. Simplifying of (27) leads to (28), shown at the bottom of the page. For the derivation of (28) it has to considered that the operation of the system, within a mains half period, is given partly by (18) and partly by (19).

$$\Delta I^2_{N,ij,\mathrm{rms}} = \frac{2}{\pi}\Delta i^2 \left[\begin{array}{c} \int_0^{\xi} \frac{1}{3}\left(\sqrt{3}M\sin(\omega_N t)\left(1-\sqrt{3}M\sin(\omega_N t)\right)\right)^2 d(\omega_N t) + \\ \int_{\xi}^{\pi/2} \frac{1}{3}\left(2\sqrt{3}\left(M\sin(\omega_N t) - \frac{1}{\sqrt{3}}\right)\left(1-\frac{\sqrt{3}}{2}M\sin(\omega_N t)\right)\right)^2 d(\omega_N t) \end{array} \right] \tag{27}$$

$$\Delta I^2_{N,ij,\mathrm{rms}} = \frac{8}{\pi}\Delta i^2 \left[\begin{array}{c} \left(\frac{9\pi}{64}M^4 - \frac{1}{\sqrt{3}}M^3 + \frac{13\pi}{16}M^2 + \frac{\pi}{6}\right) - \\ \left(\frac{3M^2}{2} + \frac{1}{3}\right)\arctan\left(\frac{1}{\sqrt{3M^2-1}}\right) - \sqrt{3M^2-1}\left(\frac{6M^2+1}{9} + \frac{1}{2}\right) \end{array} \right] \tag{28}$$

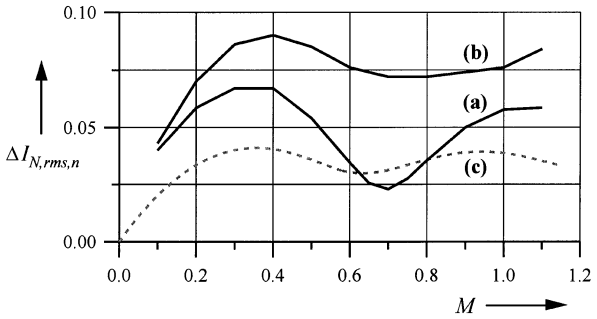

Fig. 8. Normalized rms value $\Delta I_{N,\mathrm{rms},n}$ of the phase current for the (a) three-level Δ-Rectifier and (b) the conventional direct rectifier [Fig.1(b)], while (c) is the calculated rms value $\Delta I_{N,ij,\mathrm{rms},n}$ of the ripple of the input current of a line-to-line module (used, e.g., for inductor core loss calculations). (a) and (b) are simulated.

The normalized rms value of the input inductor current ripple is defined as

$$\Delta I^2_{N,ij,\mathrm{rms},n} = \frac{1}{(\Delta i_n)^2}\Delta I^2_{N,ij,\mathrm{rms}} \text{ with}$$
$$\Delta i_n = \frac{U_O T_P}{8L} \text{ and } L = L_\Delta/3. \tag{29}$$

The global normalized rms value of the input inductor ripple current for $M \in (0 \cdots (1/\sqrt{3}))$, where the operation within a mains half period is only according to (18), can be calculated as

$$\Delta I^2_{N,ij,\mathrm{rms},n} = \left(\frac{1}{18}M^2 - \frac{8}{9\sqrt{3}\pi}M^3 + \frac{1}{8}M^4\right). \tag{30}$$

In Fig. 8 the normalized rms value of the line-to-line current and of the input phase current of a Δ-Rectifier with three-level modules, over the complete modulation index range, is depicted. It can be seen that the Δ-Rectifier [curve (a)] has a lower rms input current ripple than the conventional direct rectifier [curve (b)] over the whole modulation range. However, for calculating the core losses of an input inductor one has to keep in mind that three times the inductance value of the conventional system is employed in the Δ-Rectifier ($L_\Delta = 3L$, see Fig. 3). For a first estimation of the core losses of an input inductor, an iron powder core and a modulation index $M = 1$ are assumed. According to (28) and (29) the normalized rms value of the line-to-line ripple current is

$$\Delta I_{N,ij,\mathrm{rms},n} = 0.038 \tag{31}$$

and from (24) using an output voltage of 800 V, L_Δ of 840 μH, and switching of 50 kHz, the rms value is

$$\Delta I_{N,ij,\mathrm{rms}} = 0.038 \cdot 7.14 = 0.27\mathrm{A}. \tag{32}$$

This current ripple can now be used in basic calculations to determine the core losses for a particular inductor L_Δ. For this example, the level of current ripple for a 10-kW system is relatively low and in a commercial implementation the value of inductance could be reduced.

According to the three-level characteristic of the line-to-line module, the first harmonic of the inductor current ripple is at twice the pulse (switching) frequency, f_P. In the experimental prototype a pulse frequency of 50 kHz is used and this results in a $f_{\mathrm{Fe}} = 100$ kHz fundamental current ripple. A core loss calculation for the input inductors of a direct three-phase rectifier is given in [14].

B. Current Stresses on the Power Components

The ripple of the inductor current is not considered in the analytical calculation of the average and rms current stresses [15] of the power components. Both the three-level and two-level Δ-Rectifiers show equal current stresses on the mains side diodes, power transistors and free-wheeling diodes.

1) Mains Diodes: The average and the rms current for the mains diodes D_N is given by

$$I_{D_N,\mathrm{avg}} = \frac{\hat{I}_{N,i}}{\sqrt{3}\pi} \tag{33}$$
$$I_{D_N,\mathrm{rms}} = \frac{\hat{I}_{N,i}}{2\sqrt{3}}. \tag{34}$$

2) Free-Wheeling Diodes: The average and the rms current stress on the free-wheeling diodes D_F are

$$I_{D_F,\mathrm{avg}} = \frac{\hat{U}_{N,i}}{2U_o}\hat{I}_{N,i} \tag{35}$$
$$I_{D_F,\mathrm{rms}} = \frac{2}{\sqrt[4]{27}\sqrt{\pi}}\sqrt{\frac{\hat{U}_{N,i}}{U_o}}\hat{I}_{N,i}. \tag{36}$$

3) Power Transistors: The average and the rms current stress on the power transistors S_{ij+} and S_{ij-} are

$$I_{S,\mathrm{avg}} = \frac{1}{\sqrt{3}}\left(\frac{2}{\pi} - \frac{\sqrt{3}\hat{U}_{N,i}}{2U_o}\right)\hat{I}_{N,i} \tag{37}$$
$$I_{S,\mathrm{rms}} = \frac{1}{\sqrt{3}}\sqrt{\frac{1}{2} - \frac{4\hat{U}_{N,i}}{\sqrt{3}\pi U_o}}\hat{I}_{N,i}. \tag{38}$$

4) Output Capacitor: The rms current stress on the output capacitor (for constant, i.e., ripple free, load side current) is calculated using

$$I^2_{C_{\mathrm{out}},\mathrm{rms}} = I^2_{D_F,\mathrm{rms}} - I^2_{D_F,\mathrm{avg}} \tag{39}$$

and results in

$$I_{C_{\mathrm{out}},\mathrm{rms}} = \sqrt{\left(\frac{4}{3\sqrt{3}\pi} - \frac{\hat{U}_{N,i}}{4U_o}\right)\frac{\hat{U}_{N,i}}{U_o}}\hat{I}_{N,i}. \tag{40}$$

C. Third Harmonic

For the calculation of the average and rms current stresses on the power components an ideal sinusoidal shape of the input current for the line-to-line rectifier module has been assumed. A reduction of the peak value of the power component currents can be achieved by considering the third harmonic of the line-to-line currents (zero sequence component), which can be imagined as a current circulating inside the delta-connection [16]. This is of particular interest in connection with the magnetic dimensioning of the input inductor when saturation of the core is considered. For a minimized peak value of the line-to-line current the amplitude of the third harmonic should be one-sixth of the

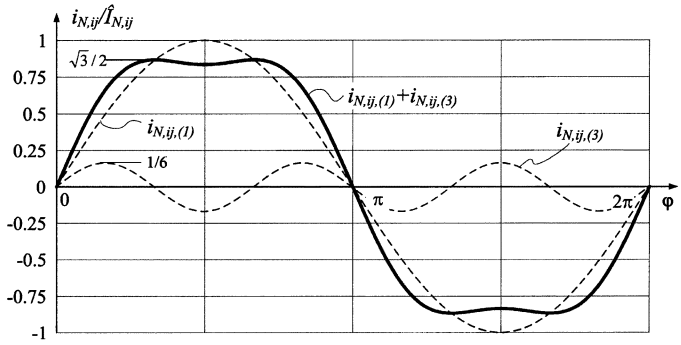

Fig. 9. Addition of third harmonic with one-sixth amplitude to a voltage fundamental.

line-to-line current fundamental. The resulting voltage waveform including the third harmonic is shown in Fig. 9.

The rms and average values of the component currents with third harmonic injection show only minor differences to the values calculated for purely sinusoidal current. For example, the average value and rms value for the mains diode current with third harmonic injection is calculated by

$$I_{D_N,\mathrm{avg}} = \frac{19}{18}\frac{\hat{I}_N}{\sqrt{3}\pi} \tag{41}$$

$$I_{D_N,\mathrm{rms}} = \frac{\sqrt{37}\hat{I}_N}{12\sqrt{3}}. \tag{42}$$

For the conventional direct rectifier a zero sequence voltage component is employed in order to extend the modulation range, $M \in 0\cdots 1$ as given for purely sinusoidal modulation, to $M \in 0\cdots 2/\sqrt{3}$. The current stress values of the conventional rectifier have been calculated based on purely sinusoidal modulation in [15]. As for the Δ-Rectifier these current values do hold with sufficient accuracy also in case a third harmonic is injected in order to extend the modulation range.

V. Simulation and Experimental Results

To confirm the operation of the Delta-Rectifier, both digital simulations using Simplorer and experimental implementation have been performed on a system with the following parameters.

- Rated power $P_O = 10.5$ kW.
- Input voltage range $U_{N,l-l} = 320\ \mathrm{V}\ldots 530\ \mathrm{V_{rms}}$.
- Module output voltage $U_O = 800\ \mathrm{V_{DC}}$.
- Switching frequency $f_P = 50$ kHz (for each switch S_{ij+} and S_{ij-}).
- Module input inductors $L_\Delta = L_{\Delta,+} + L_{\Delta,-} = 2 \times 420\ \mu$H (see Fig. 15).

A. Rectifier Operation

Shown in Fig. 10 is a photograph of the second prototype Δ-Rectifier with three individual line-to-line 3.5-kW power modules linked together with a connecting board. The modular structure of the system can be seen from the prototype. It consists of five main parts; the three line-to-line power modules, one connection board which includes the fully digital controller, measurement circuits, the housekeeping power supply and the ac-mains connector, and the fan unit at the front of the system. The overall dimensions of the system are ($W \times L \times H$ = 19.5 cm × 13 cm × 17.6 cm), thus giving a power density of 2.4 kW/dm ^{3} (or ∼40 W/in ^{3}) and a power to weight of 2.6 kW/kg.

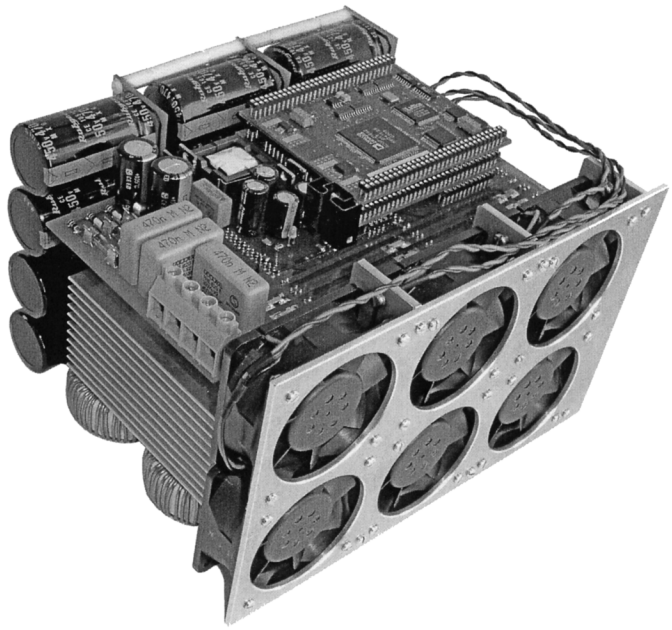

Fig. 10. Prototype of a 3 × 3.5 kW Δ-Rectifier with three-level line-to-line modules. The power density of the rectifier system is 2.4 kW/dm^3 (or ∼40 W/in^3).

The control of the system is implemented with an ADSP-2199x DSP and a PLD for generating the PWM signals of six power MOSFETs (two in each phase). The control system is designed to enable three individual dc–dc converters to be connected to the rectifier modules, in order to construct a modular high-power telecom power supply.

The system is supplied with a symmetrical three-phase voltage generated by a three-phase high power linear amplifier. For each module an output voltage controller and an underlying input ACM controller, as shown in Fig. 7(b), is implemented in the digital control system. The system represents a symmetric ohmic load to the mains, where the reference value G^* of the input conductance is multiplied by the line-to-line voltages to set the module reference currents $i^*_{N,ij}$. The digital control also defines the switching frequency, f_P, and balances the module's partial output voltages by using an opposite offset value for the duty cycle balancing signal [$d_{\mathrm{sym},ij}$ in Fig. 7(b)].

From Fig. 11, the results from the digital simulation of the system behavior are fully verified by the experimental analysis. The phase current forming equivalent rectifier input phase voltage $u'_{U,i}$ [cf. Fig. 2] shows an approximately sinusoidal shape. It can be seen that the input phase current contains a ripple component with a low amplitude despite the relatively low input inductance value. This can also be clearly seen in Fig. 12, which shows in detail the experimental waveforms. The zero-sequence component $i_{0,(n)}$ (common mode component at the switching frequency) of the line-to-line input current ripple is given by

$$i_{0,(n)} = \frac{1}{3}\left(i_{N,RS,(n)} + i_{N,ST,(n)} + i_{N,TR,(n)}\right) \tag{43}$$

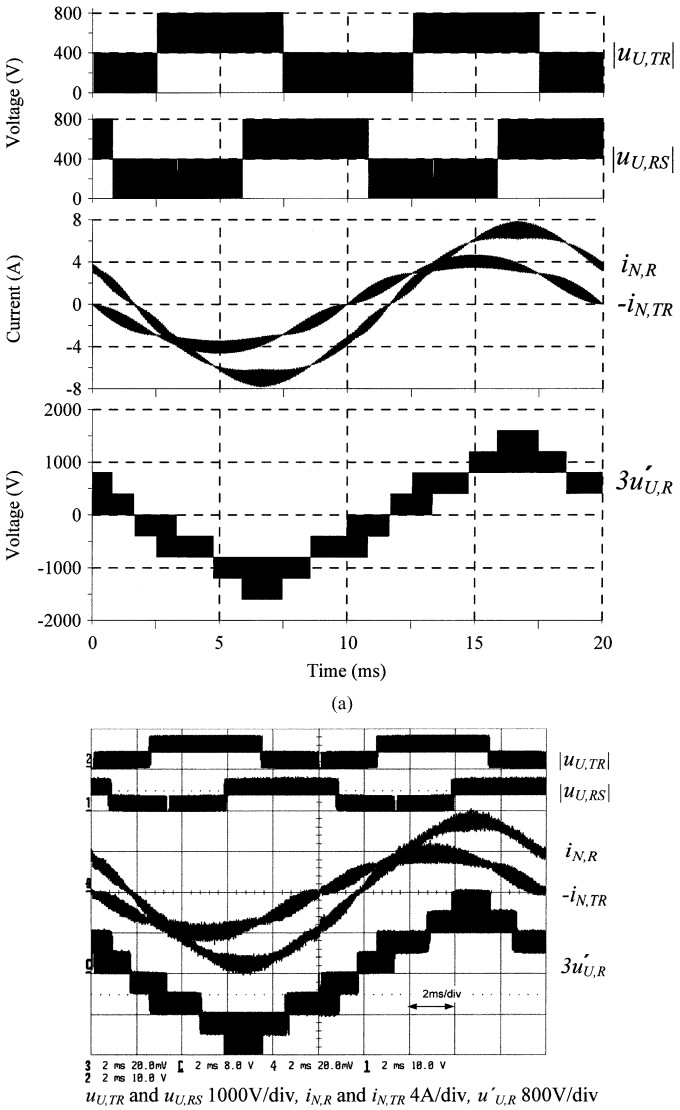

Fig. 11. (a) Digital simulation and (b) experimental results of the switch voltages of the modules RS and TR, u_{RS} and u_{TR}, the module input current-$i_{N,TR}$, mains phase current $i_{N,R}$ and the equivalent rectifier input phase voltage $u_{U,R}$.

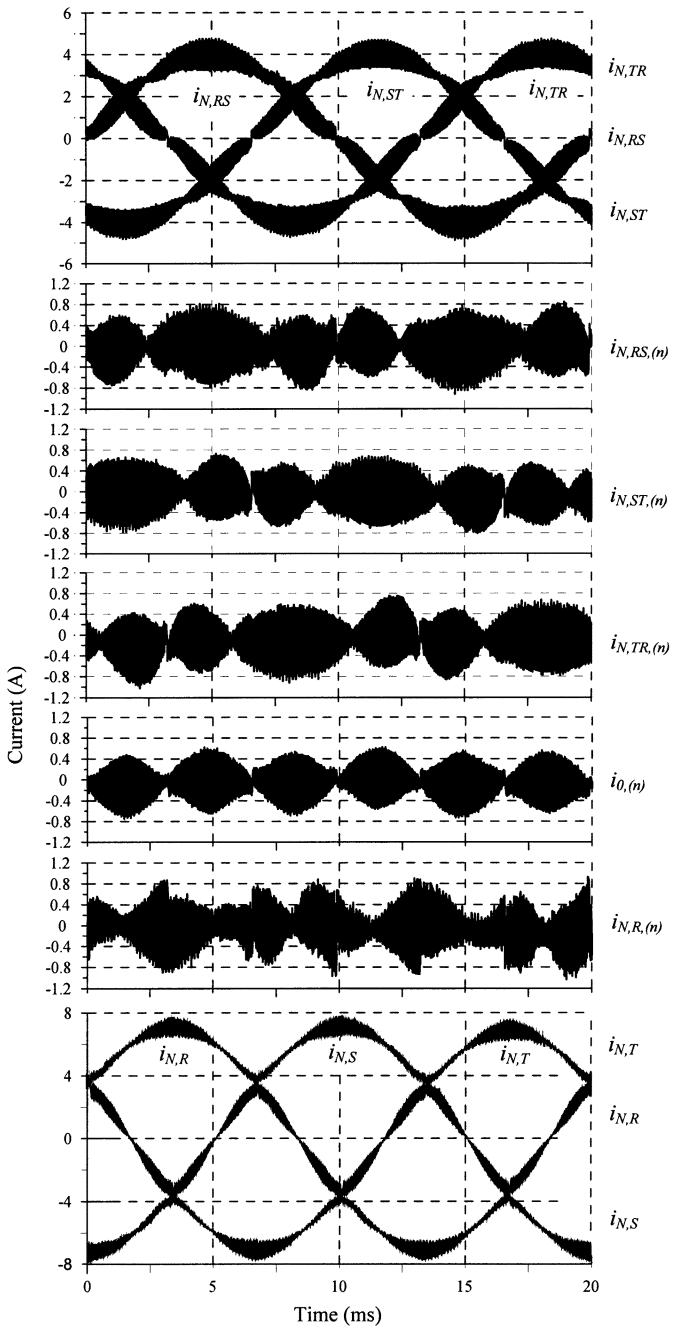

Fig. 12. Experimental results of the module input currents $i_{N,ij}$, the ripple $i_{N,ij,(n)}$ of $i_{N,ij}$, the zero-sequence $i_{0,(n)}$, the ripple $i_{N,R,(n)}$ of the phase current $i_{N,R}$ and the phase currents $i_{N,i}$ for an output power of 3.4kW.

and is circulating inside the delta connection. Therefore, this ripple has no influence on the ripple of the mains phase currents since the zero-sequence ripple components $i_{0,(n)}$ of two line-to-line module input currents cancel each other in the formation of a mains phase current (given in (44) for phase R). This results in a reduced effort to filter differential mode electromagnetic interference (EMI)

$$\begin{aligned} i_{N,R,(n)} &= i_{N,RS,(n)} - i_{N,TR,(n)} \\ &= \left(i'_{N,RS,(n)} + i_{0,(n)}\right) - \left(i'_{N,TR,(n)} + i_{0,(n)}\right) \\ &= i'_{N,RS,(n)} - i'_{N,TR,(n)}. \end{aligned} \tag{44}$$

Fig. 13 shows the harmonic spectrum of the ripple components of the mains phase currents, $\hat{I}_{N,i,(n)}$, for the ideal case produced by digital simulation and for the experimental results. Both spectrums show that the waveforms contain low amplitudes of the switching frequency f_P. The total harmonic distortion (THD) of the phase current is approximately two percent measured up to 250 kHz. In a completely ideal system, the interleaving of the power transistor control signals of each module should result in switching frequencies in integer multiples of $2f_P$. In Fig. 13(b), the experimental spectrum shows a small amount of 50 kHz (switching frequency) present. This non-ideal behavior is caused partly by an asymmetry and/or offset of the PWM carrier signals (for the multiplier-less control system), by different turn-on and turn-off delay times of the gate drive circuits, by asymmetries of the line-to-line modules, by the non-linearity of the iron powder core input inductors and

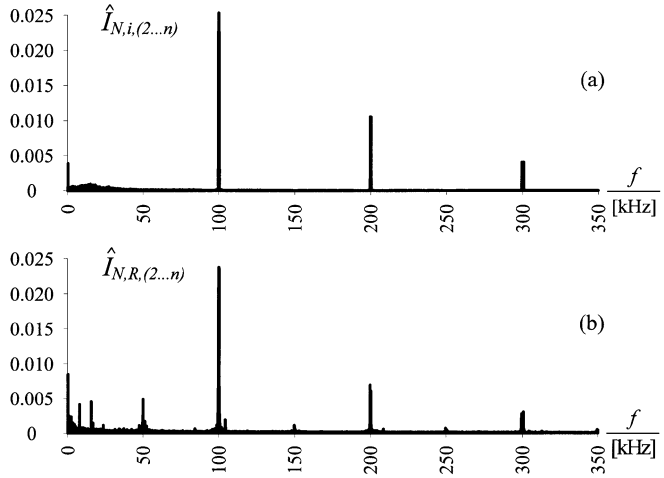

Fig. 13. Normalized spectra of the mains phase currents (with fundamental removed) produced by (a) digital simulation and (b) from experimental results (without EMI input filter). Normalization basis: $\hat{I}_{N,i,(1)}$.

by the discontinuous inductor current operation occurring in the vicinity of the module input current zero crossings.

B. Calculated and Measured Efficiency

The operational efficiency of the Δ-Rectifier and the conventional direct rectifier are compared using the analytical expressions derived in Section IV and manufacturers' data for the components listed in the Appendix. Using the operating condition as defined in Section V, the losses and operating efficiency for the Δ-Rectifier can be determined and are given in Table I. The calculated efficiency various from 96.4% to 97.8% for an input voltage range of 320 V_{RMS} to 530 V_{RMS} line-to-line. At low input voltage levels the majority of the power loss is from the power switches. It is important to note that the passive components do have significant loss due to the higher levels of current.

The losses in a conventional direct rectifier, having equal specifications, are calculated based on [15] and are listed in Table II. Comparing the data in Tables I and II shows that the efficiency of the Δ-Rectifier is lower by approximately 0.3% as compared to the conventional rectifier. This is mainly due to the extra losses in the output capacitors caused by the larger currents flowing. The differences of the semiconductor losses are not significant because the peak current stress of the Δ-Rectifier is reduced by a factor of $\sqrt{3}$ as compared to the conventional rectifier. However, the stress is applied within the whole mains period in contrast to the conventional rectifier where the peak current stress is higher but applied only for half a mains period.

The experimental efficiency of the Δ-Rectifier is determined by measuring the output power from the three dc-outputs with a voltmeter and an amp-meter and the input power with a power analyzer (model NORMA D6000). From Fig. 14, the efficiency varies from 95% at low input voltage and power (>1800 W), and up to 97.4% when operated at high input voltage and maximum load. These results confirm the accuracy of the calculated results in Table I. The efficiency is reduced at lower input voltages since the input current is higher and there are more losses in all of the components.

TABLE I
CALCULATED POWER LOSSES AND EFFICIENCY FOR A SINGLE MODULE OF THE Δ-RECTIFIER OPERATING WITH AN OUTPUT POWER OF 3500 W, AN OUTPUT VOLTAGE OF 800 V AND A SWITCHING FREQUENCY OF 50 KHZ. LOSSES IN THE EMI INPUT FILTER ARE NOT CONSIDERED

Input voltage (line-to-line rms)	**320**	**400**	**480**	**530**	V
Input voltage (line rms)	**185**	**230**	**277**	**306**	V
Input current ($i_{N,ij,rms}$)	11.0	8.8	7.3	6.6	A
Modulation M	0.65	0.82	0.98	1.08	
Switch Losses					
Switch Current (rms)	7.9	5.5	3.9	3.0	A
Conduction loss	7.5	3.7	1.8	1.1	W
Turn on switch loss	14.1	11.3	9.4	8.5	W
Turn off switch loss	4.0	3.3	2.7	2.4	W
Loss for 2 Switches	***51.1***	***36.3***	***27.7***	***24.0***	W
Freewheeling Diodes					
Loss of 2 Freewheeling Diodes	***14.1***	***13.1***	***12.3***	***11.6***	W
Mains Rectifier					
Loss of 4 Mains diodes	***19.7***	***15.2***	***12.5***	***11.0***	W
Total Semiconductor Loss	**84.9**	**64.6**	**52.5**	**46.6**	**W**
Input choke					
Copper losses @75°C	11.2	7.2	5.0	4.1	W
Iron losses	3.5	3.8	4.2	4.9	W
Loss of Input Choke $L_{\Delta}=L_{\Delta+}+L_{\Delta-}$	***14.7***	***11.0***	***9.2***	***9.0***	W
Capacitors					
Loss of Output Capacitors	***11.6***	***8.1***	***5.8***	***4.2***	W
Auxiliary power (1/3)	5	5	5	5	W
Fan power (1/3)	5	5	5	5	W
Additional Losses (1/3)	5	5	5	5	W
Total Power Loss	**126.2**	**98.7**	**82.5**	**74.8**	**W**
Efficiency	**96.4**	**97.2**	**97.6**	**97.8**	**%**

TABLE II
CALCULATED POWER LOSSES AND EFFICIENCY FOR A CONVENTIONAL DIRECT RECTIFIER OPERATING WITH AN OUTPUT POWER OF 10500 W, AN OUTPUT VOLTAGE OF 800 V AND A SWITCHING FREQUENCY OF 50 KHZ. LOSSES IN THE EMI INPUT FILTER ARE NOT CONSIDERED

Input voltage (line-to-line rms)	**320**	**400**	**480**	**530**	V
Input voltage (line rms)	**185**	**230**	**277**	**306**	V
Input current (rms)	18.94	15.16	12.63	11.44	A
Modulation index	0.65	0.82	0.98	1.08	
Losses					
Total Switch Losses	151.5	100.5	72.3	60.5	W
Freewheeling Diodes	39.3	36.4	34.5	33.6	W
Mains Rectifiers	54.3	41.7	33.8	30.2	W
Loss of Input Chokes (840μH)	40.1	30.6	26.0	22.5	W
Output Capacitors (12*470μF; ESR 0.1Ω)	15.1	8.6	4.3	2.3	W
Auxiliary power	15	15	15	15	W
Fan power, Additional Losses	30	30	30	30	W
Total Power Loss	**345.3**	**262.8**	**215.9**	**194.1**	**W**
Efficiency	**96.7**	**97.5**	**97.9**	**98.1**	**%**

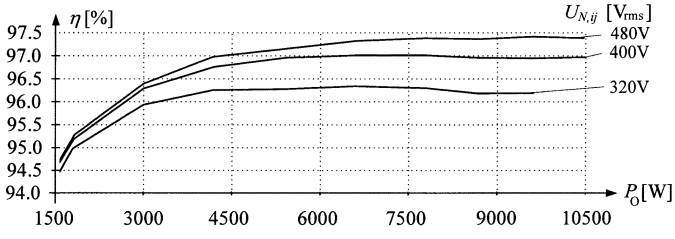

Fig. 14. Measured efficiency of the 10.5-kW prototype of the Δ-Rectifier (Fig. 10) for various mains phase voltages.

VI. DISCUSSION

Comparing the Δ-Rectifier and conventional direct rectifier in terms of their voltage and current stress on the power transis-

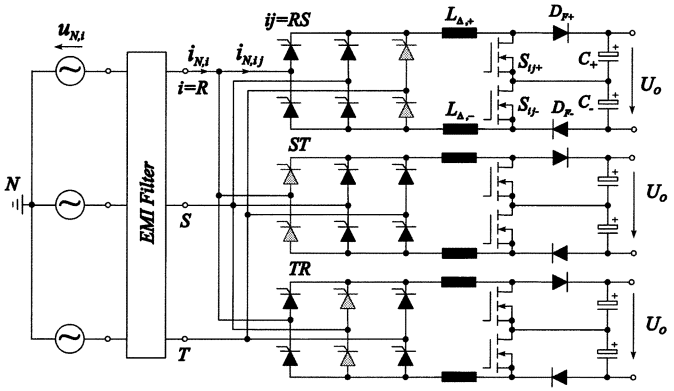

Fig. 15. Δ-Rectifier with thyristor bridge rectifiers that allow 100% power operation when a phase of the main fails (two phase operation).

TABLE III
SWITCHING DEVICES SELECTED FOR EFFICIENCY COMPARISON OF THE Δ-RECTIFIER AND CONVENTIONAL RECTIFIER

Part	Device Description
S	Infineon SPW47N60C2 @ T_{case} = 95°C
D_F	Int. Rect. HFA25PB60 @ T_{case} = 85°C
D_N	ST TYN1040 (Thyristor) @ T_{case} = 65°C
L_Δ / 2	Core: Micrometals T184-52, A_L=159nH/N^2
$C+$, $C-$	2 x Rubycon MXR 330µF 450V 105°C in parallel

tors and free-wheeling diodes and/or the realization effort of the power circuit it is found that they are very similar. Although the Δ-Rectifier has lower levels of current ripple than the conventional direct rectifier over the complete modulation range. The complexity of the control for both systems does not show any large differences. The main differences are the slightly higher efficiency for the conventional rectifier and the additional current stress in the dc link capacitors. In the case of a symmetrical mains voltage the conventional rectifier shows a significantly lower current stress on the output capacitors due to the constant power flow of the three-phase system. This is only a minor advantage in the case where a long hold-up time of the rectifier is required since a large capacitance has to be installed at the output.

Unbalanced mains voltages have no effect on control system since each module operates independently on the line-to-line voltage. The controller maintains a constant dc link voltage and this is not influenced by the unbalanced mains voltage. However, the unbalanced mains voltage causes the level of mains current ripple to increase slightly, although the level is still close to optimal.

A main advantage of the Δ-Rectifier occurs when the input single-phase diode bridges of each module are replaced by three-phase thyristor bridges, as shown in Fig. 15, it is then possible for the module to operate from a different line-to-line voltage. The thyristors shaded in grey are normally inactive and are only used to change the operating lines during a mains failure. This means that the rectifier is still able to operate from the two phases remaining in the case of a mains phase loss. Therefore the Δ-Rectifier can operate with high system reliability and offers the possibility of delivering full output power in case of a missing mains phase. In contrast, the output power of a direct rectifier [7] has to be reduced to $1/\sqrt{3}$ of the maximum output power capability $(0.58P_{O,\max})$ for two-phase operation [17]. When operating with two-phases one should take care that the resulting higher current (increase of $\sqrt{3}$) on the remaining phases does not cause any problems. Furthermore, the thyristors could also be employed to provide a soft pre-charge of the output capacitors at system start-up. To successfully implement this scheme; the measurement of the line-to-line voltages must be made before the thyristor bridge in order to determine when the lost phase returns, the boost inductor must be placed on the dc side, during two-phase operation the triangular PWM carrier for each module is adjusted to have 120° separation to ensure minimum current ripple, and the digital controller must actively control the thyristors so that they work like diodes and they switch reliably during the transition between phase loss and normal operation.

VII. CONCLUSION

The three-phase Delta-Rectifier is formed by a delta-connection of single-phase PWM rectifier modules. By analyzing the Delta-Rectifier, using an equivalent star connection, it shows that there is a redundancy in the switching states. This redundancy is employed in the current controller and is able to suppress the low frequency zero sequence current circulating inside the delta-connection of the line-to-line units. Furthermore, the system has reduced current ripple in the mains phase currents if the modulation is implemented with synchronized PWM. A simple average current mode controller based on the line-to-line currents can be implemented, therefore reducing the control complexity. Compared to the conventional direct rectifier the Delta-Rectifier has the additional advantage of being able to operate at 100% load during the loss of one mains phase. The operation of a three-level Delta-Rectifier is verified experimentally using a 10-kW laboratory prototype. The efficiency of the prototype is 97.3% at full load and the prototype waveforms show the reduced current ripple and a low THD of 2% for the mains phase currents.

APPENDIX

Listed in the Table III are the power semiconductor components selected as basis for the calculation of the efficiency of the Δ-Rectifier and of the conventional direct rectifier.

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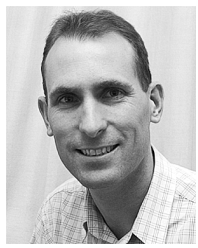
Roland Greul (M'05) received the M.Sc. degree in electrical engineering from the University of Technology Vienna, Vienna, Austria, in 2000 and the Ph.D. degree from the Power Electronic Systems Laboratory, ETH Zurich, Zurich, Switzerland, in 2005.

His interest in power electronics and control started during his M.S. thesis work on DSP-control of the Vienna Rectifier III. From 2000 to 2001, he was an Application Engineer at Siemens Automotive AG. He is currently a Post Doctoral Researcher. His research interests are in modeling and design of single and three phase ac–dc power converters.

Dr. Greul is a member of the Austrian Society of Electrical Engineering (OVE).



Simon Round (SM'99) received the B.E. (with honors) and Ph.D. degrees from the University of Canterbury, Christchurch, New Zealand, in 1989 and 1993, respectively.

From 1992 to 1995, he was a Research Associate in the Department of Electrical Engineering, University of Minnesota, Minneapolis, and a Research Fellow at the Norwegian Institute of Technology, Trondheim, Norway. From 1995 to 2003, he was a Lecturer/Senior Lecturer in the Department of Electrical and Electronic Engineering, University of Canterbury, where he performed research on power quality compensators, electric vehicle electronics, and cryogenic power electronics. He has also worked as a Power Electronic Consultant for Vectek Electronics, where he developed a "state-of-the-art" digital controller for high-power inverter systems. In September 2004, he joined the Power Electronic Systems Laboratory, ETH Zurich, Switzerland, as a Senior Research Associate. His current research interests are in the areas of silicon carbide power electronics, control of three-phase unity-power-factor rectifiers, and the application of sparse matrix converters.

Dr. Round received the University of Canterbury Teaching Award in 2001. He has been actively involved in the IEEE New Zealand South Section, where he was Vice-Chair and Chairman from 2001 to 2004.

Johann W. Kolar (SM'04) received the M.S. and Ph.D. (with highest honors) degrees in industrial electronics from the University of Technology Vienna, Vienna, Austria.

Since 1984, he has been with the University of Technology Vienna, and has been teaching and working in research in close collaboration with international industry in the fields of high performance drives, high frequency inverter systems for process technology and uninterruptible power supplies. He has proposed numerous novel converter topologies, e.g., the Vienna Rectifier and the three-phase ac–ac sparse matrix converter concept. He was appointed Professor and Head of the Power Electronic Systems Laboratory, ETH Zurich, Zurich, Switzerland, in 2001. He has published over 200 scientific papers in international journals and conference proceedings and has filed more than 50 patents. The focus of his current research is on ac–ac and ac–dc converter topologies with low effects on the mains, e.g., for power supply of telecommunication systems, more-electric-aircraft applications and distributed power systems in connection with fuel cells. Further main areas of research are the realization of ultra-compact intelligent converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multiphysics/multiscale simulation, bearingless motors, and power MEMS.

Dr. Kolar is a member of the IEEJ and of Technical Program Committees of numerous international conferences in the field (e.g., Director of the Power Quality branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 to 2000, he served as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and since 2001 as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.